64 Gb/s O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulators Integrated in a 300 mm Silicon Photonics Platform

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***Abstract*—We report the recent progress of waveguide-coupled O-band GeSi quantum confined stark effect electroabsorption modulators, monolithically integrated in a Si photonics platform on 300 mm Silicon-on-insulator wafers with 220 nm thick Si top layer. A wafer-scale analysis of static insertion loss (IL) and extinction ratio (ER) is presented, showing IL down to 7.5 dB with ER of 5 dB for a 36.8 μm long device, at drive voltages of 2 V peak-to-peak. Modulation bandwidths beyond 50 GHz are demonstrated, with an extracted junction capacitance of 57 fF and series resistance of 8.3 Ω. Finally, open eye diagrams are demonstrated for non-return-to-zero on-off keying (NRZ-OOK) modulation for data rates from 40 Gb/s up to 64 Gb/s, with dynamic extinction ratio of 2.5 dB, at 1320 nm wavelength.**

***Index Terms*—Electroabsorption modulator, multiple quantum wells, quantum confined stark effect, silicon photonics.**

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I. Introduction

SILICON photonics has attracted a lot of attention over the past years, as it offers large-scale manufacturing of photonic integrated circuits. By leveraging the well-established complementary metal-oxide semiconductor (CMOS) technology, it offers a promising platform for serving low-cost, and energy-efficient optical interconnects, as well as applications in sensing, automotive, and optical computing. Current implementations of silicon photonics transceivers typically use Si-based Mach-Zehnder or ring-based modulators [1], [2]. For next-generation transceivers, improved modulator technology is needed. On one hand, for pluggable optics, electro-optic modulators supporting data rates beyond 200 Gbps are required, with low insertion loss (IL) and high extinction ratio (ER) with low drive voltage [3]. On the other hand, for emerging co-packaged optics, ultra-compact, low-loss, high efficiency, and thermally robust modulators are needed, with low capacitive load [4]. Modulator technologies based on III-V semiconductors such as Indium Phosphide (InP) or electro-optic materials such as Lithium Niobate ($LiNbO_3$) have shown great promise towards these demanding performance metrics. However, such "exotic" devices or materials are typically produced on wafers with smaller diameter ($\leq$150 mm), in specialized fabrication lines [5]. Hybrid or heterogeneous integration of such materials on large-diameter silicon wafers typically adds substantial cost to the manufacturing process, hampering aggressive cost reduction as needed for high-volume, short-reach optical interconnect applications. On the other hand, Germanium (Ge) and Germanium Silicon (GeSi) alloys are compatible with modern Si CMOS technology and as such provide a direct pathway to cost-effective, high-volume manufacturing. As a result, these materials are an attractive choice for active photonic components such as modulators and photodetectors. Previously, bulk Ge/GeSi materials have been used to demonstrate Franz-Keldish (FK) electroabsorption modulators (EAMs), operating up to 224 Gb/s PAM-4 with reasonable IL and ER in the C-band [6], [7], [8], [8], [9]. To implement GeSi EAMs operating in the O-band, we need to exploit the quantum confined stark effect (QCSE) by using stacked Ge/GeSi multiple quantum wells (MQW) [10], [12]. The QCSE is a quantum

mechanical phenomenon that happens in MQW structures. With the application of an electric field, the MQW band structure tilts, and the exciton's absorption peak wavelength is shifted to longer wavelengths. This leads to a strong spectral shift of the optical absorption edge with relatively low bias [13], [14]. The QCSE has been considered an interesting option to design EAMs due to the strong exitonic absorption peaks [13] that could enhance the modulator ER. Since the first demonstration of the QCSE in Ge/GeSi in [13], it has been demonstrated in several configurations including surface-normal devices [15], microdisks, [16] and waveguides [17]. However, the integration of such complex MQW stacks within a silicon-on-insulator (SOI) platform is challenging due to the mismatch in lattice constant and thermal-expansion coefficient between Si and Ge. Previously, many integration options have been considered, such as GeSi virtual substrates (VS) with thickness in the range of 0.8 µm to 13 µm [10], [17], [18], [19], [20] to lower the threading dislocation densities (TDD). However, such thick buffer layers cause difficulties in coupling the light from and to the SOI waveguides. Therefore, thin fully strain-relaxed buffer (SRB) layers are preferred to achieve high coupling efficiency through simple butt coupling between the Si and GeSi waveguides. Previously, we reported high-speed QCSE EAMs using a GeSi MQW stack operating in the O-band and integrated into imec's 300 mm Si photonics platform with a 220 nm-thick top Si layer [12]. In this paper, we present the design and the wafer-scale performance of an improved version of the previously reported device. The paper is structured as follows. In Section II, we discuss the different design aspects including the design of the GeSi MQW stack, the simulation of the related absorption spectrum, and the fabrication process. In Section III, we discuss the static characterization of the modulator and a wafer-scale analysis for 78 dies measured across the 300 mm SOI wafer. In Section IV, we present the high-speed performance including s-parameter measurements, device circuit modelling, and the large-signal performance of the EAM. Finally, discussion and conclusions are drawn in Section V.

II. Device Design and Fabrication

QCSE EAMs are typically implemented in a vertical p-i-n diode configuration. The top part of the device and the SRB form the p- and n-regions of the diode, respectively, confining the electric field over the MQW region that constitutes the intrinsic region of the diode, separated from the doped regions by thin spacer layers. The GeSi MQW stack is kept thin (∼140 nm) to facilitate efficient butt coupling to a Si/poly-Si waveguide with total thickness of 380 nm thickness. The diode design features the following three differences with respect to the previously reported architecture [12]: (i) the p-type doping has been suppressed in the region immediately neighboring the MQW. This limits the high electric field in the regions where the MQW ends, which hence avoids reliability concerns due to electric field non-uniformities. Moreover, this will reduce optical losses coming from free carrier absorption (FCA). (ii) The p-region of the diode has been moved further to the top part of the device and consists of two layers, the field confinement layer (FCL) and the top contact layer (TCL). The TCL is highly doped to enable low contact resistance and achieve high speed performance. The FCL is moderately doped to reduce FCA, and to have a uniform electric field distribution over the MQW. (iii) The TCL is partially etched to reduce the metal-induced optical losses. The resulting structure forms a p-i-n diode allowing to apply an intense and uniform electric field across the intrinsic MQW region. Fig. 1(a) shows the schematic cross-section of the previously reported device architecture [12]. Fig. 1(b) and (c) show the new design introduced in this work and a corresponding transmission electron microscope image, respectively. Fig. 1(d) shows a comparison of the electric field distribution over the diode's intrinsic region for the previous (top) and new (bottom) architectures under a bias of −1 V. It could be seen that the new architecture has a uniform field over the whole MQW region, while the old one shows electric field spikes at the edges coming from the top region doping. Notice that the field intensity in the new architecture is less than the old one for the same applied bias, due to the difference in the intrinsic regions thickness.

A. MQW QCSE Stack Design and Absorption Coefficient Simulations

To target an operating wavelength in the O-band, the absorption spectrum of the QCSE MQW should have an absorption edge at a wavelength near 1.31 μm. In our stack, this is achieved by using $Ge_{0.98}Si_{0.02}$ QWs with optimized QW thickness. The thickness and Ge content of the barrier are chosen to allow for the electron confinement in the conduction band and hole confinement in the valence band of the QW, achieving a type-I band alignment at the Gamma point. In addition to that, the MQW (QWs + barriers) was optimized to achieve a strain-balanced structure [13] in which the compressive strain in the QW is compensated by the tensile strain in the barrier, allowing the growth of a plastically stable structure. Therefore, the MQW stack contains 610-nm thick $Ge_{0.98}Si_{.02}$ QWs separated by 11-nm thick $Ge_{0.71}Si_{0.29}$ barriers, whereas the 170 nm thick SRB is composed of $Ge_{0.85}Si_{.15}$. The MQW region is separated from the bottom doped SRB and the top doped regions by intrinsic $Ge_{0.85}Si_{0.15}$ spacers. The TCL and FCL have compositions of $Ge_{0.5}Si_{0.5}$ with lower Ge content than the rest of the stack to lower the optical losses coming from the FCA. Table I summarizes the details of the full stack. To simulate the near edge absorption of the MQW QCSE stack, the nextnano software [21] has been used, leveraging an 8-band K.P method [14].

Fig. 2 shows the simulated MQW absorption spectrum at reverse bias varying from 0 V to 4 V in 1 V steps. The bias is applied only on the intrinsic region of the device (bottom spacer + MQW+ top spacer). In addition to that, in the boundary conditions of this simulation, an 0.11% tensile strain is assumed. This strain develops in the GeSi SRB, due to the large thermal expansion coefficient of Ge. The value is estimated by comparing the theoretical relaxed lattice constant of the GeSi SRB and the measured in-plane and out-of-plane lattice parameters extracted from X-ray diffraction (XRD) measurements. As can be seen, the calculated absorption edges are indeed near 1310 nm. With increasing the bias, the effective band gap

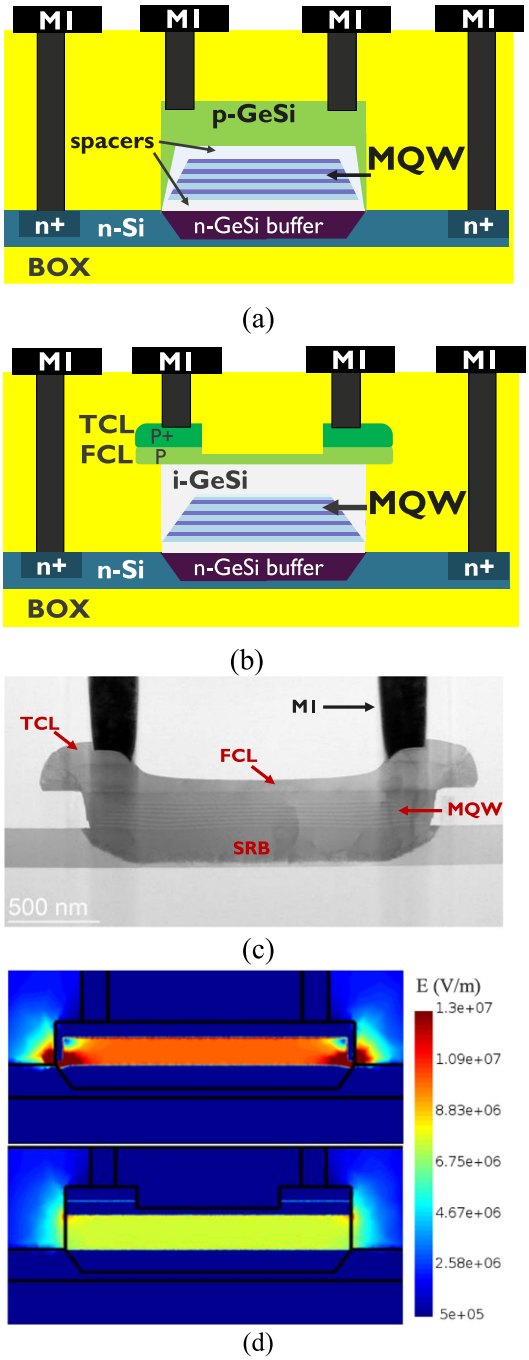

Fig. 1. Schematic of the cross-section of the modulator with (a) the previous architecture and (b) the new architecture. (c) Transmission electron microscope image of the cross-section of a fabricated device of the new architecture. (d) Electric field distribution over the MQW region for the previous architecture (top) and new one (bottom) at −1 V.

between the conduction band (C) and heavy-hole (HH) band decreases. Correspondingly, the absorption peaks shift towards lower energies (longer wavelength). Also, the absorption peak decreases and get broader since the applied bias pushes the electron and hole in opposite directions. Therefore, the exciton is more ionized and the overlap integral between the electron and hole wavefunctions decreases, hence the intensity of the absorption peak decreases and the peak broadens.

TABLE I
O-BAND GESI MQW STACK DESIGN

Layer		Composition	Doping concentration (cm^{-3})	Thickness (nm)
TCL		p^+- $Ge_{0.5}Si_{0.5}$	2.6×10^{20}	100
FCL		p -$Ge_{0.5}Si_{0.5}$	4×10^{19}	100
Top spacer		i-$Ge_{0.85}Si_{0.15}$	-	60
6x	Barrier	i-$Ge_{0.71}Si_{0.29}$	-	11
	QW	i-$Ge_{0.98}Si_{0.02}$	-	10
Barrier		i-$Ge_{0.71}Si_{0.29}$	-	11
Bottom spacer		i-$Ge_{0.85}Si_{0.15}$	-	20
Buffer		n-$Ge_{0.85}Si_{0.15}$	2×10^{18}	170

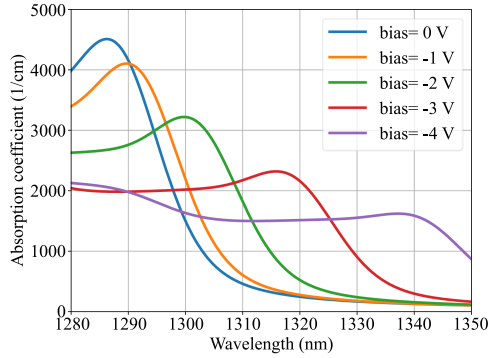

Fig. 2. Simulation of the absorption curves of the MQW stack described in Table I using nextnano software [21].

B. Fabrication Process

The device fabrication steps are summarized in Fig. 3. The SOI wafer (300 mm) is implanted with Phosphorous ions (P) to form n-doped bottom contacts. Silicon dioxide (SiO_2) is deposited and planarized, followed by wet etching to form the cavity in the Si waveguide. The wafer is then cleaned and introduced in an ASM Intrepid™ CVD reactor. After a short pre-epitaxial bake at 850 °C, the different epitaxial layers are selectively grown in the cavity of the Si waveguide. This is achieved by reduced-pressure chemical vapor deposition (RP-CVD) using conventional Ge and Si precursors. The epitaxial process starts with growing a 170-nm thick n-doped $Si_{0.15}Ge_{0.85}$ SRB layer (using PH_3 as dopant source) with subsequent anneal to reduce the TDD. Then, a 20-nm intrinsic bottom spacer layer of $Si_{0.15}Ge_{0.85}$ is grown. Afterwards, the MQW structure is grown following the strain balancing strategy described in previous section to minimize strain build-up along the epitaxial stack. Then, an intrinsic 60-nm $Si_{0.15}Ge_{0.85}$ layer is grown as a top spacer. However, it is overgrown (by controlling the growth time) to ensure the complete filling of the cavity as shown in Fig. 3(d). Then, a chemical mechanical polishing (CMP) process is used to obtain a flat top surface level with the surrounding oxide. To avoid degradation of the underlaying QCSE stack, the

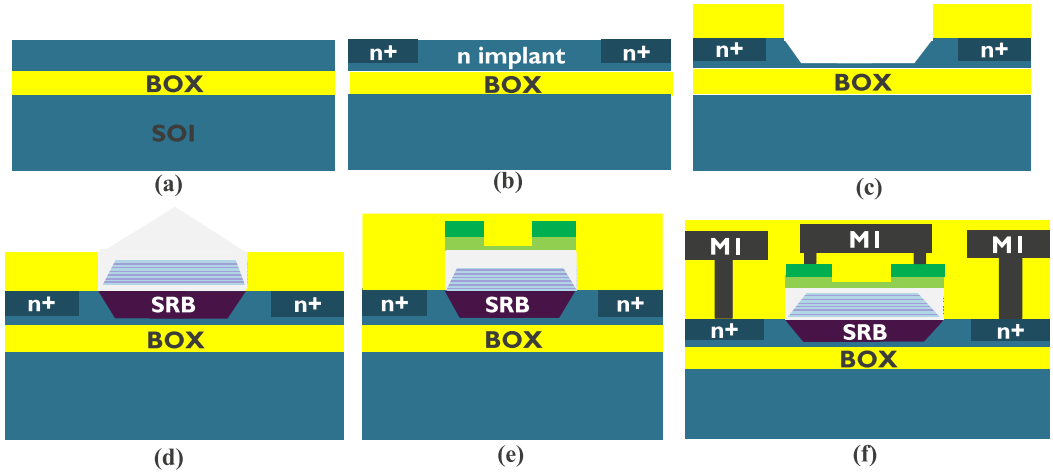

Fig. 3. Cross-section schematics describing the fabrication process flow of the device shown in Fig. 1(b). (a) Starting SOI wafer, (b) P ion-implantation for bottom contact formation, (c) wafer etching to form the Si waveguide cavities in the, (d) SRB, bottom spacer, and MQW growth, followed by top spacer overgrowth, (e) CMP followed by FCL and TCL overgrowth and partial etching, (f) Metal contacts and BEOL.

next p-doped $Si_{0.50}Ge_{0.50}$ bilayer (FCL+TCL) layers are grown at low temperature (<450 °C) after a cleaning routine is applied. The TCL is etched away in the central region of the cavity later in the process flow. The diode is contacted by metal plugs (M1) with shallow penetration in the TCL and in the n-Si substrate before continuing the process flow with the formation of conventional back-end-of-line (BEOL) contacts and interconnects.

III. Modulator Static Performance

Fig. 4(a) shows the measured IV characteristics for a 2 μm wide and a 36.8 μm long device. Dark currents of 20 nA, 0.4 μA, are measured at -1 V and -4 V bias, respectively. To measure the IL of the device, light is coupled from a tunable laser source to the device through grating couplers. Fig. 4(b) shows the measured insertion loss (IL) from 1310 nm to 1350 nm for the TE-polarization at 25 °C and for biases ranging from 0 V to -4 V in 0.5 V steps with -1 dBm input optical power. The IL includes two main contributions, the coupling loss (CL) between the Si waveguide and the GeSi waveguide, and the propagation loss (PL) along the device length. The PL includes the metal-induced losses coming from the top metal contacts, the loss due to FCA in the doped regions of the diode, the residual background loss (indirect bandgap absorption in GeSi, scattering loss, defects-induced loss), and the QCSE absorption from the MQW stack. The IL does not include losses occurring in the grating couplers as the measured IL spectra are normalized to the transmission spectrum of a neighboring reference waveguide. Fig. 4(c) shows the ER extracted from the measured IL for different bias voltage swing. An ER of ~5 dB is extracted at a wavelength of 1340 nm at 2 V peak-to-peak (between -1 V and -3 V), with a corresponding IL of 7.5 dB. To quantify the operational wavelength range of the modulator, the transmitter penalty (TP) is evaluated. The TP includes the IL, and the penalties due to limited ER [8]. It is defined as TP (dB) $= -10\log((P_1\text{-}P_0)/2P_{in})$, where P_1 and P_0 are the high-level and low-level transmitted optical power at 1-bit and 0-bit, respectively, and P_{in} is the input optical power. Fig. 4(d) show the TP corresponding to the IL shown in Fig. 4(b) at 2 V peak-to-peak. A minimum TP of ~12 dB is obtained around 1340 nm, at -1 V bias and 2 V swing, with a corresponding 1 dB bandwidth of around 20 nm (1330 nm–1350 nm) as shown in Fig. 4(d). This TP value is several dB worse than the TP in optimized C-band GeSi FK EAMs, which have a TP of 8.5 dB for 2 Vpp. To shift the minimum TP operating point towards 1310 nm, the MQW design needs to be adjusted by reducing the QW thickness to 9 nm or lowering the Ge content in the QW to 97%. Both will result in a blue shift of the exciton absorption peak due to a decrease in the bandgap.

Next, wafer-scale measurements are performed to analyze the within-wafer variability of the minimum TP (TPmin), and the IL and ER at that wavelength, the wavelength where maximum ER occurs, the CL, and the PL. The analysis is done for 78 dies measured on a 300 mm wafer. Fig. 5 shows a wafer-map of the extracted TPmin at 2 Vpp (between -1 V and -3 V). TPmin has a median value of 13.1 dB and a standard deviation (SD) of 1.31 dB. The best values for TPmin are located mostly in the center of the wafer, while the worst values of the TPmin are located at the wafer edges. Fig. 6 shows a wafer map of the measured IL, having a median value of 7.9 dB and a SD of 0.98 dB. The lowest IL values are measured in the center of the wafer, coinciding with dies having the lowest TPmin. Fig. 7 shows a wafer map of the ER at 2 Vpp (between -1 V and -3 V) corresponding to the TPmin. The ER has a median value of 4.13 dB and a SD of 0.89 dB. The low ER values are located at the wafer edges, at the same locations with high TPmin. Hence, the high values of the TPmin are due to the limited ER for the devices measured at the dies at the right and top right wafer edge. Furthermore, Fig. 8 shows a wafer map for the wavelength of maximum ER at 2 Vpp (between -1 V and -3 V), where the wavelength ranges between 1310 nm and 1341 nm with a SD of 10 nm. A center-to-edge variability is observed, likely due to a variation of the QW thickness and/or the QW Ge% across the wafer. A tighter range for the optimum operation wavelength

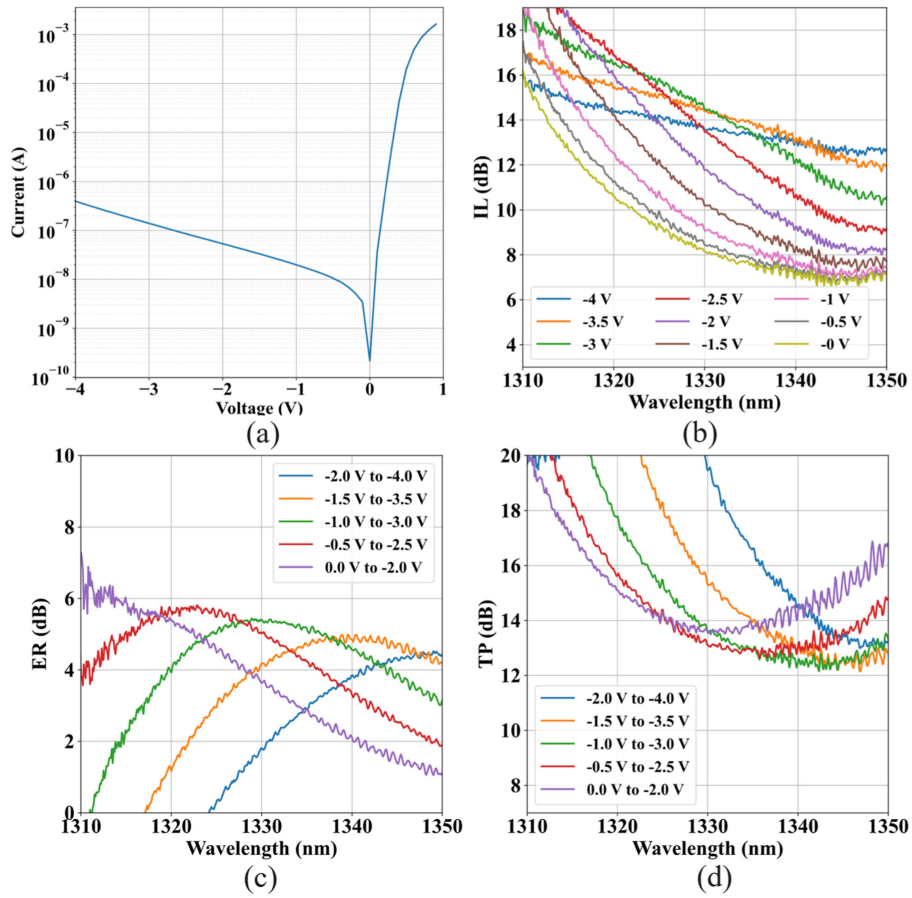

Fig. 4. (a) Measured IV characteristics and (b) insertion loss measured for the device described in Fig. 1(b). (c) Extracted ER and (d) TP for 2 V swing for devices with length of 36.8 μm and width of 2 μm.

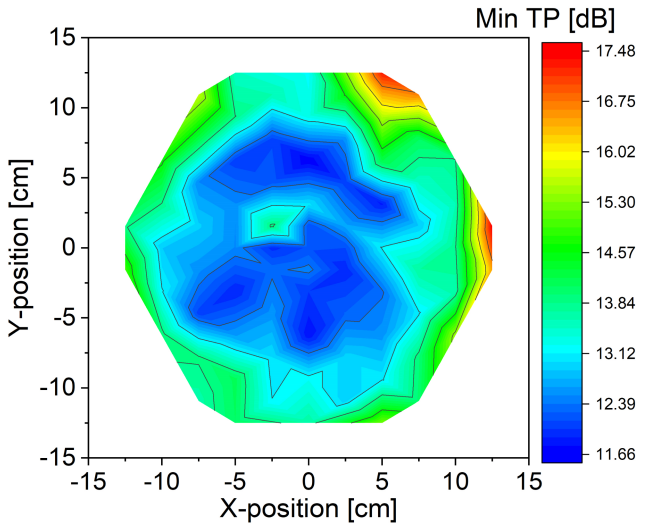

Fig. 5. Wafer-map of the minimum TP at 2 Vpp (between −1 V and −3 V) for 78 measured dies on 300 mm SOI wafer.

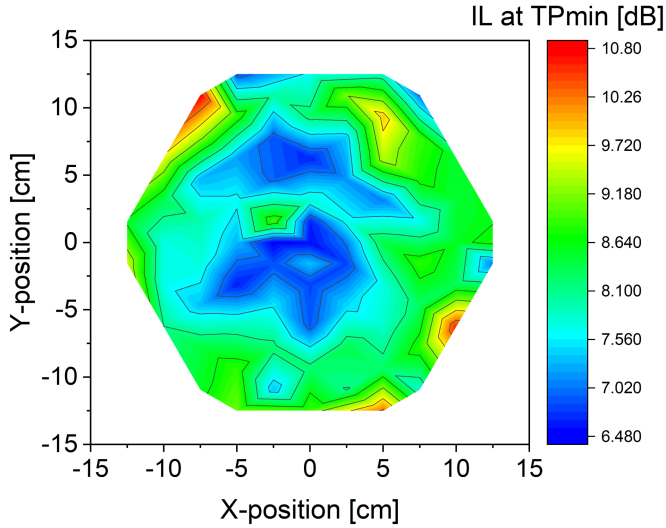

Fig. 6. Wafer-map of the IL at minimum TP for 78 measured dies on 300 mm SOI wafer.

can likely be obtained by improving the within-wafer variability of the QCSE stack. To analyze the IL of the modulator, we need to break the IL down into its two components, CL, and PL. To extract the CL between the Si waveguide and the EAM waveguide, we extrapolate the IL to 0 based on a linear regression of IL with respect to device length. Fig. 9 shows a wafer map of the extracted CL at wavelength of 1330 nm. The median value of the extracted CL is ∼4 dB with a SD of 1.19 dB. The dies

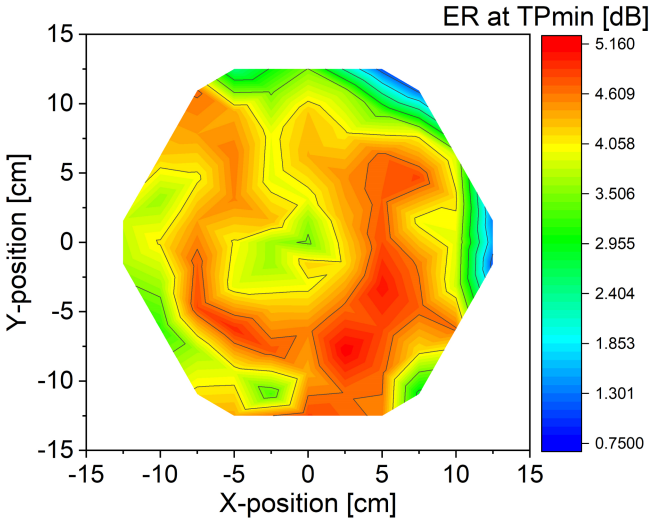

Fig. 7. Wafer-map of the ER at minimum TP for 78 measured dies on 300 mm SOI wafer.

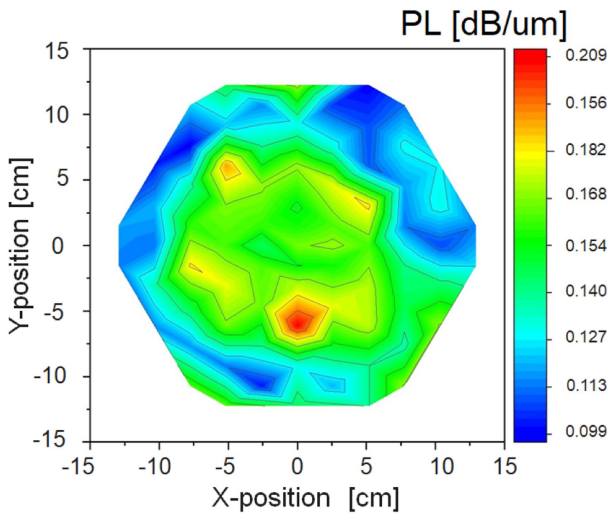

Fig. 10. Wafer-map for the extracted propagation loss (PL) at bias = 0 V and wavelength of 1330 nm, for 78 measured dies on 300 mm SOI wafer.

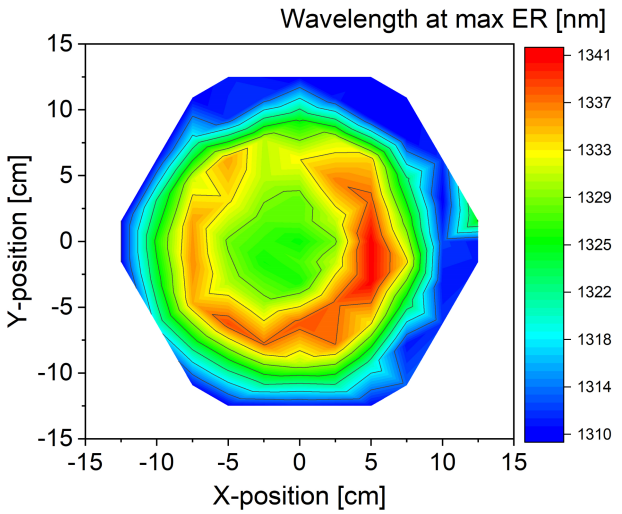

Fig. 8. Wafer-map for the wavelength corresponding to the minimum TP for 78 measured dies on 300 mm SOI wafer.

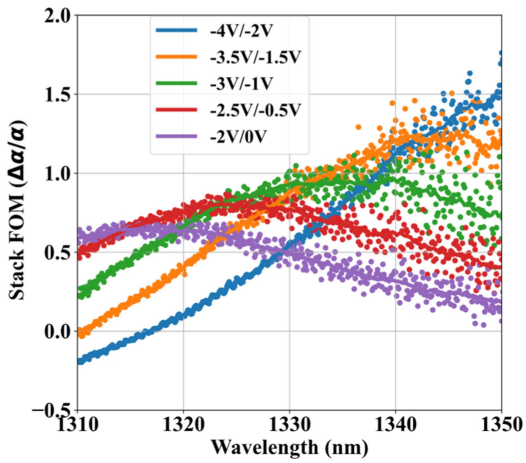

Fig. 11. MQW stack FOM ($\Delta\alpha/\alpha_{ON}$) extracted from propagation loss as a function in wavelength.

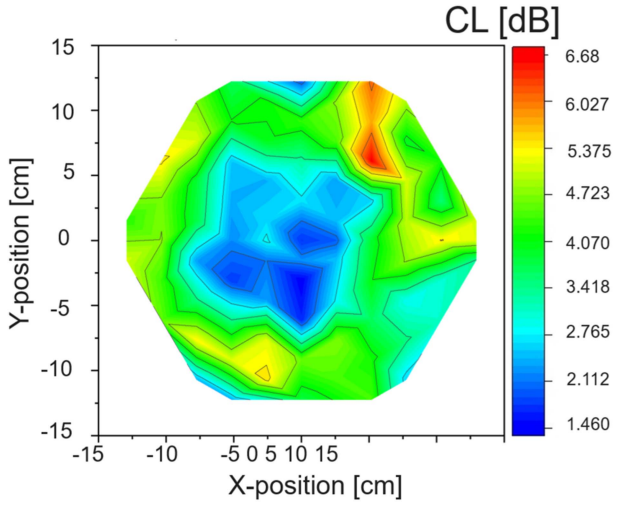

Fig. 9. Wafer-map for the extracted coupling loss at wavelength of 1330 nm for 78 measured dies on 300 mm SOI wafer.

with low CL (<2 dB) are located at the center of the wafer, which coincides with the same locations of the low TPmin and low IL in Figs. 5 and 6, respectively. The PL is also extracted, and Fig. 10 shows a wafer-map of the PL showing a median value of 0.15 dB/μm at 1330 nm with a SD of 0.02 dB/μm. The PL is a result of different contributions as explained earlier. The proposed improvement of the device design presented in Section II has

One of the important figures-of-merit (FOM) of the QCSE stack is $\Delta\alpha/\alpha_{ON}$, where $\Delta\alpha = \alpha_{OFF} - \alpha_{ON}$ is the difference in the absorption coefficient between the OFF state (high electric field and high absorption), and the ON state (low electric field and low absorption). $\Delta\alpha/\alpha_{ON}$ is more intrinsic FOM of the device that does not include the CL. It is extracted from the propagation loss as a function of wavelength, and it is shown in Fig. 11. The FOM peak between -1 V and -3 V reaches $\sim$1 at wavelength of $\sim$1335 nm, whereas at higher bias voltages, it improves to $\sim$1.5. This FOM is limited by the absorption

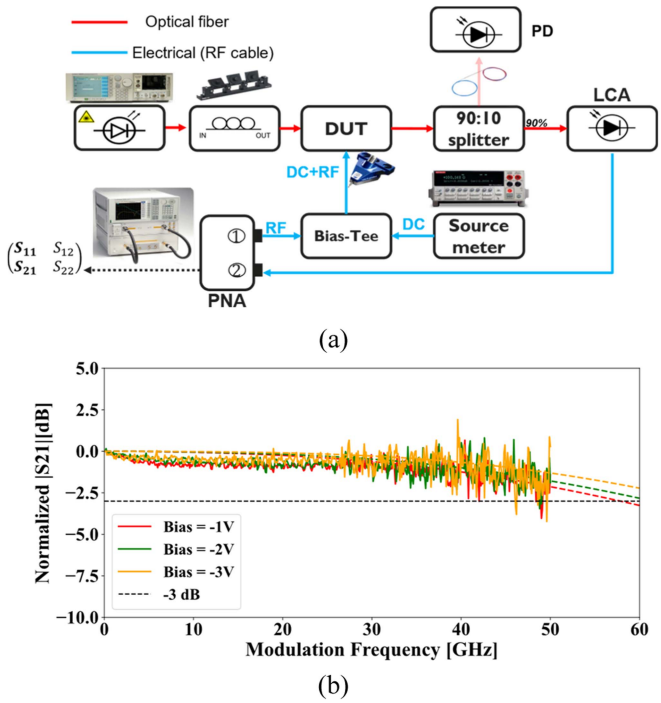

Fig. 12. (a) The experimental setup for the RF measurements. (b) Measured and simulated (dashed line) electro-optical S_{21} frequency response for the QCSE EAM.

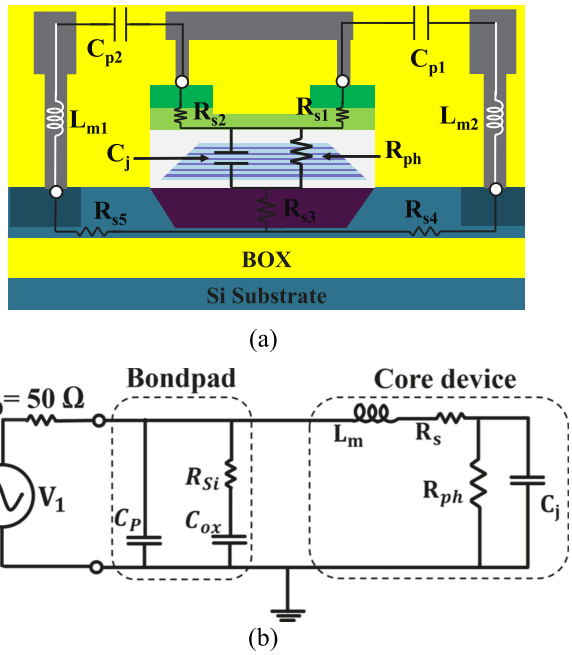

Fig. 13. (a) RLC network representation of the QCSE EAM. (b) Lumped-element circuit model used for S_{11} fitting.

mechanisms such as FCA and the other background loss discussed at the beginning of this section. Furthermore, material defectivity could play an important role, since the use of thin buffer layers (∼200 nm) leads to TDD higher than 10^9 cm^{-2} [22]. As a comparison, for the C-band FK EAM, the $\Delta\alpha/\alpha_{ON}$ is typically 1.25 for a similar applied electric field swing of 60 kV/cm [23].

The wafer-scale analysis shows that devices with the best performance (min TP, min IL, and max ER) are located the center of the wafer. The overall performance of the devices could be improved by reducing the IL (CL and PL) and increasing the ER (enhancing stack FOM). Improving the CL would require improving the process flow to mitigate any issue happening at the poly-Si/EAM interface [24]. Possible pathways to increase the stack FOM and reduce TPmin in future work is by reducing the PL from the doping and from the indirect-bandgap absorption in the $Si_{0.15}Ge_{0.85}$ layers, i.e., by considering a QCSE stack with lower Ge content in the SRB, barrier, and spacer regions.

IV. Modulator High-Speed Performance

The electro-optic high-speed performance of the QCSE EAM is demonstrated by measuring the 3 dB bandwidth using 50 GHz lightwave component analyzer (LCA). The RF measurement system is calibrated before the measurements to normalize the effects coming from the setup (cables, bias-tee, RF probe, and the photodetector (PD)). Fig. 12(a) shows the experimental setup. The light coming from the tunable laser source passing through a polarization controller is coupled to the device under test (DUT). 90% of the output light goes to the LCA, and the other 10% goes to the PD to monitor the power of the output light. The LCA transforms the modulated optical signal to an electrical one, and it goes to the performance network analyzer (PNA). We apply the RF and the DC signals to the DUT by using the bias-Tee. Fig. 12(b) shows the typical S_{21} electro-optical frequency response with various reverse bias levels with an input optical power of 1 dBm at operating wavelength of 1320 nm. The 3 dB bandwidth of the QCSE EAM is larger than 50 GHz, which is the bandwidth limitation of the LCA. Since the QCSE effect is a very fast mechanism, operating at picosecond timescales [25], [26], the 3 dB bandwidth of the QCSE EAM is limited by the RC time constant of the device. Under reverse bias, the intrinsic region thickness of the PIN junction increases because of the depletion. The larger intrinsic region yields smaller junction capacitance and so the speed of the device increases with higher bias, as can be seen in Fig. 12(b).

More insights about the device performance can be obtained considering its equivalent circuit model. The model is derived from the device cross section shown in Fig. 13(a). The model was used to fit the measured RF S_{11} and extract the device electrical parameters. The circuit model shown in Fig. 13(b) takes into account two contributions, the bondpad, and the core p-i-n device. It also considers a 50 Ω internal impedance (Z_0) of the RF driver. The bondpad contribution is de-embedded from the device through performing separate S_{11} measurements to the pad to extract its components and fixing its values in the device fitting procedures. C_p is the capacitance between the two pads, C_{ox} is the capacitance between the two pads and the Si substrate, and R_{si} is the resistance through the Si substrate between the two pads.

The model representing the core device is composed of four components, (1) the metal lines impedance L_m, (2) the series

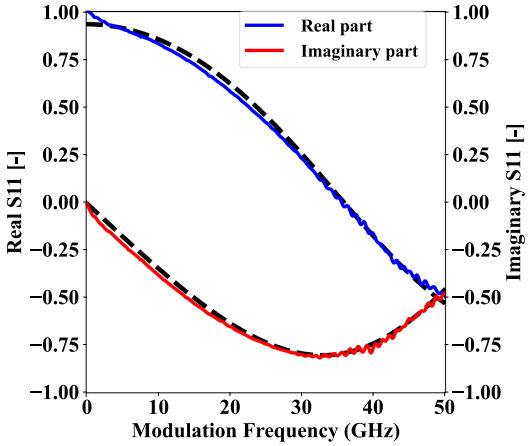

Fig. 14. S_{11} fitting using the circuit model shown in Fig. 13(b) for the real and imaginary part for parameter extraction at −3 V.

TABLE II
EXTRACTED ELECTRICAL PARAMETERS OF THE EAM EQUIVALENT CIRCUIT MODEL FROM FITTING TO S_{11} AT BIAS OF −3 V

Parameter	Value
C_p (fF)	3.7
C_{ox} (fF)	36
R_{si} (Ω)	1470
L_m (pH)	100
R_s (Ω)	8.3
C_j (fF)	57
R_{ph} (Ω)	1456

resistance of the device R_s that accounts for the resistance of the different device layers, and the ohmic contact resistance at the electrodes, (3) the device junction capacitance C_j, and (4) the photocurrent generated in the device due to the optical absorption inside the intrinsic region. The photocurrent is represented as a current path, and the impedance of this current path can be represented by a resistance (R_{ph}) parallel to the junction capacitance [27], [28]. The measured S_{11} data was fitted using the circuit model presented in Fig. 13(b) and the result is shown in Fig. 14. The S_{11} was measured at 1320 nm wavelength and −3 V bias. A good agreement between the measured S_{11} and the fitted model (dashed lines) is obtained. The extracted junction capacitance, and series resistance are 57 fF and 8.3 Ω, respectively. All extracted parameters are presented in Table II. To validate the model, we used the parameters extracted from the S_{11} fitting to simulate the S_{21} response. The simulated results, shown in Fig. 12(b), align well with the measured data. The model expects a 3 dB bandwidth of ∼58 GHz at −1 V.

The large signal modulation performance of the device is presented in Fig. 15. A non-return-to-zero on-off keying (NRZ-OOK) pseudorandom binary sequence (PRBS) signal with a pattern length of 2^{31}-1 with different data rates was generated using a bit pattern generator (SHF 12105 A). The signal was applied to the device using a 50 Ω terminated 67 GHz RF probe.

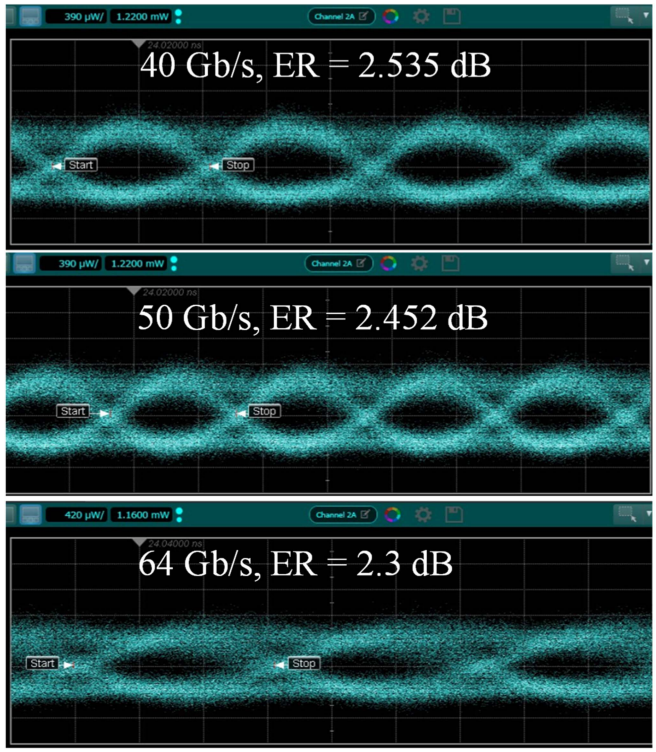

Fig. 15. Measured eye diagrams at 1320 nm and −1 V with 2 Vpp for data rates of 40 Gb/s, 50 Gb/s, and 64 Gb/s NRZ-OOK.

The modulated output signal was amplified using an O-band praseodymium-doped fiber amplifier (PDFA) before reaching the oscilloscope. The measured eye diagrams were obtained at 1320 nm wavelength with an input optical power of 0 dBm and a bias voltage of −1 V. Open eye diagrams are measured at 40 Gb/s, 50 Gb/s, and 64 Gb/s with a dynamic ER of 2.535 dB, 2.452 dB, and 2.3 dB, with a 2 Vpp respectively.

V. DISCUSSION & CONCLUSION

In this work, we have demonstrated O-band GeSi QCSE EAMs integrated in a 300 mm Si photonics platform. The new proposed device architecture has experimentally showed better performance compared to the previous one. The modified doping profile of the TCL lowered the contact resistivity of the metal contact, leading to enhanced device speed. Additionally, etching the top region has pushed the optical guided mode away from the top metals, reducing the metal-induced optical losses. Furthermore, the reduction of p-type doping in the areas adjacent to the MQW regions has significantly decreased dark current and addressed reliability concerns, as evident in the consistent EAM performance across the 300 mm SOI wafer. The best performing QCSE EAMs show an IL of 7.5 dB, an ER of 5 dB and a TP of 12 dB at wavelength of 1340 nm. The QCSE stack FOM ($\Delta\alpha/\alpha_{ON}$) is ∼1–1.5 at 2 Vpp. The modulator showed 3 dB bandwidth beyond 50 GHz, and the extracted junction capacitance and the series resistance from the equivalent circuit model at −3 V are 57 fF and 8.3 Ω, respectively. The large signal performance of the modulator showed open and wide eyes at

data rates up to 64 Gb/s at 1320 nm wavelength with 2 Vpp. Wafer-scale DC analysis was performed for 78 measured dies across the 300 mm SOI wafer. The minimum TP has a median of 13.1 dB and a SD of 1.31 dB, with corresponding IL of median value of 7.9 dB and a SD of 0.98 dB, and corresponding ER of 4.13 dB median value and a SD of 0.89 dB. The CL has a median of 4 dB with a SD of 1.19 dB, and the PL has a median of 0.15 dB/μm with a SD of 0.02 dB/μm. The best performing devices are located at the center of the wafer, and enhancing the QCSE stack FOM is a key parameter for future improvement.

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