Graphene-based Silicon Photonic Electro-Absorption Modulators and Phase Modulators

Chenghan Wu, Tom Reep, Steven Brems, Didit Yudistira, Joris Van Campenhout, Inge Asselberghs, Cedric Huyghebaert, Marianna Pantouvaki, Zheng Wang, and Dries Van Thourhout, *Member, IEEE*

***Abstract*—Since their first demonstration, graphene-based silicon waveguide modulators have evolved towards very attractive devices for adoption in future optical interconnects. In this paper, we first review state-of-the-art for graphene-based intensity modulators. Two important device configurations are considered: one using a single graphene layer, biased through the silicon waveguide itself and one using a capacitive stack of two graphene layers, which can be integrated on passive silicon and silicon nitride waveguides. We also discuss our recent work on fabricating such devices fully in a CMOS pilot line. In a next section, we review graphene-based phase modulators. Again, we compare the two types of modulators, involving a single or double graphene layer stack. In addition, we present new results, comparing modulators integrated on standard strip waveguides with modulators integrated on slot waveguides, which allow for a higher confinement of the optical field. Finally, we summarize our findings and present and outlook for the field, based on simulated results.**

***Index Terms*—Graphene, modulator, silicon photonics.**

I. INTRODUCTION

THE digital landscape is currently undergoing a remarkable transformation, driven by the relentless surge in data generation and consumption. Today, the ease with which people can seamlessly share, create, and consume information across a multitude of social media platforms is nothing short of astounding. In 2022, the utilization of data worldwide reached an 97 zettabytes, with forecasts pointing towards a substantial escalation to 181 zettabytes by 2025[1]. Additionally, a further leap is expected now Artificial Intelligence (AI) enters the stage. From revolutionizing communication and entertainment to making significant inroads in healthcare, finance, and transportation, the profound impact of AI is reshaping the way we live and interact with our surroundings.

In this evolving era of data and AI, data centers stand out as the unsung heroes of the digital age. Operating behind the scenes, they constitute the invisible infrastructure backbone that diligently supports our data-driven world. Data centers provide the critical framework required to store, process, and transmit this colossal volume of data efficiently and securely. The global data center market size is projected to grow by over $600 billion from 2021 to 2026, according to a recent report from Technavio, highlighting their significant market presence and indispensable role in realizing our digital aspirations. However, this pivotal role comes with its set of challenges, especially amidst the exponential increase in data generation and consumption. One primary challenge is the imperative to reduce power usage while handling a growing volume of data. Globally, data centers account for an annual 1%–1.5% of total worldwide electricity consumption, as outlined in studies[2, 3] These numbers already surpass the electricity consumption of some entire nations, according to the International Energy Agency (IEA). Furthermore, the forecast suggests that this staggering demand could more than triple by 2030, rocketing to an astonishing 752 terawatt hours (TWh)[4].

This energy consumption stems primarily from the vast array of computing equipment—ranging from thousands to millions of units—incessantly engaged in the processing and storage of data. At the same time, data centers generate substantial heat. To prevent overheating and maintain optimal equipment temperature, data centers rely on cooling systems including air conditioning and industrial cooling units. The operation and cooling of these machines necessitates a substantial supply of electricity. Complicating matters further, electrical interconnects face formidable integration challenges, particularly over shorter ranges. Attempts to put more wires within confined spaces have resulted in reduced wire width, consequently elevating resistance. Although increasing wire height appears to be a potential solution, it introduces a delicate trade-off, as it concurrently escalates capacitance and invites unwanted signal coupling[5]. These challenges collectively conspire to limit the speed and overall quality of

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 881603 (GrapheneCore3) and grant agreement No 952792 (2D-EPL) *(Corresponding author: Zheng Wang and Dries Van Thourhout).*

Chenghan Wu, Tom Reep and Dries Van Thourhout are with the Photonics Research Group, Department of Information Technology, Ghent University-imec, 9052 Ghent, Belgium. (e-mail: chenghan.wu@ugent.be, dries.vanthourhout@ugent.be).

Steven Brems, Didit Yudistira, Joris Van Campenhout, Inge Asselberghs are with imec, 3001 Leuven, Belgium.

Cedric Huyghebaert was with imec, 3001 Leuven, Belgium. He is currently with Black Semiconductor GmbH, Aachen, Germany (email: cedric.huyghebaert@blacksemicon.de)

Marianna Pantouvaki was with imec, 3001 Leuven, Belgium. She is currently with Microsoft UK (email: mpantouvaki@microsoft.com).

Zheng Wang was with the Photonics Research Group, Department of Information Technology, Ghent University-imec, 9052 Ghent, Belgium. He is now with State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 865 Changning Road, 200050 Shanghai, China. (e-mail: zheng.wang@mail.sim.ac.cn).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org

electrical interconnects[6-8]. As a result, the imperative of swiftly transferring, storing, and processing vast volumes of data, all while maintaining exceptionally low power consumption (less than 1 pJ/bit), has emerged as the driving force behind the advancement and adoption of optical interconnects. As an alternative to their electrical counterparts, optical interconnects could offer reduced signal loss, higher bandwidth, lower energy consumption, and minimal crosstalk[9].

Silicon photonics (SiPh) is a cutting-edge technology that aims to combine silicon-based materials with integrated circuit manufacturing techniques to realize chip-scale solutions to optical interconnects[10, 11]. Leveraging established CMOS fabrication processes, silicon photonics is now poised for cost-effective, high-volume production with exceptional yields[12]. Furthermore, the direct definition of optical components and circuits onto silicon substrates enables the seamless integration of optical and electronic functionalities on a single chip, facilitating high-speed data transmission and minimizing power consumption. Electro-optical (EO) modulators play a pivotal role in the efficacy of high-capacity optical interconnects. An optimal EO modulator should embody key characteristics, encompassing a significant extinction ratio (ER), minimal insertion loss (IL), rapid operational speed, and low power consumption. It is also advantageous for the device to possess a compact footprint and necessitate a low driving voltage, aligning seamlessly with CMOS circuitry. For modulators integrated into high-density systems, reliability, reproducibility, and compatibility with prevailing CMOS manufacturing techniques are essential prerequisites. However, it is challenging to meet abovementioned criteria simultaneously using pure silicon-based modulators[13]. Recently, graphene has emerged as a particularly promising optical material because of its exceptional electrical[14-16] and optical properties[17, 18]. These include broad-spectrum absorption, inherent ultra-high mobility, robust temperature tolerance, and compatibility with CMOS technology. These features collectively position graphene as an excellent candidate for realizing high-performance, high-speed EO modulators[13, 19, 20].

In this paper, we present a review of state-of-the-art graphene-based SiPh EO modulators, extended with some recent results obtained within our own group. In Section II, we review graphene-based electro-absorption modulators (EAMs). Two mainstream approaches to realize graphene-based EO modulators, the single-layer graphene (SLG) and dual single-layer graphene (DLG) modulator, are introduced. The SLG structure requires a doped silicon waveguide to gate the graphene, while the DLG can be implemented on to a passive Si waveguide and even a silicon nitride (SiN) waveguide. We also discuss our recent work on fabricating such devices fully in a CMOS pilot line. Following this, in Section III, graphene-based phase modulators will be introduced and our recent results on DLG phase modulators are presented. Finally, in Section IV, we provide a summary and future perspectives for graphene-based SiPh EO modulators.

II. Graphene-based Electro-Absorption Modulators

One of the most straightforward methods for encoding light signals with electrical bits involves manipulating the light intensity through the use of an EAM. Such modulators are constructed with materials that can alter their absorption in response to an external electric field. Currently, germanium-based EAMs are the predominant choice in SiPh applications and have shown low-power operation at high data rates (>50Gbit/s). Their main drawback is their strong wavelength dependence [21, 22]. In contrast, graphene exhibits ultra-broadband optical absorption, spanning from visible to THz wavelengths. Additionally, the Fermi level of graphene can be adjusted by an external electric field. Once the Fermi level exceeds half the photon energy, Pauli blocking inhibits photon absorption and renders graphene transparent. Combined with graphene's impressive carrier mobility, this opens the possibility of creating high-speed modulators[17, 18].

A. Single-layer Graphene Electro-Absorption Modulators

To construct graphene-based EAMs, forming a capacitor for gating the graphene and shift the Femi level is essential. The initial implementation of this concept involved an SLG positioned on a doped Si waveguide with a dielectric spacer. In 2011, Liu et al. from UC Berkeley for the first time experimentally demonstrated an SLG EAM[23]. In their device, an SLG was transferred onto a non-planarized p-type doped Si waveguide with dimensions of 250 nm in height and 600 nm in width. The waveguide was patterned using electron beam lithography (EBL) and subsequent dry etching. Between the SLG and the waveguide, a 7 nm aluminum oxide (Al_2O_3) layer served as the isolation layer. The structure is illustrated in Fig. 1(a). Their 40 μm long SLG EAM provided a 4 dB static modulation depth under a 4 V bias, translating to a static modulation efficiency of ~ 25×10^{-3} $dB\cdot\mu m^{-1}\cdot V^{-1}$. Small signal measurements were conducted to evaluate the high-speed performance of the modulator. A 3-dB bandwidth of 1.2 GHz was achieved at a -3.5V bias, limited by the high resistance of the lightly doped silicon layers. Although these results were not competitive with those obtained for SiPh modulators employing the plasma dispersion effect at that time, this work paved the way for the integration of graphene and other low-dimensional materials with SiPh.

To meet the requirements of large-scale SiPh chip manufacturing, the development of a CMOS compatible graphene integration process is highly desired. In 2016, our team demonstrated SLG EAMs by using SiPh chips fabricated in a standard 8-inch (200-mm) SiPh pilot line[24]. Standard 8-inch silicon-on-insulator (SOI) wafers with 2 μm buried oxide (BOX) and a 220 nm top silicon layer were used. In our devices, Si waveguides were defined with deep ultra-violet (DUV) lithography and dry etching. After oxide deposition, the wafers were planarized with chemical-mechanical planarization (CMP) for graphene integration. In addition, three phosphorous ion implantation steps were performed to

reduce device resistance. A 5 nm thick silicon oxide was thermally grown on top of the Si waveguide to serve as the isolation layer to build a SLG-oxide-Si capacitor, as depicted in Fig.1(b). A quasi-TM waveguide with dimensions of 220 nm in height and 750 nm in width was chosen to improve the light-matter interaction. A static modulation depth as large as 5.2 dB was achieved with a 50 μm long SLG EAM. Thanks to the multiple step doping process, the 3-dB bandwidth was increased to approximately 5.9 GHz. To evaluate the potential of the devices for integration with CMOS drivers, a 2.5 V peak-to-peak (Vpp) swing voltage was adopted for the eye-diagram measurements. A dynamic ER of ~2.34 dB was measured for 10 Gb/s signals at 1550 nm. The eye-diagram measurements were performed for various wavelengths ranging from 1530 nm to 1565 nm to demonstrate the ability of broadband operation. Additionally, an evaluation of the thermal stability was conducted. The devices showed temperature independent operation from 20℃ to 49℃, with predictions extending up to 175℃. The successful integration of graphene onto small coupons diced from a standard 200 mm wafer formed an initial milestone toward achieving large-scale graphene-based SiPh optical interconnects. Following this work, in 2020 also five-channel wavelength-division multiplexing (WDM) transmitters were demonstrated by integrating a micro-ring based wavelength-division multiplexer with SLG EAMs [25]. To enhance the robustness of the SLG EAMs and reduce the hysteresis, a 10 nm thick Al_2O_3 layer was deposited on top of the graphene layer as a passivation layer, as shown in Fig. 1(c). In our experiments, a 3-dB bandwidth as high as 9.5 GHz was successfully achieved with a 100 μm long SLG EAM. A total transmission rate of 125 Gbps (5 × 25 Gbps) could be achieved with a swing voltage V_{pp} = 2.5 V.

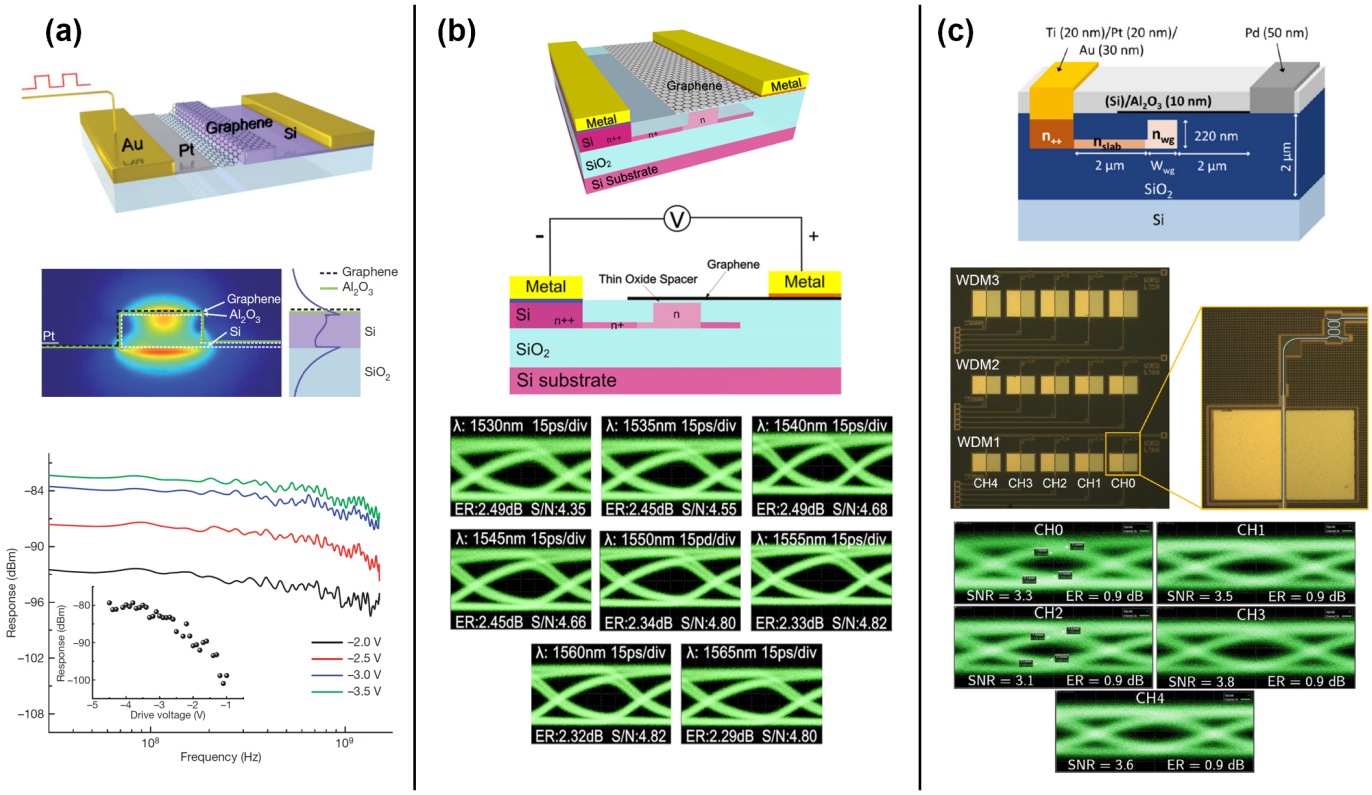

Figure. 1. (a) Schematics of the first SLG EAM fabricated with EBL and the dynamic electro-optical response of the device. Figures are adopted from [23]. (b) Schematics of the first SLG EAM on a SiPh chip fabricated in a standard SiPh foundry and eye diagrams of the device (measured at 10 Gbit/s). Figures are adopted from [24].). (c) Schematics of graphene-based WDM transmitters (with SLG EAMs) and eye diagrams of the device (measured at 25 Gbit/s). Figures are adopted from[25].

Recently, our team established a wafer-scale graphene integration process within a 12-inch (300-mm) CMOS pilot line[26]. In this process, a 6-inch large graphene sheet was transferred onto a 12-inch large SOI wafer. The integration flow started from 300-mm SOI wafers with a 220 nm crystalline Si layer and a 2 μm BOX. Standard 193 nm immersion lithography and dry etching were used for pattering Si waveguides. We optimized the CMP process to minimize the topography of the SOI wafer for the wafer-scale graphene transfer. Then the 6-inch CVD-grown graphene was transferred to the middle of the 12-inch wafer by Graphenea using a semi-dry technique. Then an Al_2O_3 passivation layer was deposited using an atomic layer deposition (ALD) process. Given the self-passivating properties of graphene, a low-temperature surface physisorption based “soak” method with tri-methylaluminum (TMA) as the precursor was used to

create a dielectric seeding layer before the ALD process. To pattern the Al_2O_3 and graphene layers, we employed a standard photolithography process with a silicon dioxide (SiO_2) hardmask. This approach ensures high throughput and cost-effectiveness. After the graphene patterning, a pre-metal dielectric (PMD) was deposited and planarized by CMP, following a standard CMOS flow. The contacts to both the graphene and the doped silicon layers were defined with a CMOS Ti/TiN/W damascene metallization process. We over-etched the oxide layer and created edge contacts on the graphene layer. Finally, the integration flow was finished with a conventional CMOS Cu damascene metallization process. We achieved an average modulation depth of 50 ± 4 dB mm^{-1} under 6V bias from measuring over 400 SLG EAMs, equivalent to an average modulation efficiency ~ 8.3±0.7 $\times 10^{-3}$ dB·μm^{-1}·V^{-1}. An electro-optical bandwidth of 15.1 ± 1.8 GHz was obtained from measuring 29 devices with 25-μm long SLG. Despite a lower modulation efficiency, which can be attributed to the device capacitance and the selected mode (quasi TE), our DC and frequency response results are comparable to the best lab-based devices reported with similar designs and CVD graphene quality.

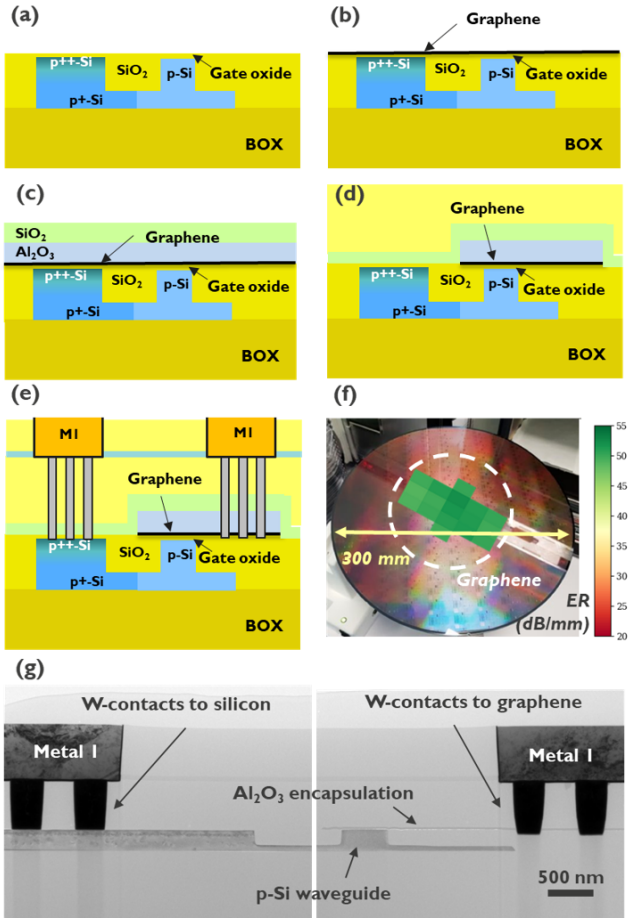

Figure. 2. (a)-(e) Integration flow of SLG EAMs fully fabricated in CMOS pilot line. (a) Standard waveguide patterning, surface planarization and Si implantations. (b) Wafer-scale graphene transfer. (c) Graphene encapsulation. (d) Graphene patterning with standard lithography. (e) Damascene contacts and final copper metal line (M1) to silicon and graphene. (f) Top-down image of 300 mm wafer after full integration. (g) Cross-sectional transmission electron microscopy (TEM) image of the final device. Figures are adopted from [26].

B. Dual Single-layer Graphene Electro-Absorption Modulators

For realizing graphene-based EAMs with better performance, the DLG structure has been proposed, which augments the interaction between graphene and the optical field within the waveguide. In the DLG configuration, two distinct SLG sheets interact with the optical mode. This design not only enhances light-matter interaction but also facilitates graphene modulation by applying a bias to the graphene-isolator-graphene capacitor. In other words, it eliminates the necessity of doped Si waveguides, which simplifies the SiPh chip fabrication process and introduces a new level of flexibility in choosing the waveguide core material. For example, this stack could also be used to build high speed modulators on silicon nitride waveguides[27].

In 2012, Liu et al. from UC Berkeley presented the first experimental demonstration of DLG EAMs on an SOI chip, which consisted of a 340 nm thick Si layer and a 2 μm thick BOX layer[28]. EBL was utilized to pattern a 400 nm wide undoped Si waveguide, and a roughly 13 nm thick layer of Al_2O_3 was chosen as the isolator between the two SLG sheets, as shown in Fig. 3(a). A 6 V bias allowed for a 6.5 dB static modulation depth with a 40 μm long DLG EAM, equivalent to a static modulation efficiency of ~27×10^{-3} dB·μm^{-1}·V^{-1}. Despite achieving impressive static modulation, the 3-dB bandwidth of this DLG EAM was only ~1 GHz, presumably limited by the ~1 kΩ high series resistance, which in principle could be improved with a better metal-graphene contact. Later in 2016, the same research group achieved a significant milestone by demonstrating a DLG EAM with a 35GHz 3-dB bandwidth. [29]. It was accomplished by relocating the DLG beneath an amorphous Si waveguide, creating a planar structure for depositing the graphene layers and using a thick gate layer (120 nm thick Al_2O_3). This approach substantially reduces resistance and capacitance of the DLG EAM However, due to the thick gate oxide, the static modulation efficiency of this device was merely ~2.7×10^{-3} dB·μm^{-1}·V^{-1} , which is only approximately 10% of their earlier reported DLG EAM[28]. This trade-off between modulation efficiency and bandwidth is intrinsic to almost all graphene-based modulators as we will see in the following sections.

Building on these pioneering efforts, Giambra et al. from CNIT made significant progress in building DLG EAMs with waveguides fabricated in standard SOI pilot lines [30]. In their study, polycrystalline hexagonal boron nitride (hBN) was utilized as a protective layer to maintain the quality of graphene in the DLG EAM, as illustrated in Fig. 3(b). Moreover, to reduce the series resistance, they implemented an optimized metal contact comprising 7 nm of nickel (Ni) and 60 nm of gold (Au). With those improvements, a 29 GHz 3dB-bandwidh was achieved. With a driving voltage as low as V_{pp} = 3.5 V, ~1.7 dB and ~1.3 dB dynamic ER at data rates of

10 Gbps and 50 Gbps respectively were obtained. Despite these advancements, this DLG EAM still exhibited a relatively low static modulation efficiency of ~2.8×10^{-3} dB·μm^{-1}·V^{-1} (~3dB modulation depth under 9V bias for a 120 μm long device).

In addition to the standard straight strip waveguide, various alternative structures have been explored to enhance static modulation efficiency. E.g. ring resonators were investigated as the cavity could enhance light-matter interaction between the optical mode and graphene within the DLG stack. The first RR DLG EAM was demonstrated by Phare et al. from Cornell University in 2015[31]. In their RR DLG EAM, a SiN waveguide with a width of 1000 nm and height of 300 nm supporting a single quasi TE-mode was chosen to create 40 μm radius RRs, with SiO_2 serving as both the top and bottom cladding, as illustrated in Fig. 3(c). The waveguides were patterned with 248 nm DUV lithography and dry etching. Next, SiO_2 was deposited, and a standard CMP process was employed to planarize the top surface for graphene integration. In the 30 μm long DLG structure, a 65 nm thick Al_2O_3 layer served as the isolation layer. By virtue of the resonating structure, their DLG EAM reached a remarkable static modulation efficiency of ~50×10^{-3} dB·μm^{-1}·V^{-1}. Furthermore, a 3-dB bandwidth of ~30 GHz was achieved under a -30 V bias. Nonetheless, the resonating nature also renders the EAM wavelength-depended, diminishing one of the main advantages of graphene modulators. Thus, our team proposed and experimentally demonstrated the use of slot waveguides to enhance light-matter interaction[32], as depicted in Fig. 3(d). The slot waveguide confines light within a thin and low-refractive index region, thereby enhancing the interaction between light and graphene[33]. The dimensions of our slot waveguide (680 nm width with a 180 nm gap) are such that they can be defined with standard DUV lithography techniques, which enables large-scale fabrication and integration in standard SiPh platforms. Due to the enhanced light-matter interaction, our device exhibited an impressive static modulation efficiency of 38×10^{-3} dB·μm^{-1}·V^{-1}. The 3-dB bandwidth was measured to be ~ 16 GHz.

To explore the experimental limits of DLG EAMs, Agarwal et al. from ICFO utilized hBN-encapsulated exfoliated graphene to construct DLG EAMs[34], aiming for the highest quality material. The silicon chip was fabricated on the 200 mm SiPh line of IMEC, and the DLG structure was prepared using EBL-based laboratory processes. Their ~60 μm long DLG structure features a 10 nm thick layer of hafnium oxide (HfO_2) as the isolation layer, as shown in Fig. 3(e). The DLG was built on an undoped silicon waveguide with a width of 750 nm and a height of 220 nm to support the fundamental quasi-TM mode, which offers stronger light-matter interaction compared to the fundamental quasi-TE mode. The DLG EAM achieved a 3-dB bandwidth of ~39 GHz, simultaneously with a notably high static modulation efficiency of ~37×10^{-3} dB·μm^{-1}·V^{-1}. Additionally, this DLG EAM set a world-record with a 5.2 dB dynamic ER at 40 Gbps under a driving voltage V_{pp}= 3.5 V.

In addition to high modulation efficiency and frequency response, low insertion loss is a crucial parameter for facilitating industrial adoption. Applications like high-performance computing and data communications involve the integration of numerous components and nodes, making low insertion loss vital for maintaining signal quality and energy efficiency as the system scales. Given the strong relationship between IL and ER, the introduction of the transmission penalty (TP) concept ensures a fair and effective evaluation of various modulator designs. It is defined as[12]:

$$\mathrm{TP} = \frac{2P_{in}}{P_1 - P_0} \tag{1}$$

where P_1 and P_0 are the high and low output power levels, respectively, and P_{in} represents the input power ($P_{in}>P_1>P_0$). Also, TP can be calculated as function of the ER (ER= P_1/P_0 with ER(dB) = $10\log(P_1/P_0)>0$) and the IL (IL= P_{in}/P_1 with IL(dB) = $10\log(P_{in}/P_1)>0$):

$$\frac{1}{\mathrm{TP}} = \frac{1}{2}\frac{1}{\mathrm{IL}}\left(1-\frac{1}{\mathrm{ER}}\right) \tag{2}$$

Note that Equation (2) has to be calculated on a linear scale. A lower TP results in decreased power consumption in optical networks[35], which is highly desired.

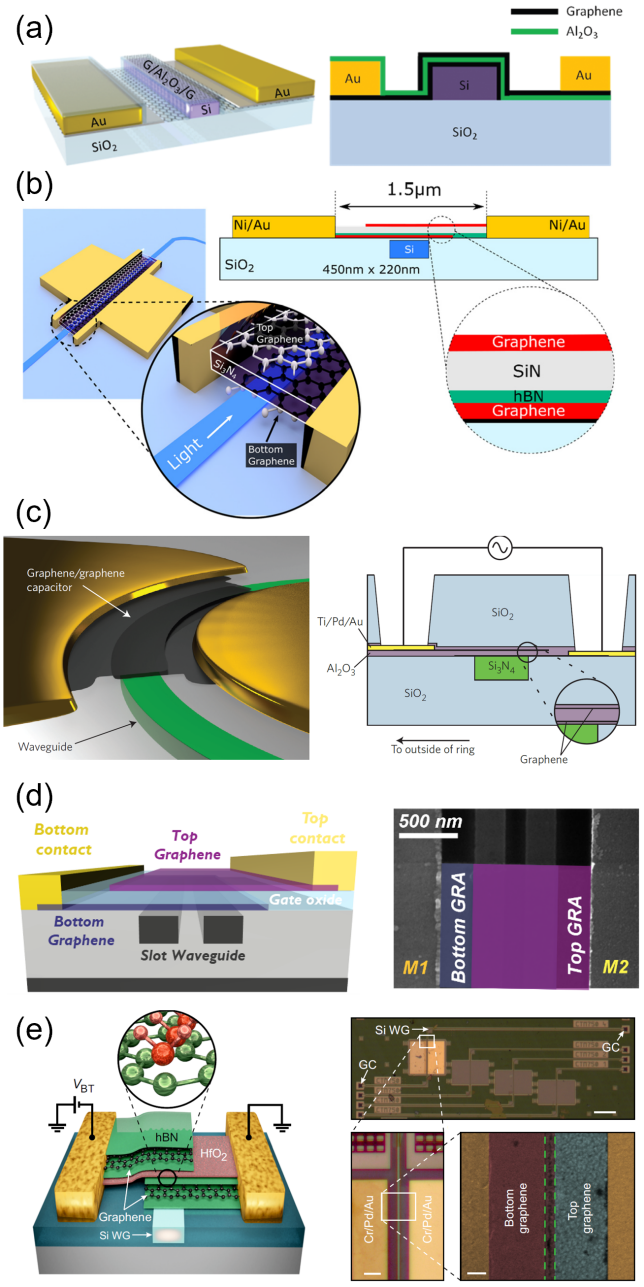

Figure. 3. (a) The first DLG EAM. Figures are adopted from[28]. (b) The first DLG EAM with hBN-encapsulated graphene. Figures are adopted from[30]. (c) The first DLG EAM on a SiN waveguide. Figures are adopted from[31]. (d) The first DLG EAM on a slot silicon waveguide patterned with DUV. Figures are adopted from[32]. (e) The DLG EAM with the highest 3-dB bandwidth. Figures are adopted from [34].

In Table I, we provide a summary of the performance, including TP, modulation efficiency (ME), and 3-dB bandwidth (BW) of the abovementioned EAMs. It is worth noting that the calculated TP is based on the V_{pp} reported from each paper. Although a higher V_{pp} value enables better TP results, it raises questions about compatibility with CMOS driving circuits. As demonstrated in[32], we achieved a TP of 8.9 dB at V_{pp} = 2 for a DLG EAM built on a conventional strip waveguide, highlighting its competitive standing against state-of-the-art Ge devices utilizing the Franz-Keldysh (FK) effect[22, 36]. In Table II, we compare these characteristics with various other types of SiPh EAMs.

TABLE I

PERFORMANCE OF SILICON PHOTONIC GRAPHENE ELECTRO-ABSORPTION MODULATORS

References	V_{pp} (V)	TP (dB)	ME ($\times 10^{-3}$ dB·μm^{-1}·V^{-1})	BW (GHz)	Bit rate (Gbps)
[23]	4	NA	25	1.2	NA
[24]	8	8.37	13	5.9	10
[26]	6	7.9±1.7	8.3±0.7	12.6 ± 0.9	NA
[28]	6	8.11	27	1	NA
[29]	25	8.23	2.7	35	NA
[30]†	9	26	2.7	29	50
[31]	10	15.6	50	30	22
[32]	2	8.9	26	12.5	NA
[32]*	2	23	38	15.9	NA
[34]†	0.5	17	37	39	40

† The devices refrained from maximizing the ER due to concern about the breakdown voltage. * Slot waveguide

TABLE II
PERFORMANCE OF VARIOUS SILICON PHOTONIC ELECTRO-ABSORPTION MODULATORS

Materials	Wavelength (nm)	V_{pp} (V)	Extinction ratio (dB)	Insertion loss (dB)	Transmission Penalty (dB)	BW (GHz)	Bit rate (Gbps)
Ge[36]	1605	3	14.2	5.7	8.9	>67	>80
GeSi[37]	1566	4	7.5	10.6	14.5	56	56
GeSi[38]	1300	2	5.2	7.6	12.2	50	60
III-V[39]	1300	2.2	>10	4.8	<8.3	>67	50
Graphene[34]	1550	>6	4.4	7.8	12.8	39	40

III. GRAPHENE-BASED PHASE MODULATORS

To encode light signals in complex formats, phase modulation emerges as a crucial technique. In the domain of graphene, the absorption and refractive index are intricately linked to the Fermi level and the interplay between intraband and interband transitions, triggered by incident photons[19]. When the Fermi level aligns within half the photon energy, interband transitions dominate, resulting in heightened absorption. Conversely, as the Fermi level surpasses half the photon energy, interband transitions become suppressed due to Pauli blocking, rendering graphene transparent. In this scenario, changes in absorption primarily stem from intraband transitions, while alterations in the refractive index are explained by the Kramers-Kronig relationship. Notably, with a sufficiently substantial bias, absorption related to interband transitions can be effectively mitigated, paving the way for near-pure phase modulation capabilities using graphene. This attribute has emerged as a coveted asset in the realm of optical signal processing. In a pioneering experiment, researchers at AMO fabricated a 200 μm long DLG structure, with a 90 nm thick Al_2O_3 isolation layer, on top of one arm of a Mach-Zehnder interferometer (MZI)[40]. The MZI was constructed with silicon waveguides having a width of 375 nm and a height of 220 nm partially planarized with a layer of spin-coated hydrogen silsesquioxane (HSQ) for graphene integration. A phase modulation efficiency $V_\pi L$ = 30 V·cm was observed, notably worse than for SiPh devices at that moment but this experiment kickstarted research in the domain. Also in this case both SLG and DLG type devices were demonstrated.

A. Single-layer Graphene Phase Modulators

In 2018, Sorianello et al. from CNIT demonstrated, for the first time, a high-speed SLG SiPh phase modulator [41], which was implemented on a MZI. The SiPh chip for the device was fabricated in the IMEC iSiPP25G silicon photonics platform. The MZI was based on p-type doped silicon ridge waveguides with a 60 nm slab, a width of 480 nm, and a height of 220 nm. The SLG was placed on the doped silicon waveguide, separated by a 10 nm spacer of high-quality thermal SiO_2 to create a capacitor. The device achieved an impressive static modulation depth of approximately 35 dB, and a $V_\pi L$ value of around 0.28 cm·V was extracted. This $V_\pi L$ value surpassed that of conventional high-speed SiPh phase modulators ($V_\pi L$ > 1 cm·V), which typically operate in the depletion mode. Moreover, the device showed a ~5GHz 3-dB bandwidth. The SLG phase modulator could readily achieve a dynamic ER of 3.94 dB at 10 Gbps with a driving voltage V_{pp} = 2 V.

B. Dual Single-layer Graphene Phase Modulators

As SLG phase modulators still require doped Si waveguides, hindering the goal of achieving a pure phase modulator with graphene, constructing DLG phase modulators with undoped Si or SiN waveguides is more appealing. To realize this objective, we designed and fabricated DLG MZI modulators (MZMs). In our study, we designed two types of DLG MZMs: one constructed with a conventional strip waveguide (MZM-STRIP-DLG) and another with the aforementioned slot waveguide (MZM-SLOT-DLG). The strip waveguide had a width of 450 nm, and the slot waveguide had a width of 680 nm with a 180 nm wide slot inside. The input light is coupled to the chip by grating couplers (GCs) and then divided into two paths by a multi-mode interferometer (MMI. After passing through the DLG active area, the separated light beams are recombined at the output to interfere constructively or destructively. The MZM-SLOT-DLG comprises of two mode converters in each arm to convert between strip waveguides and slot waveguides. Both types of devices are unbalanced with one arm having a 40 μm longer strip waveguide.

The fabrication of the waveguides followed the process outlined above. After the definition of the waveguides and CMP, we proceeded to conduct unbiased transmission measurements on strip and slot based MZMs before the DLG integration. In Fig. 4(a), interference fringes due to the length difference between the two arms of the MZMs can be observed in the transmission spectra. Both types of MZMs showed low insertion loss and a high extinction ratio between the maximum and minimum transmission levels, indicating well-designed MZMs and accurately fabricated waveguides. Then the SOI wafer was diced for graphene processing. The integration of the DLG, including transfer, patterning and contacting, follows the procedure outlined above and in our previous report[32]. The only deviation is the use of HfO_2 as the gate oxide instead of Al_2O_3. The selection of the high-k dielectric enables a higher breakdown voltage, facilitating pure phase modulation with minimal loss. The process

involves depositing 1 nm of Si by thermal evaporation and 10 nm HfO_2 by ALD. Figure 4 (b) presents a schematical cross-section of the devices, and Figure 4 (c) shows a top-down microscope image of the MZM-STRIP-DLG (top) and the MZM-SLOT-DLG (bottom).

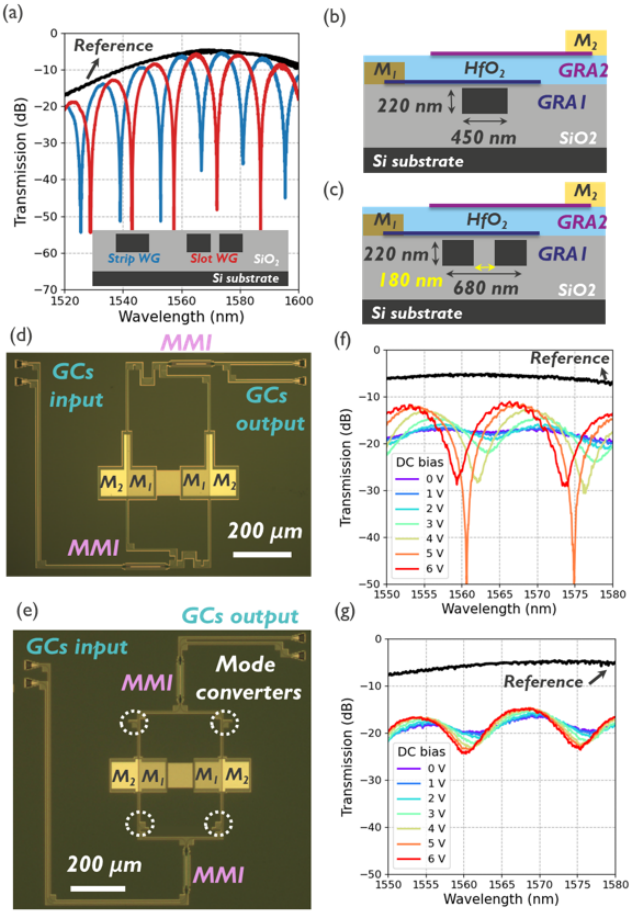

Figure. 4. (a) Transmission of passive strip and slot waveguides based MZM prior to DLG integration. Schematic cross-section of (b) MZM-STRIP-DLG and (c) MZM-SLOT-DLG. Top-down microscope images of (d) MZM-STRIP-DLG and (e) MZM-SLOT-DLG. Fiber-to-fiber transmission spectra of (f) 200 μm long MZM-STRIP-DLG and (g) 50 μm long MZM-SLOT-DLG at different DC voltages. The voltage on the left arm of the MZM is swept while a constant 6V bias is applied on the right arm.

After integrating the DLG, the MZMs underwent biased transmission measurements. To maximize transmitted power, the DLG on the right arm was biased at 6 V (near the voltage where graphene approaches transparency) while the voltage on the left arm DLG was swept. Figure 4. (d) and (e) show the wavelength-dependent transmission of a MZM-STRIP-DLG (200μm length) and a MZM-SLOT-DLG (50μm length) for a 0 V to 6 V voltage sweep. When the applied voltage is less than 2 V, the interference fringes visibility considerably decreases or even disappears. This is predominantly due to the loss difference between the left and right DLG, with the right arm being transparent and the left arm remaining absorptive. Due to the decreased absorption in the left DLG, the fringe depth for the MZM-STRIP-DLG increases with increasing bias and reaches its maximal value for a 5V bias. At this voltage, the loss difference between the two arms is minimal, resulting in the largest extinction ratio. When the voltage further increases, the depth of the fringes decreases again, which can be attributed to the lower loss in the left arm relative to the right arm. In an ideal situation, the maximum depth would be obtained when the same voltage is applied to both arms. However, this condition can be altered by local graphene doping concentrations in the experimental devices. As shown in Fig.4(e), the MZM-SLOT-DLG demonstrates a similar trend. Throughout the sweep, the fringe depth increases but is always less than 10 dB, significantly smaller than that of MZM-STRIP-DLG. The primary reason for this discrepancy lies in the substantial disparity in loss between the two arms of the MZM-SLOT-DLG, where the left arm consistently exhibits higher absorption than the right arm. As both arms of the MZMs feature a DLG with identical dimensions, the discrepancy in loss between the MZM-SLOT-DLG's arms may arise from misalignment during the EBL fabrication process. Given the mirror-symmetric design of our MZMs, a misalignment to the right (left) in the top (bottom) contact results in a reduced distance between the metal contact and the waveguide on the left arm compared to the right arm. This could potentially lead to higher loss in the left arm than the right arm. In both types of MZMs, the metal offset (M_{off}) is designed at 500 nm for both contacts. According to simulations reported in[32], this value may not be sufficient for slot waveguide-based devices, resulting in reduced tolerance for misalignment. Conversely, due to being in the safe region, the huge loss difference was not observed in the MZM-STRIP-DLG, which was fabricated simultaneously on the same chip.

To characterize and compare the efficiency of both types of MZMs, the wavelength shift of the fringes was measured and converted to a phase change, from which the change in effective index could be calculated. Since the change in effective index is independent of length, it allows for a direct comparison of the efficiency between MZM-STRIP-DLGs and MZM-SLOT-DLGs as shown in Fig. 5(a). Both types of MZMs exhibit the typical up-and-down index modulation observed in simulations for biased DLG devices. As the voltage is swept from -2 to 2 V, effective index changes of 1.11×10^{-3} and 1.78×10^{-3} are measured for the MZM-STRIP-DLGs and MZM-SLOT-DLGs, respectively. Similar enhancements for the slot waveguide based MZM are observed in the voltage range of 2 to 6 V. This improvement is attributed to the enhanced mode interaction in the slot waveguides, which leads to increased performance. Figure 5(b) shows $V_\pi L$ as a function of voltage. The best $V_\pi L$ values found for the MZM-STRIP-DLG and the MZM-SLOT-DLG are 0.0954 and 0.0789 V·cm, respectively. With a driving voltage of 2 V, this means that the MZM-STRIP-DLG and the MZM-SLOT-DLG require only 477 μm and 395 μm of DLG length to achieve a π-phase shift. These $V_\pi L$ values outperform the lowest reported values for lithium niobate

MZMs (~1.8 V·cm)[42] and silicon-insulator-silicon (SIS) MZMs (0.2~0.7 V·cm) [43, 44] MZMs, and are comparable to III-V MZMs (0.047 V·cm) [45].

To achieve optimal data transmission rates, signal integrity, and facilitate advanced modulation formats in optical communication systems, the loss of the device is also a critical factor. While having an identical MZM structure without graphene would have been ideal for serving as a reference to distinguish losses between passive waveguides and the DLG, such a design was not available. Consequently, we proceeded with the assumption that all calculated insertion losses originated from the DLG itself. By normalizing these losses with the corresponding active length, we calculated the propagation loss of DLG MZMs as a function of DC bias, as shown in Fig. 5(c). The higher losses in the MZM-SLOT-DLG can be attributed to the metal offset, which was designed too small. From these results, the phase modulator figure of merit $FOM_{pm} = \alpha \cdot V_\pi \cdot L$ [19] can be calculated. Our MZM-STRIP-DLG showed a best FOM_{pm} of 27.6 dB·V (at V_{DC} =4.5V), which outperforms other graphene-based MZMs (66 and 3000 dB·V)[41, 46], and is comparable to SIS MZMs (15~35 dB·V)[43]. However, the MZM-SLOT-DLG shows a FOM_{PM} of only 168 dB·V at V_{DC} = 3.5V due to the high propagation loss associated with the metal contacts. This is similar to what happened for slot based DLG EAMs[32], which also showed a higher intrinsic modulation efficiency but exhibited higher insertion losses, resulting in an overall decreased TP.

S-parameter measurements were carried out to characterize the bandwidth of our DLG MZMs. In order to effectively measure the frequency response, one arm of the MZM was biased at a constant voltage (6V). Figure 5(d) depicts the normalized S_{21} results. The extracted 3 dB bandwidth was determined to be 4.2 and 5.5 GHz for 100 μm long MZM-STRIP-DLG and 50 μm long MZM-SLOT-DLG, respectively. We summarize and compare our results on graphene phase modulators with other approaches to SiPh phase modulators in Table III.

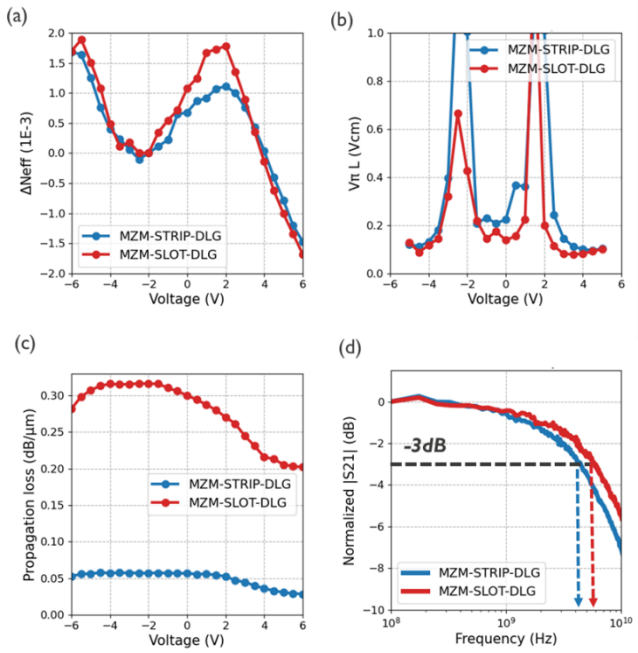

Figure. 5. Extracted (a) effective index change (b) $V_\pi L$ and (c) propagation loss as a function of DC bias for MZM-STRIP-DLG (blue) and MZM-SLOT-DLG (red). (d) Normalized S21 response of both types of MZM.

TABLE III
PERFORMANCE OF VARIOUS SILICON PHOTONIC PHASE MODULATORS

Approaches	Working principle	Wavelength (nm)	$V_\pi L$ (V·cm)	Loss (dB/cm)	FOM_{pm} (dBV)	BW (GHz)	Bit rate (Gbps)
Si MOSCAP[47]	Carrier plasma	1300	0.16	35	5.6	N/A	25
Si PIN junction[48]	Carrier plasma	1550	2	28	56	37	70
Si PN junction[49]	Carrier plasma	1550	1.5	27	40.5	N/A	112
$LiNbO_3$ integration[50]	Pockels effect	1550	2.55	5	12.8	70	100
$BaTiO_3$ integration[51]	Pockels effect	1550	0.2	6.5	1.3	2	25
III-V integration[52]	Carrier plasma & band filling	1550	0.09	26	2.34	2	32
Graphene integration[41]	Fermi level tuning	1550	0.28	236	66.1	5	10
This work (MZM-STRIP-DLG)	Fermi level tuning	1550	0.0954	289	27.6	4.2	NA
This work (MZM-SLOT-DLG)	Fermi level tuning	1550	0.0789	2130	168	5.5	NA

VI. CONCLUSION AND OUTLOOK

In conclusion, the field of graphene-based silicon photonics modulators has undergone significant development since their initial demonstration in 2011. Subsequent progress involved iterative optimization of the devices, ultimately leading to their successful integration into a CMOS pilot line, a significant milestone highlighted in our recent publication[26]. Each stride in this trajectory not only signifies progress within the field but also contributes to narrowing the gap toward the commercialization of graphene photonics devices. However, for graphene-based modulators to dominate high-speed optical communication applications, several further improvements are imperative.

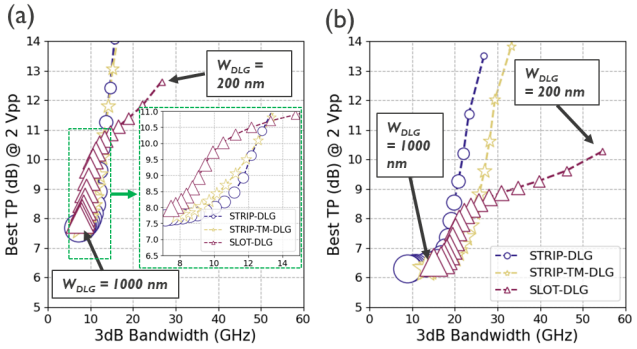

Figure. 6. Simulated transmitter penalty (TP) and bandwidth (BW) for DLG-EAM modulators with capacitor width varying from 200 nm to 1000nm (step = 50 nm), as illustrated by the size of the markers. Three different device types were considered (strip waveguide with TE and TM mode, slot waveguide with TE mode). A 20 nm gate oxide thickness and 2 Volt V_{pp} was assumed in the calculations, and for each simulation the length was adapted to get an extinction ratio of 4dB. In the simulations the graphene quality was varied from 'standard' (15meV scattering rate) to 'better than currently available' (1.2meV scattering rate).

As discussed earlier, designing graphene-based modulators requires several trade-offs to be considered. To illustrate this further, Figure 6 shows how the calculated transmitter penalty (TP) and bandwidth (BW) vary as the width of the capacitive DLG stack W_{DLG} changes. In these calculations, we assumed a drive voltage of 2 Volt and a gate oxide thickness of 20 nm, which was found to result in good compromise between TP and BW. The graphene scattering rate assumed in the simulations was 15 meV and 1.2 meV in Fig. 6 (a) and (b) respectively. The first value, 15 meV, is believed to be representative for CVD-grown graphene layers now readily available in devices processed using wafer-scale compatible processes. The second value, 1.2 meV, represents high quality graphene, as found in hBN encapsulated flakes. In each simulation, the length of the modulator was adapted to keep the extinction ratio (ER) fixed at 4 dB. Three different combinations of waveguide type (strip/slot) and polarization were considered. In each case the bandwidth of the device increases if W_{DLG} decreases because of a reduction in capacitance. However, this leads to a stronger overlap of the optical field with the unbiased regions of the top and bottom graphene layer, and hence higher losses and a higher TP. Also, in general, the TM mode performs better than the TE mode, as it has a higher overlap with the graphene layers. Use of the slot waveguide (with TE mode) becomes interesting at smaller W_{DLG}, a result of the strong field confinement in the center of the slot. Further details can be found in our recent publication[32]. Finally, comparing Fig. 6 a) and b) clearly shows the importance of improving the quality of the graphene available for wafer-scale manufacturing. Insufficient graphene quality introduces additional losses and exhibits reduced mobility, limiting both static and dynamic performance. Therefore, the development of a wafer-scale, CMOS-compatible transfer of high-quality graphene remains critical to realize the full potential of graphene-based devices. Also, following the transfer, graphene requires a suitable dielectric layer to preserve its high quality during subsequent device processing. This dielectric should possess a low defect density with high breakdown strength and should not damage graphene during deposition. Currently, 2D hexagonal boron nitride is the preferred solution due to its clean van der Waals interface, but it is only suitable for encapsulation, not as a proper gate oxide, owing to its low dielectric constant. As a result, the deposition of an ideal dielectric, using wafer-scale methods, whether a single material or a stack of various dielectrics, is an interesting research topic, especially with a focus on scaling up in a CMOS pilot line. Beyond these considerations, the enhancement of contact resistance to enable a higher speed response and exploration of alternative waveguide cross-sections to strike a better balance between efficiency and loss can be pivotal avenues of further exploration. Each of these research directions can shorten the distance to industrial readiness, thereby paving the way for take-up of graphene-based devices in industrial applications. At this moment it remains difficult to predict however what application could be the main driver for this. Given the compactness and simplicity of graphene modulators short range optical interconnects such as those needed for high performance computing applications seem an attractive target. However, these typically require very low driving voltages. Another attractive feature is the broadband response. Although only limited research has been carried out in this direction, graphene EA modulators can in principle directly be used for wavelengths beyond 1600 nm or even beyond 2000 nm. This would have the additional advantage that the driving voltage can be lowered accordingly. Also, graphene modulators could be directly integrated with graphene-based detectors[53, 54]. This could reduce the complexity and hence cost of the overall integration scheme, relevant for e.g. sensing applications. A final option, not discussed yet above, is to use graphene as a transparent contact and not as the active layer. This approach was used recently to demonstrate a Graphene-Organic Hybrid Phase Modulator with >270 GHz Modulation Bandwidth[55] .

REFERENCES

[1] P. Taylor, "Amount of data created, consumed, and stored 2010-2020, with forecasts to 2025," *Statista. Available online: https://www.statista.com/statistics/871513/worldwide-data-created/ (accessed on 24 October 2023),* 2022.

[2] E. Masanet, A. Shehabi, N. Lei, S. Smith, and J. Koomey, "Recalibrating global data center energy-use estimates," *Science,* vol. 367, no. 6481, pp. 984-986, 2020.

[3] M. Dayarathna, Y. Wen, and R. Fan, "Data center energy consumption modeling: A survey," *IEEE Communications surveys & tutorials,* vol. 18, no. 1, pp. 732-794, 2015.

[4] M. Koot and F. Wijnhoven, "Usage impact on data center electricity needs: A system dynamic

forecasting model," *Applied Energy,* vol. 291, p. 116798, 2021.

[5] R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," *Proceedings of the IEEE,* vol. 89, no. 4, pp. 490-504, 2001.

[6] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and short-circuit power of CMOS gates driving lossless transmission lines," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 46, no. 8, pp. 950-961, 1999.

[7] J. D. Owens, W. J. Dally, R. Ho, D. Jayasimha, S. W. Keckler, and L.-S. Peh, "Research challenges for on-chip interconnection networks," *IEEE micro,* vol. 27, no. 5, pp. 96-108, 2007.

[8] D. A. Miller, "Optical interconnects to electronic chips," *Applied Optics,* vol. 49, no. 25, pp. F59-F70, 2010.

[9] Q. Cheng, M. Bahadori, M. Glick, S. Rumley, and K. Bergman, "Recent advances in optical technologies for data centers: a review," *Optica,* vol. 5, no. 11, pp. 1354-1370, 2018.

[10] G. T. Reed and A. P. Knights, *Silicon photonics: an introduction*. John Wiley & Sons, 2004.

[11] Y. Shi *et al.*, "Silicon photonics for high-capacity data communications," *Photonics Research,* vol. 10, no. 9, pp. A106-A134, 2022.

[12] M. Pantouvaki *et al.*, "Active components for 50 Gb/s NRZ-OOK optical interconnects in a silicon photonics platform," *Journal of Lightwave Technology,* vol. 35, no. 4, pp. 631-638, 2017.

[13] A. Rahim *et al.*, "Taking silicon photonics modulators to a higher performance level: state-of-the-art and a review of new technologies," *Advanced Photonics,* vol. 3, no. 2, pp. 024003-024003, 2021.

[14] K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid State Communications,* vol. 146, no. 9-10, pp. 351-355, 2008.

[15] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nature nanotechnology,* vol. 3, no. 8, pp. 491-495, 2008.

[16] A. S. Mayorov *et al.*, "Micrometer-scale ballistic transport in encapsulated graphene at room temperature," *Nano Letters,* vol. 11, no. 6, pp. 2396-2399, 2011.

[17] F. Bonaccorso, Z. Sun, T. Hasan, and A. Ferrari, "Graphene photonics and optoelectronics," *Nature Photonics,* vol. 4, no. 9, pp. 611-622, 2010.

[18] Q. Bao and K. P. Loh, "Graphene photonics, plasmonics, and broadband optoelectronic devices," *ACS Nano,* vol. 6, no. 5, pp. 3677-3694, 2012.

[19] M. Romagnoli *et al.*, "Graphene-based integrated photonics for next-generation datacom and telecom," *Nature Reviews Materials,* vol. 3, no. 10, pp. 392-414, 2018.

[20] C. Qiu, H. Zeng, and Y. Su, "Recent progress in graphene-based optical modulators on silicon photonics platform," *National Science Open,* vol. 1, no. 3, p. 20220031, 2022.

[21] D. Feng *et al.*, "High speed GeSi electro-absorption modulator at 1550 nm wavelength on SOI waveguide," *Optics Express,* vol. 20, no. 20, pp. 22224-22232, 2012.

[22] S. A. Srinivasan *et al.*, "56 Gb/s germanium waveguide electro-absorption modulator," *Journal of Lightwave Technology,* vol. 34, no. 2, pp. 419-424, 2015.

[23] M. Liu *et al.*, "A graphene-based broadband optical modulator," *Nature,* vol. 474, no. 7349, pp. 64-67, 2011.

[24] Y. Hu *et al.*, "Broadband 10 Gb/s operation of graphene electro‐absorption modulator on silicon," *Laser & Photonics Reviews,* vol. 10, no. 2, pp. 307-316, 2016.

[25] C. Alessandri *et al.*, "5× 25 Gbit/s WDM transmitters based on passivated graphene–silicon electro-absorption modulators," *Applied Optics,* vol. 59, no. 4, pp. 1156-1162, 2020.

[26] C. Wu *et al.*, "Wafer‐Scale Integration of Single Layer Graphene Electro‐Absorption Modulators in a 300 mm CMOS Pilot Line," *Laser & Photonics Reviews,* p. 2200789, 2023.

[27] L. A. Shiramin and D. Van Thourhout, "Graphene modulators and switches integrated on silicon and silicon nitride waveguide," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 23, no. 1, pp. 94-100, 2016.

[28] M. Liu, X. Yin, and X. Zhang, "Double-layer graphene optical modulator," *Nano Letters,* vol. 12, no. 3, pp. 1482-1485, 2012.

[29] H. Dalir, Y. Xia, Y. Wang, and X. Zhang, "Athermal broadband graphene optical modulator with 35 GHz speed," *ACS Photonics,* vol. 3, no. 9, pp. 1564-1568, 2016.

[30] M. A. Giambra *et al.*, "High-speed double layer graphene electro-absorption modulator on SOI waveguide," *Optics Express,* vol. 27, no. 15, pp. 20145-20155, 2019.

[31] C. T. Phare, Y.-H. Daniel Lee, J. Cardenas, and M. Lipson, "Graphene electro-optic modulator with 30 GHz bandwidth," *Nature Photonics,* vol. 9, no. 8, pp. 511-514, 2015.

[32] C. Wu *et al.*, "High-efficiency dual single layer graphene modulator integrated on slot waveguides," *Optics Express,* vol. 31, no. 22, pp. 36872-36882, 2023.

[33] S. Jahani *et al.*, "Controlling evanescent waves using silicon photonic all-dielectric metamaterials for dense integration," *Nature Communications,* vol. 9, no. 1, p. 1893, 2018.

[34] H. Agarwal *et al.*, "2D-3D integration of hexagonal boron nitride and a high-κ dielectric for ultrafast graphene-based electro-absorption modulators," *Nature Communications,* vol. 12, no. 1, p. 1070, 2021.

[35] J.-B. Quélène, A. Michard, N. Michit, J.-F. Carpentier, P. Le Maître, and Y. Le Guennec, "Carrier Depletion Silicon Ring Modulator Power Penalty Versus Power Coupling Coefficient," *Journal of Lightwave Technology,* vol. 36, no. 14, pp. 3023-3029, 2018.

[36] Y. Liu *et al.*, "80Gb/s NRZ Ge waveguide electro-absorption modulator," *Optics Express,* vol. 30, no. 19, pp. 34276-34286, 2022.

[37] L. Mastronardi *et al.*, "High-speed Si/GeSi hetero-structure electro absorption modulator," *Optics Express,* vol. 26, no. 6, pp. 6663-6673, 2018.

[38] S. A. Srinivasan *et al.*, "60Gb/s waveguide-coupled O-band GeSi quantum-confined Stark effect electro-absorption modulator," in *Optical Fiber Communication Conference*, 2021: Optica Publishing Group, p. Tu1D. 3.

[39] Y. Tang, J. D. Peters, and J. E. Bowers, "Over 67 GHz bandwidth hybrid silicon electroabsorption modulator with asymmetric segmented electrode for 1.3 μm transmission," *Optics Express,* vol. 20, no. 10, pp. 11529-11535, 2012.

[40] M. Mohsin *et al.*, "Experimental verification of electro-refractive phase modulation in graphene," *Scientific Reports,* vol. 5, no. 1, p. 10967, 2015.

[41] V. Sorianello *et al.*, "Graphene–silicon phase modulators with gigahertz bandwidth," *Nature Photonics,* vol. 12, no. 1, pp. 40-44, 2018.

[42] C. Wang, M. Zhang, B. Stern, M. Lipson, and M. Lončar, "Nanophotonic lithium niobate electro-optic modulators," *Optics Express,* vol. 26, no. 2, pp. 1547-1555, 2018.

[43] A. Abraham, S. Olivier, D. Marris-Morini, and L. Vivien, "Evaluation of the performances of a silicon optical modulator based on a silicon-oxide-silicon capacitor," in *11th International Conference on Group IV Photonics (GFP)*, 2014: IEEE, pp. 3-4.

[44] M. Webster, K. Lakshmikumar, C. Appel, C. Muzio, B. Dama, and K. Shastri, "Low-power MOS-capacitor based silicon photonic modulators and CMOS drivers," in *2015 Optical Fiber Communications Conference and Exhibition (OFC)*, 2015: IEEE, pp. 1-3.

[45] J.-H. Han, F. Boeuf, J. Fujikata, S. Takahashi, S. Takagi, and M. Takenaka, "Efficient low-loss InGaAsP/Si hybrid MOS optical modulator," *Nature Photonics,* vol. 11, no. 8, pp. 486-490, 2017.

[46] H. Watson, "Graphene Modulators for Silicon Photonic Optical Links," 2021.

[47] J. Fujikata, S. Takahashi, M. Takahashi, M. Noguchi, T. Nakamura, and Y. Arakawa, "High-performance MOS-capacitor-type Si optical modulator and surface-illumination-type Ge photodetector for optical interconnection," *Japanese Journal of Applied Physics,* vol. 55, no. 4S, p. 04EC01, 2016.

[48] Y. Sobu, T. Simoyama, S. Tanaka, Y. Tanaka, and K. Morito, "70 Gbaud operation of all-silicon Mach–Zehnder modulator based on forward-biased PIN diodes and passive equalizer," in *2019 24th OptoElectronics and Communications Conference (OECC) and 2019 International Conference on Photonics in Switching and Computing (PSC)*, 2019: IEEE, pp. 1-3.

[49] K. Li *et al.*, "Electronic–photonic convergence for silicon photonics transmitters beyond 100 Gbps on–off keying," *Optica,* vol. 7, no. 11, pp. 1514-1516, 2020.

[50] M. He *et al.*, "High-performance hybrid silicon and lithium niobate Mach–Zehnder modulators for 100 Gbit s− 1 and beyond," *Nature Photonics,* vol. 13, no. 5, pp. 359-364, 2019.

[51] F. Eltes *et al.*, "An integrated optical modulator operating at cryogenic temperatures," *Nature Materials,* vol. 19, no. 11, pp. 1164-1168, 2020.

[52] T. Hiraki *et al.*, "Heterogeneously integrated iii–v/si mos capacitor mach–zehnder modulator," *Nature Photonics,* vol. 11, no. 8, pp. 482-485, 2017.

[53] D. Schall *et al.*, "50 GBit/s photodetectors based on wafer-scale graphene for integrated silicon photonic communication systems," *ACS Photonics,* vol. 1, no. 9, pp. 781-784, 2014.

[54] Y. Salamin, P. Ma, B. Baeuerle, A. Josten, A. Emboras, and J. Leuthold, "100 Gbit/s Graphene Photodetector," in *Integrated Photonics Research, Silicon and Nanophotonics*, 2018: Optica Publishing Group, p. IW1B. 2.

[55] P. Ma *et al.*, "Low-Loss Plasmonically Enhanced Graphene-Organic Hybrid Phase Modulator with> 270 GHz Modulation Bandwidth," in *European Conference and Exhibition on Optical Communication*, 2022: Optica Publishing Group, p. Th3B. 4.

Chenghan Wu received the B.Sc. degree in Material and Optoelectronic Science from National Sun YatSen University, Kaohsiung, Taiwan, in 2014, and received the M.Sc. degree in Material Science and Engineering from National Taiwan University, Taipei, Taiwan, in 2017. Currently, he is pursuing a Ph.D. degree in Photonic Engineering at Ghent University, Ghent, Belgium, starting from 2018.

In 2016, he served as a 6-month international scholar at imec, focusing on innovating graphene transfer processes. In 2018, he joined imec, Leuven, Belgium, as a doctoral researcher and progressed to the role of R&D Engineer until the end of 2022. His research interests revolve around the design, integration, and characterization of 2D materials, particularly graphene and transition metal dichalcogenides, for use in silicon photonics devices. He has contributed to the academic

community with over 10 publications in refereed journals and conferences.

Zheng Wang received the B.Sc. degree in Mathematics and Physics from Tsinghua University, Beijing, China, in 2012, and the Ph.D. degree from The University of Texas at Austin, Austin, Texas, USA, in 2017.

From 2018 to 2021, he was a R&D Project Leader at imec, working on heterogeneous integration of graphene on silicon and silicon nitride (SiN) photonic integrated circuits (PICs). From 2021 to 2022, he was a Deputy Director the Shanghai Industrial μTechnology Research Institute (SITRI). In 2012, he joined the State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS). His research interests include the design fabrication, and characterization of PICs and the integration of low-dimensional materials (such as graphene, TMDCs, and hBN) on silicon and SiN PICs. He has over 40 publications in refereed journals and conferences.

Dries Van Thourhout received M.Sc. in engineering physics and the Ph.D. degree from Ghent University, Ghent, Belgium, in 1995 and 2000, respectively.

From October 2000 to September 2002, he was with Lucent Technologies, Bell Laboratories, New Jersey, USA, working on the design, processing, and characterization of InP/InGaAsP monolithically integrated devices. In October 2002, he joined the Department of Information Technology (INTEC), Ghent University. Since 2008, he has been a Full-time Professor. He is currently chair of the Photonics Research Group, an imec associated lab at Ghent University. He has submitted 14 patents, has authored or coauthored more than 270 journal papers and has presented invited papers at all major conferences in the domain. His research focuses on the design, fabrication, and characterization of integrated photonic devices. His main research interests include silicon nanophotonic devices and the integration of novel materials (III-V, graphene, ferro-electrics, and quantum dots) on these waveguides to expand their functionality. He is working on applications for telecom, datacom, optical interconnect, and sensing. Prof. Van Thourhout is a member of the IEEE Photonics Society and SPIE, and a fellow of OSA. He was the recipient of both an ERC Starting Grant (ULPPIC) and ERC Advanced Grant (NARIOS).