Packaging of Ultra-dynamic Photonic Switches and Transceivers for Integration into 5G Radio Access Network and Datacenter Sub-systems

G. Van Steenberge, G. Roelkens, P. Ossieur, J. Missinne, J. Van Asch, J. Zhang, S. Qin
Imec and Ghent University, Gent, Belgium

J. Van Campenhout
Imec
Leuven, Belgium

J. Van Kerkhof, M. M. Milosevic
PHIX Photonics Assembly
Enschede, The Netherlands

P. Bakopoulos, D. Syrivelis
NVIDIA
Athens, Greece

E. Mentovich
NVIDIA
Yokneam, Israel

K. Morozov
Innolume
Dortmund, Germany

S. Stracca, A. Bigongiari
Ericsson Research
Pisa, Italy

T. Joerg, D. Schlick
AT&S AG
Leoben, Austria

T. Braun, M. Wöhrmann, R. Gernhardt
Fraunhofer Institute for Reliability and Microintegration
Berlin, Germany

Q. Cheng, T. Li, R. Penty
Cambridge University
Cambridge, United Kingdom

2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) | 979-8-3503-3498-2/23/$31.00 ©2023 IEEE | DOI: 10.1109/ECTC51909.2023.00129

***Abstract*—We report the development of a fully non-blocking optical switch fabric, enabling a deterministic and dynamic network infrastructure. Focus is on scalable photonic integration and packaging technologies required to develop a low-cost switch fabric, including micro-transfer-printing of amplifiers, FOWLP for dense photonic-electronic integration, and optical/thermal packaging solutions on IC-substrates.**

***Index Terms*—scalable, photonic integration and packaging, switch fabric, micro-transfer-printing, FOWLP, optical redistribution layer, high-density substrates**

I. Introduction

Today's internet works predominantly on a best-efforts basis. In contrast, the demand is surging from time-sensitive applications, such as 5G fronthaul, Industry 4.0 (industrial automation), autonomous vehicles, data center computing-memory disaggregation, and augmented/virtual reality. These impose stringent requirements on the networking capacity, determinism (latency and jitter control), dynamics, and guaranteed delivery. Optical switching has been widely studied for applications in data centres and transport networks, as it brings the potential advantages of low latency, power efficiency, and low cost, mainly by eliminating the intermediate optical transceivers and electronic processing between two nodes. Reconfigurable Optical Add-Drop Multiplexers (ROADMs) and Micro-Electro-Mechanical System (MEMS)-based space switches are broadly applied for optical circuit switching networks enabling multiplexing in the wavelength/space domain. They are connection-oriented, being deterministic through the reservation of a complete wavelength/path but inflexible and typically switch on microsecond or millisecond timescales. The switching network can be made highly dynamic by applying optical slot switching via time-division multiplexing (TDM). However, capacity can be limited by the time slot reservations and when multiple flows compete, the determinism will be compromised.

This calls for a new optical switching paradigm that fully exploits the space, wavelength, and time domains, offering a powerful route to higher connectivity and throughput, while maintaining determinism. Within the Horizon Europe project PUNCH, a fully non-blocking N×N×Nλ optical switch fabric is being developed, allowing wavelength routing from any input port to any output port (see also Fig. 1). To ensure low cost per port, optical switching technologies must demonstrate a path towards high-volume manufacturing. Silicon photonics has been identified as a key enabling technology, providing a high-level of integration and compatibility with CMOS processes. However, large-scale switch fabrics pose huge challenges in terms of optical and electrical packaging. For example, for an N×N switching device, there are N^2 electrical and 2N optical interconnects to be made. Furthermore, insertion loss is limiting commercial uptake, motivating the integration of semiconductor optical amplifiers (SOA) to provide on-chip gain. Today, despite the use of complex photonic integrated circuits (PICs), the fabrication of a complete optical device still requires a large amount of sequential assembly steps. Integration of PICs, electronic interface circuits, III-V optical gain elements and fiber attachment parts is still based on legacy approaches, using active alignment or manual processes on the level of individual devices, limiting scalability and cost efficiency.

To reduce the packaging cost and reach the full potential of silicon photonics based optical switches, a more disruptive approach is required, shifting complexity from device-level, sequential assembly to substrate-level, parallelized pla-

This work was supported by the European Union's Horizon Europe Research and Innovation Program under Agreement 101070560 (PUNCH).

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00129

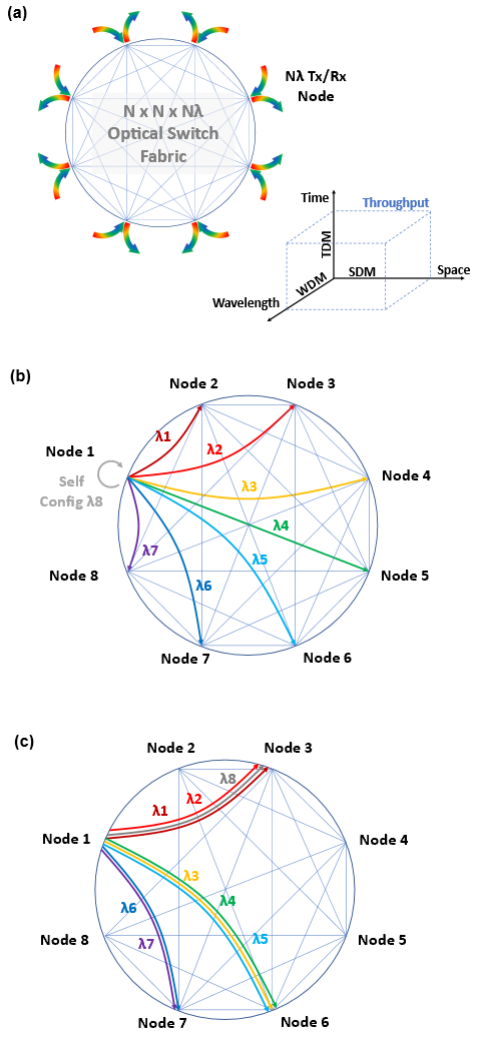

Fig. 1. (a) A conceptual figure of a fully non-blocking N×N×Nλ optical switch fabric. (b) Illustration of all-to-all reconfigurable interconnection by allocating a wavelength to any pair of nodes. (c) Illustration of bandwidth steering by allocating multiple wavelength capacity between hot nodes in order to resolve congestion.

nar fabrication. Within the Horizon Europe project PUNCH, full thermal, electrical, and optical packaging solutions are incorporated, leveraging semiconductor packaging technology compatible with high-volume manufacturing. The development of a III-V foundry process for micro-transfer-printing-compatible semiconductor optical amplifiers enables lossless optical switching on the silicon photonics platform. Custom designed electronic ICs to actuate, control, and power-monitor scaled switch fabrics are densely integrated with the photonic ICs into a heterogeneous fanout wafer-level package (FOWLP), processed on a 200 mm reconstructed wafer platform. In addition, the optical interfacing to the photonic ICs is accomplished using an optical redistribution layer, providing an optical fanout on organic IC-substrates, and allowing for a scalable optical fiber packaging solution.

This paper introduces these emerging photonics integration and packaging technologies being developed within the PUNCH project, along with the first experimental results from interfacing PICs with a polymer waveguide based optical redistribution layer. As a future outlook, the novel integration and packaging processes will also be applied within PUNCH for manufacturing of optical transceivers providing the interface between the optical switches and electronic resources (e.g. compute, memory, and storage).

II. Fully Non-Blocking Reconfigurable Optical Switch Fabric

A fully non-blocking space-and-wavelength reconfigurable optical switch fabric would necessitate multiple parallel switching planes that are bookended with (de)multiplexers in order to decouple space switching and wavelength selective switching. The duplication of switching planes, however, poses immense challenges to managing the complexity and footprint of the integrated switching subsystems. The PUNCH project proposes a new design approach that leverages a novel 2×2×Nλ wavelength selective switching element that can be implemented in any single-plane multi-stage switch topology.

A. 2×2×Nλ Wavelength Selective Switching Element

The 2×2×Nλ wavelength selective switching element comprises a symmetrical Mach-Zehnder interferometer (MZI) and multiple pairs of over-coupled micro-ring resonators (MRRs), shown in Fig. 2a. The over-coupled MRRs operate as highly-efficient, compact, and narrowband phase shifters, and a pair of such MRRs can operate differentially to create a symmetric MZI passband at a specific wavelength channel [1].

The design of a 2×2×Nλ SE requires examination of the geometrical parameters of MRRs to register their resonance wavelengths at a specific grid. The PUNCH space-and-wavelength switch is designed to be compatible with the CW-WDM MSA for co-packaged optics.

B. Scaling to a Fully Non-Blocking 8x8xNλ Reconfigurable Optical Switch Fabric

The developed 2×2×Nλ wavelength selective SE will be scaled to N×N×Nλ using a single-plane multi-stage switch topology, the dilated Banyan, shown in Fig. 2b, and also forms a modest-scale building block that can effectively lead to a larger-scale switching fabric. Signal fan-out is carried out by the 2×2×Nλ SEs while signal fan-in is done by passive combiners to simplify the device control circuitry, and thus the device packaging. SOA gain blocks will be added using micro-transfer printing technology (introduced in the next section) to compensate for the insertion loss. The redundant ports in the last stage will be connected to on-chip PDs for power monitoring, forming a feedback loop to the SOA bias controller for power equalization. Larger port count non-blocking switches assembled in the Clos topology will be realised using waveguide shuffles, on the PIC or making use of the polymer waveguide based optical redistribution layer.

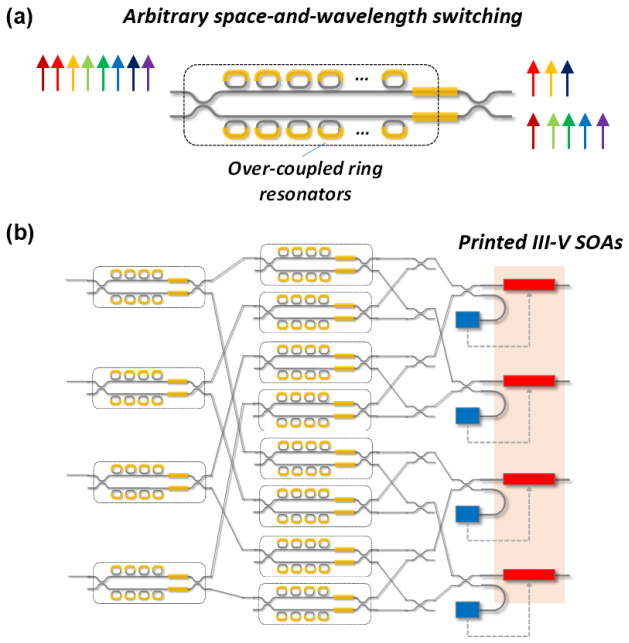

Fig. 2. (a) Proposed 2×2×8λ SE with 8 pairs of MRR phase shifters. (b) A 4×4×4λ dilated Banyan switch building block.

III. Micro-Transfer Printing for III-V Semiconductor Optical Amplifier Integration

The integration of III-V semiconductor devices on silicon photonic integrated circuits is of paramount importance to build complex, high-performance photonic systems-on-chip. Particularly in the context of optical switches, the integration of semiconductor optical amplifiers is required to obtain net-zero insertion loss. Several methods are pursued to integrate III-V opto-electronic components on a silicon photonics platform (flip-chip integration, micro-transfer printing, die-to-wafer bonding, hetero-epitaxial growth). Micro-transfer printing stands out as a very attractive approach as it combines advantages of flip-chip integration (III-V component fabrication in a III-V foundry, pre-testing of the components) and advantages of die-to-wafer bonding (high-throughput integration and robust evanescent optical coupling).

The concept of micro-transfer printing is illustrated in Fig. 3 for the case of integrating III-V semiconductor devices on a silicon substrate. The technique uses a PDMS stamp to pick up large arrays of thin-film devices from a source substrate and print them to a target substrate, as shown in Fig. 3(top). The pick-up and release process is determined by the kinetically-controlled adhesion of the thin-film devices to the stamp. As shown in Fig. 3(bottom), through the incorporation of a release layer in the material stack and the use of an encapsulation layer, the micron-scale III-V semiconductor thin-film devices can be released from the substrate, keeping them in place using tethers, after which the devices can be picked up by the stamp (thereby fracturing the tethers) and printed in a massively parallel way (1000s of devices can be transferred in one operation) on the target wafer. Micro-transfer printing is a back-end integration process that decouples the processing of the III-V and silicon devices and integrates the finished, known good devices afterwards. This implies that standard semiconductor processes can be used for the III-V semiconductor and silicon processing. Moreover, the back-end integration allows for using gold-contacts to III-V materials (which provides the best contacts), in contrast to front-end integration in a CMOS fab where gold is banned because it kills the performance of silicon transistors. The latest innovations on micro-transfer printing tools enable achieving an amazing alignment accuracy of 0.5 micron 3 sigma, even when printing large arrays of devices (area of 2 cm × 2 cm, fitting several 1000s of devices). Proof-of-concept III-V/Si demonstrations have been realized of Fabry-Perot lasers [2], DFB lasers [3] and photodiode integration [4] on silicon PICs. In PUNCH the micro-transfer printing of O-band quantum dot SOAs will be brought to TRL 6.

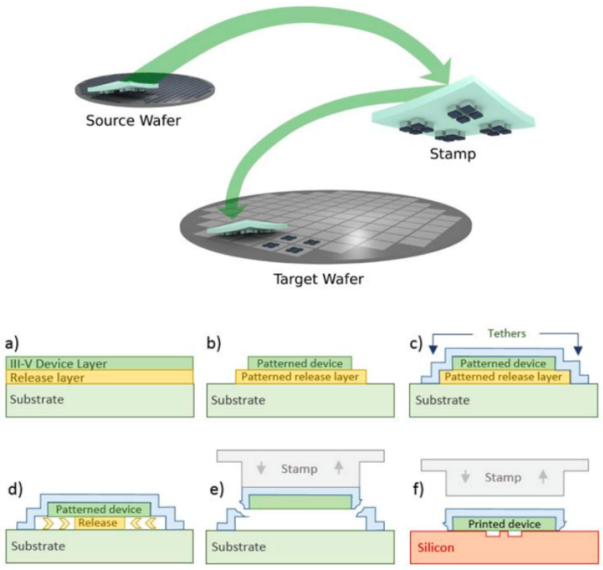

Fig. 3. (top) Micro-transfer printing uses a stamp to pick up devices from a source wafer and to print those devices on a target wafer. (bottom) By etching the release layer the processed and tested III-V devices are released from the source wafer and can be transferred to a target wafer.

IV. Quantum Dot Semiconductor Optical Amplifiers

In PUNCH, quantum dot (QD) semiconductor optical amplifiers are integrated on the silicon photonics switches, providing optical amplification over the entire wavelength range of interest (O-band). Quantum dots were proposed soon after the realization of quantum well materials almost thirty years ago. However, despite many attempts, functional devices were not realized until about two decades ago, following the development of self-assembly techniques during epitaxial growth which allowed the realization of the first quantum dot lasers emitting at $\sim$1 μm wavelength. Since then, tremendous progress has been made by improving the QD epitaxy, with

emission/absorption wavelengths engineered up to 1350 nm on GaAs substrates, well compatible with the CW-WDM MSA standard addressed in PUNCH. As GaAs-based technology is much cheaper than InP-based technology it is very attractive to substitute conventional InP-based quantum well by GaAs-based QD amplifiers. Moreover, the broad gain spectrum makes them an excellent choice for multi-wavelength signal amplification, with little gain variation between the different channels. On top of that the high temperature operation, the low amplified spontaneous emission (because of higher inversion level due to a high amount of upper energy level states) and the lower non-linear effects (lower self-gain modulation because of shorter capture time in QDs, hence faster gain recovery; lower cross-gain modulation because of lower homogeneous broadening; lower cross-phase modulation, because of reduced linewidth enhancement factor (QD$\sim$2 vs. QW$\sim$5)) makes them ideal for the envisioned applications. Evanescent coupling between Si and III-V is used to provide gain by the GaAs QD region, which will require suitable mode overlap with this gain region. Within PUNCH, a III-V foundry process for developing micro-transfer printing compatible GaAs QD SOAs is being established.

V. Control and Configuration Electronics to Power-monitor, Control and Actuate a Scaled Switch Fabric

The optical switch control electronics are integrated in a single, multi-channel custom-design integrated circuit. Each channel consists of a dedicated driver that needs to deliver either sufficient voltage swing (10 V to 15 V, to drive the thermo-optic or electro-optic switches) or drive current (100s of mA in the case of the SOAs), with nanosecond rise- and fall times.

VI. Fanout Wafer-Level Packaging for Dense Integration of PICs and EICs

Multiple approaches exist for integrating PICs with interfacing EICs. 2D integration where the PIC and EIC are placed side by side and connected with wirebonds is the simplest approach, but the wirebond inductance can introduce significant parasitics, and the density is limited as connections can only be made between one shared edge. 3D integration where the EIC is flipped on top of the PIC provides dense pitches on the order of 50 μm, with microbumps having minimal parasitics. However, a drawback of 3D integration is the need for wire bonding or TSVs when interconnecting the transceiver to the electronic resources (e.g. compute). 2.5D integration where the PIC and EIC are integrated on a common interposer substrate and electrically interconnected with the help of redistribution layers is getting more and more attention. While interposers can be constructed from a variety of materials (incl. silicon, glass and organics), within PUNCH we will leverage fanout wafer-level packaging (FOWLP).

Fan-out wafer-level packaging is an emerging type of advanced packaging technology in the semiconductor industry that is rapidly gaining popularity. FOWLP starts with known good die (KGD) assembly on carrier wafer, followed by embedding in an epoxy mold compound (EMC), back-grinding to provide surface planarity, and debonding of the reconstructed wafer from the carrier. The electrical redistribution layer based on thin film technology is finally applied on the reconstructed molded wafer, providing die-to-die connectivity [5]. The process flow is illustrated by Fig. 4. The heterogeneous integration capability of FOWLP is superior to any other packaging technology: multiple pre-tested elements with different functionalities can be placed very close together (down to 100 μm) during the reconstruction, resulting in modules with very short interconnects. The 200 mm FOWLP process developed within PUNCH enables a two-layer thin film ERDL with line/spacing of 10/10 micron, playing a crucial role in electrical packaging of the PUNCH large-scale switch fabrics. The ERDL is used to connect the thin chip integrated III-V components with the PIC as well with the EIC and periphery.

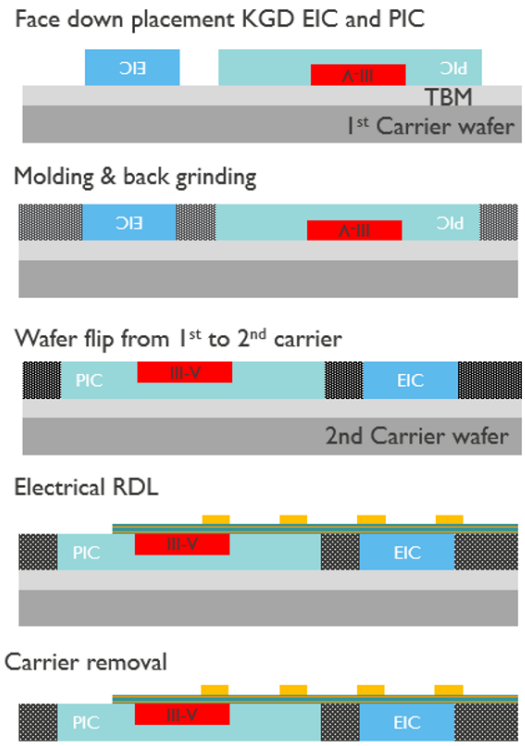

Fig. 4. PUNCH fan-out wafer-level packaging process flow for dense integration of PICs with EICs, enabled by the electrical redistribution layer.

VII. PIC interfacing using optical redistribution layers

The ORDL is based on polymer optical waveguides, consisting of a higher index core sandwiched in between lower index cladding layers. Different polymers are commercially available with excellent properties in terms of low optical loss, refractive index controllability, high temperature stability, compatibility with reflow soldering, good adhesion, dimensional stability, low birefringence and stable optical properties. Prime can-

didate waveguide materials include EpoCore/EpoClad from micro resist technology (Germany), or organic–inorganic hybrid resins from Nissan Chemical Ind., Ltd. (Japan). Typical polymer waveguide cross-sectional dimensions are $5 \times 5\,\mu\text{m}^2$, see also Fig. 5 [6] [7]. For coupling between the ORDL and PIC, PUNCH investigates adiabatic coupling based on SiN or Si tapers.

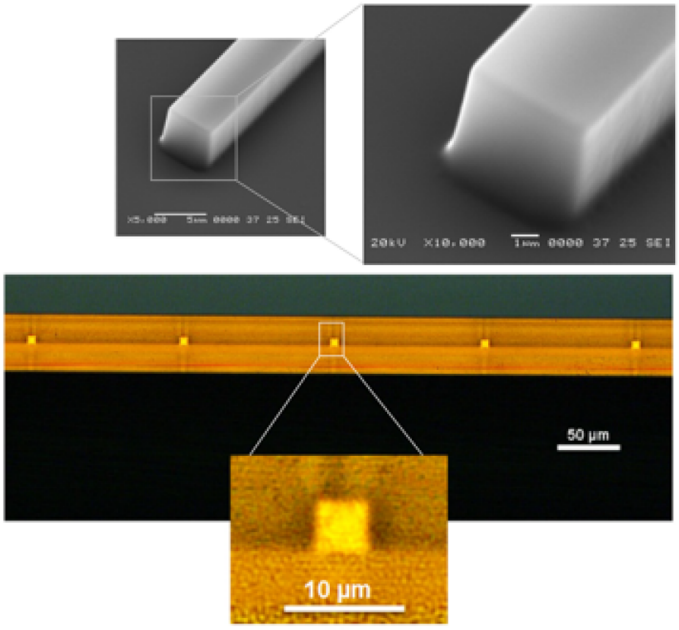

Fig. 5. Polymer waveguide based ORDL for interfacing different PICs and PICs with fiber arrays.

The exact taper layout is defined based on a semi-analytical method, by ensuring a large overlap between consecutive sections in the taper [8]. A representative EME simulation result (using Lumerical) is included in Fig 6, showing the SiN-ORDL coupler loss as function of taper length, for various wavelengths in the O-band. Designs with coupler lengths below 1 mm, while maintaining a coupler loss below 1 dB for both polarizations over the entire O-band spectrum, are available. When investigating the tolerance for aligning the ORDL with respect to the PIC, we find a 1-dB lateral alignment tolerance of $\pm 1.8\,\mu$m. In addition, PUNCH is developing a scalable solution for optical fiber packaging, using the ORDL. Indeed, the ORDL provides fan-out capabilities between the dense pitch of waveguides on the PIC and the coarse pitch of fiber arrays, e.g. $250\,\mu$m for standard 1×12 fiber-arrays.

VIII. Hybrid Integration on Organic Substrates

Multiple FOWLP packages containing the PIC and EICs will be integrated onto a high-density substrate containing the ORDL. Multiple approaches for integrating the fanout package onto the high-density substrate are being investigated, including flip chip technology and substrate embedding. More detailed implementations will be shared as part of future work.

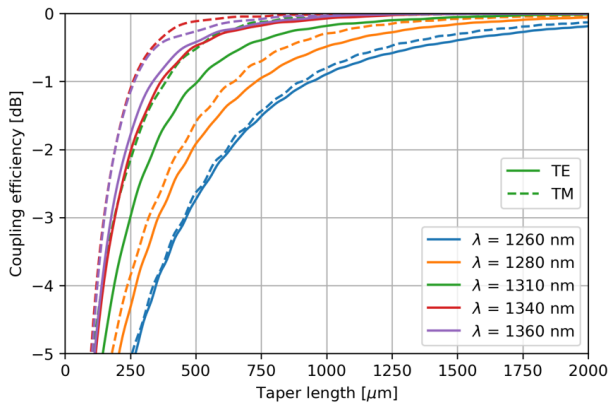

Fig. 6. Broadband behaviour of the adiabatic SiN-ORDL coupler, resulting from Lumerical Mode EME simulations.

IX. Future Demonstrations

In the Datacenter context, optical circuit networks are widely considered as a networking fabric that enables the organization of fine-grained resources into independent pools [9]. Optical circuits allow for savings in power and latency by reducing the number of hops in the network: less transceivers, less retimers, less ASICs with processing and queueing which are all very important for materializing datacenter resource disaggregation. In this networking setup, the optical switch has the very important role of creating, timely and on-demand, the circuit network permutations that combine the datacenter resources which are required by the arriving jobs. We will demonstate a disaggregated memory architecture that will be built around PUNCH switch and evaluate on full-fledged prototype platform all the key performance aspects of cloud datacenter workloads.

X. Conclusions

PUNCH offers a solution for time-deterministic and time-sensitive networks by developing a new optical switching paradigm which (I) breaks the trade-off between flexibility (ultra-dynamic reconfigurability) and determinism (guaranteed latency and jitter) by offering an all-to-all reconfigurable interconnect; (II) reduces congestion by activating bandwidth steering so that additional capacity can be allocated between hot nodes in the network; (III) provides unparalleled dynamics and bandwidth efficiency by further enabling multiplexing in the time domain with fast reconfigurable capability. A 2×2×Nλ wavelength selective switching element will be scaled to a fully non-blocking 8x8xNλ reconfigurable optical switch fabric. The development of a III-V foundry process for micro-transfer-printing-compatible semiconductor optical amplifiers enables loss-less optical switching on a silicon photonics platform. Custom configuration electronic ICs to actuate, control, and power-monitor a scaled switch fabric will be densely integrated with the photonic ICs into a heterogeneous fanout wafer-level package, processed on a 200mm reconstructed wafer platform. In addition, the optical interfacing to the

photonic ICs will be accomplished using an optical redistribution layer, providing an optical fanout on high-density organic substrates, and allowing for a scalable optical fiber packaging solution. In future, the novel integration and packaging processes will also be applied for manufacturing optical transceivers providing the interface between optical switches and electronic resources. The optical switch and transceiver prototypes will be demonstrated in memory disaggregation in data centers, and in the context of a 5G RAN Transport Network.

REFERENCES

[1] Y. Huang, Q. Cheng, A. Rizzo, and K. Bergman, "Pushpull microring-assisted space-and-wavelength selective switch," Opt Lett. 2020 May 15;45(10):2696-2699.

[2] J. Juvert, T. Cassese, S. Uvin, A. de Groote, B. Snyder, L. Bogaerts, G. Jamieson, J. Van Campenhout, G. Roelkens, D. Van Thourhout, "Integration of etched facet, electrically pumped, C-band Fabry-Perot lasers on a silicon photonic integrated circuit by transfer printing," Optics Express 26(17), p.21443, 2018.

[3] J. Zhang, B. Haq, J. O'Callaghan, A. Gocalinska, E. Pelucchi, A. José Trindade, B. Corbett, G. Morthier, G. Roelkens, "Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser," Optics Express 26(7), 8821-8830, 2018.

[4] G. Muliuk , K. Van Gasse, J. Van Kerrebrouck, A. José Trindade, B. Corbett, D. Van Thourhout, and G. Roelkens, "4x25Gbit/s polarisation diversity silicon photonics receiver with transfer printed III-V photodiodes," IEEE Photonics Technology Letters 31(4), 287-290, 2019.

[5] T. Braun, K.F. Becker, O. Hoelck, S. Voges, R. Kahle, M. Dreissigacker, M. Schneider-Ramelow, "Fan-Out Wafer and Panel Level Packaging as Packaging Platform for Heterogeneous Integration," Micromachines, 2019 May 23;10(5):342.

[6] A. Elmogi, E. Bosman, J. Missinne, and G. Van Steenberge, "Comparison of epoxy- and siloxane-based single-mode optical waveguides defined by direct-write lithography," Optical Materials, Volume 52, 2016, Pages 26-31.

[7] A. Elmogi, A. Desmet, J. Missinne, H. Ramon, J. Lambrecht, P. De Heyn, M. Pantouvaki, J. Van Campenhout, J. Bauwelinck, and G. Van Steenberge, "Adaptive Patterning of Optical and Electrical Fan-Out for Photonic Chip Packaging," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019, pp. 1757-1763.

[8] J. Van Asch, J. He, J. Missinne, G. Lepage, J. Van Campenhout, and G. Van Steenberge, "Design of a Broadband Adiabatic Coupler for Interfacing PICs to Optical Redistribution Layers," IEEE Benelux Photonics Chapter, Annual Symposium 2022, Eindhoven, The Netherlands.

[9] C. Pinto et al, "ThymesisFlow: A Software-Defined, HW/SW co-Designed Interconnect Stack for Rack-Scale Memory Disaggregation,", IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020.