Modeling the Electrical Degradation of Micro-Transfer Printed 845 nm VCSILs for Silicon Photonics

Michele Zenari, *Student Member, IEEE*, Matteo Buffolo, *Member, IEEE*, Carlo De Santi, *Member, IEEE*, Jeroen Goyvaerts, Alexander Grabowski, *Member, IEEE*, Johan Gustavsson, Roel Baets, *Life Fellow, IEEE*, Anders Larsson, *Life Fellow, IEEE*, Günther Roelkens, *Senior Member, IEEE*, Gaudenzio Meneghesso, *Fellow, IEEE*, Enrico Zanoni, *Life Fellow, IEEE*, and Matteo Meneghini

***Abstract*—This article deals for the first time with the electrical degradation of novel 845 nm vertical-cavity silicon-integrated lasers (VCSILs) for silicon photonics (SiPh). We analyzed the reliability of these devices by submitting them to high current stress. The experimental results showed that stress induced: 1) a significant increase in the series resistance, occurring in two separated time-windows and 2) a lowering of the turn-on voltage. To understand the origin of such degradation phenomena, we simulated the *I-V* characteristics and the band diagrams by a Poisson-drift-diffusion simulator. We demonstrated that the degradation was caused by the diffusion of mobile species capable of compensating the p-type doping. The diffusing species are expected to migrate from the p-contact region in the top distributed Bragg reflector (DBR) towards the active layers.**

***Index Terms*—Degradation, diffusion, impurities, silicon photonics (SiPh), vertical-cavity silicon-integrated laser (VCSIL).**

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Michele Zenari, Matteo Buffolo, Carlo De Santi, Gaudenzio Meneghesso, and Enrico Zanoni are with the Department of Information Engineering, University of Padua, 35131 Padua, Italy (e-mail: michele.zenari@dei.unipd.it; matteo.buffolo.1@unipd.it; carlo.desanti@unipd.it; gauss@dei.unipd.it; zanoni@dei.unipd.it).

Jeroen Goyvaerts is with LIGENTEC SA, 1024 Ecublens, Switzerland (e-mail: jeroen.goyvaerts@ligentec.com).

Alexander Grabowski, Johan Gustavsson, and Anders Larsson are with the Photonics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden (e-mail: alexander.grabowski@chalmers.se; johan.gustavsson@chalmers.se; anders.larsson@chalmers.se).

Roel Baets and Günther Roelkens are with the Photonics Research Group, Ghent University-imec, 9052 Ghent, Belgium (e-mail: roel.baets@UGent.be; gunther.roelkens@UGent.be).

Matteo Meneghini is with the Department of Information Engineering and the Department of Physics and Astronomy, University of Padua, 35131 Padua, Italy (e-mail: matteo.meneghini@unipd.it).

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I. Introduction

OVER the last decade, silicon photonics (SiPh) research and development have severely increased both the complexity and compactness of integrated photonics [1]. SiPh enables a wide range of applications, including datacom and telecom applications [2], sensors [3], and light detection and ranging systems (LIDARs) [4]. One of the key features that enables the widespread of SiPh is represented by the low-loss silicon waveguides (WGs) that can be integrated in highly scaled optical systems through conventional CMOS processes. Moreover, CMOS fabrication techniques provide improved scalability and low costs: as data rates are predicted to increase from 100 Gb/s to Tb/s by 2030 [5], [6], it is essential to reach high modulation bandwidths and to scale down the power consumption. SiPh can meet both these requirements [7] by properly designing the signal conditioning circuitry and the signal source, i.e., laser diodes. Indeed, concerning the power requirements, laser diodes have a significant impact on terms of power consumption inside a photonic integrated circuit (PIC). These semiconductor devices are responsible for converting electrical power into optical power, thus influencing the power efficiency of the entire PIC [8]. Among the different types of laser diodes, the most promising for the 850–950 nm communication window are the so-called vertical-cavity surface-emitting lasers (VCSELs). VCSELs ensure low threshold current and high-power efficiency. Moreover, these devices have low active region volume making them suitable for being directly modulated without the use of any external device [9]. Nonetheless, the integration of laser sources onto silicon substrates has always been problematic. Indeed, optoelectronic devices such as lasers diodes are commonly composed of direct gap III−V materials. Silicon is an indirect bandgap semiconductor, therefore is not suitable for an efficient emission of light [10]. In order to combine the efficiency of III–V materials and all the advantages provided by silicon manufacturing processes, different strategies can

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be adopted to integrate III−V LDs on silicon or silicon on insulator (SOI) substrates [11]. The direct growth of compound semiconductors onto Si [12] leads to the generation of crystalline defects caused by the lattice constant mismatch and the thermal expansion coefficient mismatch between the different materials. Defects can grow and propagate through the device, possibly resulting in poor optical performances and reduced lifetimes [13]. Another integration approach is represented by the so-called hybrid integration [14], which consists in growing the laser onto a native substrate and then boding it to the target substrate on which the PIC is formed. In the last decades, this integration approach evolved a lot, allowing many new types of integration methods to be industrialized. One of these techniques is known as "micro-transfer printing" [15]. This fabrication process consists in growing the VCSEL on a native substrate to obtain a high-quality device. Afterwards, by etching a sacrificial layer (placed close to the substrate), it is possible to detach the VCSEL which is picked-up with a stamp. Finally, the VCSEL is transferred to the target substrate (commonly Si or SiN) and attached to it by adhesive bonding. The resulting device is called vertical-cavity silicon-integrated laser (VCSIL). The feasibility of this process has recently been demonstrated by Roelkens et al. [15]. Despite the devices showed very-good performance, their stability over operating life has not been investigated, yet. In particular, it has been not addressed whether micro-transfer printing is responsible or not for reliability concerns.

In our previous work [16], we focused on the optical degradation of these novel devices. In particular, we addressed the degradation to the diffusion of impurities affecting differently the optical characteristics depending on the region in which they were migrating. The aim of this new study is to prove a more comprehensive understanding of the previously identified degradation process, by modelling the electrical variations through physics-based simulations, and by correlating them with the previously observed worsening of the optical characteristics. The outcome of our new work demonstrated that the variation in series resistance and turn-on voltage of the device are both caused by the diffusion of impurity species, which also affect the optical characteristics, that predominantly acts as p-dopant compensator or nonradiative recombination center (NRRC), depending on the region in which these impurities are diffusing at a particular stage of the experiment. Indeed, at the beginning, defects are affecting the reflectivity and/or absorption of the top distributed Bragg reflector (DBR) mirror increasing the threshold current. At the same time, the same impurities affect the electrical properties of the device increasing the series resistance. During the last part of the aging process, the defects reach the active layers causing not only an enhanced optical degradation but also a second variation of the series resistance. This degradation mode is remarkably new, since most of the past reports on the degradation of oxide-confined VCSELs blamed the presence of extended defects (such as dark line defects) and/or cracks, mostly coming from the oxide layers, as the root cause of the poor device lifetime observed [17], [18], [19]. These defects are supposed to be already present in the semiconductor material after device growth, worsening the radiative efficiency or acting as preferential sites for the formation of additional defects. This study is of fundamental importance to understand the reliability-limiting factors and to improve the electrical characteristics of these novel devices, to provide long-lasting and efficient PICs based on SiPh.

II. Samples Under Test

The devices analyzed within this work are VCSILs emitting at 845 nm. Each device consists of a III−V VCSEL, designed for bottom-emission, and a SiN_x WG realized on a silicon substrate. The structure, starting from the top, includes a Ti/Pt/Au disk-shaped p-contact that serves both as electrode and as a top reflector. The top DBR is p-doped with carbon and consists of 29 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. At the bottom of the p-DBR, within the layer closest to the separate confinement heterostructure (SCH) region, a 30 nm $Al_{0.98}Ga_{0.02}As$-layer is included for the formation of an oxide aperture, about 4 μm wide, through selective wet oxidation. The presence of this aperture laterally confines the current, and consequently the optical mode to the center of the circular VCSEL structure. The active area of the laser is located below the aperture and consists of a $1-\lambda$ thick SCH and a multiquantum-well (MQW) structure containing five 4 nm thick $In_{0.10}Ga_{0.90}As/Al_{0.37}Ga_{0.63}As$ QWs. The bottom DBR is n-doped and is composed of 23 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. A Ni/Ge/Au n-contact is positioned a few DBR mirror pairs below the active volume. At the bottom of the n-DBR, a 527 nm $Al_{0.12}Ga_{0.88}As$ buffer layer is purposely included to tune the cavity length between the bottom DBR and the diffraction grating. Underneath this layer, a 4 nm GaAs layer serves as an etch stop layer with respect to an $In_{0.49}Ga_{0.51}P$ sacrificial layer, which is required for the micro-transfer printing process, as will be discussed below. The thin GaAs layer absorbs light at 850 nm, although the impact is minimized since the etch-stop layer is placed outside of the III−V cavity and the standing wave pattern has a node in correspondence of the thin GaAs layer.

Below the VCSEL, aligned with the oxide aperture, a diffraction grating was placed to couple the optical mode into a SiN/SiO_2 WG. The grating also provides polarization-dependent and mode-selective feedback, resulting in an extended cavity laser defined by the top oxide thickness of the cladding above the WG. The polarization selective feedback lowers the TE threshold gain to a value smaller than the TM threshold gain. As a result, the VCSIL emission is preferentially TE-polarized, and is laterally out-coupled into two SiN_x WGs to form the vertical-cavity silicon-nitride-integrated laser structure. The light inside the WGs propagates in both directions, and is out-coupled by means of a grating coupler [20] located on each side. Fig. 1 depicts a simplified schematic of the devices under test. Further information regarding the device epitaxy, growth, and fabrication can be found in [21].

III. Methodology

For our experimental purposes, one comprehensive sample has been aged and characterized on-wafer. Temperature control was achieved through a thermoelectric cooler

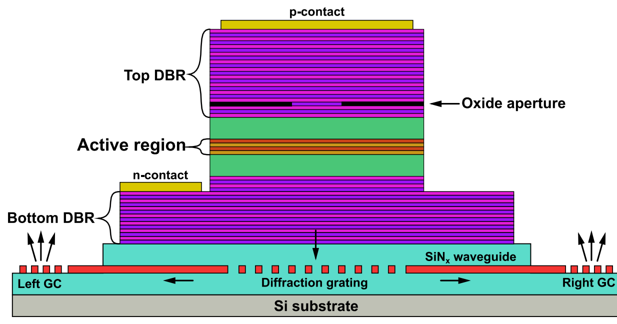

Fig. 1. Simplified cross section schematic view of the samples under investigation.

(TEC)-controlled baseplate. The electrical characterization was performed by means of an HP 4142 source-meter. Impedance measurements were performed by means of a Keysight E4980A LCR meter. Both stress and characterization were carried out at a fixed baseplate temperature of $T_{\text{AMB}} = 25$ °C.

To evaluate the degradation kinetics as a function of time, the devices were submitted to a constant-current stress experiment. The stress experiment was interrupted at different stages to evaluate the effects of device degradation by carrying out electrical (I-V, C-V) measurements. In this work, we analyze the results of a constant current aging test carried out at 3.5 mA. The stress current was chosen accordingly to our previous work [16] to observe the degradation kinetics in a reasonable amount of time (<30'000 min). Considering that the diameter of the oxide aperture is 4 μm, and that the average threshold current at room temperature (RT) is about 170 μA ($\approx$1350 A/cm^2), the corresponding stress current density is about 27 kA/cm^2, thus representing a highly accelerated stress condition.

IV. Simulation Framework

In order to simulate the electrical characteristics of the devices under test, we employed a commercial Poisson-drift-diffusion simulator [Synopsis Sentaurus Technology Computed Aided Design (TCAD)]. The simulations were carried-out by only considering the laser epitaxy of the VCSEL. Since we are interested in analyzing the changes in the electrical characteristics, we have not simulated the lasing of the same (this is not restrictive, since the variations of the turn-on voltage and of the series resistance affect the electrical properties of the lasers also below threshold).

The structure of the device was generated according to the description provided in paragraph II. The energy level for carbon p-doping was set to $E_V + 0.024$ eV, whereas the silicon n-doping energy level was imposed to $E_C - 0.005$ eV [22]. The metal–semiconductor contact at the p-side was implemented using 4.33 eV for the work function of the metal, corresponding to the value of Ti [23]. The tunneling contribution at the metal–semiconductor junction was considered according to the nonlocal barrier tunneling model described in [24]. The tunneling model accounts also for image force-induced barrier lowering of the conduction-band and valence-band edges [25].

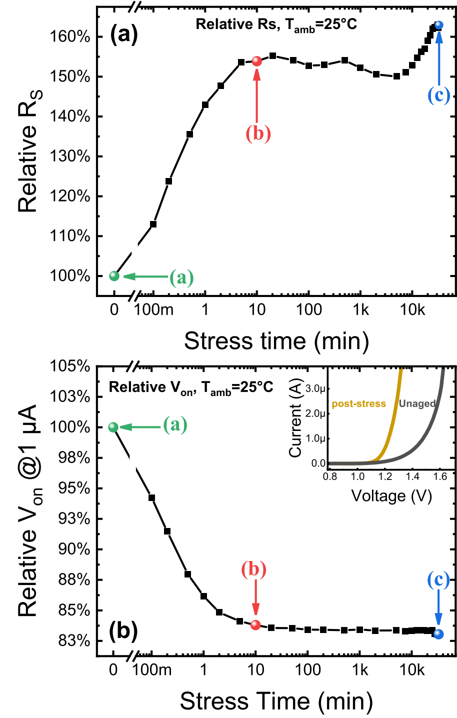

Fig. 2. (a) Series resistance kinetics. (b) Variation during stress of the turn-on voltage calculated for a current of 1 μA, in the inset is shown that the comparison of the unaged and post-stress I-V curves.

V. Experimental Details

From the outcome of the constant current stress test, we observed two different electrical degradation processes: a series resistance (R_S) increment and a turn-on voltage (V_{on}) lowering. Concerning the former, we indicated in Fig. 2 three remarkable points, case (A) which refers to the unaged series resistance, case (B) which indicates the end of the first series resistance increment, and ultimately, case (C) which indicates the amount of the second series resistance increment at the end of the aging experiment. In our previous work, where we investigated the worsening of the optical characteristics of VCSILs, we addressed the degradation process to the diffusion of impurities from the p-contact towards the active region. According to the results of the previous study [16], the degradation is divided into two phases: during Ph1 impurities cross the top DBR and worsen the mirror properties (also increasing the series resistance), whereas Ph2 is activated once the impurities reach the active region, starting a second series resistance increment and a strong decrease in the nonradiative recombination lifetime within the wells (see Fig. 8 from [16]). From the conclusions of the previous work and the inspection of the series resistance degradation, we supposed that impurities, hydrogen most likely [26], were responsible for compensating the p-doping inducing both series resistance increment and lowering of the turn-on voltage.

On the other hand, to explain the observed lowering in turn-on voltage [Fig. 2(b)], we have to briefly consider the outcomes of impedance spectroscopy analysis carried out before/after stress. In particular, through previous investigations, we observed an increase in the 1 MHz small-signal

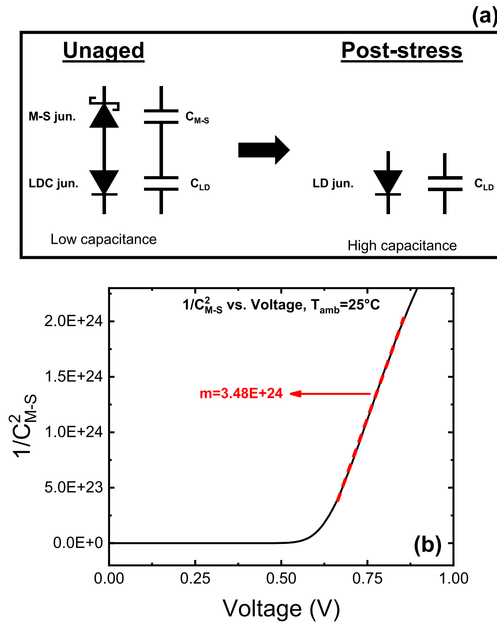

Fig. 3. (a) Schematic electrical model: unaged versus poststress. (b) $1/C^2$ versus voltage curve for determining the p-doping of the $M-S$ junction.

capacitance in the 0.5 ÷ 1 V range (see Fig. 9(a) in [16]). This behavior was explained by considering the stress-induced annealing of the parasitic Schottky contact, and related depletion capacitance, initially formed at the M-S interface.

To support this interpretation, we modeled the aforementioned variation by considering that the unaged C-V is equivalent to the series of the M-S and laser capacitance, whereas the poststress C-V describes only the laser capacitance [see scheme in Fig. 3(a)]. Knowing the formula of the series of two capacitances, we can estimate the C-V profile of the M-S junction by rearranging the formula

$$C_{\text{series}} = \frac{C_{\text{LD}} \cdot C_{M\text{-}S}}{C_{\text{LD}} + C_{M\text{-}S}} \Rightarrow C_{M\text{-}S} = \frac{C_{\text{series}} \cdot C_{\text{LD}}}{C_{\text{LD}} - C_{\text{series}}}. \quad (1)$$

By expressing the inverse of the square of capacitance versus the dc voltage, we can obtain the doping (N_d) of the parasitic M-S junction from the slope (m) of the curve [27]

$$N_d = \frac{2}{q\epsilon_s m A} \quad (2)$$

where q is the fundamental charge, A is the diode area, and ε_s is the electric permittivity of the semiconductor. According to the results [Fig. 3(b)], the apparent p-doping is about $7.56\cdot 10^{19}$ cm^{-3}: considering that the p-doping of the layer in contact with the metal is doped with a concentration of $1\cdot 10^{20}$ cm^{-3} this means that the compensating impurities are present in a concentration approximately equal to $3.44\cdot 10^{19}$ cm^{-3}.

In order to precisely calculate the concentration of doping compensation, we simulated the laser diode capacitance to estimate the parasitic capacitance that are not considered in the previous model. Indeed, from the results of our simulations, the laser capacitance at 0 V is approximately 200 fF but the corresponding experimental value is around 275 fF. The capacitance measured in reverse bias is practically fixed (200 fF) because the space charge region is determined from the intrinsic region (laser cavity) as the DBRs are heavily doped ($>1\cdot 10^{18}$ cm^{-3}). Nonetheless, we experimentally measure a higher capacitance as in the model we do not consider any parasitic effect. The difference among the experimental and simulated capacitance confirms that the device is affected by a parasitic contribution of ≈70–80 fF. If we consider the parasitic capacitance as a capacitor connected in parallel with the series of the M-S and lasers capacitors (for both unaged and post-stress curves), the outcome of the previous ($7.56\cdot 10^{19}$ cm^{-3}) calculations returns $3.08\cdot 10^{19}$ cm^{-3} as p-doping of the M-S junction. As a result, the apparent concentration of compensating impurities would be around $6.92\cdot 10^{19}$ cm^{-3}.

VI. Modeling of Degradation Process

According to the experimental evidence, the possible phenomena responsible for the observed electrical degradation of the VCSEL may include as follows.

1) Generation/propagation of defects and/or cracks from the bonding interface due to the micro-transfer printing [28].
2) Variation in the oxide aperture geometry and/or composition during the aging experiment. Variation in the conductivity of semiconductor regions close to the oxide aperture [29].
3) Diffusion of compensating impurities from the p-contact layers towards the active region.

The first two hypotheses are excluded since they would not explain the variation in the turn-on voltage exhibited by the I-V curves during the early stages of the stress experiment. Therefore, the possible cause of degradation can be identified in a diffusing species capable of compensating the p-type doping. In the previous section, hydrogen was already mentioned as a possible compensating species prone to diffuse [26], but the role of other defects is not excluded. Based on the previous considerations, the stress-induced variation in the electrical characteristics of the laser was modeled by considering a time-dependent redistribution of compensating impurities initially located in proximity of the p-contact. In particular, the electrical characteristics of the laser were simulated for each of the aforementioned cases [labeled (A), (B), and (C)]. The shape of the impurity profile was chosen by considering Fick's second law of diffusion, which describes the diffusion of a material inside another material, and whose general solution can be written as [30]

$$c(x,t) = \frac{1}{\sqrt{4\pi Dt}} e^{-\frac{x^2}{4Dt}} \quad (3)$$

where $c(x,t)$ is the concentration of the diffusing species, t is the time, x is the distance, N_0 is the initial concentration, and D is the diffusion constant. According to this formula, the diffusion profile is a Gaussian, whose amplitude and standard deviation (σ) are regulated by a square root dependence. Therefore, to emulate the electrical behavior (R_S and V_{on}) during the stress experiment, we selectively included in the simulated structure three different Gaussian distributions of shallow donors, whose spatial parameters have been tuned in

order to match the I-V curve of the device for each of the three aforementioned scenarios, with the constraints given by (3). These distributions emulate the time-dependent relocation of the compensating impurities supposedly occurring during the stress.

VII. Simulations Results: Series Resistance

At first, we focused on reproducing the series resistance variation. During this modeling stage, we considered both the n-contact and the p-contact as ideal ohmic electrodes (i.e., they can provide any current without voltage drops). Based on this configuration, we alternatively inserted the three shallow dopant profiles described in the previous section. The initial Gaussian profile, case (A), was chosen to have a peak n-doping concentration of $5{\cdot}10^{19}$ cm^{-3}, which is consistent with the apparent $6.92{\cdot}10^{19}$ cm^{-3} extrapolated from the C-V curves. We decided not to stick to a particular initial value as the actual parasitic capacitance cannot easily be determined with high accuracy. In fact, to properly measure the parasitic would be needed to precisely know the deposition of both metal contacts and passivation layers in order to address both submount and laser chip parasitic capacitances [31]. Together with the peak concentration, we chose a $\sigma \approx 30$ nm, in order to place the Gaussian close enough to the p-contact: these values were chosen in order to emulate the non-ideality of the p-contact as we suppose that the doping compensation close to the p-contact layers is affecting the M-S junction. The other two Gaussian profiles were calculated from (2), thus emulating the residual profiles of a diffusing species moving through the top DBR according to a diffusion process originated at the p-contact. Consequently, the integral of the three profiles is the same, that is, the total number of simulated impurity atoms remains unaltered within the whole structure. This last feature is crucial as we are considering that the total number of impurities is not varying during the diffusion, but are only relocated. The results of the three I-V simulations are shown in Fig. 4. Both curve (B) and (C) show a series resistance increment, but the increment from (A) to (B) is slightly more pronounced than the (B) to (C) variation, in agreement with the experimental results. Below, the three cases are further commented.

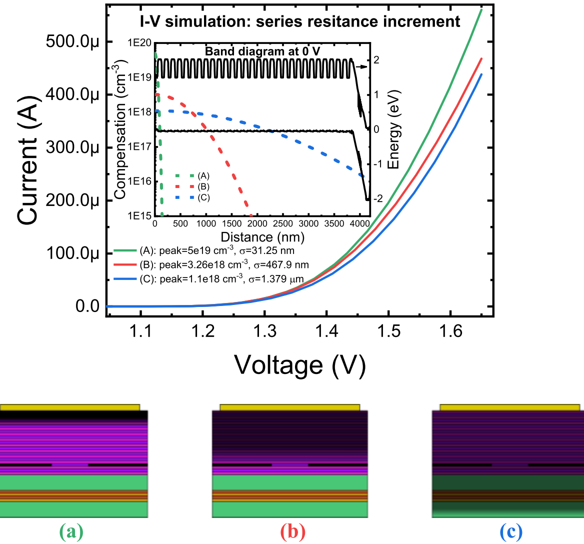

Fig. 4. I-V simulation of the series resistance increment. The impurities are supposed to diffuse from the p-contact towards the active region, causing the partial compensation of the p-doping. The inset in the graph reports the three Gaussian profiles of compensating impurity superimposed to the band diagram at 0 V. (a)–(c) Three phases of compensating impurity diffusion.

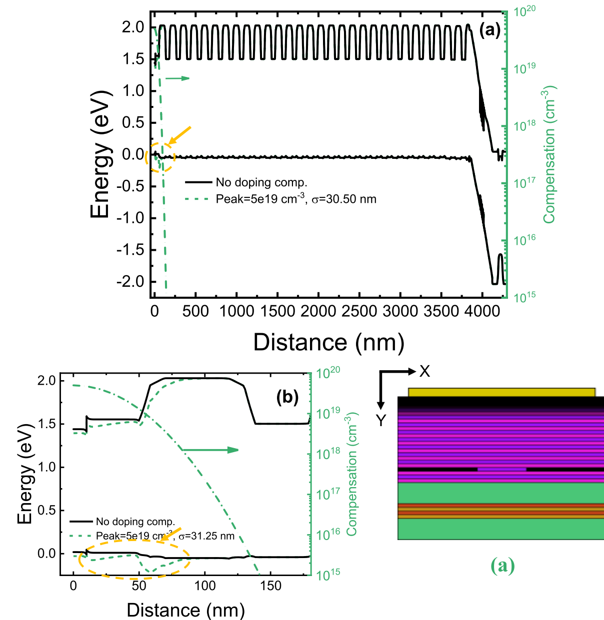

Fig. 5. (a) Band diagram comparison at 0 V: no doping compensation versus case (A) compensation. (b) Band diagram comparison at 0 V: zoomed-in view the region affected by the doping compensation.

A. Case (A): Unaged Device

In the scenario represented by case (A), the impurities are placed close to the p-contact in the upper part of the top DBR. In such condition, the compensating action of the impurities induces the generation of potential barriers in the valence band which are not present in the band diagram of the ideal device [see Fig. 5(b)]. Since the anode contact injects holes to the valence band edge, the new barriers locally limit the hole current, thus increasing the equivalent series resistance.

B. Case (B): Ph1 Degradation

During phase 1, the impurities are supposed to cross the top DBR, therefore we simulated a Gaussian profile with a lower peak concentration ($3.26{\cdot}10^{18}$ cm^{-3}) and, consequently, with a larger standard deviation ($\sigma = 468$ nm). In such condition, the doping compensation is still inducing the formation of some unwanted potential barriers (Fig. 6) in the valence band. Compared to case (A), case (B) features potential barriers, in particular toward the bottom part of the top DBR. The resulting series resistance confirms the increment observed through the experimental measurements.

C. Case (C): Ph2 Degradation

After the onset of the second degradation phase, Ph2, impurities start approaching the active region. In this case, the

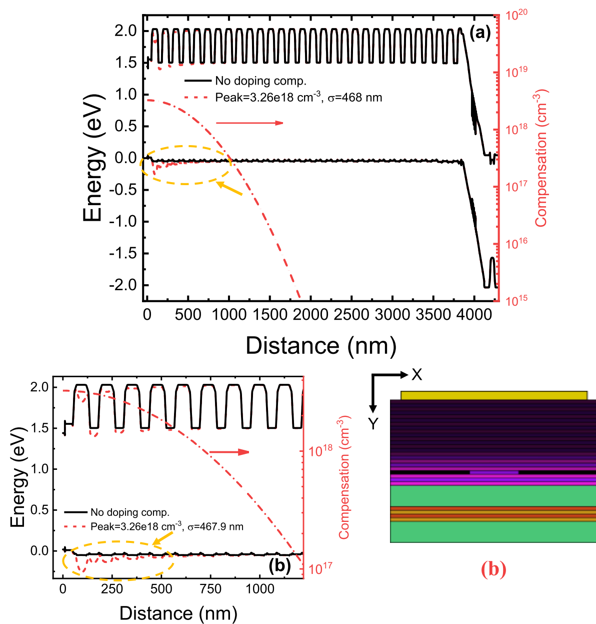

Fig. 6. (a) Band diagram comparison at 0 V: no doping compensation versus case (B) compensation. (b) Band diagram comparison at 0 V: zoomed-in view the region affected by dopant compensation.

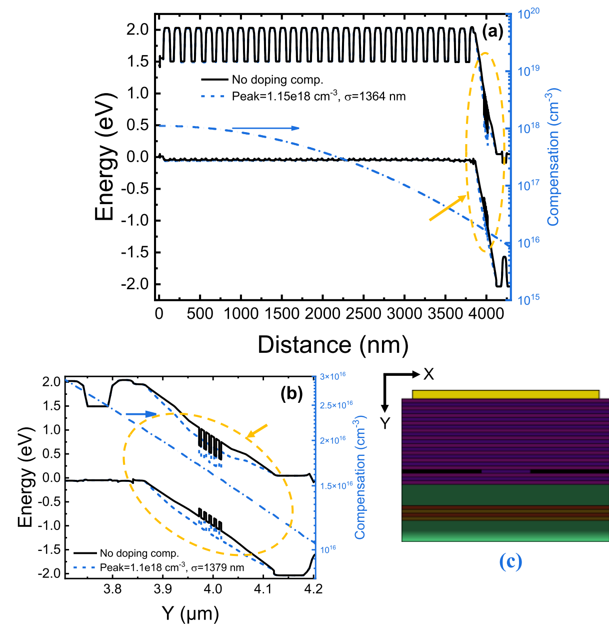

Fig. 7. (a) Band diagram comparison at 0 V: no doping compensation versus case (C). (b) Band diagram comparison at 0 V: zoomed-in view the region affected by the doping compensation.

impurities profile was modeled through a Gaussian curve with a larger standard deviation ($\sigma = 1379$ nm) and lower peak concentration ($1.15{\cdot}10^{18}$ cm^{-3}). As can be seen from Fig. 7, in this case, the Gaussian tail is very close to the active layers. Additionally, we can see that in this stage both the valence and conduction band edges are bending differently with respect to the simulation without impurities. These variations are sufficient to induce a further series resistance increment as the doping compensation in the top DBR is marginally affecting the valence band edges. The anomalous bending of the band edges could limit the carrier flow towards the active layers and/or induce the current to flow away from the center of the device (current shunting) because of the local increment of resistance.

Concerning this last hypothesis, since the band bending takes place close to the oxide aperture, it may be responsible for varying the current distribution imposed by the oxide layers. In a more realistic view, part of the impurities could remain locally stuck in the DBR layers, thus maintaining the series resistance increment of case (B) [see also the flat R_S kinetics after point (B) in Fig. 2(a)] and only a fraction of the initial amount of impurities reach the active region activating Ph2. However, since this would imply not only a more complex simulation framework but also a much more difficult analytical description, we decided to follow the simplified modeling, being aware of the aforenoted limitations. Nonetheless, this straightforward model allowed us to achieve reasonable results, providing quantitative data on the process ongoing in the devices.

VIII. Simulations Results: Turn-on Voltage

In this paragraph, we present the results of the simulation of the I-V characteristics carried out by including the nonideal metal–semiconductor junction that we assume to be formed at the p-contact in the unaged device. Therefore, in the following results, the simulator considered the misalignment between the work function of the metal and the Fermi level in the semiconductor. Moreover, we included in the model also the contribution of the intraband hole tunneling through the potential barrier formed in correspondence of the (spurious) p-Schottky contact at the M-S interface. The addition of these models allowed us to reasonably emulate both the series resistance and turn-on voltage variation through the action of a single process, i.e., a time-dependent relocation of compensating impurities from the top DBR. Fig. 8(a) reports the comparison between cases (A) and (B) with the unaged and poststress experimental curves. The graph shows that the unaged I-V characteristic can be accurately matched with a tunneling mass $m_{t,h} = 0.43$ (the electron tunneling mass, $m_{t,e}$ does not influence the tunneling at the p-side) which determines the magnitude of the tunneling current through the barrier highlighted in Fig. 8(b).

To match the experimental curves for low injection levels (<1 nA), we introduced the Shockley–Read–Hall (SRH) recombination in the barriers of the quantum wells with a carrier lifetime $\tau_{\mathrm{SRH,n}} = \tau_{\mathrm{SRH,p}} = 7$ ns. More details on the model of the SRH recombination implemented by the simulator can be found in [24]. When we simulate case (B), a great fraction of the compensating n-doping moved away from the p-contact region compared to case (A). As a consequence, the thickness of the potential barrier shown in Fig. 8(a) shrinks, thus favoring the tunneling of holes also at lower voltages. In fact, from the experimental data [Fig. 2(b)], we observed that the turn-on voltage lowering has reached saturation ($\approx$1.6 V) which is observed in other oxide confined VCSEL operating at 850 nm [32], [33]. By observing the simulated I-V characteristics of case (B) in comparison with

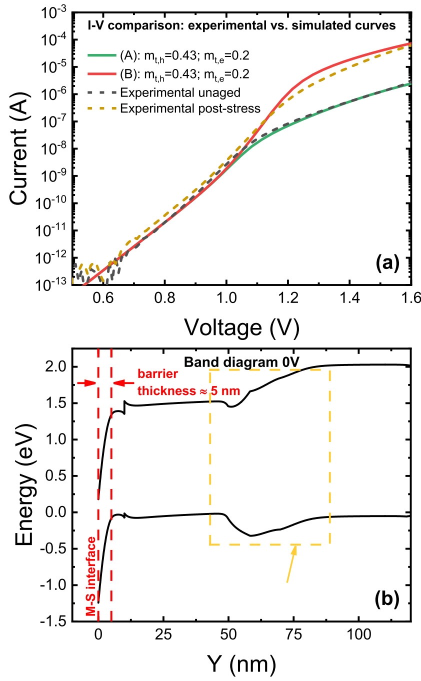

Fig. 8. (a) I-V comparison: experimental curves (dashed) versus simulated curves (solid). (b) Band diagram at 0 V for case (A) with metal–semiconductor modeling. The yellow rectangle indicates the potential barrier formed as a consequence of doping compensation.

TABLE I
SIMULATION PARAMETERS

Case	peak (cm^{-3})	σ (nm)	$\tau_{SRH,(n,p)}$ (ns)	$m_{t,h}$	$m_{t,e}$
(A)	$5\cdot10^{19}$	30.5	7	0.43	0.2
(B)	$3.26\cdot10^{18}$	467.9			
(C)	$1.15\cdot10^{18}$	1379			

Table 1. Parameters employed to simulate the three cases labeled as (A), (B), and (C).

the experimental I-V poststress, we can notice that the two curves are not perfectly superimposed above 1.2 V. From the differences between the two curves, we can observe that also the post-stress I-V characteristic cannot be represented with a single diode model. This may indicate that the annealing of the p-contact was not fully achieved even at the end of the stress procedure. This confirms the previous hypothesis regarding the partial trapping of diffusing impurities in the upper part of the top DBR occurring between the stress-induced device variations depicted by case (B) and (C). The main parameters used to simulate the electrical variation during the stress are summarized in Table I.

IX. Conclusion

In summary, in this work, we have analyzed and modeled the electrical degradation of the I-V characteristics of novel VCSIL devices submitted to a constant current stress at 3.5 mA (27 kA/cm^2). In agreement with previous studies, the degradation was found to be compatible with the diffusion of impurities able to passivate the p-doping. Initially, the impurities compensate the p-doping close to the p-contact metal, resulting in a delayed turn-on voltage of the I-V curve. When applying bias, the p-contact is annealed and the impurities start to migrate from the top of the p-DBR towards the active region, resulting in a first series resistance increment. At this point, as the impurities leave the region close to the p-contact, the turn-on voltage lowers reaching its final value after about 10 min. When the diffusing species approach the oxide aperture, and therefore the active layers, we observed a second series resistance increment associated with the worsening of the optical properties [16]. By means of numerical simulations, we modeled the degradation process through diffusion of a compensating impurity, which could also act as NRRC within the well region which allowed us to qualitatively reproduce both series resistance and turn-on voltage. The physical origin of the mobile species has been tentatively associated with hydrogen, since this element can easily be unintentionally introduced during the growth process and passivate carbon atoms, according to prior reports. The study demonstrated the importance of how proper growth/processing of contacts can improve the electrical performances of III−V devices and thus boost the energy efficiency of VCSILs.

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