Micro-Transfer Printing for Heterogeneous Si Photonic Integrated Circuits

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Abstract—**Silicon photonics (SiPh) is a disruptive technology in the field of integrated photonics and has experienced rapid development over the past two decades. Various high-performance Si and Ge/Si-based components have been developed on this platform that allow for complex photonic integrated circuits (PICs) with small footprint. These PICs have found use in a wide range of applications. Nevertheless, some non-native functions are still desired, despite the versatility of Si, to improve the overall performance of Si PICs and at the same time cut the cost of the eventual Si photonic system-on-chip. Heterogeneous integration is verified as an effective solution to address this issue, e.g. through die-wafer-bonding and flip-chip. In this paper, we discuss another technology, micro-transfer printing, for the integration of non-native material films/opto-electronic components on SiPh-based platforms. This technology allows for efficient use of non-native materials and enables the (co-)integration of a wide range of materials/devices on wafer scale in a massively parallel way. In this paper we review some of the recent developments in the integration of non-native optical functions on Si photonic platforms using micro-transfer printing.**

Index Terms—**Integrated optoelectronics, photodiodes, printing, semiconductor lasers, silicon on insulator technology, wafer-scale integration, waveguide components.**

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I. Introduction

PHOTONIC integrated circuits enable the miniaturization of photonic systems by integrating key optical functions on a single chip. SiPh is emerging as an important platform to realize such PICs, as one can leverage the CMOS technology infrastructure for realizing these circuits on 200 mm and 300 mm wafers with high yield. Moreover, the high refractive index contrast enables compact optical circuits and high-speed detectors and modulators due to the strong light-matter interaction. Besides using Si waveguides one can also realize the waveguides in silicon nitride (SiN), offering lower waveguide losses and a wider operational wavelength window. These SiN waveguides can either be combined with Si waveguides on the same platform, or constitute a separate, passive platform [1].

While passive optical functions, high speed modulation and detectors can be integrated in Si PICs, the platform lacks wafer-scale semiconductor optical amplifiers and lasers, which are realized in direct bandgap III-V semiconductors. Besides this functionality, some applications also require other functions, such as linear, ultra-high speed phase modulators, optical

isolators, strong non-linear materials or electronic integrated circuits, leading to the concept of heterogeneous Si PICs, where off-the-shelf Si PICs are complemented with non-native optical functions, using wafer-scale processes to integrate these non-native devices/materials onto the platform.

Si PICs with a Si device layer of 220 nm are emerging as one of the standard platforms, which is capable of addressing the 1200–2500 nm wavelength range, limited on one hand by the absorption of the silicon, and on the other hand by the limited mode confinement beyond 2500 nm.

In order to have optical gain in this wavelength range, either InP, GaAs (quantum dot active regions) or GaSb semiconductor optical amplifiers need to be integrated [2]. InP or GaSb diodes are also capable to go beyond the 1600 nm cut-off wavelength of integrated Ge photodiodes (PDs). The SiN waveguide platform (typically 150–400 nm thick SiN waveguides) has a wider transparency window extending further into the visible/near-infrared. Implementing optical amplifiers and lasers for this wavelength range requires the heterogeneous integration of GaN [3] and GaAs [4], [5] diode structures.

For modulators, different solutions exist, either using native Si modulators relying on the plasma dispersion effect (1200–2500 nm) or SiGe electro-absorption modulation (C+L band, O band devices under development), or requiring non-native materials such as $LiNbO_3$ [6], PZT [7] and III-V semiconductors [8]. Such materials can also be used for nonlinear optical functions. For non-reciprocal optical functions (optical isolators and circulators), typically magneto-optic materials such as Ce:YIG are to be integrated [9].

Finally, PICs require electronics to drive and control the photonic devices/circuits. The integration of photonic and electronic functions can be realized in different ways, ranging from monolithic integration to wire-bonding. Typically the electronics is implemented in (Bi)CMOS technology.

As the required functionality of a PIC increases, so does the need for integrating different optical functions on a single chip. This requires technologies to integrate the different materials and devices mentioned above on 200 mm and 300 mm Si photonic wafers. Currently, different technologies are being developed to address this need. The ultimate approach is hetero-epitaxial growth on silicon, as it is the most scalable approach. However, the quality of the grown materials is inferior to when it is grown on its native substrate [10], [11], posing challenges for device performance and reliability. Moreover, front-end integration of new materials requires modifying the SiPh process flow and can cause contamination issues. Die-to-wafer bonding and wafer-to-wafer bonding are technologies that bypass some of the issues of the hetero-epitaxial growth (material quality) as the materials are grown on their native substrate after which they are bonded to the Si photonic wafer (Fig. 1(a)), typically after the Si front-end processes are complete [12], [13]. This technology still requires substrate removal and the patterning of the devices (on a 200 mm/300 mm wafer scale) after bonding using lithographic techniques, which however enables the highest possible alignment accuracy and throughput, but is a complex process to develop. Also, yield can be an issue especially when yield-sensitive devices such as laser arrays need to
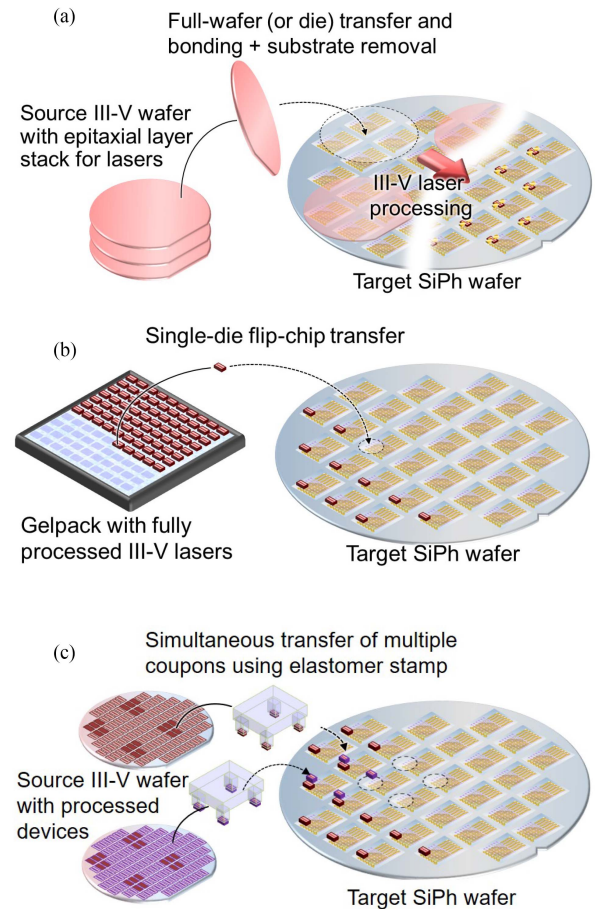
Fig. 1. Illustration of the III-V-on-Si integration on a SiPh wafer through (a) wafer-to-wafer bonding, (b) flip-chip and (c) micro-transfer printing. Reproduced with permission from J. Zhang et al., in APL Photonics (invited), 4, p.paper 110803, doi:10.1063/1.5120004 (2019). AIP publishing.

be integrated, as no pre-testing of the components is possible prior to integration. Fig. 1(b) illustrates the integration of III-V devices on a SiPh substrate through a flip-chip process. This approach on the other hand takes pre-fabricated opto-electronic components that are/can be pre-tested and aligns them using passive alignment techniques to the Si waveguide circuits (after the front-end and back-end is completed), followed by a soldering process. Using state-of-the-art tools an alignment accuracy of ± 0.5 μm 3σ or better can be obtained, enabling efficient optical coupling [14], [15]. The integration process is however quite slow, typically 100 units per hour. Micro-transfer printing starts from a finished Si photonic wafer (front-end + back-end). Only a local back-end opening where the devices need to be integrated is required to enable the optical coupling between the III-V devices and the waveguide circuits. As the components of interest are pre-fabricated on the source wafer prior to their integration on a target SiPh wafer, pre-testing is possible. The PDMS stamp can be patterned to define an array of posts so that a subset of source coupons can be picked-up and printed in a single printing operation, thereby enabling an efficient use of the III-V source material and a scale-out of a dense array of components on the (smaller) source wafer to a sparse array on the

TABLE I
A COMPARISON BETWEEN DIFFERENT III-V-ON-Si WAFER-SCALE HETEROGENEOUS INTEGRATION STRATEGIES

Technology	Integration density	CMOS compatibility	Efficiency of III-V material use	Alignment accuracy	Versatility in (co-)integration of non-inherent functionalities	Throughput	Cost	Maturity
Flip-chip	Low	Back-end compatible	Medium	Medium	Medium	Low	High	Mature
Heterogenous bonding	Medium	Back-end compatible	Medium	High	Low	High	Medium	Mature
µTP	High	Back-end compatible	High	Medium	High	High	Low	R&D
Epitaxial growth	Potentially high	Potentially front-end compatible	Very high	High	Low	High	Low	R&D

(larger) target wafer, as shown in Fig. 1(c). Using state-of-the-art tools $\pm$ 0.5 μm 3σ alignment accuracy can be obtained for reticle-sized stamps (2 cm $\times$ 2 cm) [16]. One printing cycle takes approximately 45 seconds. However, in one such cycle a large array of devices can be transferred, resulting in a high throughput integration. At no point individual dies need to be diced or handled (as is the case for flip-chip integration). Last but not least, this approach also allows for the intimate integration of different materials/devices on a common substrate. The pro and cons of the aforementioned heterogeneous integration technologies are summarized in Table I.

In this paper we propose the use of another integration approach, micro-transfer printing (μTP), that combines the advantages of die-to-wafer bonding integration (high throughput integration) with those of flip-chip integration (pre-fabrication and pre-testing of the nonnative components, high alignment accuracy integration, no disruption of SiPh process flow). After a discussion of the technology (Section II), we will discuss several proofs-of-concept of the technology for heterogeneous PICs (Section III) after which we present a conclusion and outlook (Section IV).

II. MICRO-TRANSFER TECHNOLOGY

The concept of μTP and the pre-fabrication of III-V components on the source wafer is illustrated in Fig. 2(a). Special for the μTP approach is that a release layer is to be integrated below the device layer stack. After patterning the devices in dense arrays on the source wafer, the devices are anchored to the wafer (either to the device layer or to the substrate) by using (typically dielectric) tether structures, after which the release layer is selectively under-etched, making the patterned components free-standing and kept in place by the tether structures. Next, a poly-dimethylsiloxane (PDMS) stamp is laminated against the released devices (called coupons hereafter) and the stamp is retracted fast from the source wafer. Due to the strong adhesion between the stamp and the devices in this process, the tethers break, thereby transferring the devices to the stamp. After device pick-up, the stamp with the device array is transferred to the target wafer, where it is aligned to the target wafer using pattern recognition (through the transparent PDMS stamp). The printing process requires laminating the stamp to the target wafer, followed by a slow retraction of the stamp (sometimes complemented with a shear force on the stamp) to leave the coupons on the target wafer. Depending on the type of devices that are transferred, the printing can be done on top of the back-end consisting of multiple dielectric and metal layers of
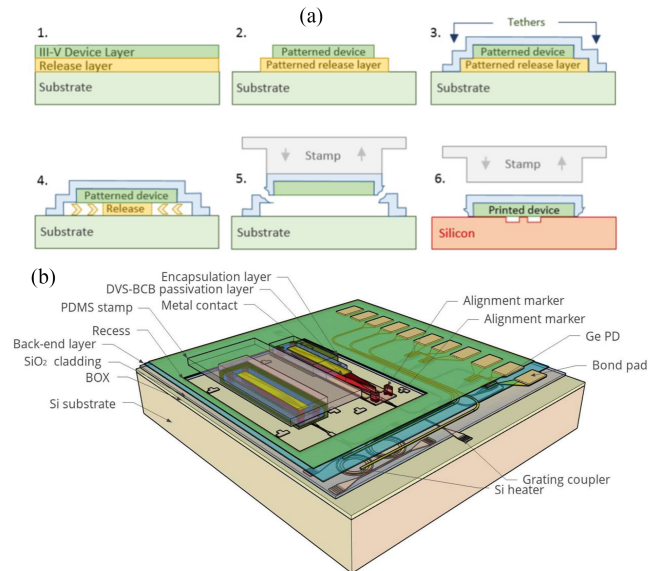
Fig. 2. Concept of μTP. (a) Pre-fabrication of III-V devices on their native substrate in dense arrays and the μTP integration on a target Si substrate. (b) Illustration of the integration of III-V-on-Si devices on a Si photonic wafer with back-end layers. Only a local opening (recess) is required to enable close contact of the III-V components to the Si device layer. Reproduced with permission from J. Zhang et al., in APL Photonics (invited), 4, p.paper 110803, doi:10.1063/1.5120004 (2019). AIP publishing.

the SiPh wafer, or in recesses where the local cladding layers over the Si waveguides were removed in the back-end, thereby enabling an intimate integration with the Si (SiN) device layer.

In order to enhance the adhesion of the coupons to the target wafer, often an adhesive bonding agent (e.g. divinylsiloxane bisbenzocyclobutene (DVS-BCB)) is applied [17], although molecular bonding is also possible, if the surface roughness of both mating surfaces is sufficiently low. Typically, after the printing process only a metallization is required to connect the transfer-printed components to the SiPh back-end [19], [20]. Fig. 2(b) illustrates the micro-transfer printing of pre-fabricated III-V components on a complex Si PIC, where only a local recess is needed to allow for an intimate integration of the III-V layers and the target Si waveguide circuits. Fig. 3(a) illustrates a proposed III-V/Si taper structure for the integration of C band InP SOA on the imec iSiPP50 g platform. This design provides over 1 μm lateral alignment tolerance that meets the placement accuracy provided by the micro-transfer printing system. The III-V/Si hybrid waveguide consists of a 4.5 μm wide III-V waveguide and a 2.5 μm wide poly-Si/Si rib waveguide with a thin DVS-BCB bonding layer in between. The poly-Si/Si rib
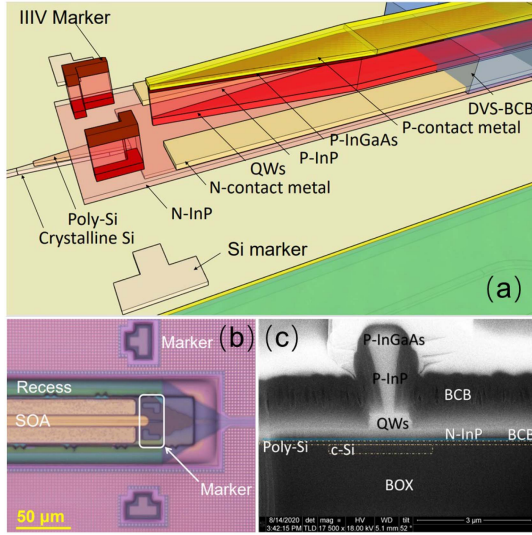
Fig. 3. (a) Schematic layout of a proposed III-V/Si taper structure with over 1 μm lateral alignment tolerance. (b) Microscope image of a transfer-printed InP SOA, showing the III-V taper structure and the markers. (c) Focus ion beam cross section image near the III-V/Si taper tip.

waveguide is formed by a 220 nm thick wire waveguide and a 160 nm thick slab poly-Si overlay layer. Fig. 3(b) shows a microscope image of the taper section of a transfer-printed InP SOA on an imec's iSiPP50 g chip where a set of fiducial markers on the SOA coupon and on the SiPh substrate, respectively, are used to enable the automatic alignment in the transfer printing process using pattern recognition. Fig. 3(c) shows a representative focus ion beam (FIB) image of the III-V/Si hybrid waveguide close to the taper tip.

In the next section we will discuss several proof-of-concept demonstrations that were realized in recent years. This includes the integration of InP DFB lasers, SOAs, C-band tunable lasers, wide tuning range lasers with >100 nm tuning range, mode-locked lasers on Si or SiN waveguide circuits, as well as GaAs VCSELs and PDs. Also LiNbO$_3$ phase shifters, Si PDs and InGaAs uni-traveling carrier PDs have been demonstrated.

III. PROOF-OF-CONCEPT DEMONSTRATIONS

A. III-V-on-Si DFB Laser With Integrated Booster

III-V-on-Si DFB lasers can be realized by using a hybrid waveguide laser cavity where the Bragg grating is patterned in the Si device layer and the gain is provided by the III-V optical amplifier coupon printed on top of the grating. Adiabatic III-V-on-Si taper structures are used at both sides of the coupon to couple the optical mode to the underlying Si waveguide circuits. Taking into account the alignment accuracy of the μTP system, an alignment-tolerant III-V-on-Si taper structure was introduced to ensure robust operation of the integrated III-V-on-Si devices constructed using μTP. C-band single mode III-V-on-Si DFB lasers have been demonstrated through this approach, as reported in [21], however, the laser output power is limited to 7 mW. Recently, a III-V-on-Si DFB laser with a co-integrated III-V-on-Si optical booster was demonstrated by
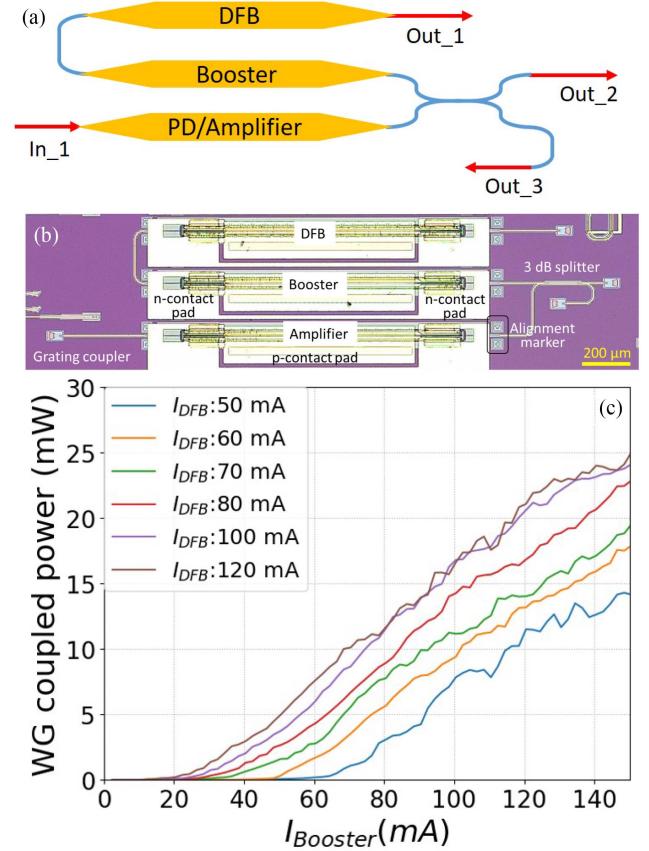
Fig. 4. (a) Schematic layout of the III-V-on-Si DFB laser with a co-integrated III-V-on-Si booster. The amplifier is used as a reference device. (b) Microscope image of the fabricated device. (c) Waveguide-coupled power as a function of applied booster current for different DFB bias currents.

transfer printing an array of identical pre-fabricated III-V waveguide amplifier structures onto the Si PIC. The schematic layout of the III-V-on-Si integrated circuit and the resulting device are respectively shown in Fig. 4(a) and (b). The bottom device can be used either as a photodetector to detect the back reflection from the optical system or as a reference optical amplifier to investigate the performance of the integrated booster.

The Si waveguide circuits were fabricated at imec, by 193 nm Deep-UV (DUV) lithography. The adopted platform includes a 400 nm thick crystalline Si device layer, features a 180 nm etch step to define the waveguide structures, and is planarized with SiO$_2$ down to the silicon device layer. The DFB laser cavity is based on a hybrid waveguide structure where a III-V amplifier waveguide is overlaid on a uniform second-order Bragg grating incorporated in a 4.5 μm wide Si rib waveguide, with a thin layer of DVS-BCB in between. Meanwhile, the booster and the photodetector/amplifier are based on a 3 μm wide continuous Si rib waveguide. The length, period and duty cycle of the Bragg grating are 600 μm, 475 nm and 75%, respectively. The pre-fabricated InP waveguide structures are 1140 μm long, consisting of a 780 μm long straight III-V rib waveguide and a pair of 180 μm long taper structures at both sides [22]. The III-V waveguides has a 3.2 μm wide p-cladding mesa and a 4.8 μm wide active region. A set of fiducials, both on the III-V

coupon and Si target, are used to align the III-V device to the target waveguide circuit using pattern recognition in the transfer printing process. Fig. 4(b) shows the resulting device, including deposited metal contact pads.

The aforementioned device was characterized on a temperature-controlled stage at $20\,^{\circ}$C. A pair of Keithley current sources, in combination with several DC probes, were used to simultaneously apply the bias current to the DFB laser and the booster. The light coupled out of grating coupler Out_2 was collected using a standard single mode fiber. Fig. 4(c) shows a set of measured waveguide-coupled powers as a function of applied bias current to the booster for different DFB bias currents. These measured waveguide-coupled powers were obtained by calibrating out the insertion losses introduced by the grating coupler and the integrated 3 dB splitter/combiner. The threshold of the DFB laser is 75 mA and it operates at 1540 nm. The waveguide-coupled output power reaches up to 25 mW with an overall applied current of 270 mA (DFB+booster). While the side mode suppression ratio (SMSR) reduces for these higher output levels, the device was still able to achieve 28 dB SMSR at maximum output power. The maximum wall-plug efficiency of the demonstrated device (DFB+booster) is around 4%.

B. C-Band Optical Transmitter With Integrated Widely Tunable Laser

The previous section showcases the realization of III-V-on-Si integrated circuits on planarized Si PICs. In this section, we will demonstrate the integration of III-V-on-Si widely tunable lasers on an advanced photonics platform with a back-end layer stack, namely imec's iSiPP50 g, using μTP. A variety of passive components and high-speed Si and Si/Ge active components are available on this platform. However, a local back-end opening (recess) is required to access the Si waveguide and enable co-integration of the III-V devices and the Si structures. Compared to die-to-wafer bonding, this approach minimizes the disruption to the established Si photonics process flow. In contrast to the use of a planar target substrate, here a spray-coating technique is adopted to deposit a thin and uniform DVS-BCB bonding layer in the recesses [23]. Following this method, we demonstrated an integrated III-V/Si optical transmitter with a widely tunable III-V-on-Si laser.

Fig. 5(a) shows the schematic of the proposed transmitter, which consists of a C-band widely tunable laser, a high-speed Si Mach-Zehnder interferometer(MZI) modulator and a tunable splitter in between. The latter can be configured to send a fraction of the light to a Ge photodetector to monitor the laser output. The MZI modulator incorporates a 1.5 mm long Si carrier-depletion phase modulator and a thermal phase shifter in each arm. The widely tunable laser has a ring cavity consisting of two micro-ring resonators with slightly different radii (25 μm and 27 μm) to select a single longitudinal cavity mode over a 40 nm wavelength range in C-band using integrated micro-heaters. Furthermore, the ring cavity includes a 1.15 mm long active region where the SOA is integrated and a directional coupler to couple out the laser light towards the modulator. A Sagnac loop mirror, formed by connecting the two output ports of a 1×2 MMI, is attached
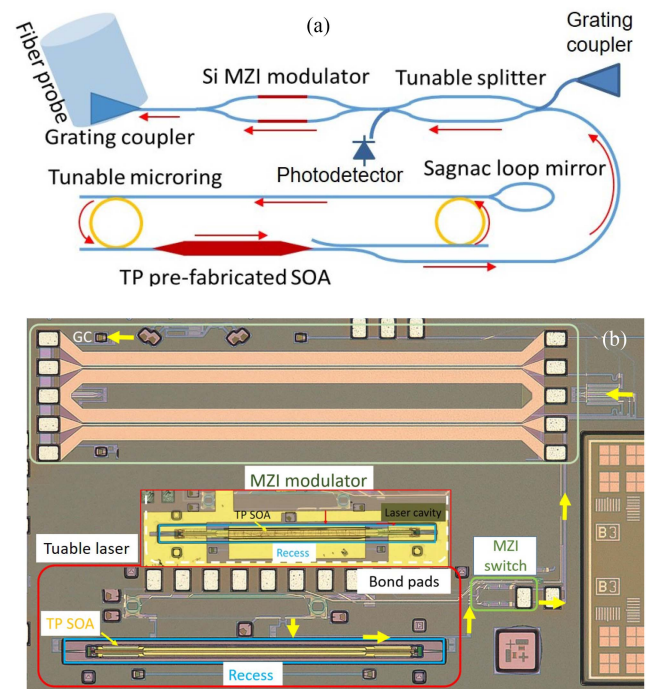
Fig. 5. (a) Schematic layout of the integrated optical transmitter. (b) Microscope image of PICs with a micro-transfer-printed III-V amplifier in the pre-defined recess. The inset microscope image shows the micro-transfer-printed SOA after metallization.

to one port of one of the micro-ring resonators to provide an external feedback. This explicit feedback technique ensures that the counter-clockwise propagating mode is coupled into the clockwise propagating mode, thereby obtaining unidirectional operation [24]. The overall length of the laser cavity is around 3.4 mm. The active region has a 220 nm thick and 3 μm wide crystalline Si (c-Si) wire waveguide overlaid with a 160 nm thick poly-Si slab. On top of this poly-Si/Si waveguide, a thick SiOx cladding layer is present. A poly-Si/Si taper structure is used to convert the optical mode from the standard 220 nm c-Si strip waveguide, used elsewhere in the transmitter, to the poly-Si/Si waveguide that is part of the active region of the laser. The SiOx cladding over the active region with an area of 80 μm × 1335 μm is first removed using a combination of reactive ion etching (RIE) and a short BHF wet cleaning, resulting in a 3.6 μm deep recess. After that a thin DVS-BCB layer ($<$ 50 nm) is spray-coated on the photonic chip at EV Group. Subsequently, the transfer printing of pre-fabricated III-V SOAs was performed using an X-Celeprint μTP-100 lab-scale printer. The photonic circuit with a transfer-printed SOA is shown in Fig. 5(b).

First, the fabricated III-V-on-Si tunable laser was characterized at $20\,^{\circ}$C without the modulator. The differential resistance of the μTP III-V SOA is 6.5 Ω at 130 mA and the maximum waveguide-coupled power is found to be 2 mW at 130 mA bias. The threshold of the laser is around 100 mA when operating at 1553 nm and the maximum wall-plug efficiency is about 0.7 %. By actuating both heaters of the micro-ring resonators, contributing to the Vernier filtering effect, and the phase section simultaneously, over 40 nm tuning range was achieved, as shown in Fig. 6(a). Secondly, optical back-to-back transmission

Fig. 6.   (a) Wavelength tuning over 40 nm in C-band. (b) Measured NRZ eye diagrams at 28 Gbit/s and 40 Gbit/s for different wavelengths.

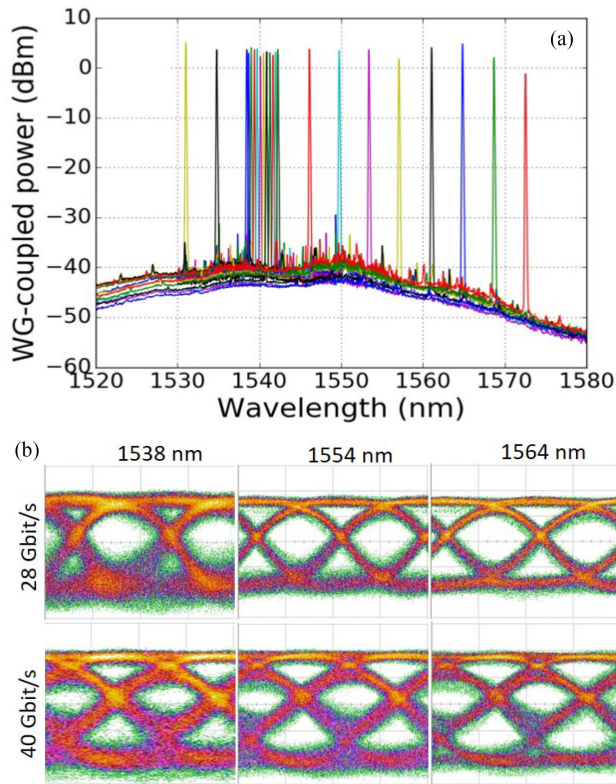Fig. 7.   (a) Microscope picture of a sample of coupons of InP based semiconductor optical amplifiers including an InGaAlAs multi-quantum-well. (b) Microscope picture of integrated heterogeneous III-V-on-SiN mode-locked lasers. (c) scanning electron microscopy of a III-V semiconductor optical amplifier. (d) Optical spectrum generated by a heterogeneous III-V-on-SiN mode-locked laser. (e) Electrical spectrum of a heterogeneous III-V-on-SiN mode-locked laser.

experiments were performed on a high-speed setup at $20\,°C$. An arbitrary waveform generator (AWG) was used to generate two identical 2^9-1 long non-return-to-zero PRBS signals. Those signals were boosted by RF amplifiers, combined with the correct bias levels using a pair of bias tees, and subsequently injected into the MZI modulator using a GSGSG RF probe. The bias current applied onto the integrated SOA was kept at 130 mA. The modulated optical signal was detected by a commercial high-speed optical receiver after being boosted through an EDFA. A sampling scope was used to present the electric output signal from the optical receiver. Open eyes were found at 28 Gbit/s and 40 Gbit/s over the C-band wavelength range and a set of representative results are shown in Fig. 6(b).

C. Heterogeneous III/V-on-SiN Integrated Mode-Locked Lasers

Integrated mode-locked lasers find their use in a large number of applications such as in spectroscopic sensing, distance measurements, frequency metrology and optical communication. As the noise performance and comb line spacing are linked to the cavity length, there is a large interest to extend the laser cavity. This has in recent years driven the development of heterogeneous III-V-on-Si lasers with long passive waveguide cavities. There have already been multiple demonstrations of heterogeneous III-V-on-Si mode-locked lasers. However, the pulse energy, noise performance, and stability of these mode-locked lasers are limited by the relatively high linear and nonlinear waveguide

loss, and the high temperature sensitivity of Si waveguides, which is not the case for SiN waveguides. Indeed, SiN platforms show low waveguide loss, negligible two-photon absorption at telecom wavelengths, and small thermo-optic coefficient enabling low-noise mode-locked lasers with high pulse energies and excellent temperature stability. In this section we discuss and demonstrate the on-chip integration of mode-locked lasers, using transfer-printing technology for the heterogeneous integration of the gain medium, consisting of an InP semiconductor optical amplifier with an InAlGaAs multi-quantum well active region, on a passive SiN waveguide cavity.

The SiN photonic circuits are fabricated on 200 mm Si wafers in a CMOS pilot line and include an amorphous Si waveguide layer for efficient coupling from the SiN to the III-V amplifier. An optical microscope picture of a source sample of semiconductor optical amplifiers is shown in Fig. 7(a). The semiconductor optical amplifiers used in this work differ from the ones use for cw-lasers by the inclusion of a small saturable absorber section in the center allowing the mode-locking operation. The coupons are printed on the SiN platform and post-processing is done to provide contact-pads to the device. At this step the laser is operational (see Fig. 7(b)). A view of a semiconductor optical amplifier from scanning electron microscopy is presented in Fig. 7(c). The mode-locked laser emits at wavelengths centered around 1585 nm as shown on the recorded optical spectrum in Fig. 7(d). The optical comb, converted into an electrical signal using a fast PD, is presented in Fig. 7(e). The lines are equally spaced by 3 GHz, corresponding to the repetition rate of the laser.

Fig. 8. (a) Schematic layout of the combined tunable laser cavity design, (b) Transfer printed SOA on PIC, (c) Stitched microscope image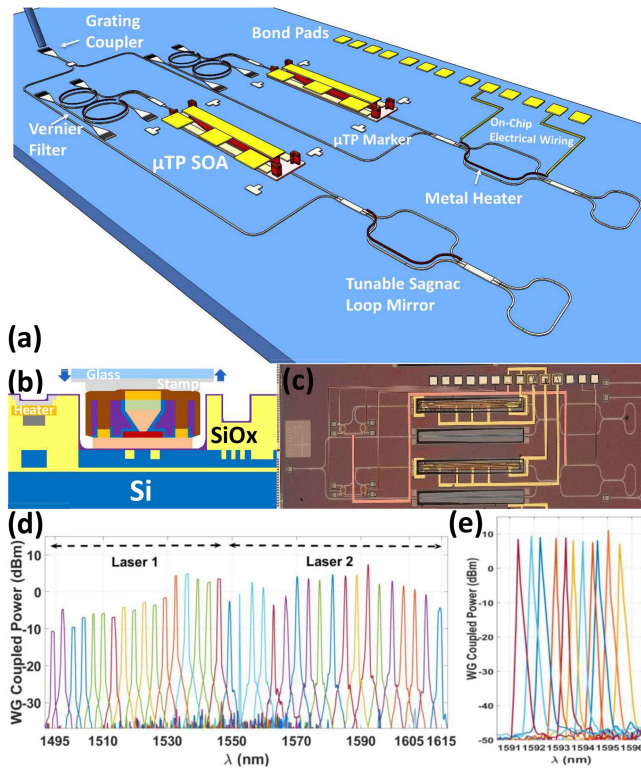 of the combined widely tunable lasers, (d) Coarse-tuning behavior of the WTL, (e) Fine-tuning behavior of the WTL. Reproduced with permission from E. Soltanian et al., Optics Express, 30(22), p.39329-39339 doi:10.1364/OE.470497. © The Optical Society.

More details about heterogeneous III/V-on-SiN mode-locked lasers can be found in the references [25], [26].

D. Tunable Laser on Si PICs With >100 nm Tuning Range

Here, we use micro-transfer-printing for the integration of pre-fabricated InP-based SOAs as the gain section in a SiPh cavity to realize widely tunable lasers (WTLs). The PICs are fabricated in imec's SiPh pilot line on 200 mm SOI wafers with a 400 nm thick Si device layer and a $2\,\mu m$ thick buried oxide layer (BOX), including a back-end stack incorporating the heaters and metal tracks. The III-V SOAs which are $40\,\mu m$ wide and 1 mm long, are fabricated by III-V Lab in a dense array with a vertical pitch of $70\,\mu m$ on the InP substrate. Prior to the μTP a combination of dry-etch (by RIE) and wet-etch (by BHF) was firstly applied to the SiPh chip to locally remove the back-end stack, to form the recess where the InP-based SOA will be integrated. The locally opened recess is slightly longer and wider than the pre-fabricated III-V SOA. Next, a thin DVS-BCB adhesive layer with a thickness of about 100 nm was spray-coated to enhance the bonding strength between the III-V SOA and the underlying Si-waveguide, enabling a high-yield printing process.

Fig. 8(a) shows the schematic view of the WTL realized by combinig two individual extended laser cavities in a single-mode waveguide connecting to a grating coupler as the output of the WTL laser. A SOA with a gain peak wavelength of about

1525 nm is printed on one of the laser cavities, while the other cavity has a SOA with a gain peak wavelength around 1575 nm. Each individual external cavity consists of a tunable Sagnac loop mirror to optimize the reflectivity of the out-coupling mirror, a deep recess to print the pre-fabricated SOA, a phase section based on thermo-optic tuning, and a pair of thermally tunable microring resonators (MRRs) with a slightly different radius ($27\,\mu m$ and $29.3\,\mu m$) to form a Vernier filter. The free spectral range (FSR) of each ring is around 4 nm and the combined FSR of the Vernier filter is around 50 nm in the envisioned wavelength range. The 1 mm long SOAs include a pair of $180\,\mu m$ long adiabatic tapers for an efficient coupling between the III-V SOA and the underlying Si-waveguide. An additional pair of adiabatic $50\,\mu m$ long Si-tapers is used to couple the optical mode between the $3\,\mu m$ wide Si-waveguide underneath the III-V SOA and the single-mode rib waveguide.

The schematic cross section of μTP of pre-fabricated III-V SOAs on imec's 400 nm SOI platform is shown in Fig. 8(b), while Fig. 8(c) shows the microscope image of the fabricated WTL with final metalization after μTP was done.

To characterize the WTL, the sample is placed on a temperature-controlled stage stabilized at $15\,^{\circ}C$. The threshold current of both the lasers is around 60 mA, while each SOA has a differential resistance of about $10\,\Omega$ biased at 140 mA. The maximum waveguide-coupled power and the wall-plug efficiency are 13 mW and 4.2%, respectively. Fig. 8(d) shows the discrete wavelength tuning by thermally tuning one of the micro-rings and phase section of each laser, which resulted in a tuning range of 120 nm. These spectra were obtained by calibrating out the insertion loss of the fibre grating coupler. The phase section is used to adjust the phase of the laser cavity to be matched with the tuned filter. By thermally tuning both the micro-rings and the phase section simultaneously the fine-tuning is achieved, as shown in Fig. 8(e).

E. InP UTC Photodetectors Integrated on SiN PICs

Next-generation datacom and telecom applications increasingly adopt Si photonic technologies to drive performance and integration to the next level. More recently, SiN platforms gain traction thanks to the availability of very low-loss waveguides and some of the best integrated filters. Several applications put very high requirements on the bandwidth of photodetectors. However, as previously stated, these are not natively available on SiN platforms. One type of high-performance photodetector is the uni-travelling-carrier (UTC) PD. Here, carrier transport is limited to high-mobility electrons, which results in a much higher transit-time bandwidth. UTC PDs also show better power handling thanks to a reduced space-charge screening effect. Integration of such PDs on SiN has been demonstrated by means of die-to-wafer bonding [27], but only achieves limited bandwidth. Using micro-transfer-printing, we demonstrated the integration of UTC PDs on a SiN PIC [28]. To this end, compact waveguide PDs are fabricated on a source III-V wafer with small mesa size of 2×12 to 2×20 μm^2. Together with the surrounding cathode contacts, this results in very compact PD coupons as small as $100\,\mu m^2$. These coupons are anchored to the
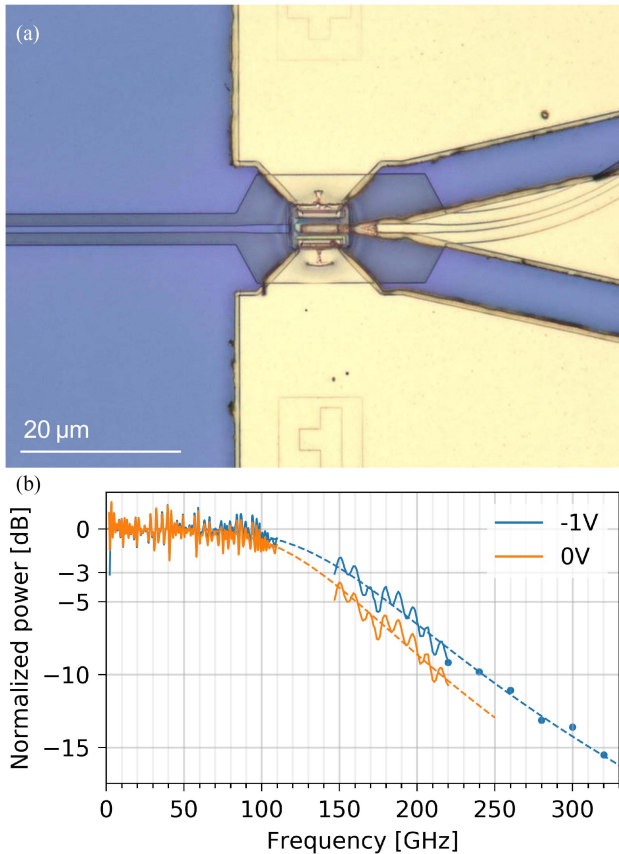
Fig. 9.   (a) Close-up of a transfer-printed UTC PD on a SiN waveguide. (b) The 3-dB bandwidth is 153 GHz at −1 V bias and 135 GHz at zero bias.

Fig. 10.   (a) Microscope image of a micro-transfer printed and post-processed LN phase modulator on the silicon nitride target PIC. (b) Image of a taper in LN micro-transfer printed on a silicon target chip. (c) Measured phase change as a function of voltage for a 1 mm long device, the fitted curve estimates a 5.8 Vcm half-wave voltage length product.

substrate using two or four SiN tethers. After transfer-printing these coupons, vias are etched in this SiN layer, to open up the contacts. A final metal layer allows electrical probing of the device. Fig. 9(a) shows a post-processed transfer-printed photodetector on a SiN waveguide. These UTC PDs show a waveguide-referred responsivity of $0.3\,\mathrm{A/W}$ at 1550 nm, a dark current below 10 nA for a bias voltage above -1 V, and saturation currents above $4\,\mathrm{mA}$ at -1 V bias. The bandwidth was verified using a set of mm-wave power meters and resulted in a 3-dB bandwidth of 155 GHz at -1 V bias voltage, and record-high 135 GHz at zero bias, as shown in Fig. 9(b).

F. LiNbO₃ on SiN

Si PICs already include a variety of modulator devices but they are still missing low loss, ultra-high speed, pure phase modulation such as the one found in Pockels effect modulators. Lithium niobate (LN) is a popular choice for these devices [30], [31] because of their wide transparency window and large Pockels coefficient. Furthermore LN has strong nonlinear coefficients that make it an interesting material for many nonlinear and quantum optics applications [32] such as frequency conversion [33] and photon-pair sources using spontaneous parametric down-conversion. We demonstrated a phase modulator using thin film LN micro-transfer-printed on top of SiN waveguides [34]. In order to perform the μTP of LN we etch the coupons from a 300 nm thin film LNOI wafer (commercially purchased from

NanoLN) using a hard mask of either Cr or a-Si and use Ar milling to pattern the coupons. In this demonstrator the coupon is 1 mm long and $60\,\mu$m wide. After the release etch using hydrofluoric acid, the coupons are picked up and printed on top of 300 nm thick SiN waveguides. This creates hybrid waveguides where the light is confined by the SiN waveguide while a large portion of the mode overlaps the LN layer. We use this hybrid structure to avoid having to pattern waveguides in the LN. These waveguides are part of a Mach-Zehnder modulator structure on-chip to convert the phase change into an amplitude change. Electrodes are finally added to complete the modulator structure seen in Fig. 10(a). The modulator is measured at 1550 nm using DC voltages. The resulting phase change can be seen in Fig. 10(c). Fitting to these results indicates a half-wave voltage-length product of 5.8 Vcm which is close to the expected 6.0 Vcm. From the 13 dB extinction ratio we estimate a 4 dB loss per coupon. From simulations we expect almost a 2 dB loss per facet of the coupon indicating the propagation losses are low. Since the demonstration of this device we have made progress towards increasing the length of the printed devices in an attempt to reduce the half-wave voltage and started incorporating taper structure to our coupons to reduce the coupling losses at the facets. An example of our printed taper structures can be seen in Fig. 10(b).
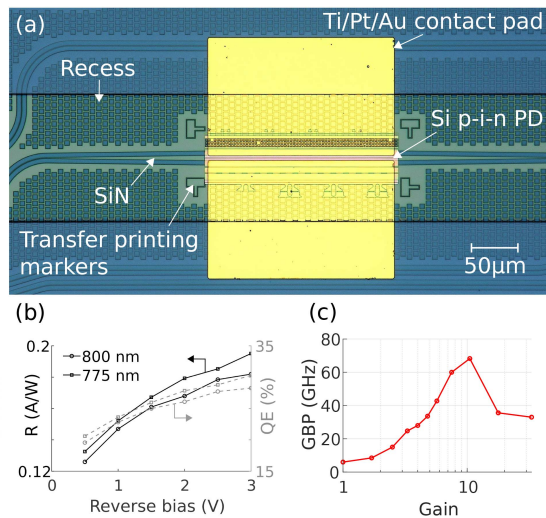
Fig. 11. (a) Micrograph of a micro-transfer printed and post-processed PD on the silicon nitride target PIC. (b) Measured PD responsivity (R) and external quantum efficiency (QE). (c) Gain-bandwidth product (GBP) as a function of the avalanche gain for an optical input power of −26 dBm. Reproduced with permission from S. Cuyvers et al., Optics Letters, 47(4), p.937-940 doi:https://doi.org/10.1364/OL.447636 (2022) . © The Optical Society.

G. Si PDs on SiN PICs

Demonstrations of photodetectors on SiN PICs have predominantly targeted telecom wavelengths. Yet, several applications require light sources and detectors at wavelengths in the (near)-visible spectral region. To this end, we recently demonstrated the first micro-transfer printed Si p-i-n PDs on SiN for wavelengths below 850 nm [35]. The PD consists of a doped Si rib waveguide and is fabricated on imec's iSiPP25 G integrated SiPh platform. Furthermore, the SiN target PIC is fabricated on imec's plasma-enhanced chemical vapor deposition (PECVD) BioPIX SiN platform. A 2 μm deep recess is locally etched in the Si oxide cladding using dry etching techniques to expose part of the SiN waveguides, enabling evanescent coupling to the micro-transfer printed Si PD above it.

Prior to μTP, the photodetectors are encapsulated and suspended on the source SOI wafer. Although a photoresist encapsulation is not strictly required - the tethers can also solely be defined in the Si device layer itself - the Si device layer is only 220 nm thick, making it mechanically fragile. A photoresist encapsulation is therefore included to safeguard the device integrity. The sacrificial SiO_2 layer underneath the Si coupons is underetched using HF vapor. In contrast to liquid HF, vapor-phase HF provides a near perfect picking yield as it does not suffer from capillary forces which can lead to a collapse of the suspended Si layer. After transfer printing, the photoresist encapsulation is removed using an oxygen plasma and Ti/Pt/Au metal contacts are added. A microscope picture of the post-processed PD on the SiN PIC is shown in Fig. 11(a). The waveguide-referred responsivity and quantum efficiency, defined with respect to the power in the SiN waveguide, are depicted in Fig. 11(b). Similar responsivities around 0.19 A/W and quantum efficiencies around 30% at −3 V bias voltage were obtained for 775 nm and 800 nm. Furthermore, a low dark

current of 107 pA was measured at a reverse bias voltage of 3 V. To quantify the photodetector bandwidth, its impulse response was captured using an oscilloscope and a 775 nm picosecond laser. By Fourier transforming the measured impulse response and dividing it by the Fourier transform of the time-domain optical picosecond pulse trace, a 3 dB bandwidth of 6 GHz at −1.5 V bias is obtained, a value that is currently dominated by the RC time delay of the PD. Furthermore, to serve applications where high receiver sensitivities are essential, avalanche gain multiplication is demonstrated. Detailed measurement results of the avalanche gain and current-voltage relations for different optical input powers are provided in [35]. Fig. 11(c) depicts the measured gain-bandwidth product (GBP) as a function of the gain, displaying a peak GBP of 68 GHz at 45 V reverse bias for an optical input power of −26 dBm. These results showcase that micro-transfer printed PDs can conveniently extend the scope of commercial SiN platforms to serve applications beyond the telecom domain such as biosensing, imaging and quantum photonics.

H. GaAs VCSELs & PIN PDs on SiN PICs

Most of the efforts of heterogeneous laser integration has been focused on edge-emitting lasers and amplifiers, due to their natural fit with planar PICs. However, standalone VCSELs have been widely used in a large variety of applications due to their excellent performance (i.e. low lasing threshold current), ranging from data-communication [38], sensing [40] and metrology [39]. Thus far, they have not enjoyed the same success on PICs due to their vertical emission profile being hard to integrate onto the planar PICs. Recently, we have demonstrated the integration of waveguide-coupled VCSELs through the use of micro-transfer-printing [36]. A grating coupler interface is used for coupling to the SiN waveguide. Due to polarization-selective feedback, the diffraction grating coupler assists in locking the polarization of the VCSEL to the preferred TE-polarization of the waveguide. Fig. 12 highlights the integration procedure and showcases the use of the waveguide-coupled VCSEL as a narrowband tunable laser for NIR sensing. The reported VCSELs have been characterized both prior and after transfer-printing, on transparent Sapphire substrates and on SiN PICs. The results measured on the transparent substrate clearly indicate that the LIV properties are maintained between GaAs substrate (top-emission) and Sapphire substrate (bottom-emission), with the exception of the earlier onset of thermal roll-over due to the higher thermal impedance of the non-native substrate. The waveguide-coupled VCSELs have similar thermal roll-over as on Sapphire substrate, with an approximate 50% output power drop from 25 °C to 85 °C. Moreover, the waveguide-coupled VCSELs still have a sub-mA lasing threshold for oxide apertures between 3 and 5 μm. The dual-side (combined) waveguide-coupled power can exceed 110 μW, with a 48 dB SMSR maintained over a 5 nm tuning range. The power conversion efficiency is measured to be 2.4% for this demonstrated device. Combining the VCSEL with waveguide-coupled PIN PDs [37] makes for a compact, integrated and low-power consuming sensing platform on Silicon Nitride PICs. The PIN PDs are bottom illuminated by a
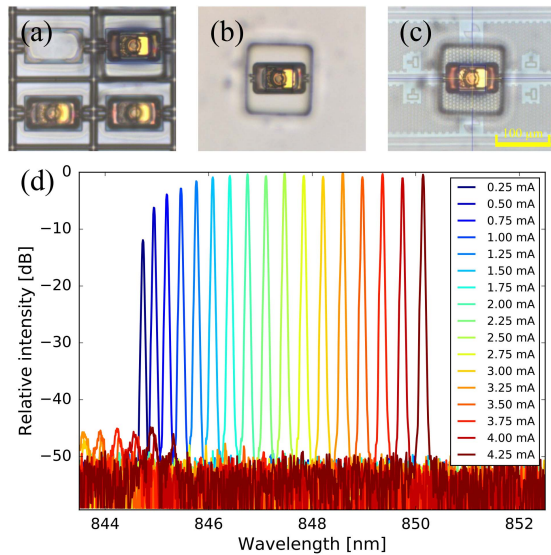
Fig. 12. Microscope images of the transfer-printed VCSEL; (a) pick-up with the stamp from the source substrate, (b) transfer to the target SiN PIC; (c) printing after aligning to the SiN grating coupler. (d) Shows the waveguide coupled spectra of a transfer-printed VCSEL as a narrowband tunable laser. Reproduced with permission from J. Goyvaerts et al. Optica, 8(12), p.1573-1580 doi:https://doi.org/10.1364/OPTICA.441636. © The Optical Society.

Fig. 13. Photoresist device coupon and GaAs nanobeam printed on top of SiN circuitry.

diffraction grating coupler, and have a thick absorption layer to maximize absorption after vertical diffraction. The detectors have responsivities of up to 0.3 A/W, corresponding to approximately 45% external quantum efficiency at 850 nm wavelength. The PDs were also integrated on top of the output channels of an arrayed waveguide grating spectrometer and showed no deterioration of the cross-talk between the different device channels.

I. Towards Heterogeneously Integrated Single-Photon Sources

Nowadays, highly efficient single-photon sources have matured up to the point where simultaneous high single-photon purity and indistinguishability can be reliably achieved in GaAs nanobeam waveguides [41]. Still, its monolithic platform suffers from propagation losses in the order of 10 dB/mm due to scattering in waveguides. Heterogeneous integration on low-loss SiPh-based platforms waveguides could overcome this bottleneck towards scalable quantum hardware. Based on a homemade transfer-printing apparatus that allows for incredibly accurate alignment ($\pm$50 nm), μTP of competing highly efficient semiconductor quantum dot single-photon sources has already been successful [44]. However, this approach renders incompatible with commercial μTP installations that have to cope with larger misalignment tolerances to allow high throughput integration. In [45], we report on the integration of a nanobeam quantum dot emitter on a SiN waveguide using a conventional μTP process that is able to maintain high coupling efficiency with increased lateral displacement. Here, the emitter section consists of a straight section of 300 nm width and 160 nm thickness. This work involves printing standalone GaAs nanobeam waveguides, tapered from both sides, on top of a SiN interposer. Printing structures of such reduced dimensions poses new challenges
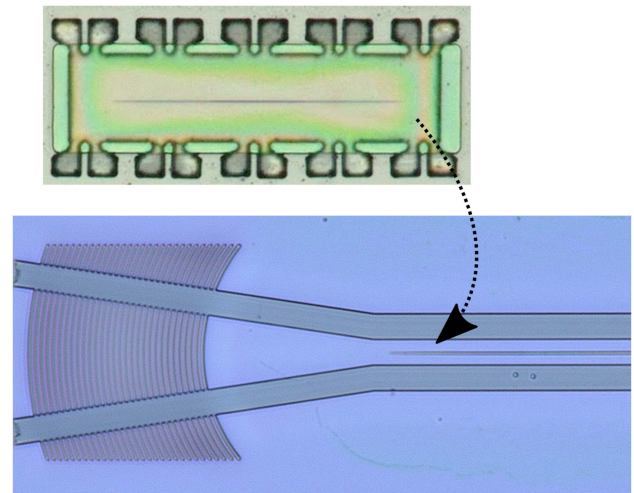
that are less significant for III-V lasers or PDs [42] discussed in previous sections. Still, the developed printing process remains largely inspired by these more rigid devices, while it also relates to previous efforts for printing confined material structures such as graphene films [43]. Some adaptations were required to manage the internal stresses in the coupon.

The GaAs membrane containing a layer of self-assembled InAs quantum dots is patterned as typically on its native substrate with electron beam lithography and RIE etching. Similar to the original monolithic approaches based on suspended devices [41], wafers contain an adequate sacrificial layer of AlGaAs. First, this release layer is dry etched to locally expose the GaAs substrate and tethers are defined in a photoresist encapsulation layer. This encapsulation layer further shields the structure and fully accounts for the stress impinging on the GaAs nanobeam during the process. This can be mitigated with a photoresist coupon design of sufficient size and symmetric tether spacing, distributing stresses evenly over the suspended coupon. After underetching in HCl, devices are micro-transfer printed on top of 300 nm LPCVD SiN waveguides. These were patterned using electron beam lithography and RIE etching. A 50 nm thick DVS-BCB layer is used for bonding and is cured after printing and resist removal.

To cope with a lateral alignment accuracy of 750 nm (3σ) between GaAs nanobeam and SiN waveguide, a piecewise linear taper design is used. This has been optimized for efficient mode coupling tolerant to misalignment while also taking into account a significant tradeoff with propagation losses over its length. Fig. 13 shows a SiN waveguide with an integrated GaAs nanobeam on top. Transmission measurements that entail in- and outcoupling as well as propagation losses of the 120 μm long waveguide device were demonstrated with 3 dB of overall excess losses.

Further steps can be envisioned based on advances in the monolithic GaAs platform. The use of a reverse biased vertical p-i-n junction that embeds the InAs quantum dots can reduce charge noise responsible for dephasing effects. Similar

to the previous section, this μTP approach should also allow for GaAs-on-SiN fabrication compatible with commercial foundry photonic platforms, ultimately paving the way for larger-scale quantum information processing.

IV. CONCLUSION AND OUTLOOK

The device demonstrations described above are promising proof-of-concepts that highlight the potential of μTP technology for heterogeneous PICs. As the technology is very versatile, other demonstrations, dealing with the μTP of InAs/GaAs quantum dot lasers, Ce:YIG magneto-optic materials for optical isolators, periodically poled LiNbO$_3$ for nonlinear optics, BiCMOS electronics etc. are underway. However, there is still a way to go for this technology to be used as a manufacturing technology. Scaling up the technology to 200 mm and 300 mm wafers is underway. Continuous improvements on device performance (e.g. laser wall plug efficiency) and studying and improving yield and reliability need to be carried out. If these hurdles can be overcome, we believe μTP technology has a bright future for next generation photonic/electronic integrated circuits.

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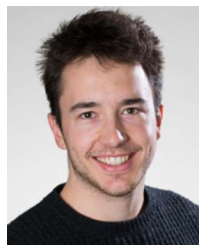
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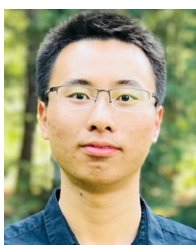
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**Guy Lepage** photograph and biography is not available at the time of publication.

Peter Verheyen photograph and biography is not available at the time of publication.

Joris Van Campenhout (Member, IEEE) photograph and biography is not available at the time of publication.

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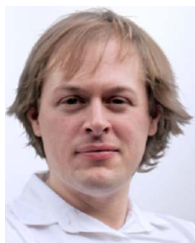
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