Scalable Nano-Opto-Electromechanical Systems in Silicon Photonics

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***Abstract*— Recent advances in integration of Nano-Opto-Electromechanical Systems in Silicon Photonics enable fundamental photonic operations such as switching, phase shifting or power equalization on-chip. The unique combination of high optical efficiency, low electric power consumption and compact footprint, provides outstanding opportunities in scalability to large-scale photonic integrated circuits.**

Keywords—Photonic MEMS, NOEMS, Silicon Photonics, Photonic Integrated Circuits.

I. Introduction

Silicon Photonics has over the past years rapidly evolved into a mature technology for photonic integrated circuits (PICs). Active research and development is pursued to further enhance current PIC technology, and the advances in technology have fueled a steadily increasing number of integrated photonic components on an individual PIC, giving rise to large and complex circuits with tens of thousands of individual building blocks [1]. While the availability of such high density photonic integration allows to tackle entirely new concepts such as programmable photonics [2], the increase in complexity poses at the same time tight constraints on the requirements for power consumption, footprint and optical performance of the individual building blocks. Recent analysis has shown, that among the physical effects available to interact with the photonic signals on-chip for device tuning, optical switching, or even modulation, are mechanically movable waveguides [3]. Such Nano-Opto-Electromechanical Systems (NOEMS) make use of established Micro-Electro-Mechanical Systems (MEMS) technology, giving birth to the emerging technology basis of Silicon Photonic MEMS.

II. Integration of MEMS Technology in Silicon Photonic Platforms

To fully unfold the power and potential of Silicon Photonic MEMS technology, the individual functional NOEMS components must be integrated in standard silicon photonics platforms, alongside the highly optimized standard platform photonic components such as high-speed photodetectors, modulators, grating couplers, etc.

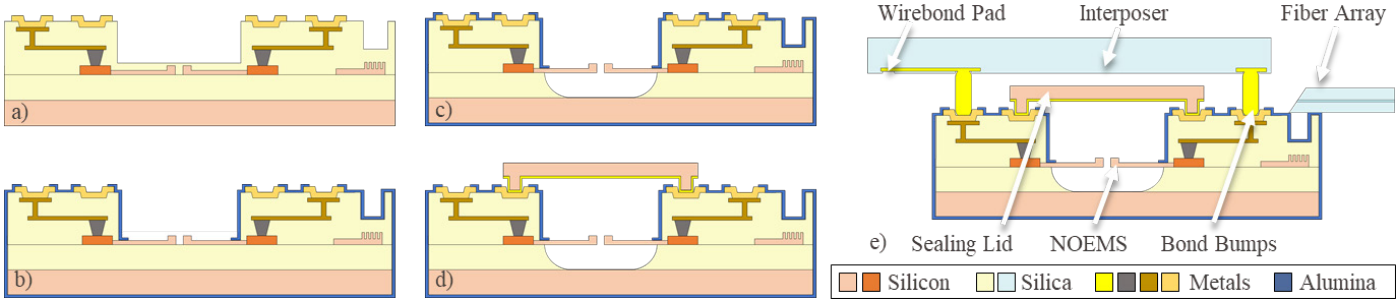

Fig. 1. Schematic respresentation of the microfabrication and assembly sequence to scale Nano-Opto-Electromechanical Systems to large-scale Photonic Integrated Circuits. The a) standard platform silicon photonic circuit is b) passivated with a protective masking layer, protecting the chip during c) sacrifical layer etching. d) Sealing of the freestanding devices provides long term reliability, and is compatibe with e) flip-chip bonding to an electrical interposer, that allows to redistribute thousands of electrical signals to externally located wirebond bads, while providing at the same time access for large port-count fiber arrays for optical I/O.

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Consequently, our work is building on the standard iSiPP50G platform developed by IMEC, Belgium, which is recognized as one of the most advanced Silicon Photonics platforms today [4]. We have developed a technology platform to selectively remove areas of the cladding material surrounding the silicon waveguides in the standard platform, by a custom process sequence including Alumina atomic layer deposition and structuring, serving as hard mask during a subsequent HF Vapor sacrificial layer etch, that releases the NOEMS structures selectively. Particular care has been taken to ensure wafer level compatibility with the full platform in terms of thermal budget and materials [5], as summarized in Figs. 1a-c. In order to ensure long term reliability of the NOEMS devices, they are individually encapsulated using a wafer-level sealing process [6] (Fig. 1d). With a thickness of the sealing cap in the range of only 25 µm, they are fully compatible with flip-chip bonding to custom interposers, as illustrated in Figure 1e.

III. Scaling Photonic MEMS and Interfaces: From Devices to Large-Scale Circuits

Primary requirements on Silicon Photonic MEMS technology for scaling are low optical losses, compact footprint, broadband operation and low power consumption. In our technology platform, we have demonstrated several individual components, such as the exemplary NOEMS power coupler shown in Fig. 2a, as well as phase shifters, switches, etc. These components are broadband, exhibit low loss and compact footprint, and require low power for actuation, underlining the suitability for scaling to large circuits. The inherent capability to compensate for fabrication tolerances provides the possibility to mitigate component variability and the seamless integration into the platform design framework provides convenient access for circuit designers to scale from devices to circuits [7]. To interface large-scale photonic integrated circuits, thousands of electronic driving signal must be individually controlled. While in principle it is possible to integrate electronics in the same silicon as the photonic devices, the technology mismatch of photonics and electronics makes this approach costly. Alternatively, application specific electronic integrated circuits can be flip-chip bonded to PICs, yet this approach typically requires long turn-around times and can prove costly, in particular during development. We have thus implemented electronic-photonic interfacing by flip-chip bonding to custom glass interposers (Fig. 1e) that can conveniently redistribute the individual electrical contacts to peripherally arranged pads for wirebonding to electronic printed circuit boards, while at the same time allowing access to fiber grating couplers that can be permanently coupled to dense fiber arrays for high port count optical I/O. A fully sealed device with accessible electrical and optical I/O is shown in Fig. 2b, and the fully integrated Silicon Photonic MEMS technology stack including sealing caps and flip-chip bonding to glass interposers is shown in the photograph of Fig. 2d.

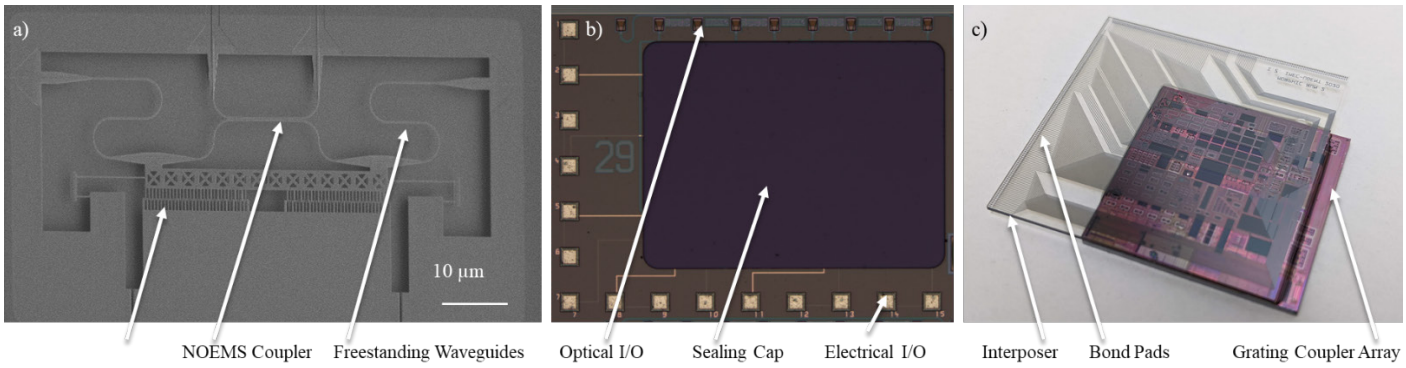

Fig. 2. Large-Scale Silicon Photonic MEMS technology platform, consisting of a) individual NOEMS such as electrostatic comb drive actuated power couplers, b) sealing caps, and c) flip-chip assembled inter-poser, provding re-distribution of electrial I/O for wirebonding to driving circuitry while providing at the same time access for large port-count fiber arrays for optical I/O.

IV. Conclusions

Our recent advances in integration of Nano-Opto-Electromechanical Systems in standard Silicon Photonics demonstrate low optical loss, low electrical power consumption, and small footprint. Combined with hermetic sealing and flip-chip bonding to electrical interposers, we thus experimentally demonstrate the potential for scaling to large-scale Silicon Photonic MEMS circuits.

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References

[1] T. J. Seok, K. Kwon, J. Henriksson, J. Luo, and M. C. Wu, "Wafer-scale silicon photonic switches beyond die size limit," Optica, vol. 6, no. 4, p. 490, Apr. 2019.

[2] W. Bogaerts et al., "Programmable photonic circuits," Nature, vol. 586, no. 7828, pp. 207–216, Oct. 2020.

[3] C. Errando-Herranz et al.,"MEMS for Photonic Integrated Circuits," IEEE J. Sel. Top. Quantum Electron., pp. 1–1, 2019.

[4] M. Pantouvaki et al., "Active Components for 50 Gb/s NRZ-OOK Optical Interconnects in a Silicon Photonics Platform," J. Light. Technol., vol. 35, no. 4, pp. 631–638.

[5] N. Quack et al., "MEMS-Enabled Silicon Photonic Integrated Devices and Circuits," IEEE J. Quantum Electron., vol. 56, no. 1, pp. 1–10, Feb. 2020.

[6] G. Jo et al., "Wafer-level vacuum sealing for packaging of silicon photonic MEMS," in Silicon Photonics XVI, Online Only, United States, Mar. 2021, p. 11.

[7] W. Bogaerts et al., "MORPHIC: Programmable photonic circuits enabled by silicon photonic MEMS," in Silicon Photonics XV, San Francisco, United States, Feb. 2020.