

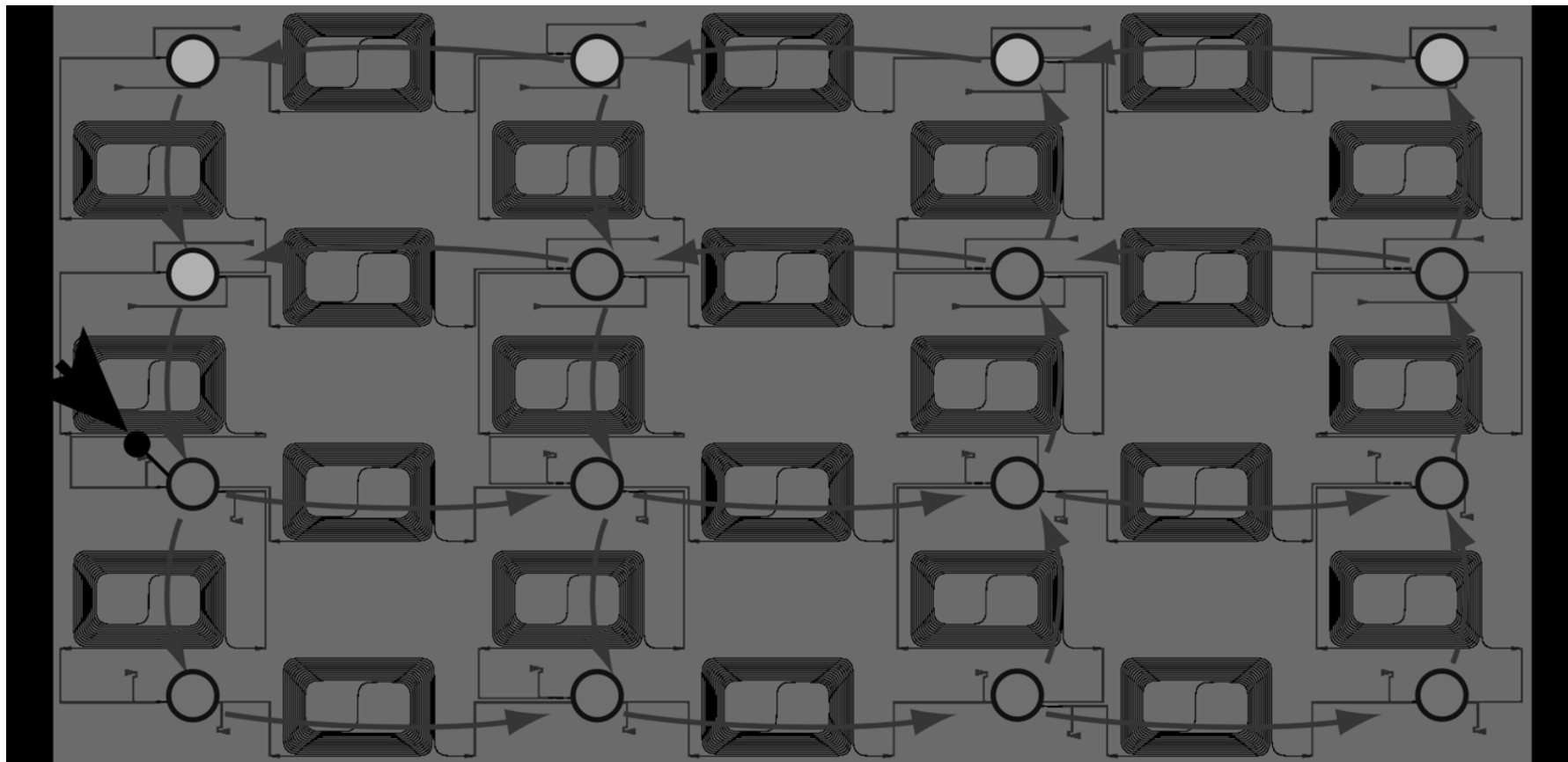


Photonic reservoir computing using silicon chips

Kristof Vandoorne, Pauline Mechet, Martin Fiers, Thomas Van Vaerenbergh, Bendix Schneider, Andrew Katumba, Floris Laporte, David Verstraeten, Benjamin Schrauwen, Joni Dambre and Peter Bienstman

THE BLACK BOX

What can this chip do?



Several things!

- Do arbitrary boolean calculations with memory on a bitstream
- Recognise arbitrary 5-bit headers at 12.5 Gbps
- Perform speech recognition of isolated digits
- Does not consume any active power
- Easily upscalable to higher speeds

How does it do it?

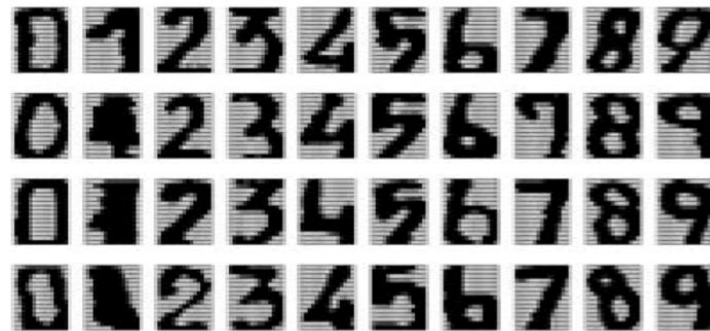
Using “Reservoir computing”, a brain-inspired technique to solve pattern recognition problems in a fast and power-efficient way



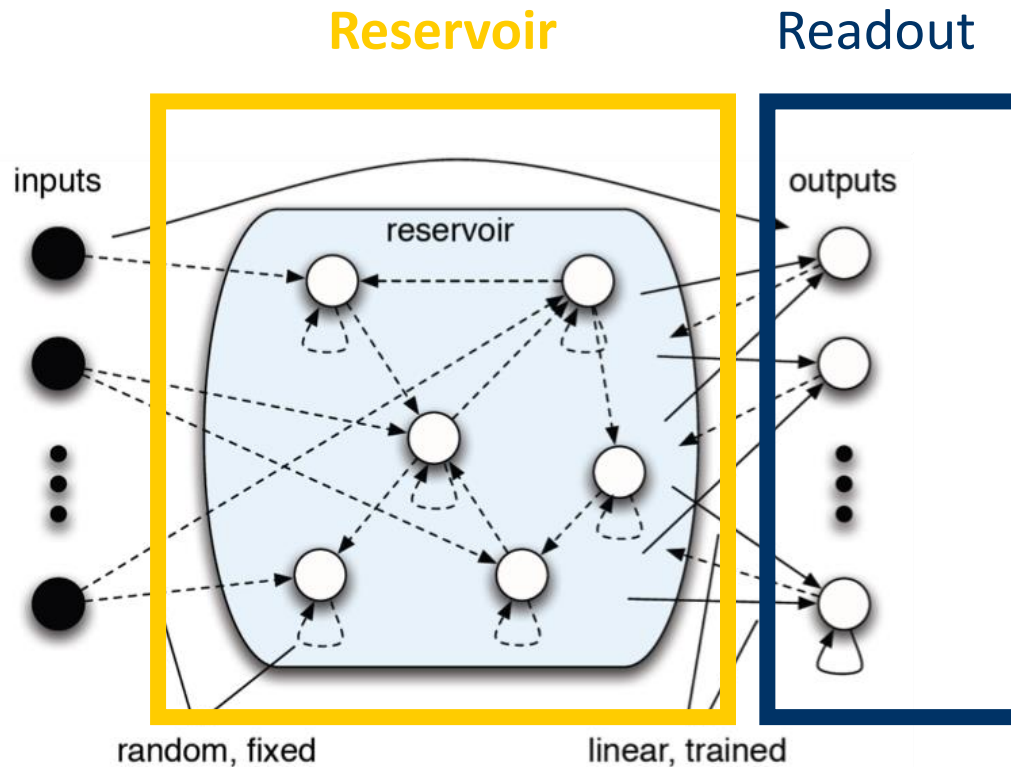
WHAT IS RESERVOIR COMPUTING?

What is reservoir computing?

- From field of machine learning (2002)
- Related to neural networks
- So far mainly in software
- Very successful:
 - Better than state-of-the-art digit recognition
 - Speech recognition
 - Robot control
 - ...

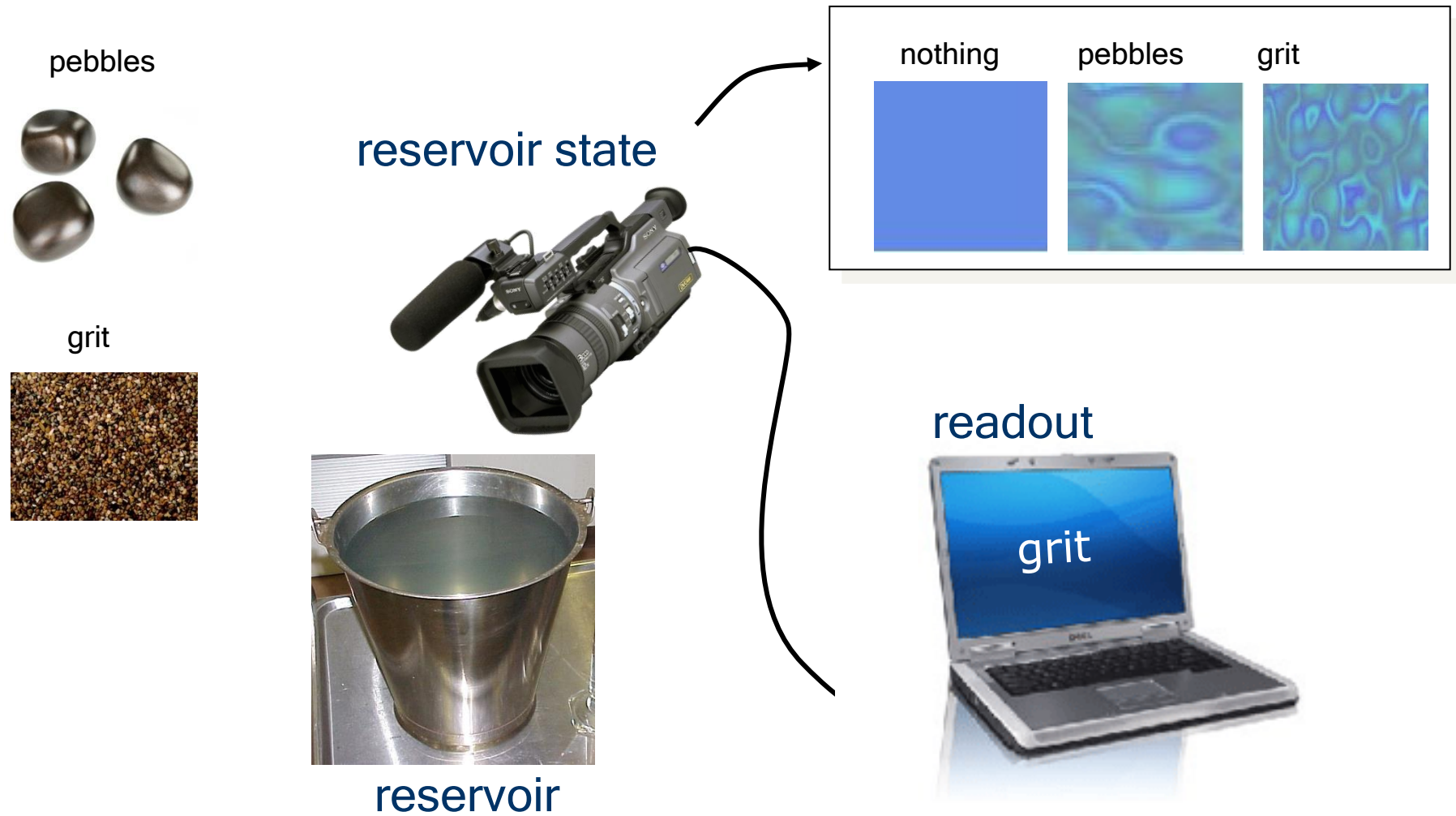


Reservoir computing

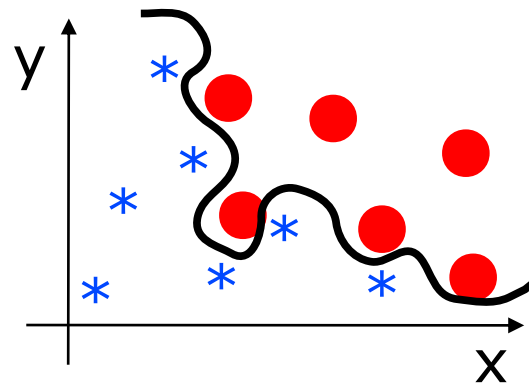


Don't train the neural network,
only train the linear readout

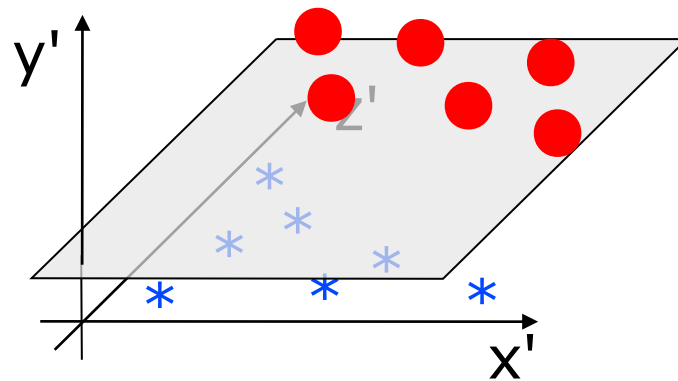
A hardware implementation...



Why does it work?



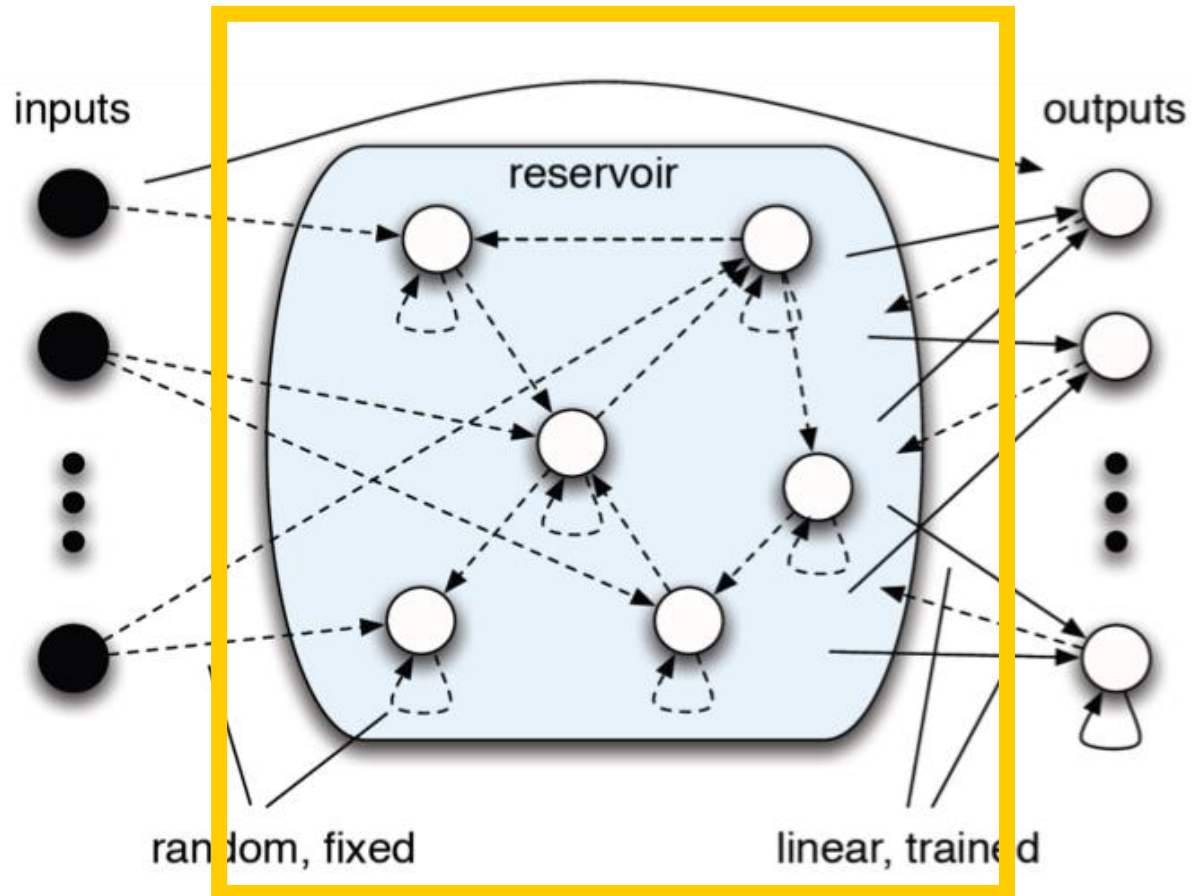
To higher
order space



PHOTONIC RESERVOIR COMPUTING

Photonic reservoirs

Photonics



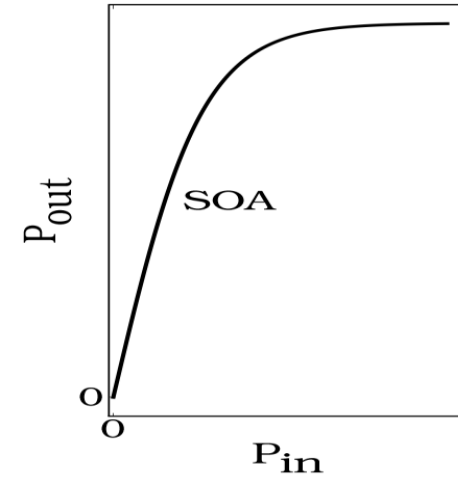
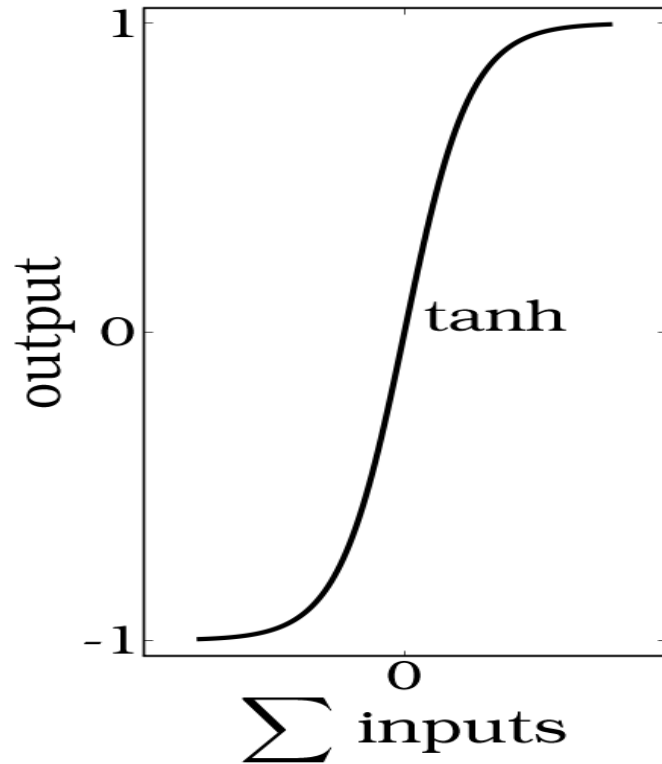
Why photonics?

- Faster
- More power efficient
- Richer dynamics in nodes
- Light has a phase

The very beginning...

OPTICAL AMPLIFIER NETWORKS

Use SOAs as neurons



Looks like tanh, but positive signals only

SOA model

The gain in the SOA model is dependent on the **input power** and its **own history**

$$P_{out}(\tau) = P_{in} \exp[h(\tau)]$$

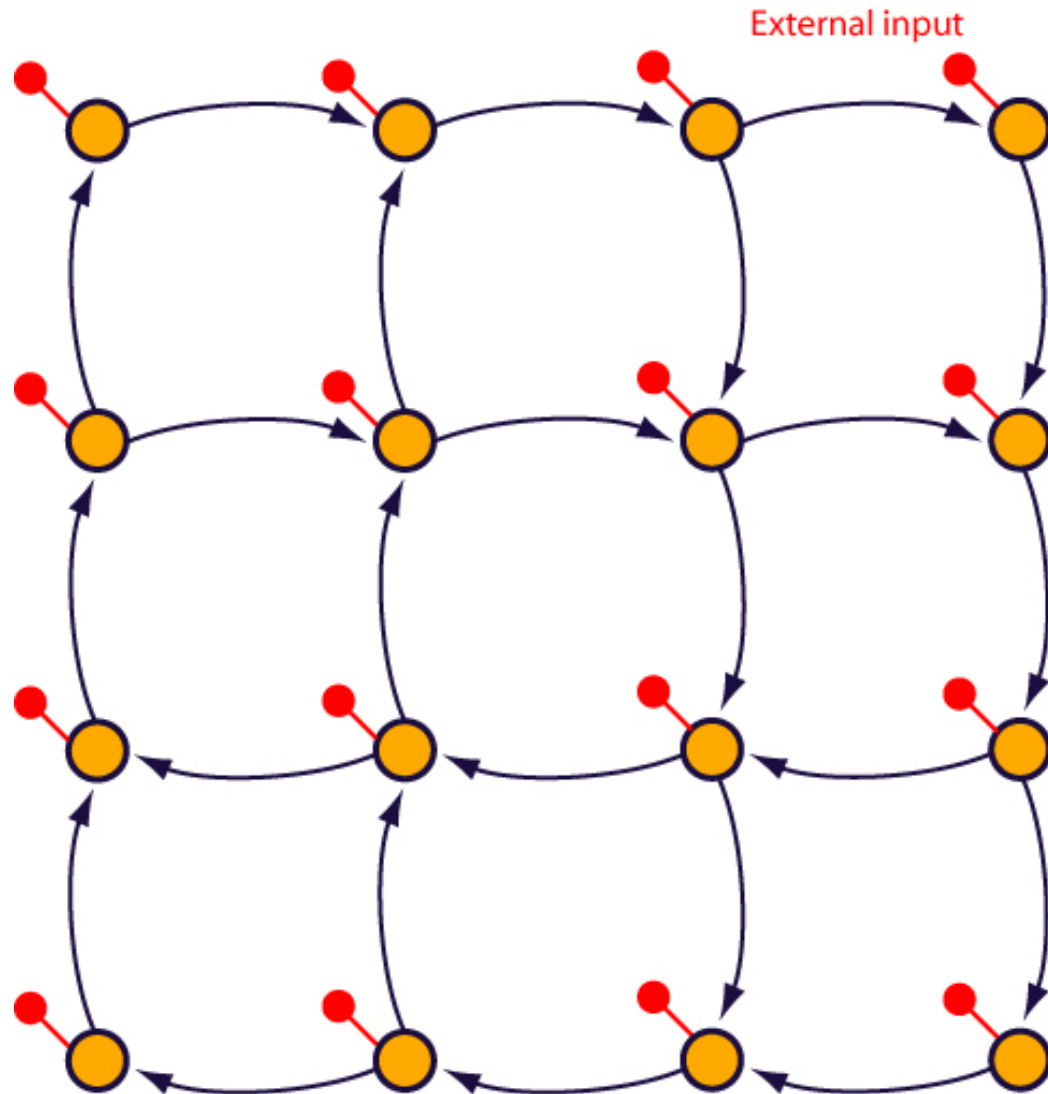
$$\phi_{out}(\tau) = \phi_{in} - \frac{1}{2} \alpha h(\tau)$$

$$h(\tau) = \int_0^L g(z, \tau) dz$$

$$\frac{dh}{d\tau} = \frac{g_0 L - h}{\tau_c} - \frac{P_{in}(\tau)}{P_{sat} \tau_c} [\exp(h) - 1]$$

Swirl topology

81 SOAs



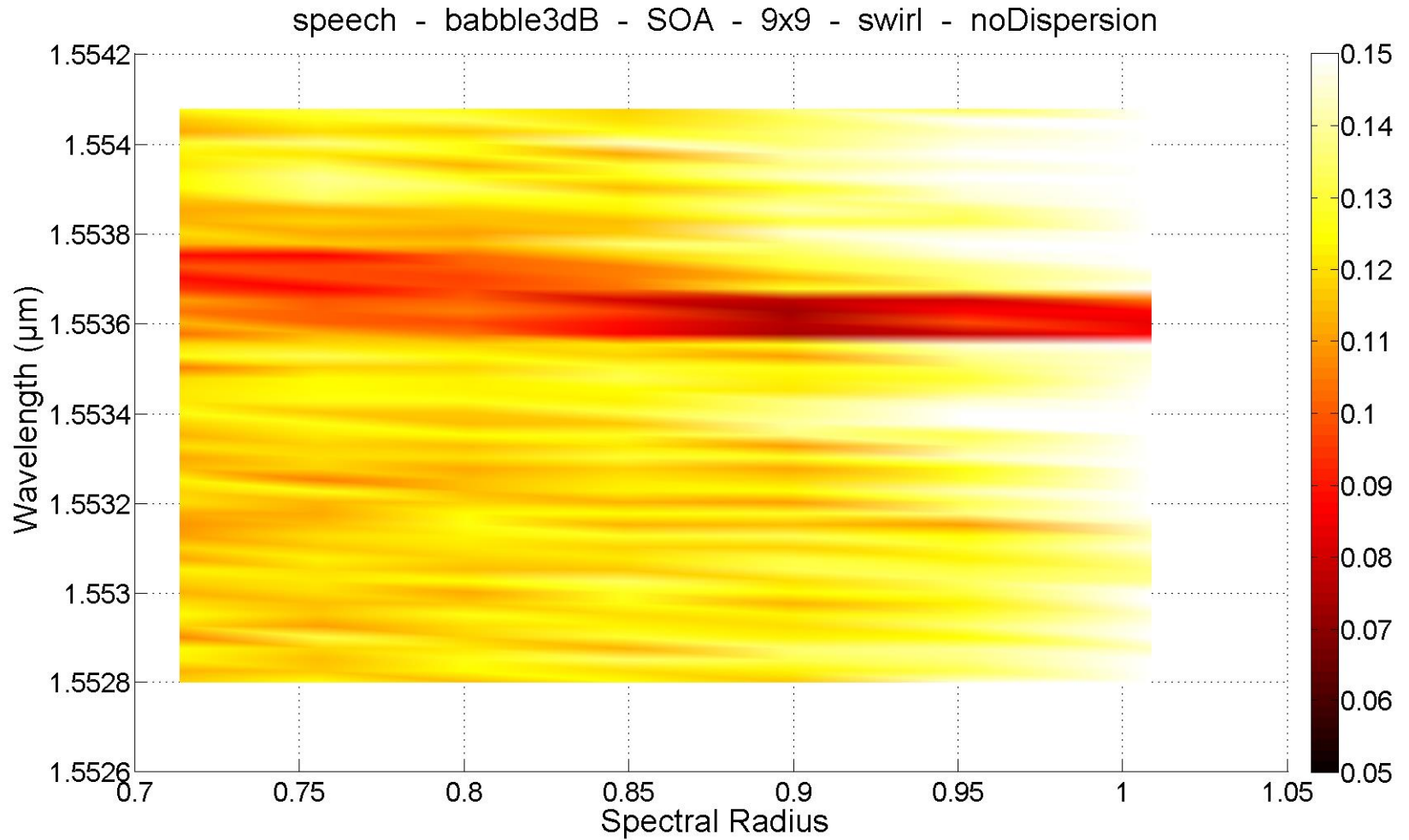
Speech corpus

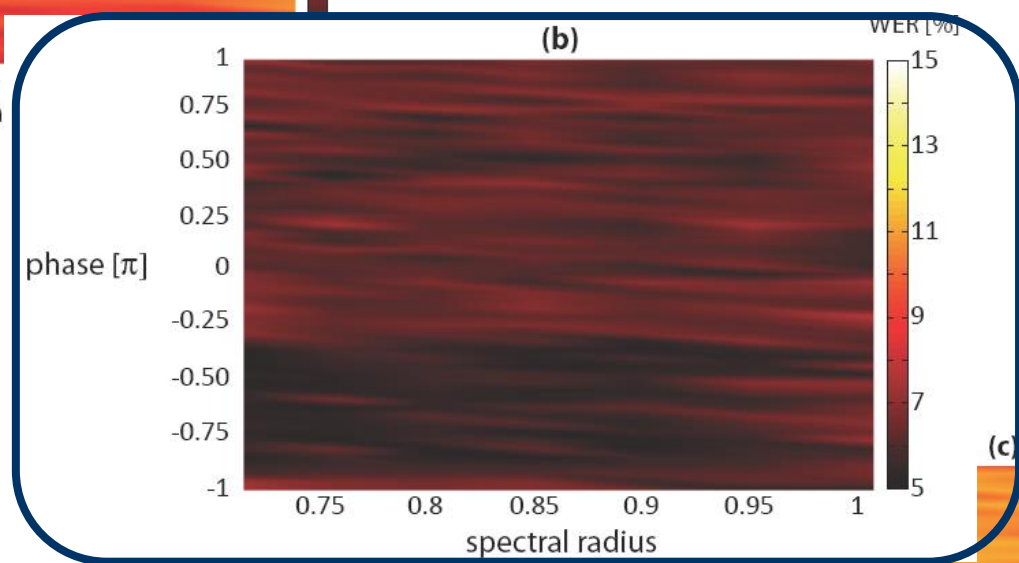
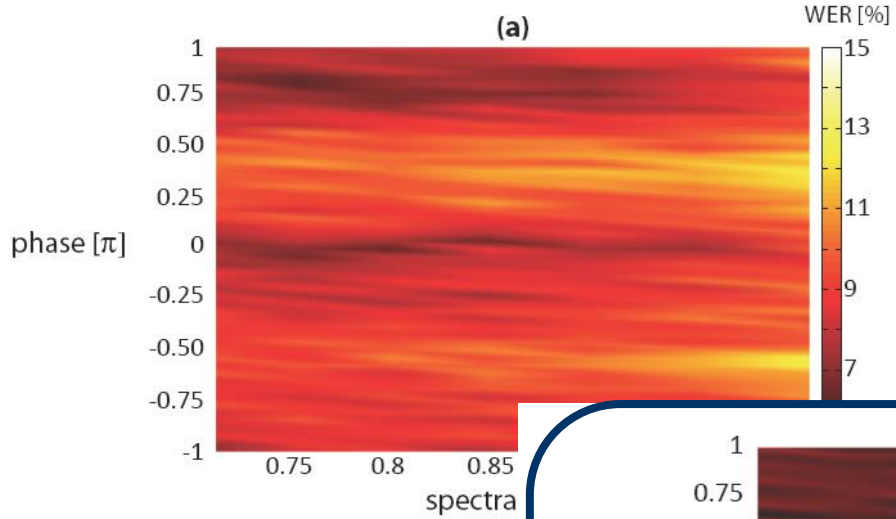
5 female speakers, saying
10 times the same 10 digits,
ranging from zero to nine

Time scales

- dynamics of light signal should be on time scale of SOA dynamics and chip delays
- convert 1 sec speech to 1 ns light signal
- 9 orders of magnitude upconversion

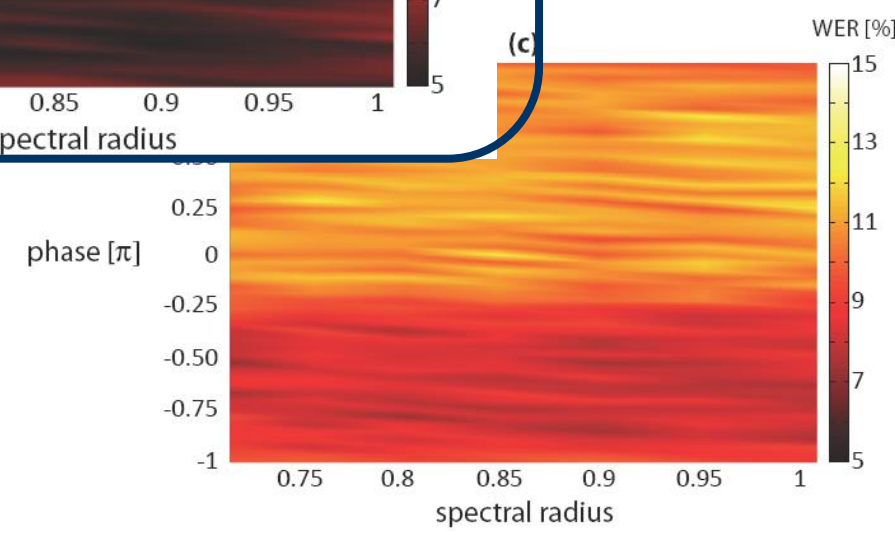
Word error rate





187.5 ps

312.5 ps

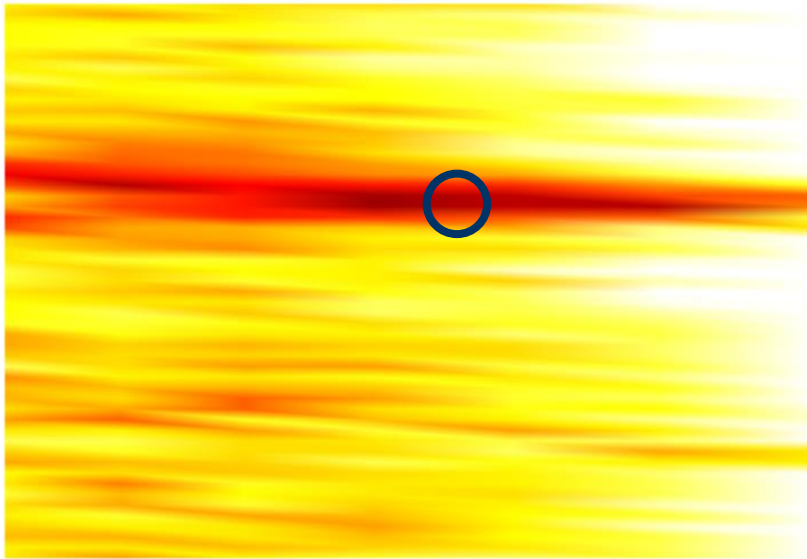


Optimal delay

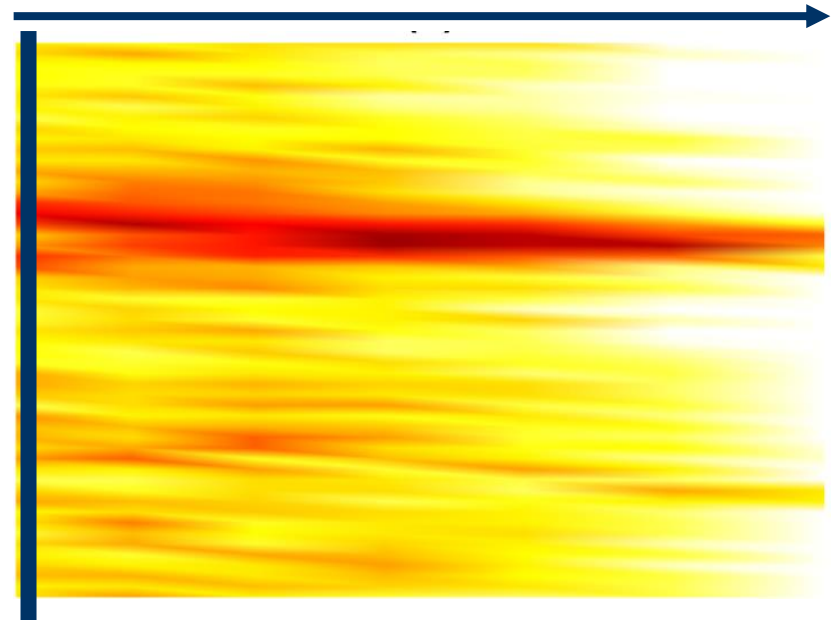


Reducing 2D plots to single number

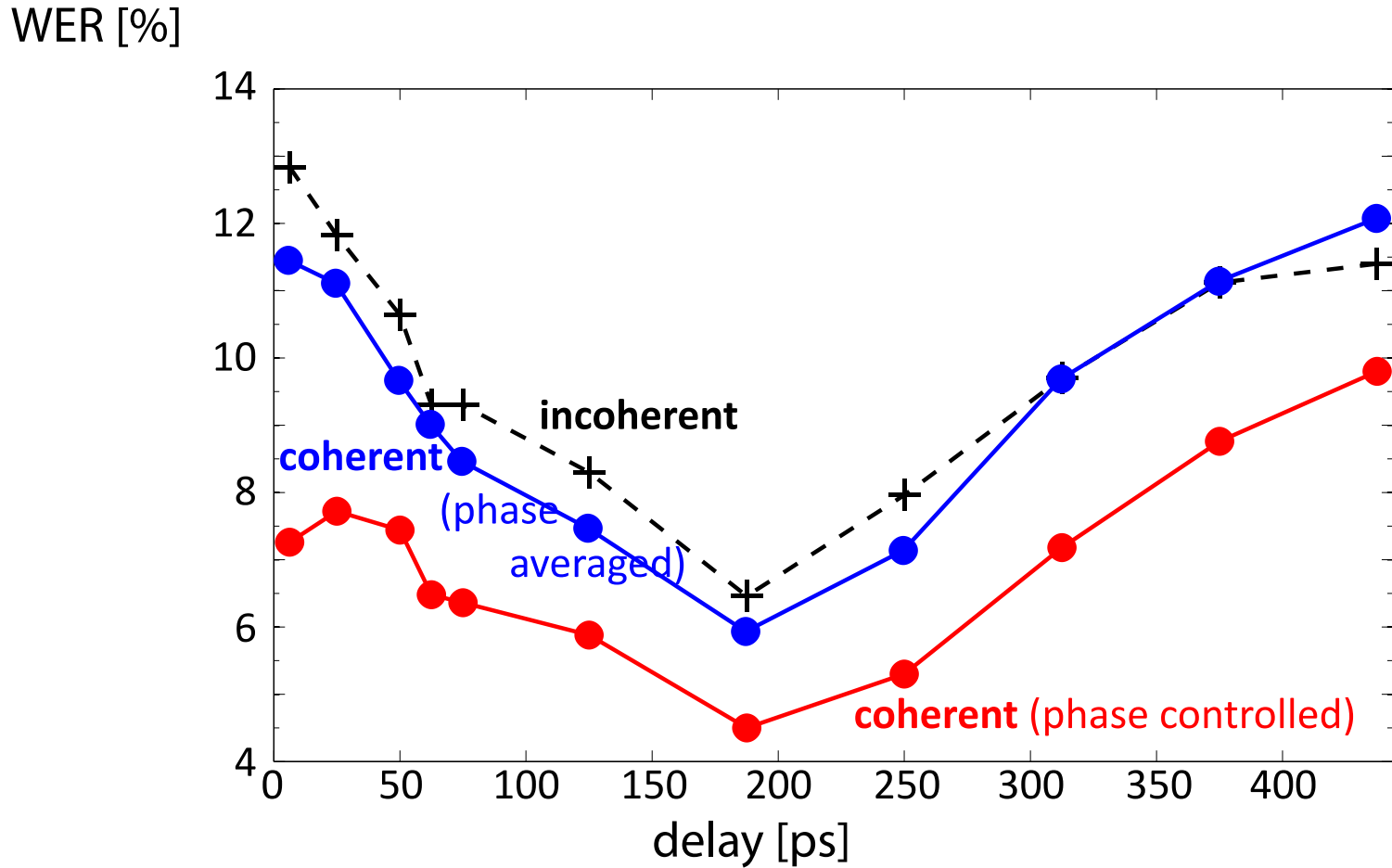
Absolute minimum
(phase controlled)



Minimum
(phase averaged)



Controlling the phase offers clear advantage



The next step...

PASSIVE SILICON RESERVOIRS

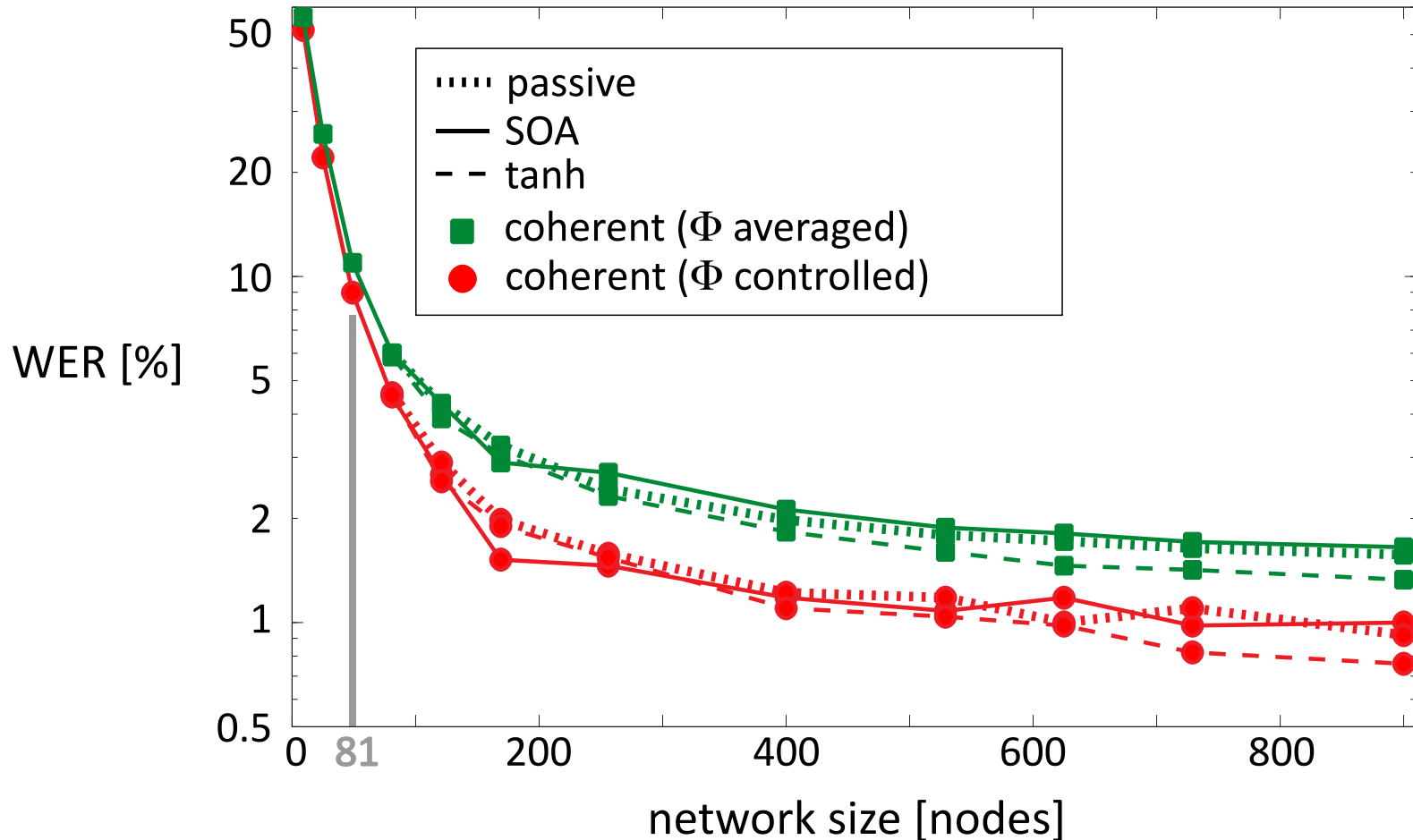
What happens if you remove the SOAs?

Passive Silicon reservoir

- silicon photonics: mature technology
- nodes become simple splitters/combiners
- non-linearity in readout suffices
- no need for amplifiers which consume power
- no longer limited by timescale of non-linearity

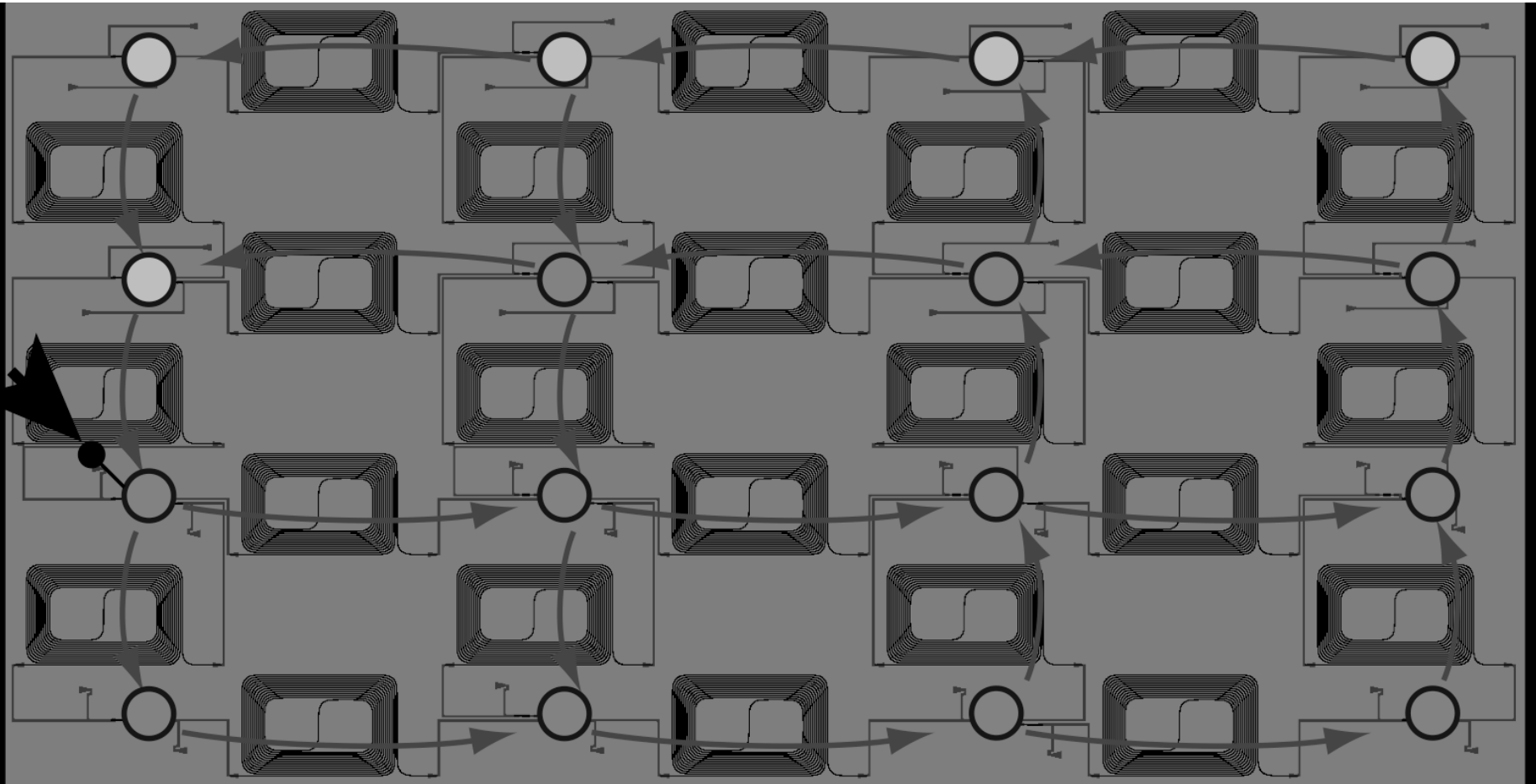
Vandoorne et al, Nature Comms, 5, 3541, 2014

Speech task: passive reservoirs (no amplifiers)

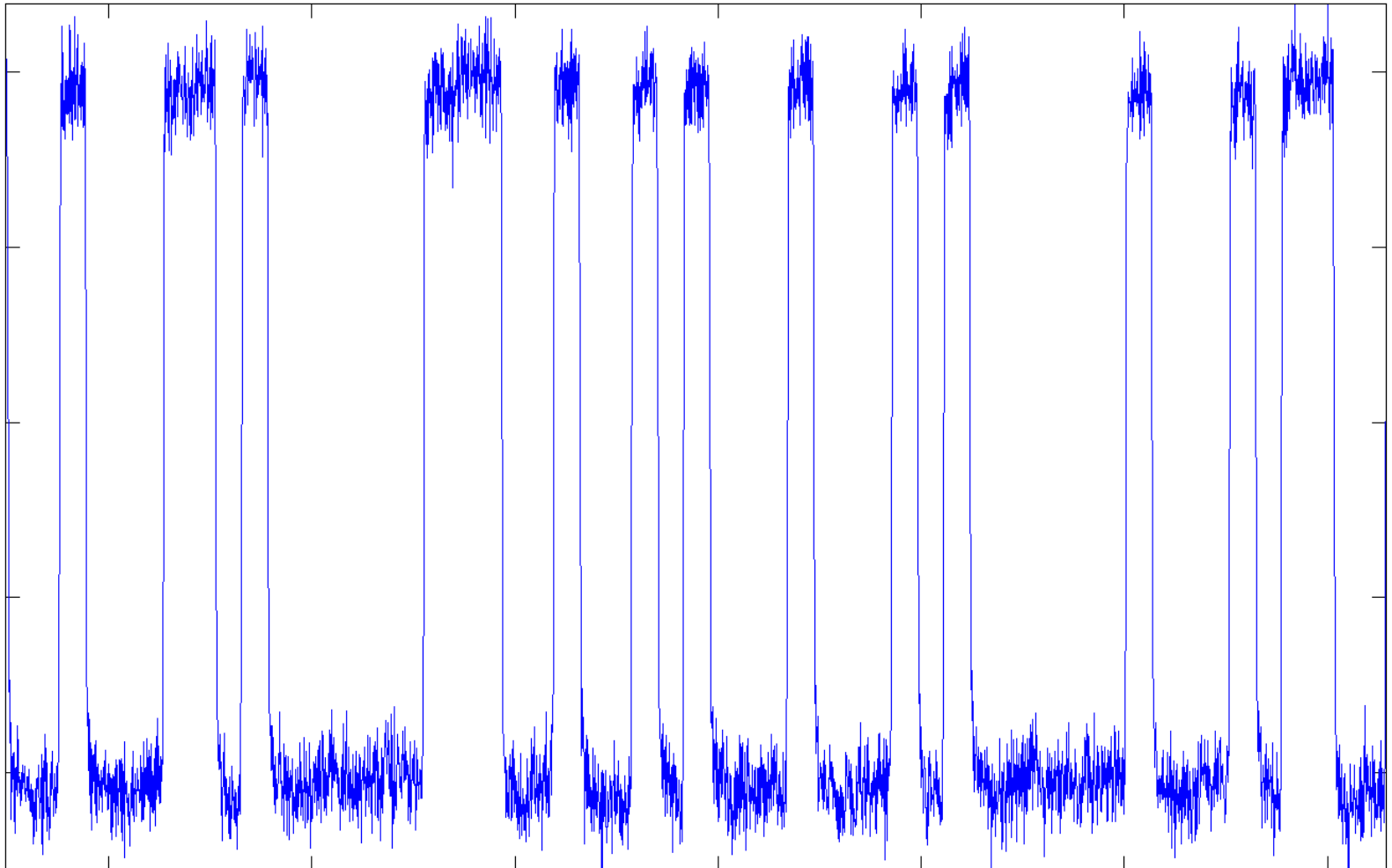


NL coming from the detector suffices!

16 node swirl network where 11 nodes could be measured from 1 input



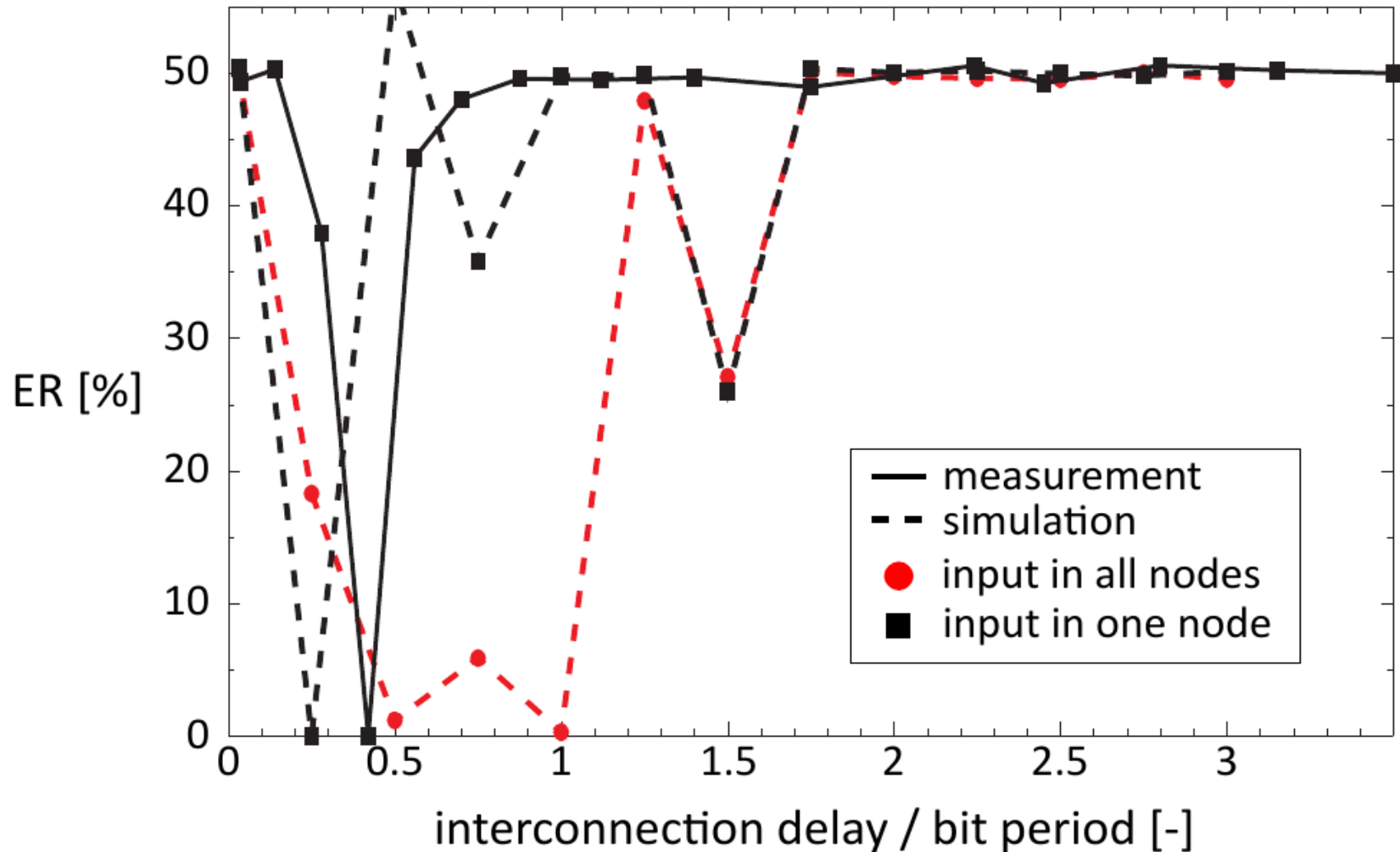
The input: 11136 bits modulated at 1531 nm with speeds between 125Mbit/s and 12.5Gbit/s



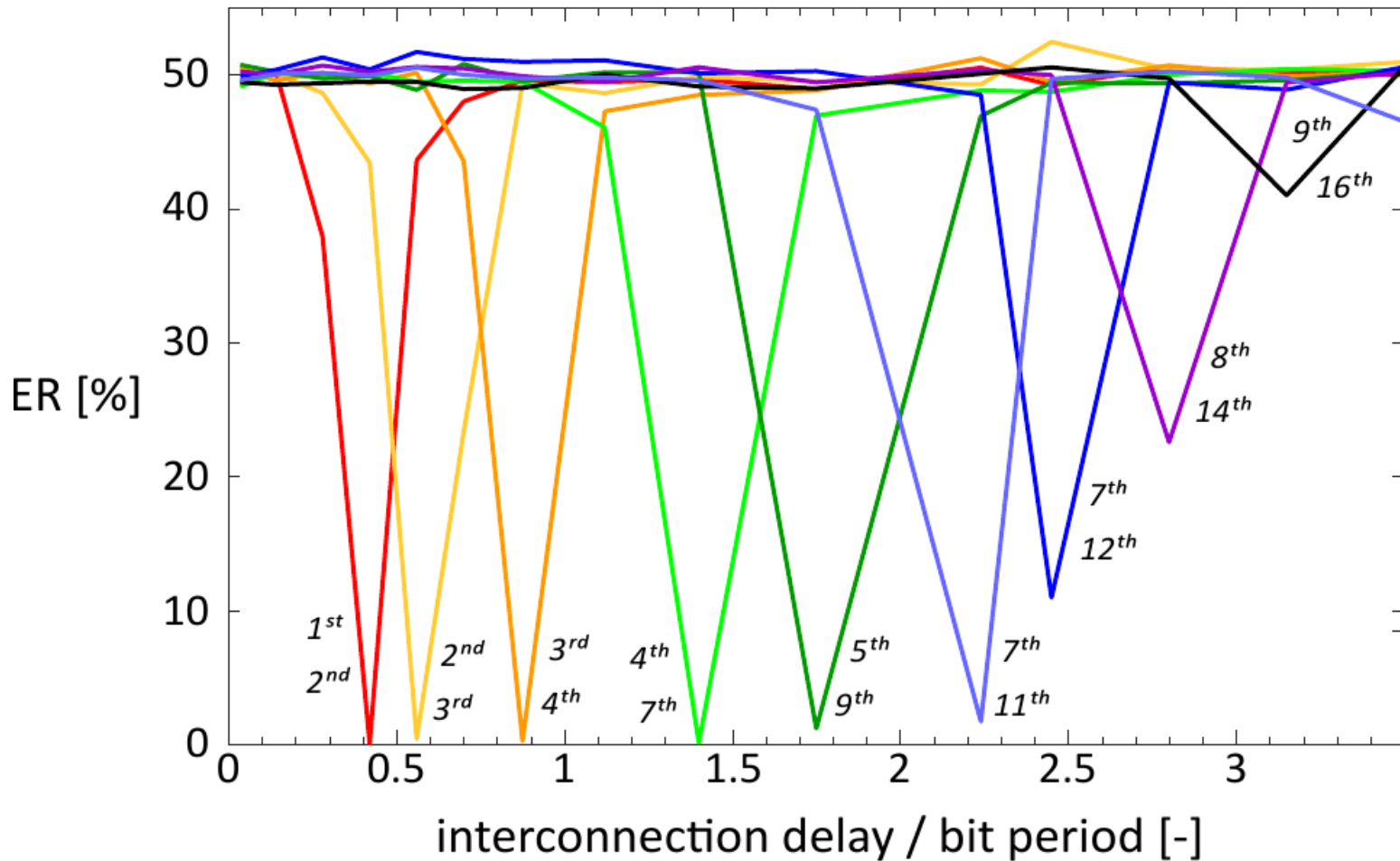
First task: desired output should be the XOR of every bit with the previous bit.

Hard task in machine learning (non-linear!)

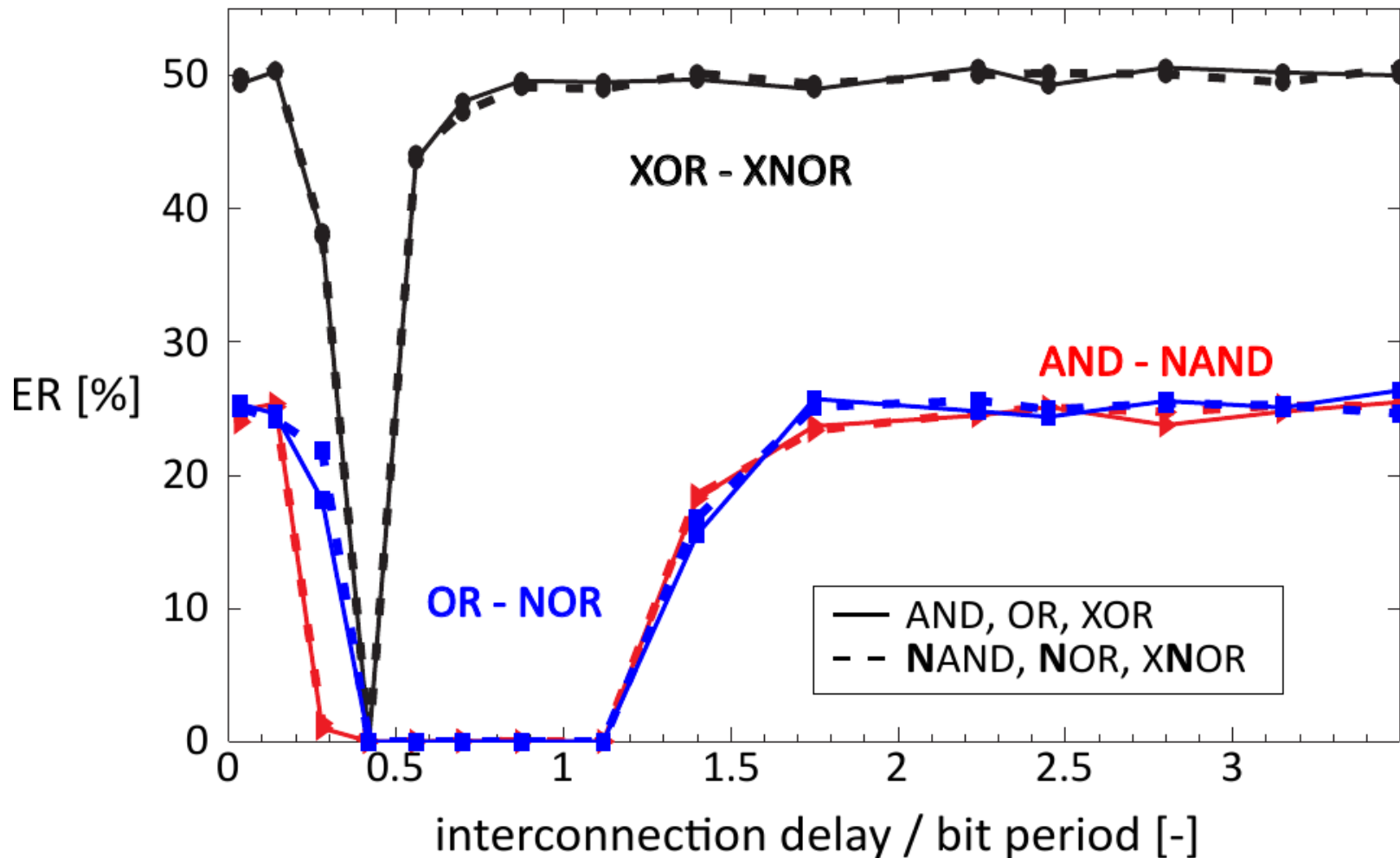
Measurements and simulations for the XOR task correspond



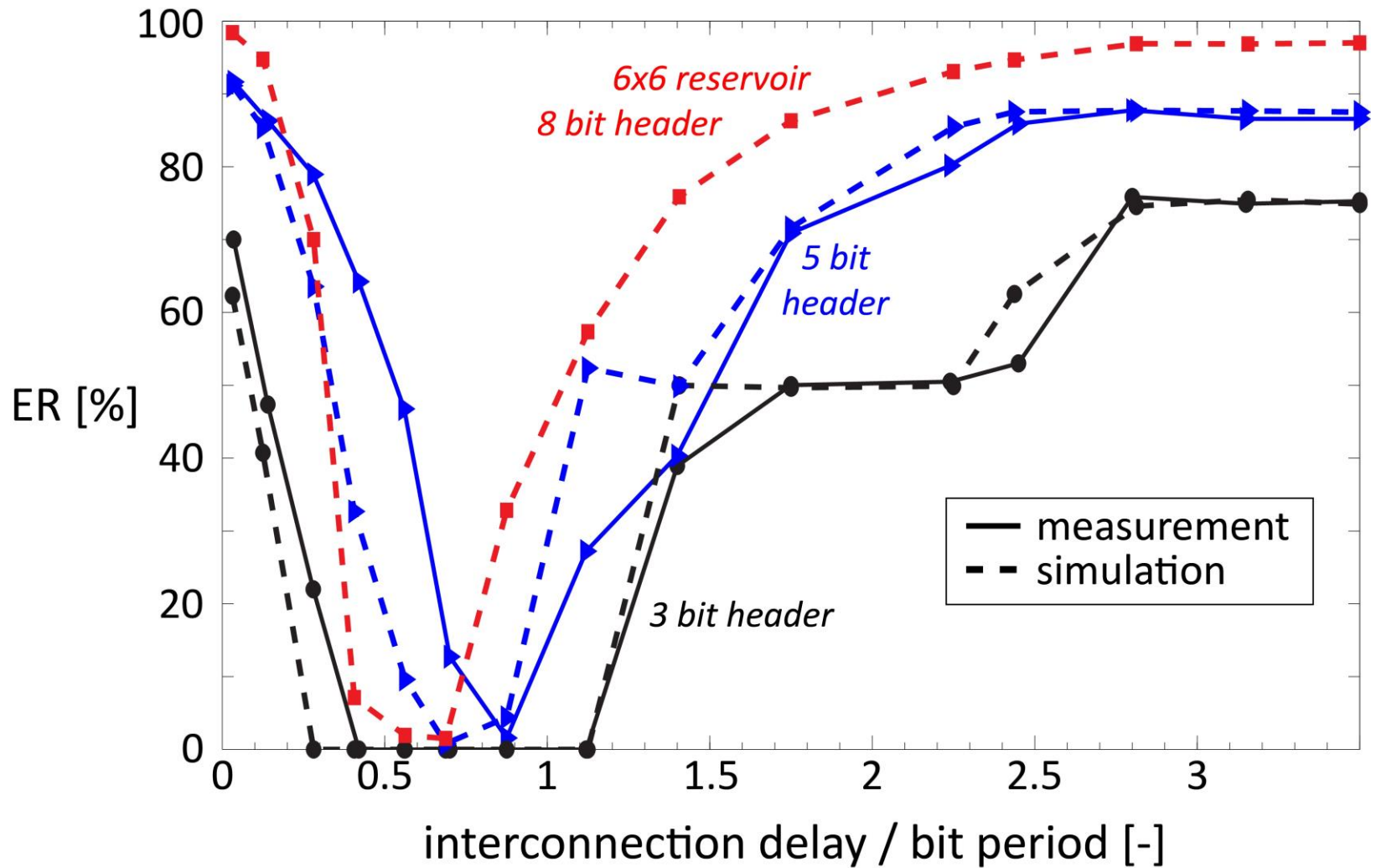
The XOR task can be solved at different speeds and different bit combinations



Other Boolean tasks can be solved as well (with the same reservoir states)



Header recognition



Advantages

- Scalability:
 - Note that we spent a lot of effort to slow down the signal!
 - Easily scalable to higher speeds by shortening the delays
- No active power consumption on chip
- Same generic chip can be used for
 - digital tasks (simulation confirmed by experiment)
 - analog tasks (theory only, no suitable equipment)

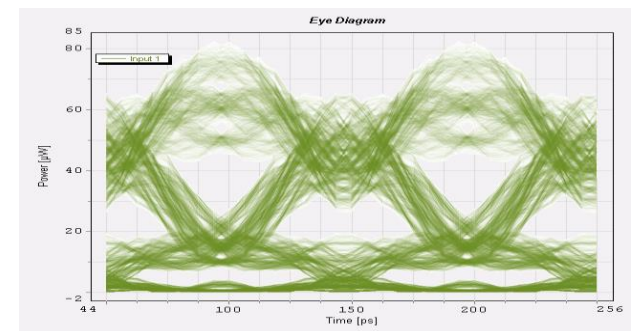
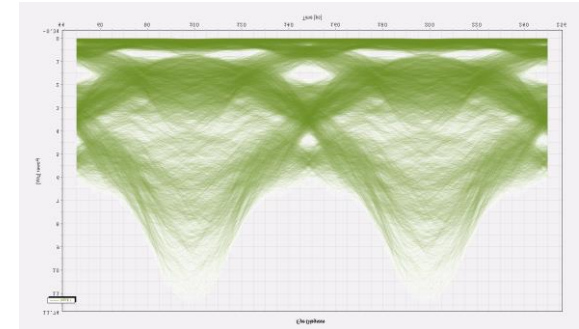
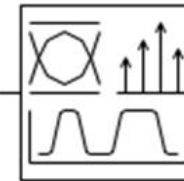
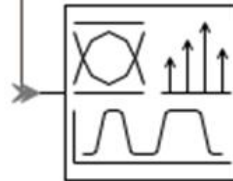
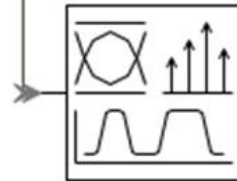
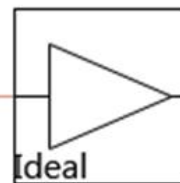
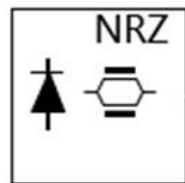
APPLICATIONS

Telecom task: non-linear equalization of optical links

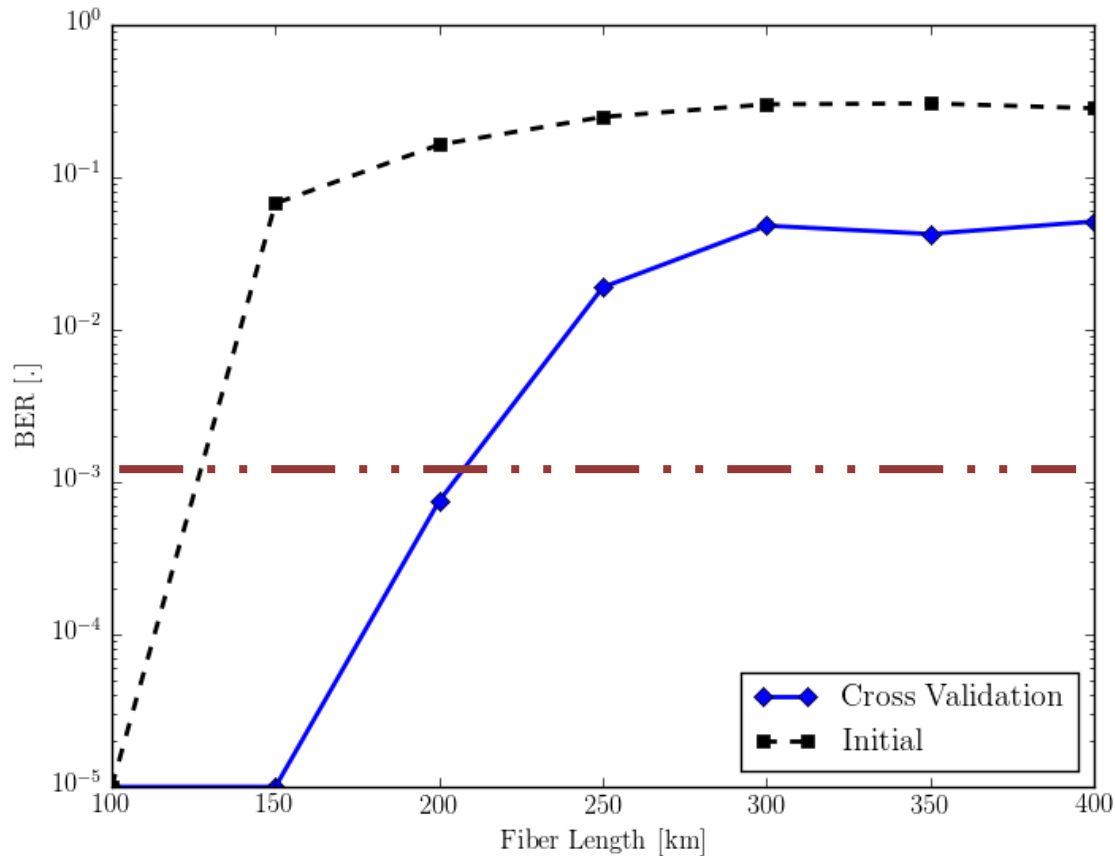
Transmitter:
Modulator + Laser

Length = 150.0e3 m

EDFA



Equalization results with passive SOI chip



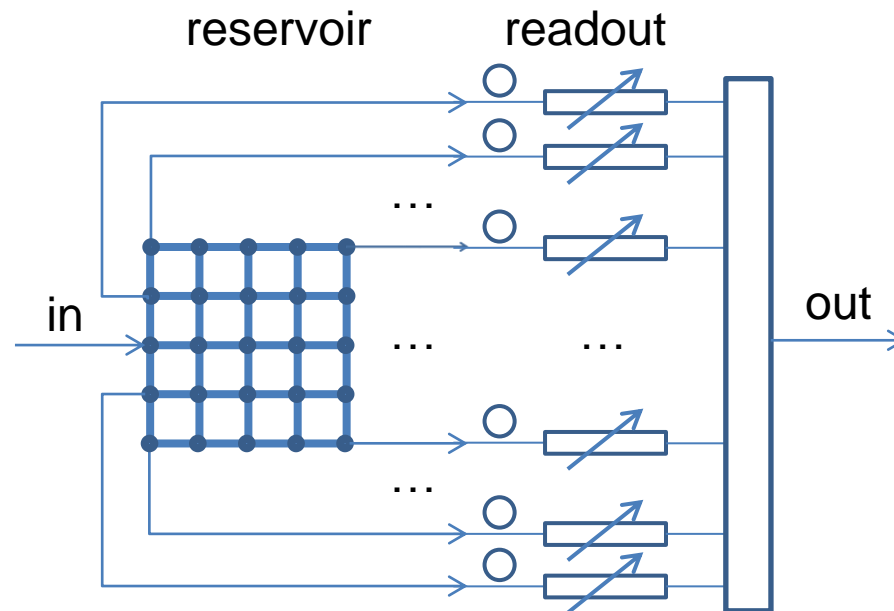
Metro Links

Up to 200 km below FEC Limit

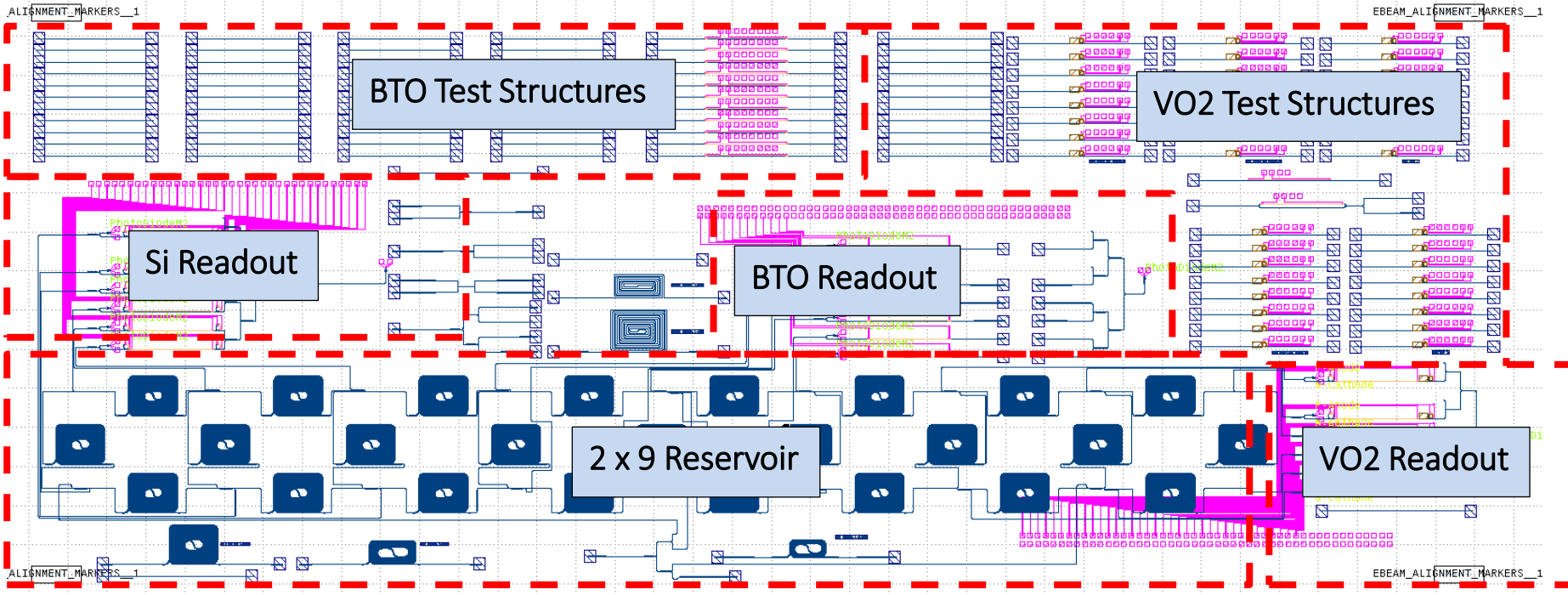
Scaling this up



- PhResCo: recently started H2020 European project (KULeuven, IBM, UGent, Supelec, IHP)
- Integrated readout on chip:



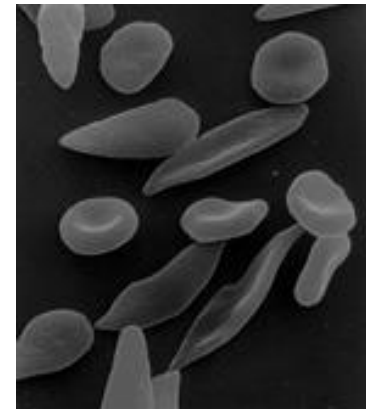
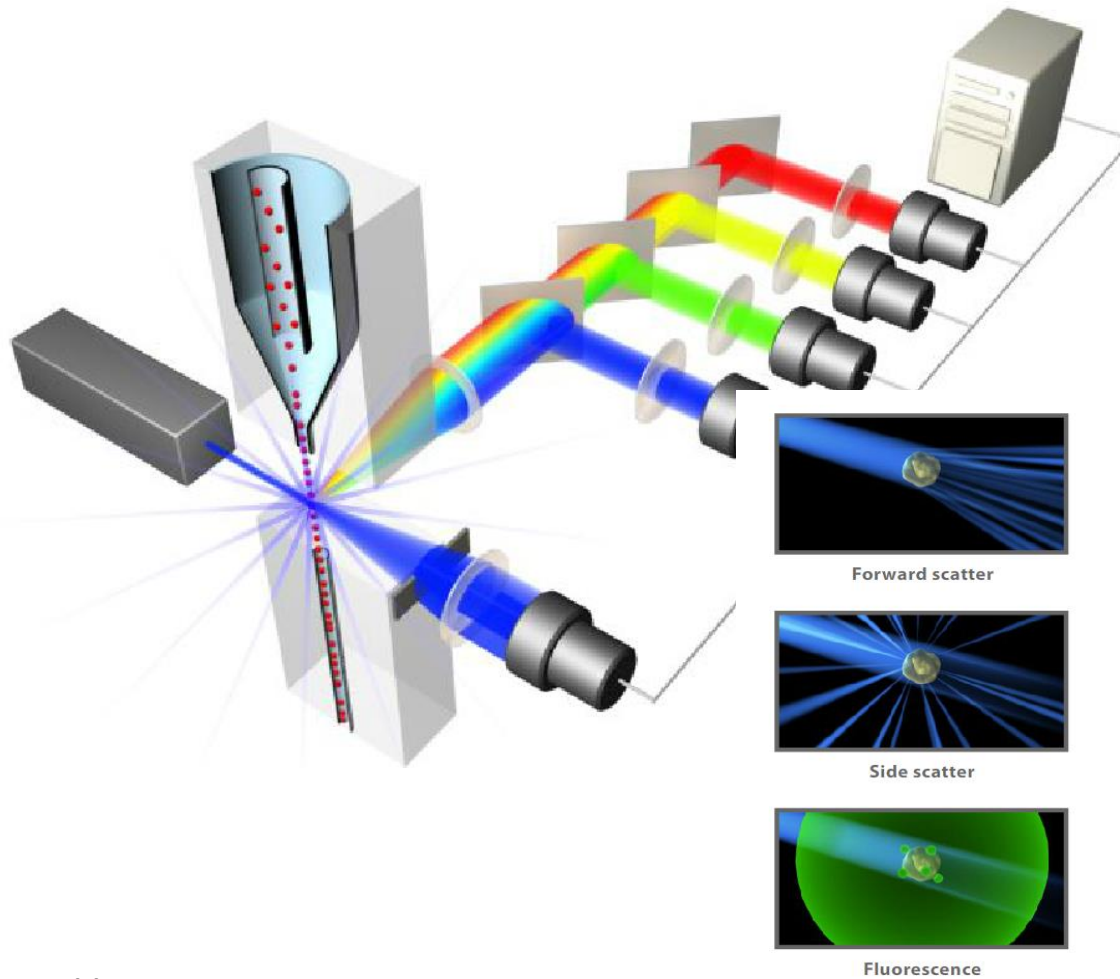
First design: comparing 3 different technologies



Conclusions

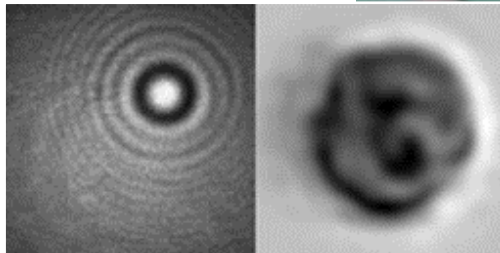
Neuromorphic computing
is interesting new paradigm
for photonics information processing

Flow cytometry

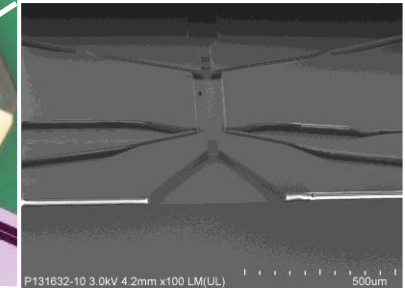
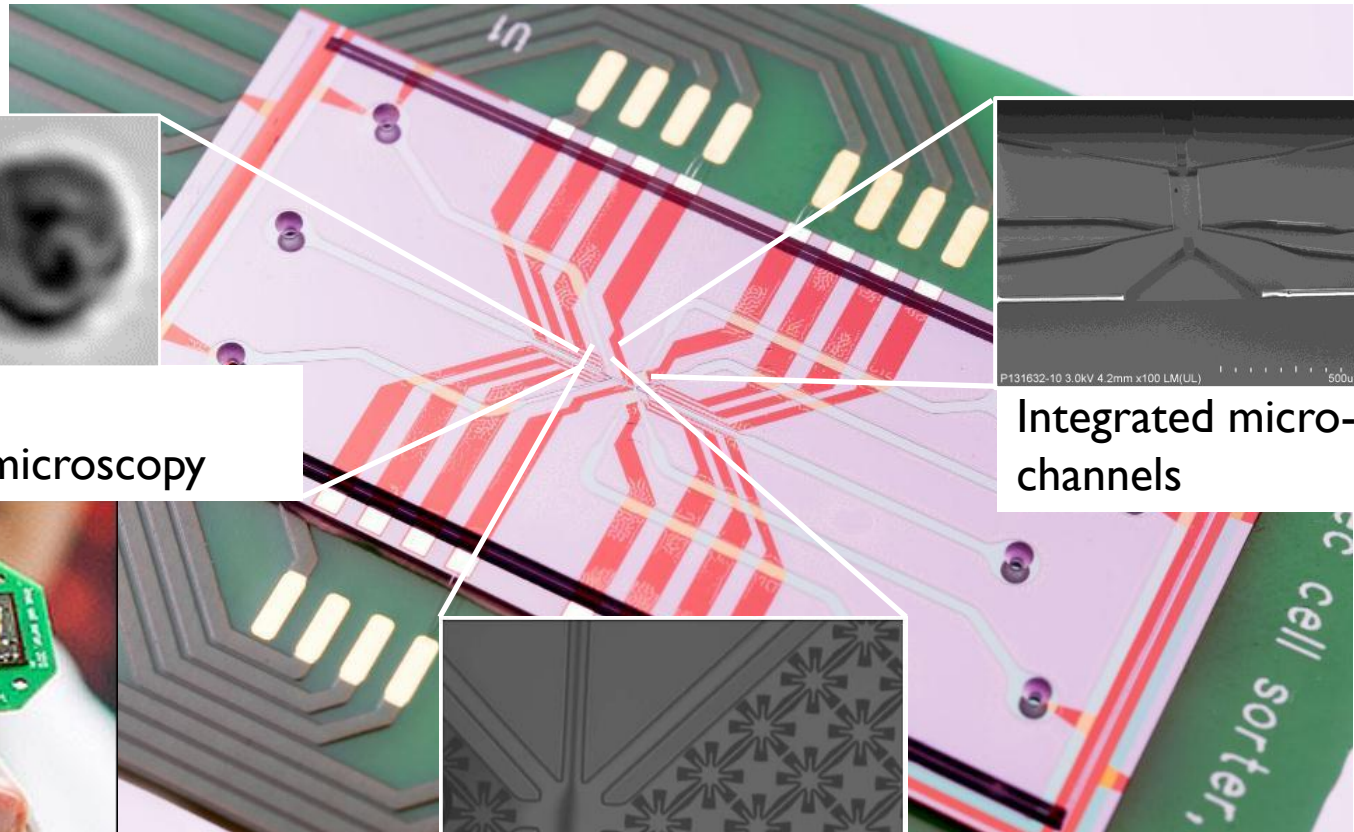
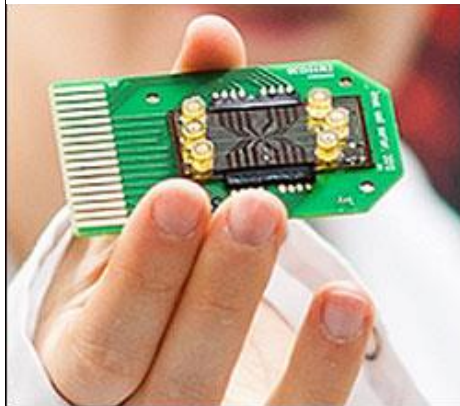


<http://www.lifetechnologies.com>

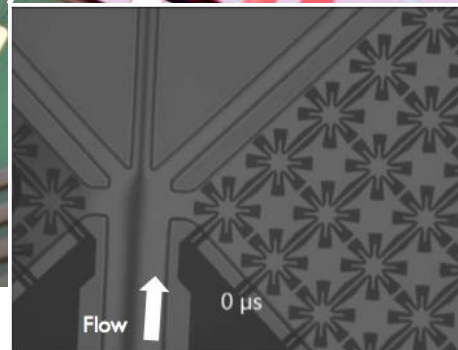
Imec cell sorter



On-chip Fast high-resolution microscopy



Integrated micro-fluidic channels



On-chip high speed cell sorting

Computational complexity

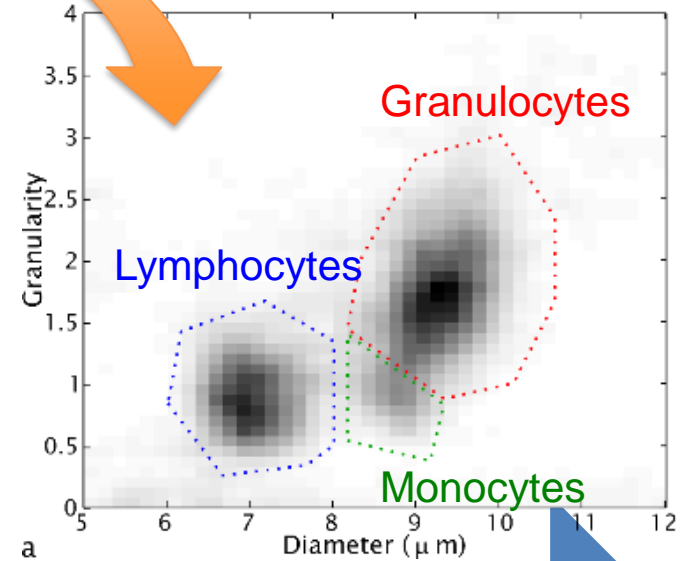
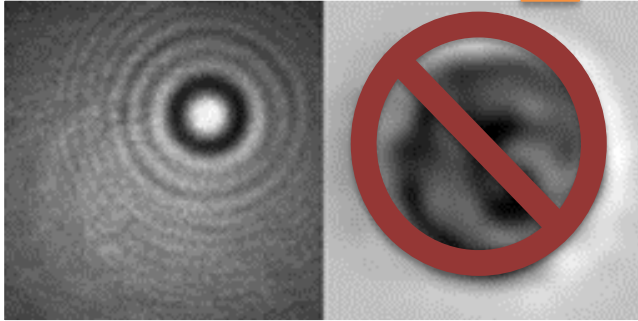
- Complex convolution or sequence of 2D FFTs
- 512x512 pixels/image
- 1M cells/sec
- 482nd Top 500 Flex for measurement

#	Site	System	Cores	Performance[TF/sec]	Power [kW]
482	Automotive United States	IBM Flex System x240, Xeon E5-2670 8C 2.600GHz, Infiniband FDR IBM	8,336	157.7	181

<http://www.top500.org/>

Algorithm

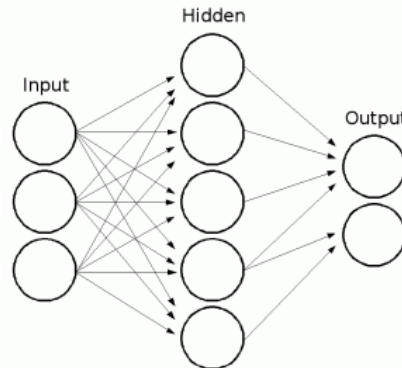
Methods



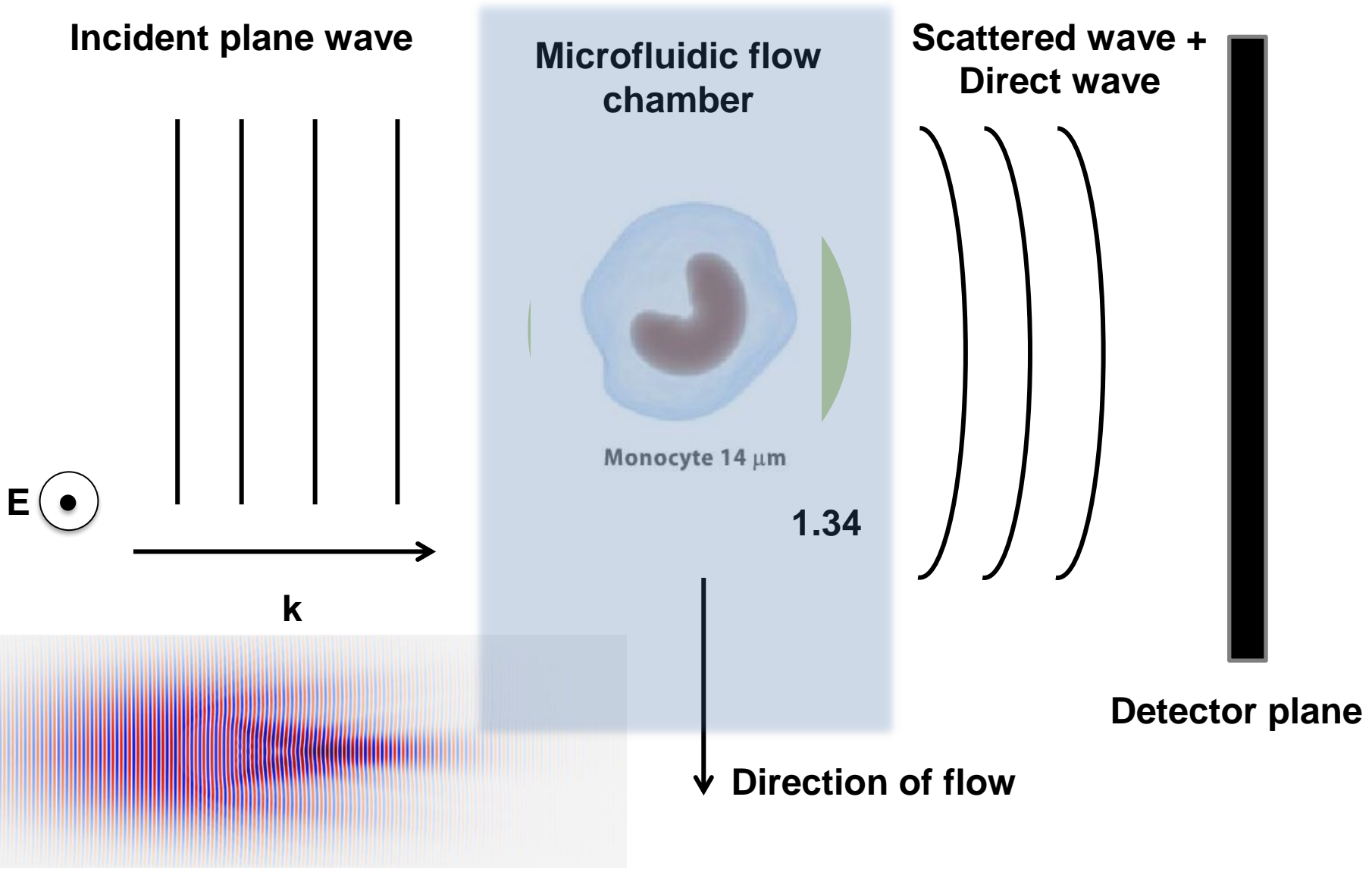
~~numerical reconstruction~~

feature selection

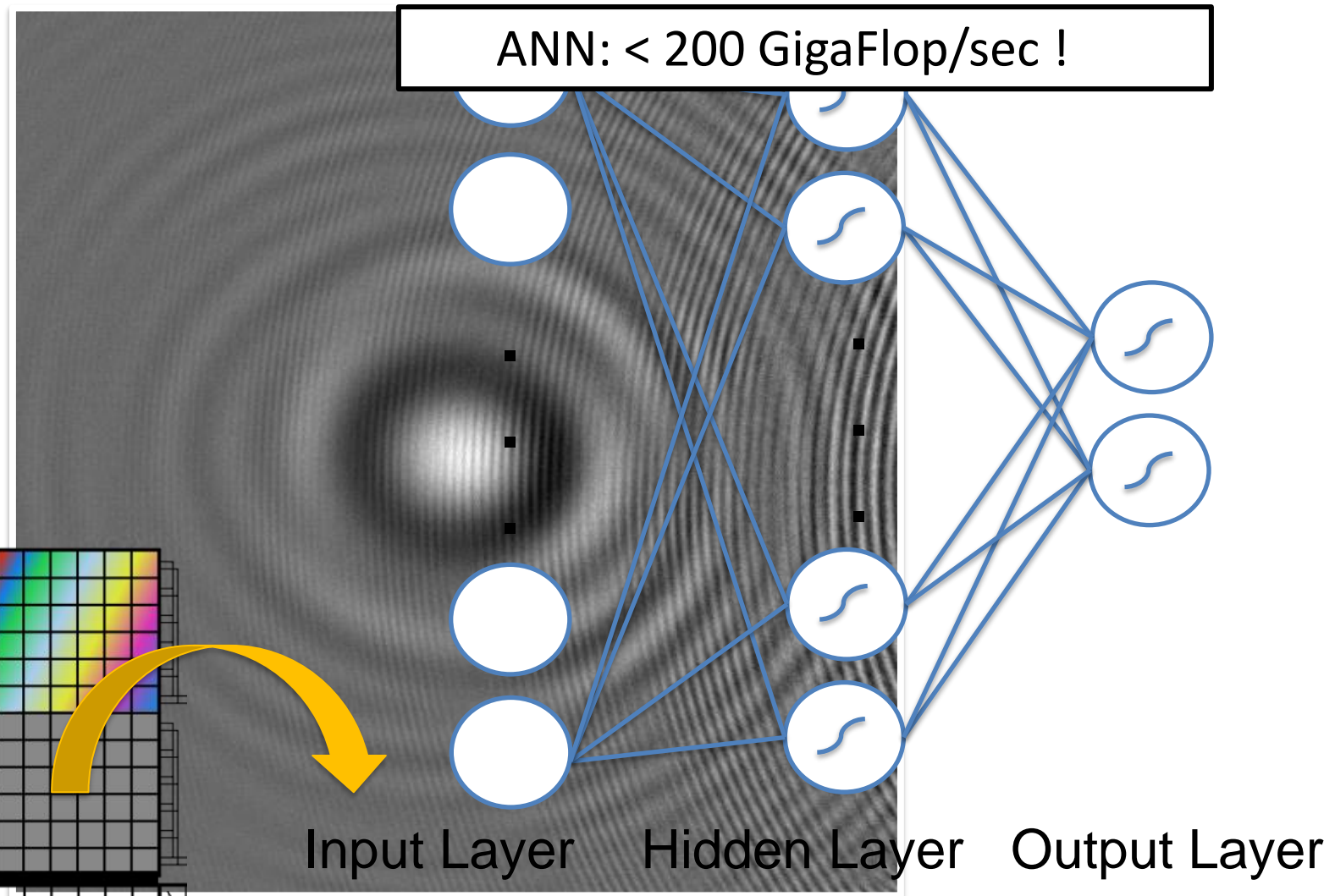
classification



Real experimental data



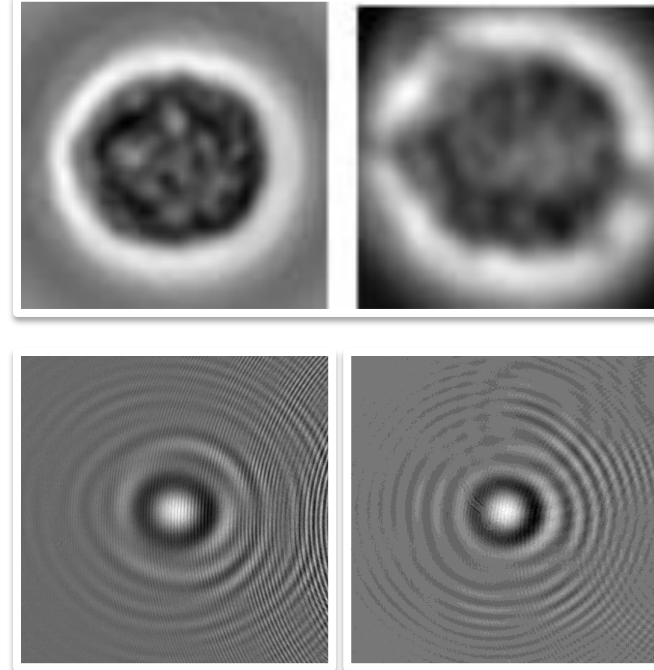
Neural network - pipeline



Three-part WBC classification

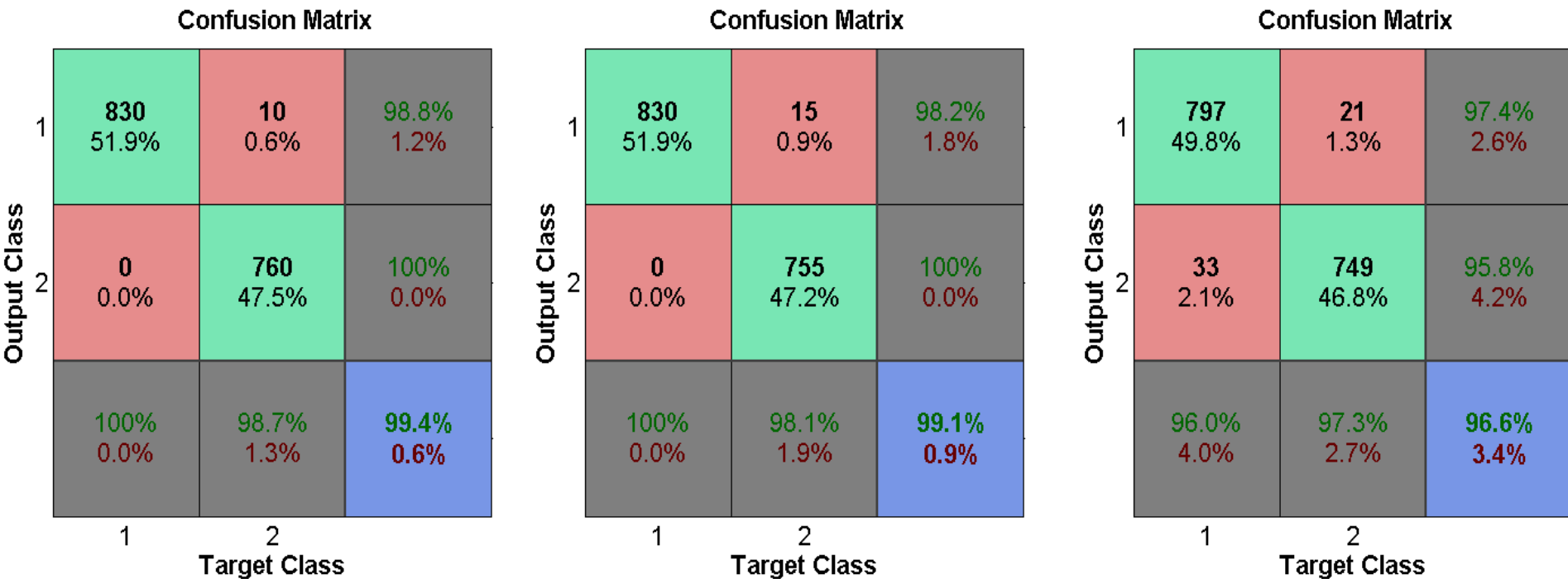
- Dataset of ~7500 non-purified WBC:
Granulocytes (59.8%),
Lymphocytes (34.6%),
Monocytes (5.6%)
- Use of 10 random folds for cross-validating (CV) the results
- Adding noise to weights at fixed SNR

Results



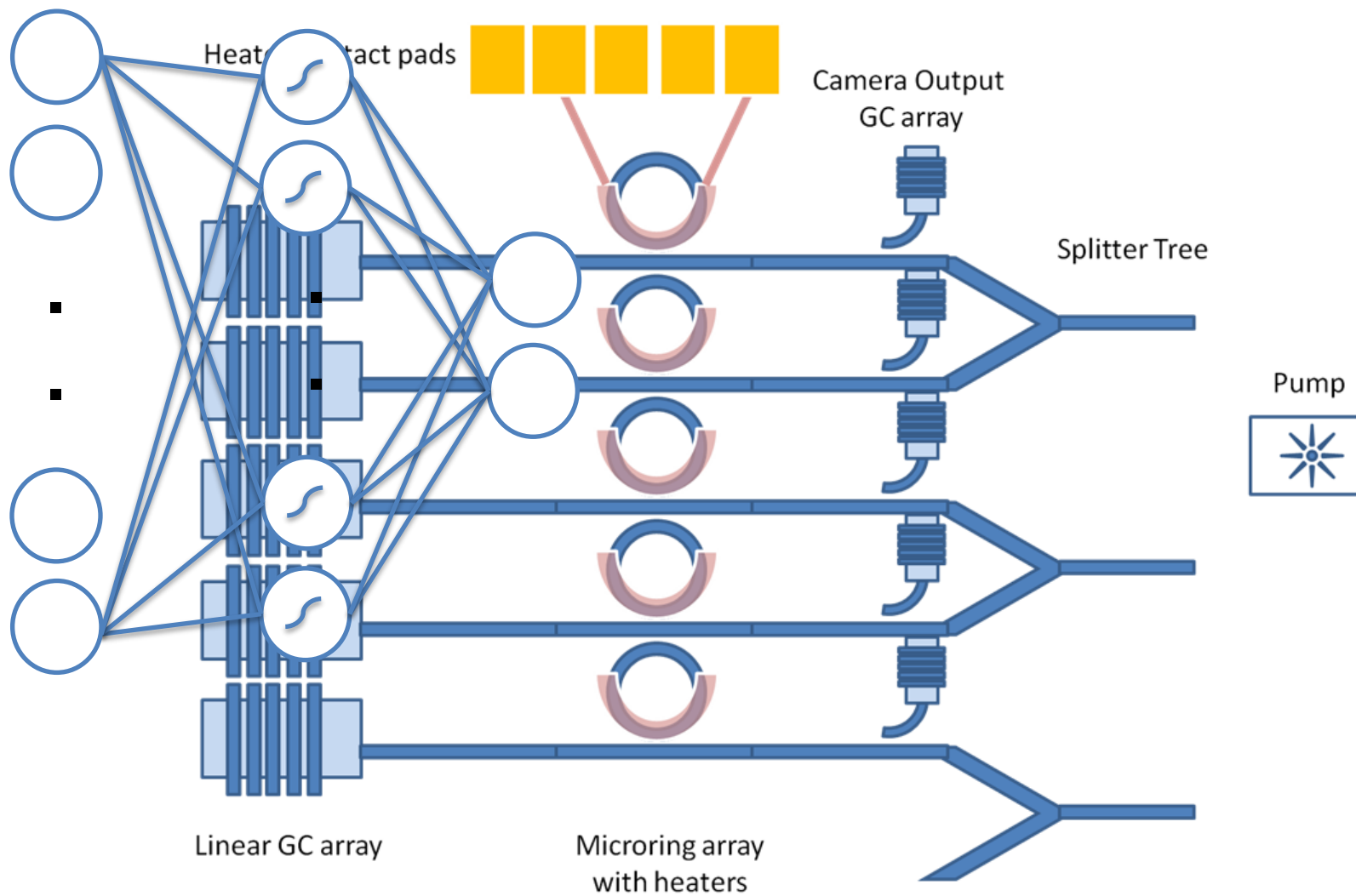
Purified monocyte/granulocyte classification

Averaged classification results with increasing signal-to-noise ratio (from left to right: 30dB, 10 dB, 3 dB)



Class 1 = monocytes
Class 2 = granulocytes

Towards a hardware solution

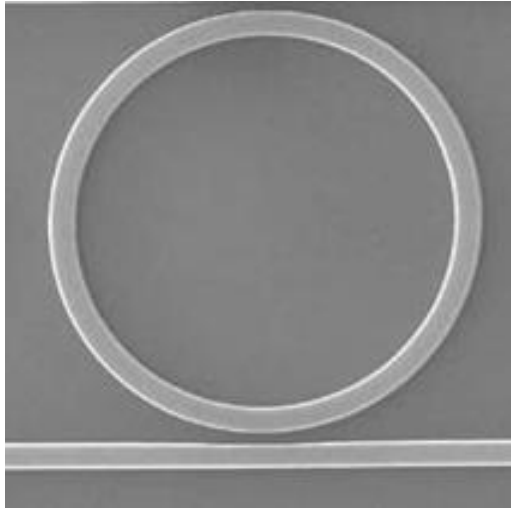


Conclusions

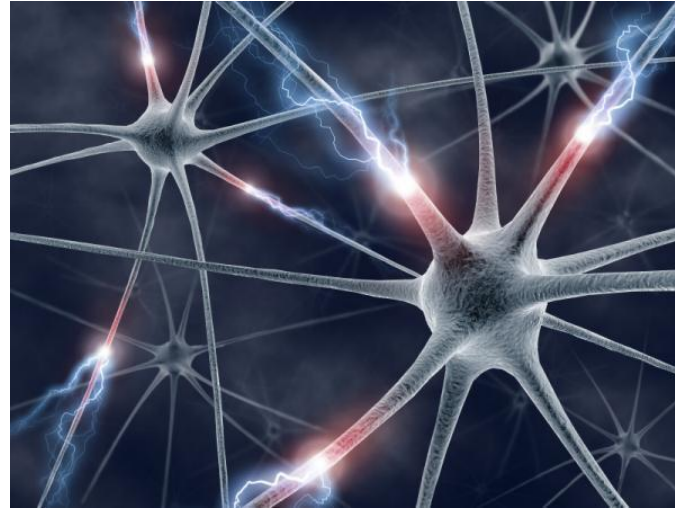
Neuromorphic computing
is interesting new paradigm
for photonics information processing

EXCITABLE SILICON RINGS

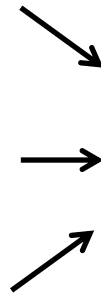
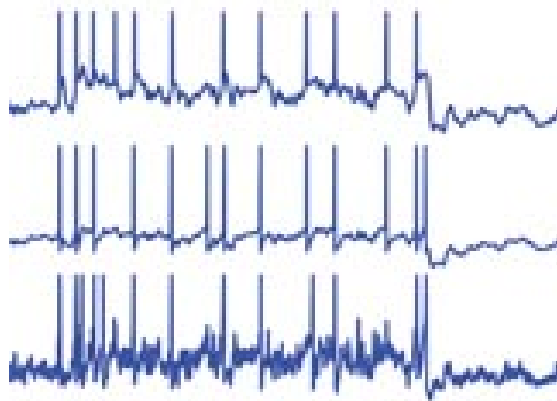
Building a photonic spiking neuron



=



?

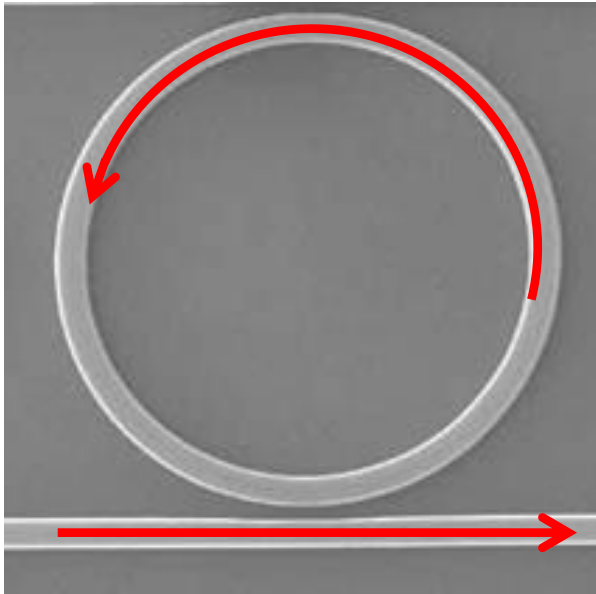


Research question

- People have seen excitability in photonics before, but never cascaded it on chip

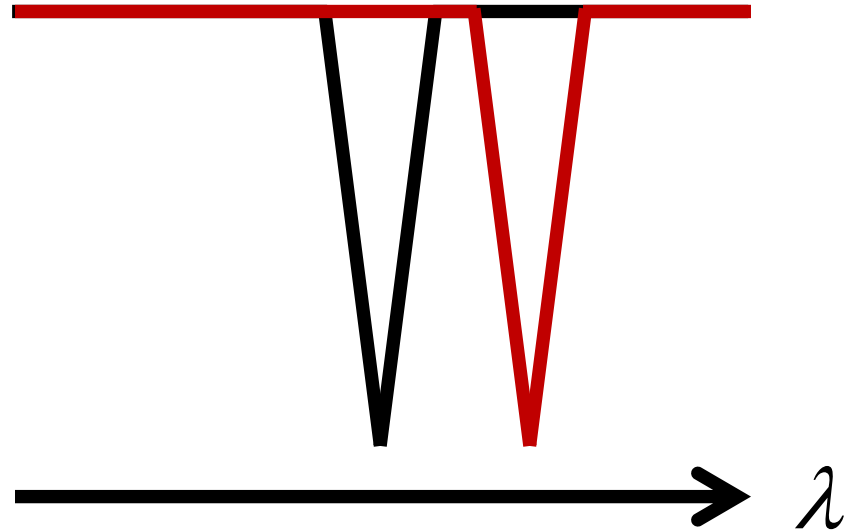
- Can we cascade excitability on-chip using ring-resonator neurons?

Thermo-optic effect causes redshift



Light circulation in ring

Heating of the ring



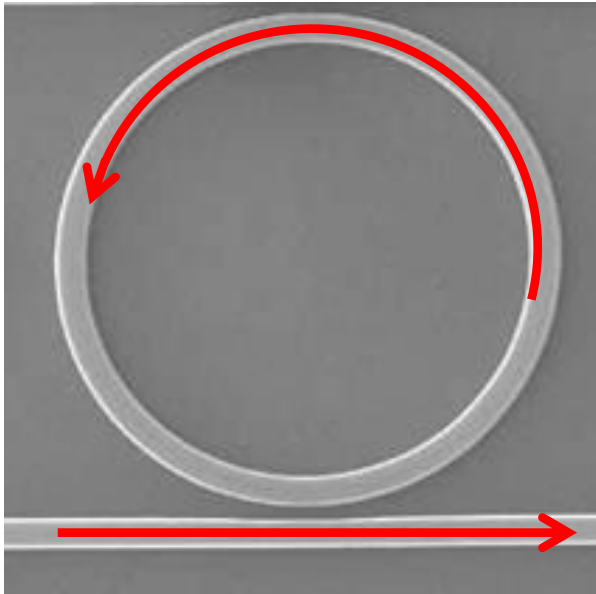
$$re^{i\phi}$$

resonance dip/peak

$$\Delta T$$

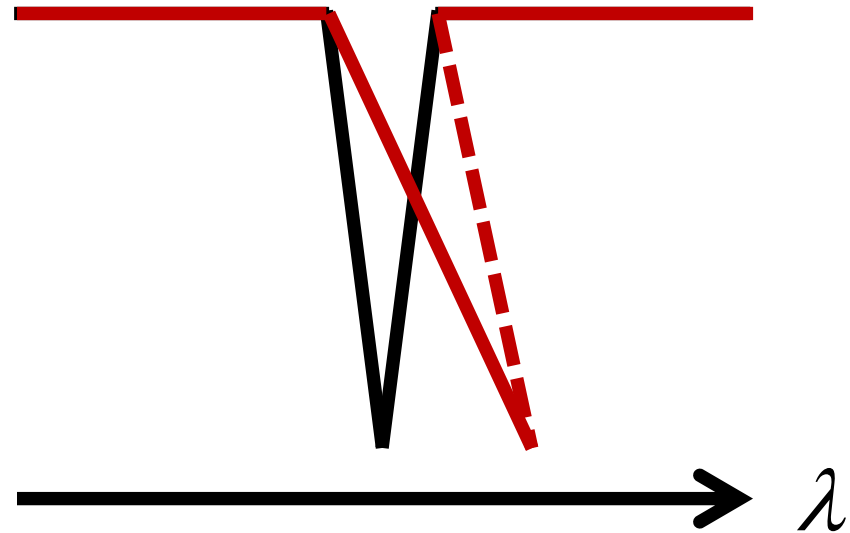
redshift

Self-heating causes bistability



Light circulation in ring

Heating of the ring



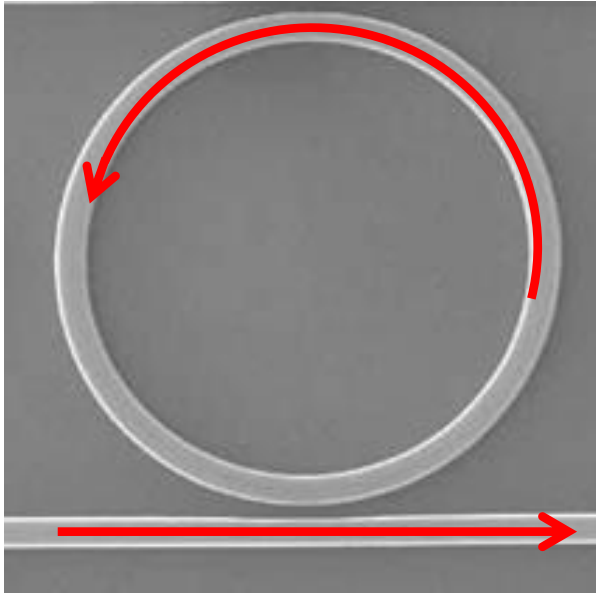
$$re^{i\phi}$$

resonance dip/peak

$$\Delta T$$

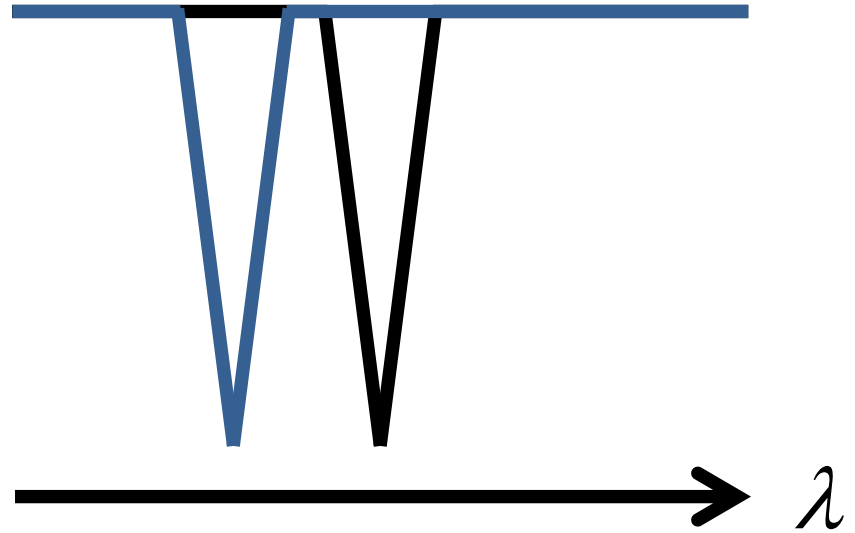
redshift

Free carriers cause blueshift



Light circulation in ring

Free carriers

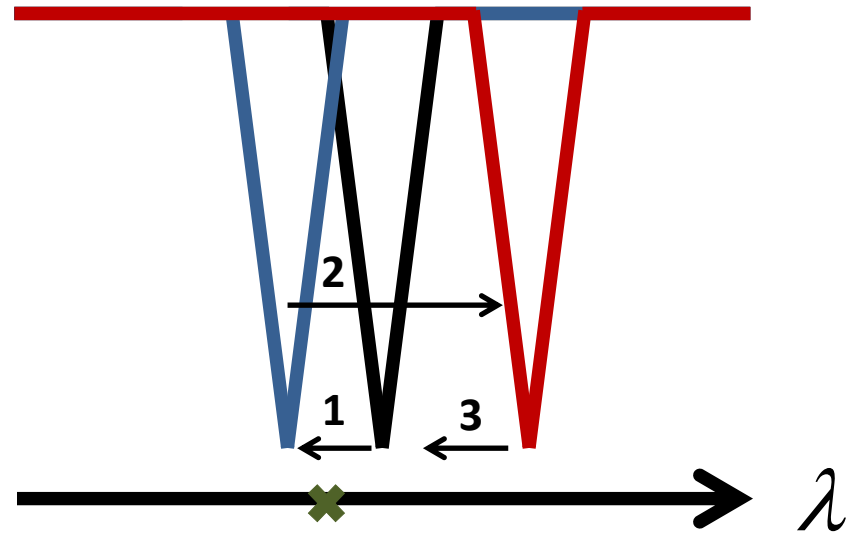


resonance dip/peak

N

blueshift

Combination free carrier and thermal effect can cause self-pulsation



Light circulation in ring

$$re^{i\phi} \quad \sim \text{ps}$$

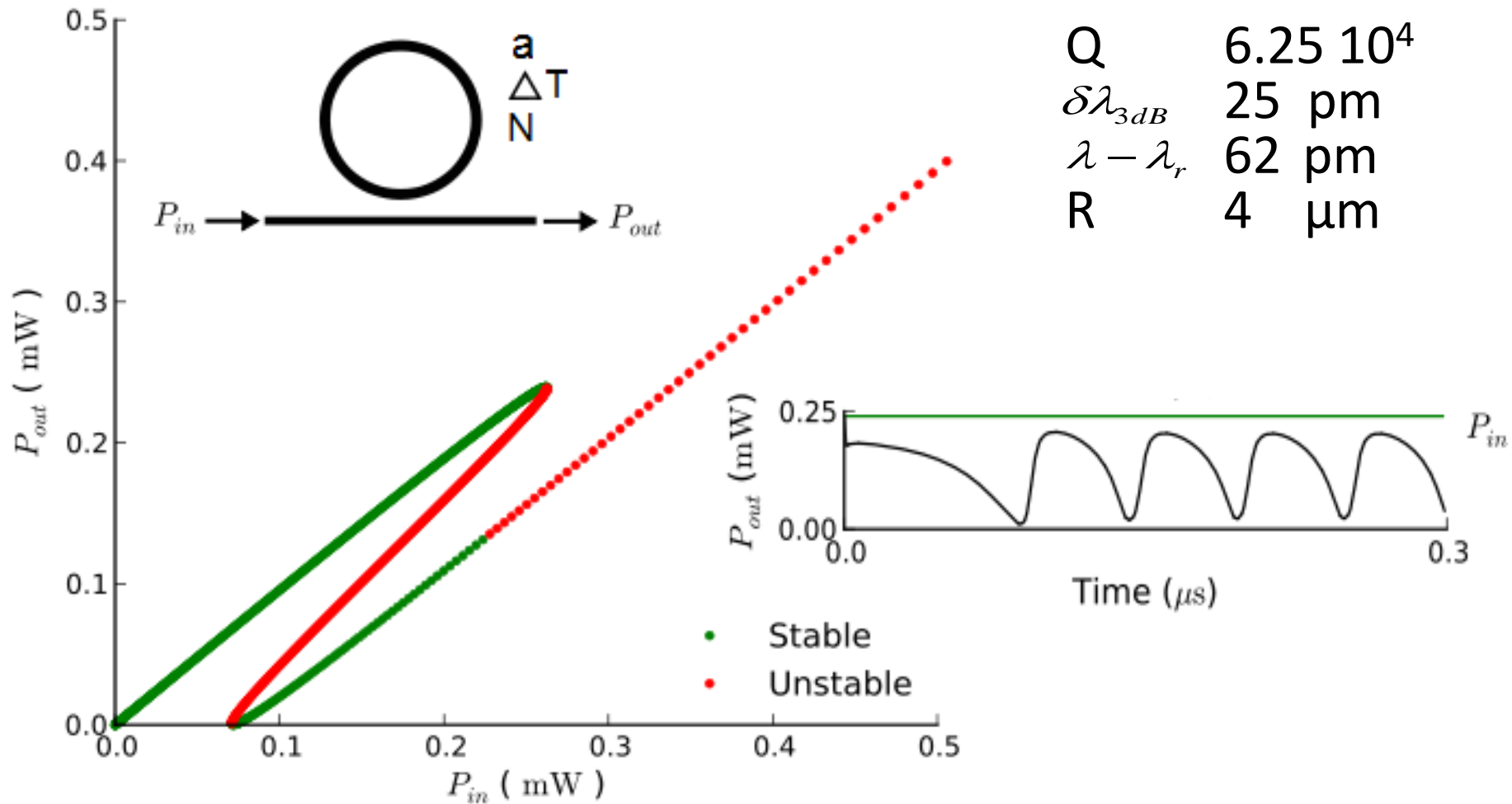
Cooling of the ring

$$\Delta T \quad \sim 100 \text{ ns}$$

Free carriers

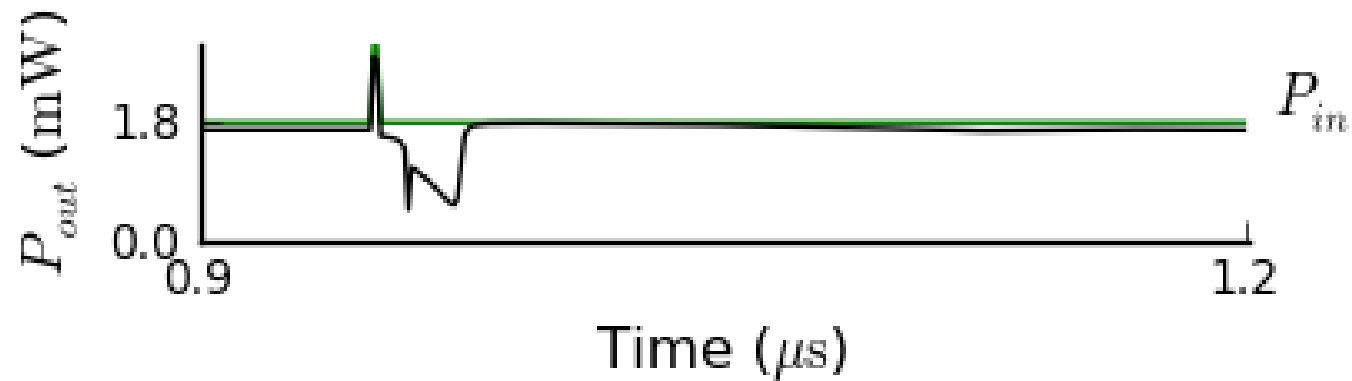
$$N \quad \sim \text{ns}$$

Simulations: bistability and self-pulsation

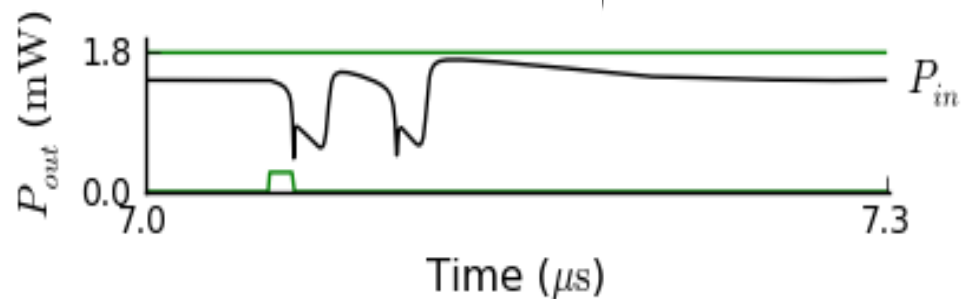
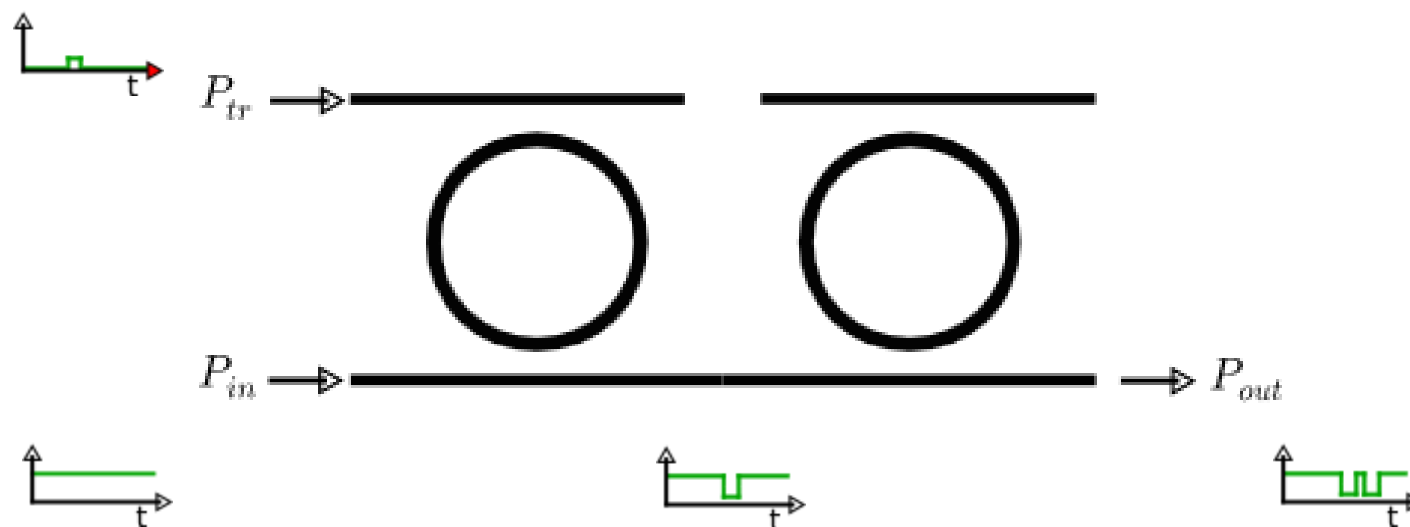


Simulation: excitability

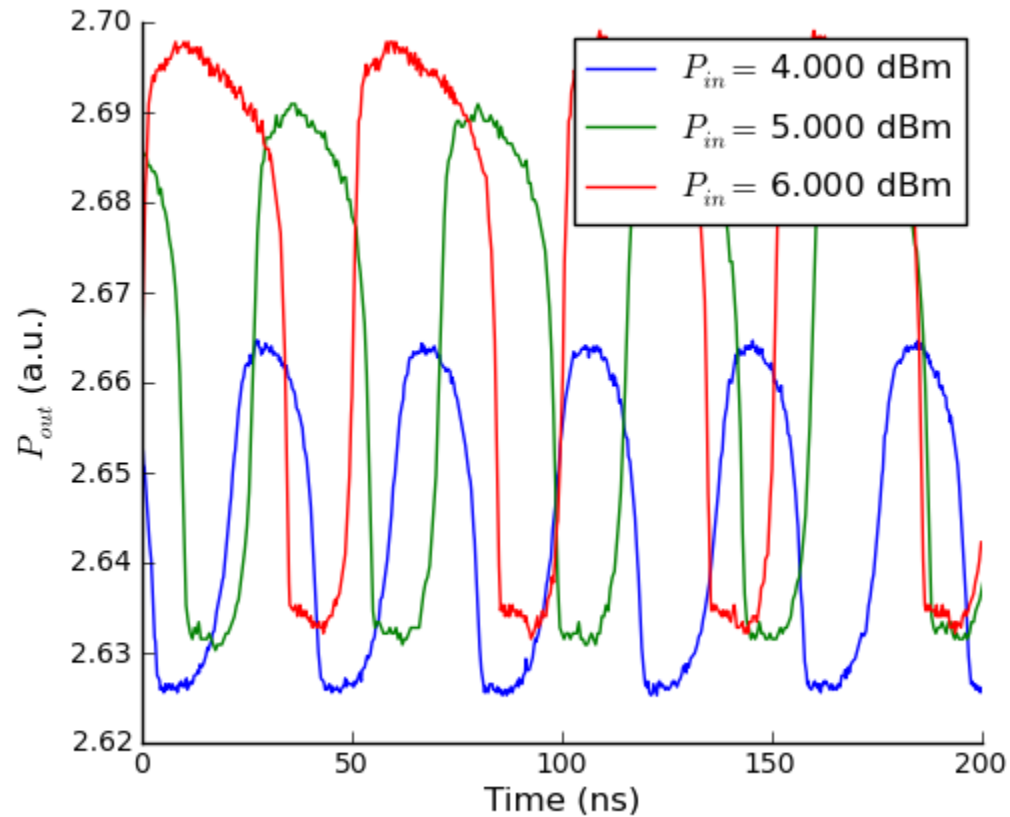
Wavelength and input power 'near' self-pulsation...



Simulation: cascadability

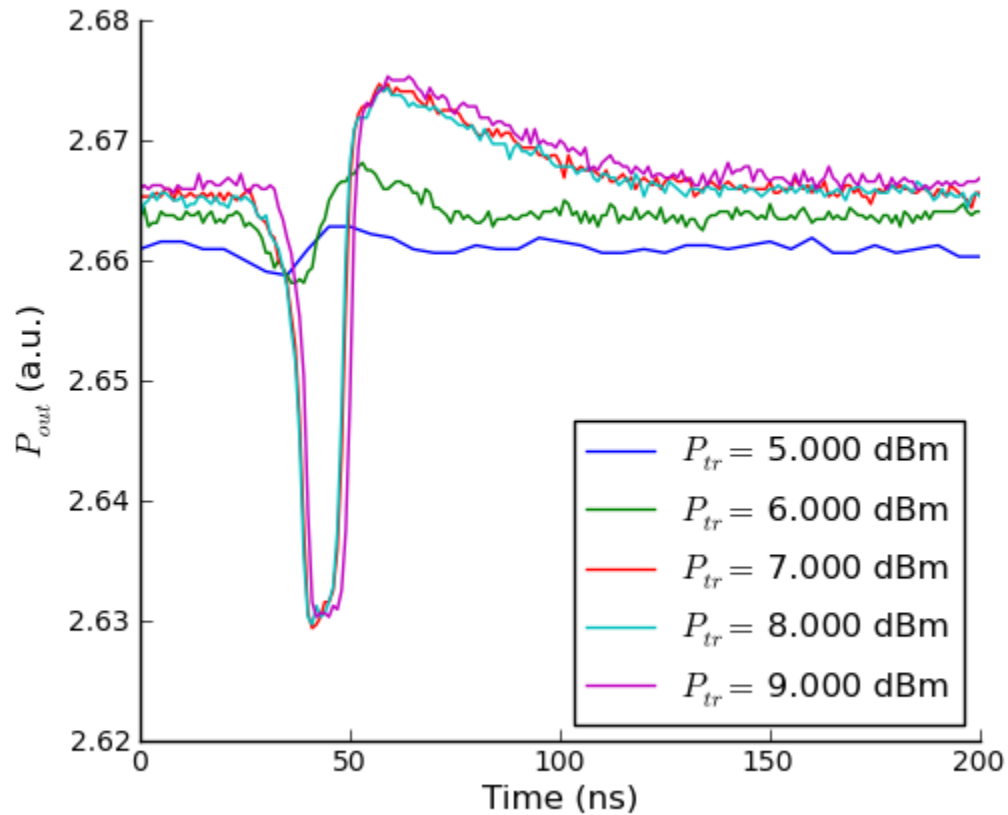


Experiment: self-pulsation

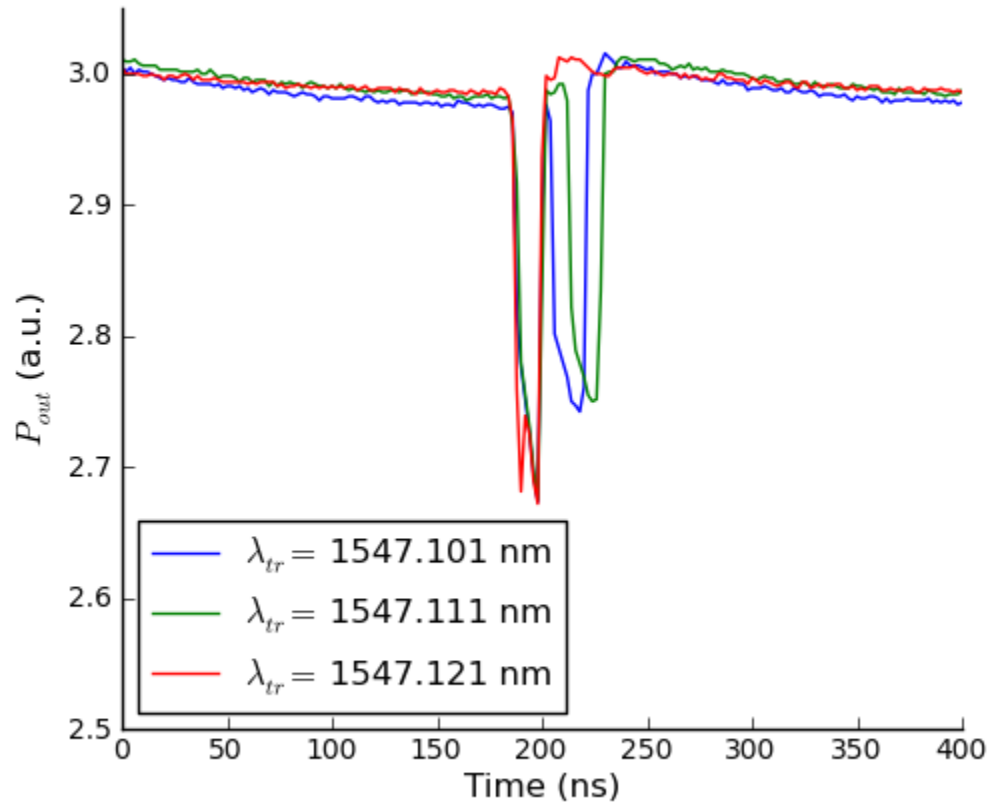


Experiment: excitability

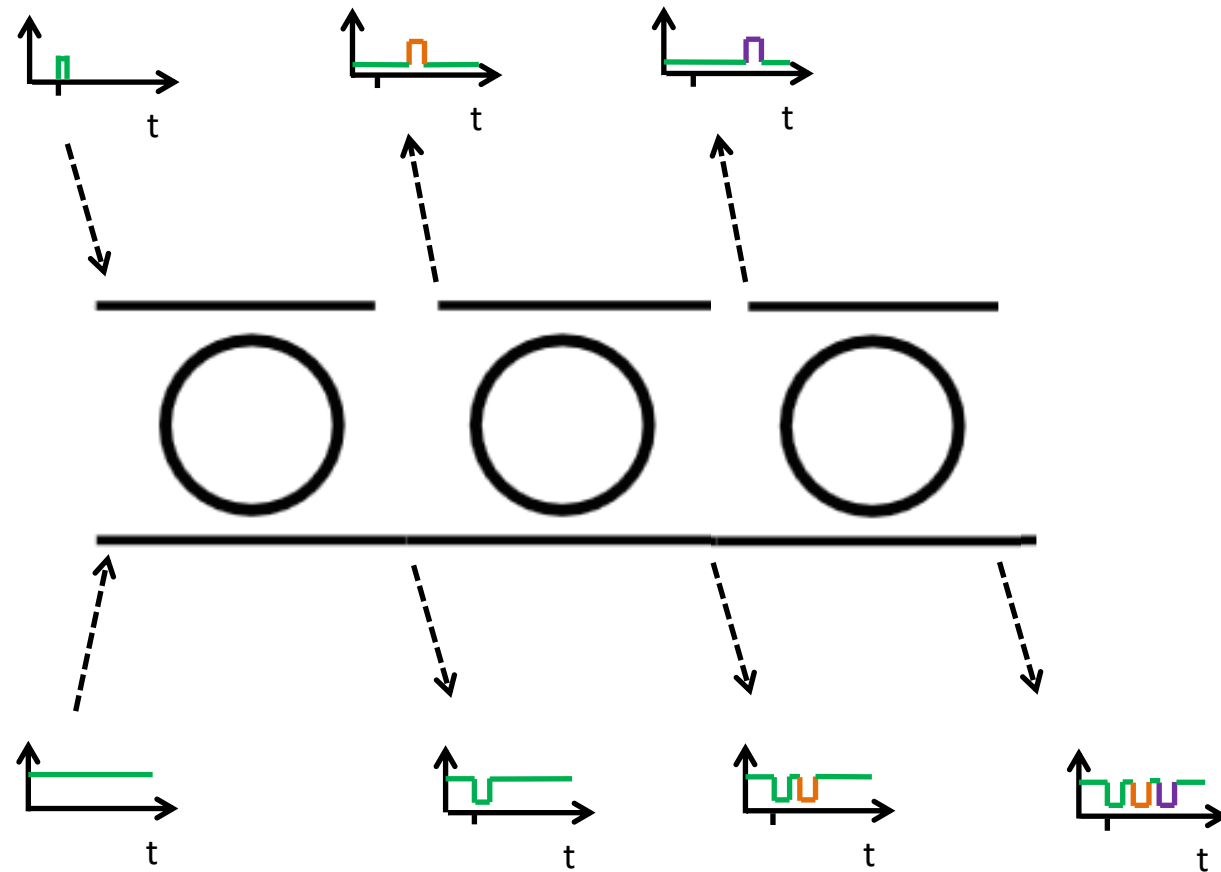
Pulses excited by external trigger signal:



Experiment: cascadability

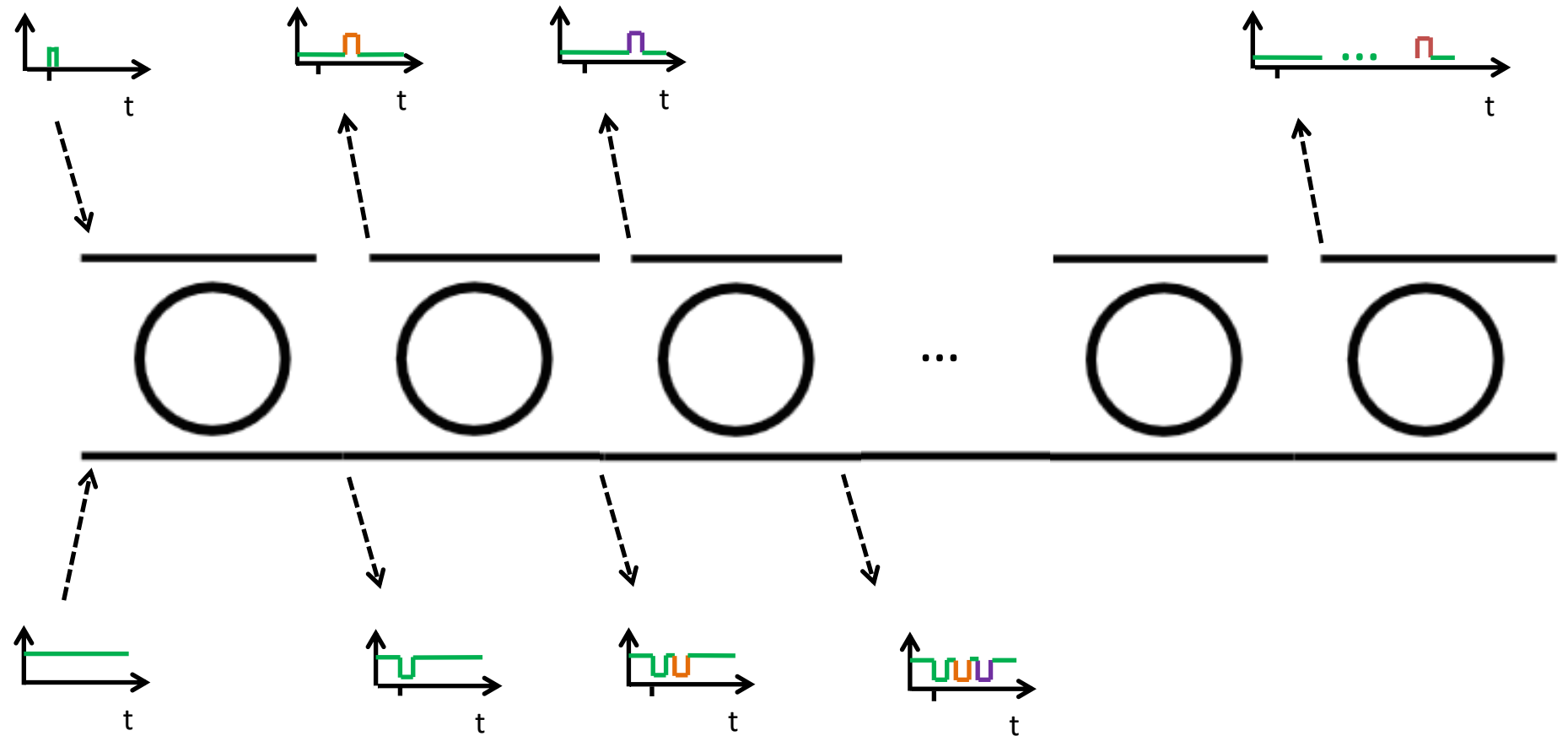


Cascading rings = creating a delay line

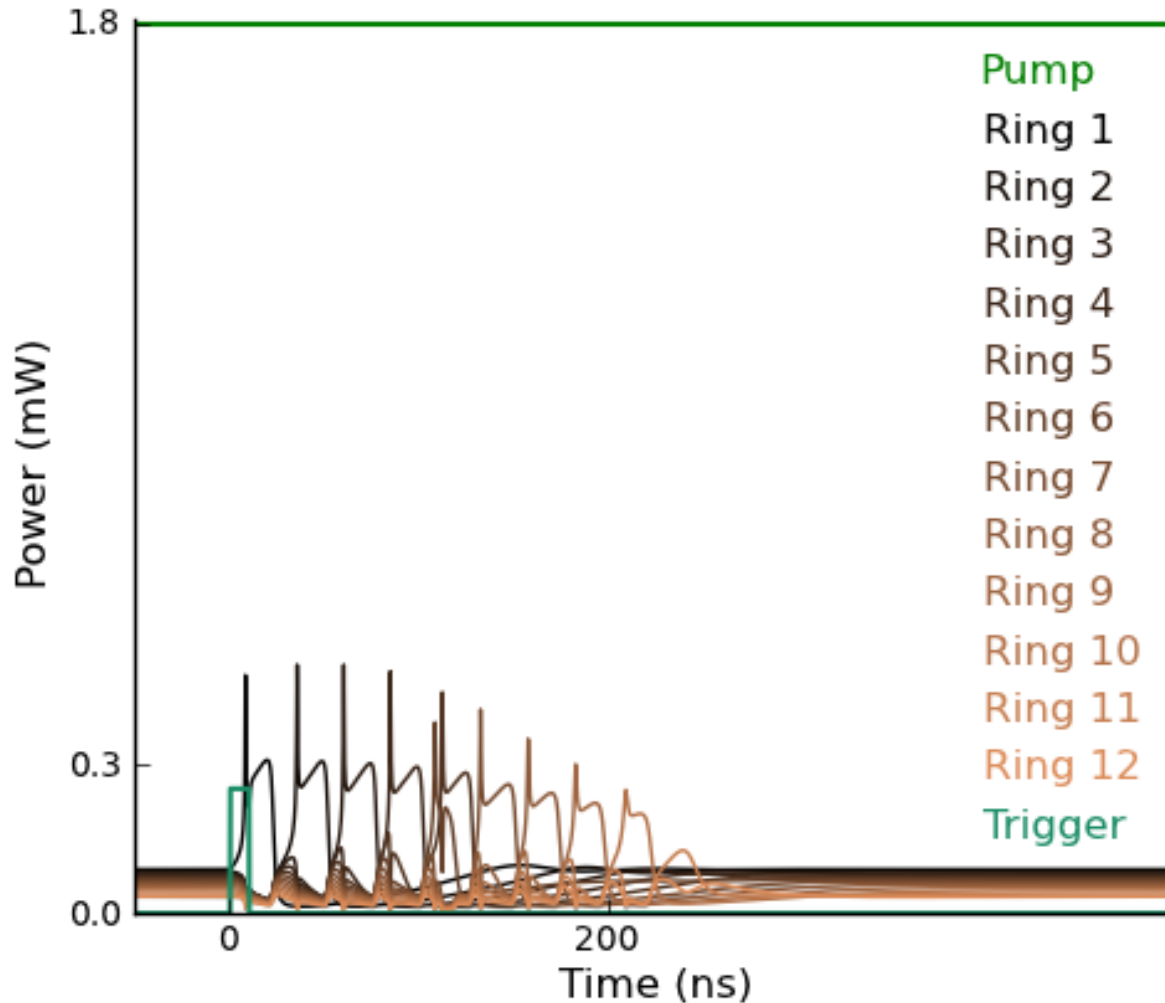


Cascading rings = creating a delay line

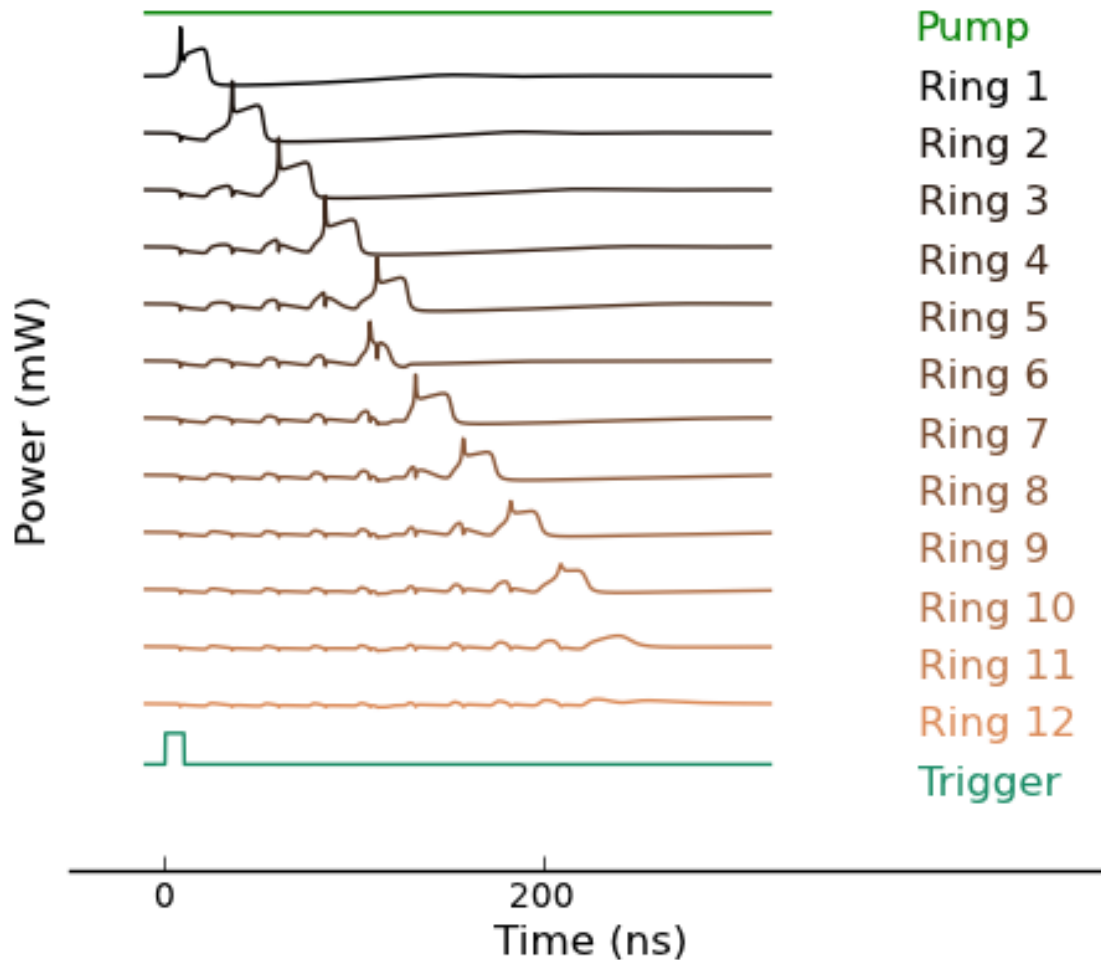
Max ~ 9-10 rings



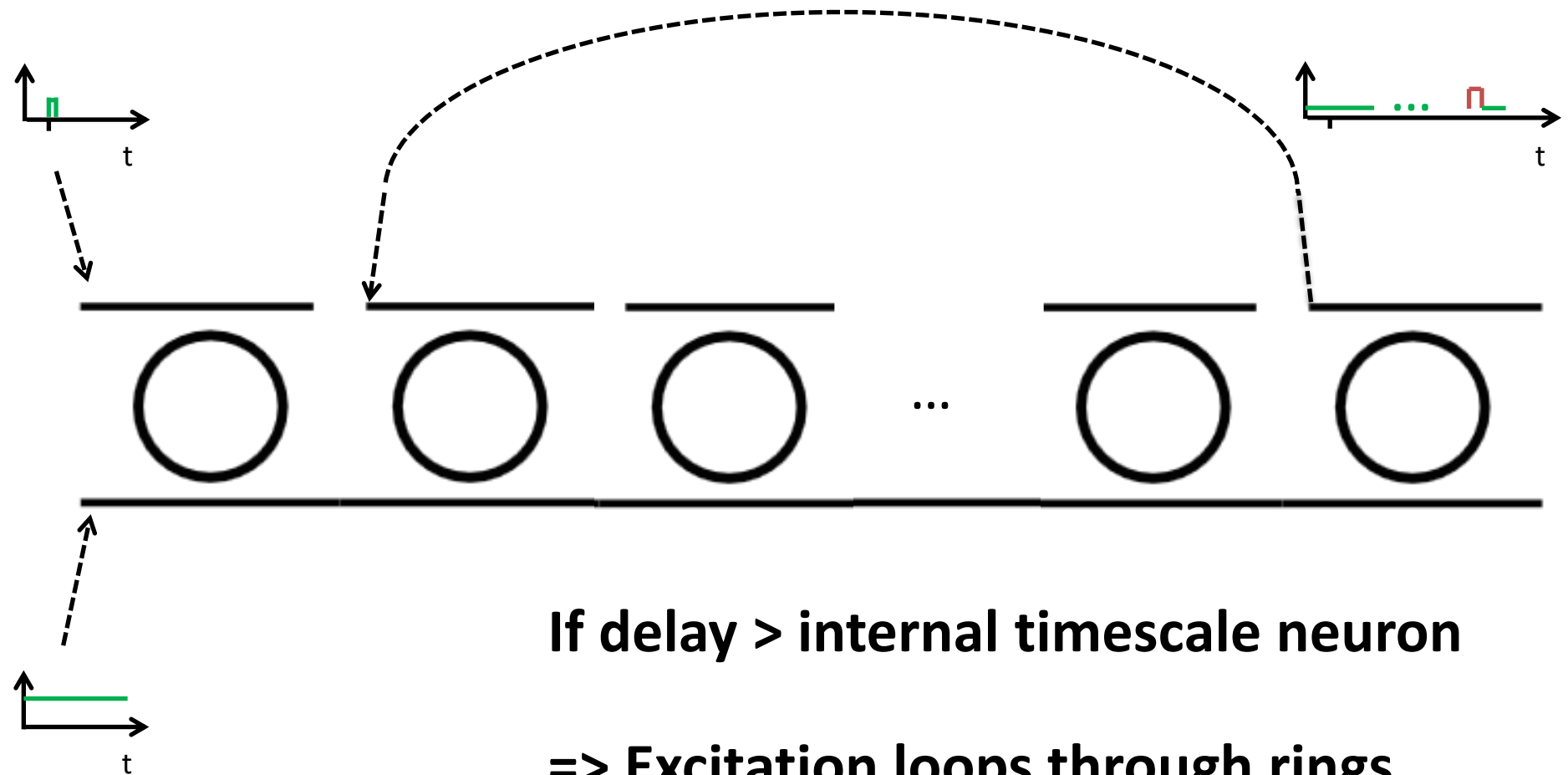
10 rings result in a ~200 ns delay of a 15-20 ns pulse



10 rings result in a ~200 ns delay of a 15-20 ns pulse



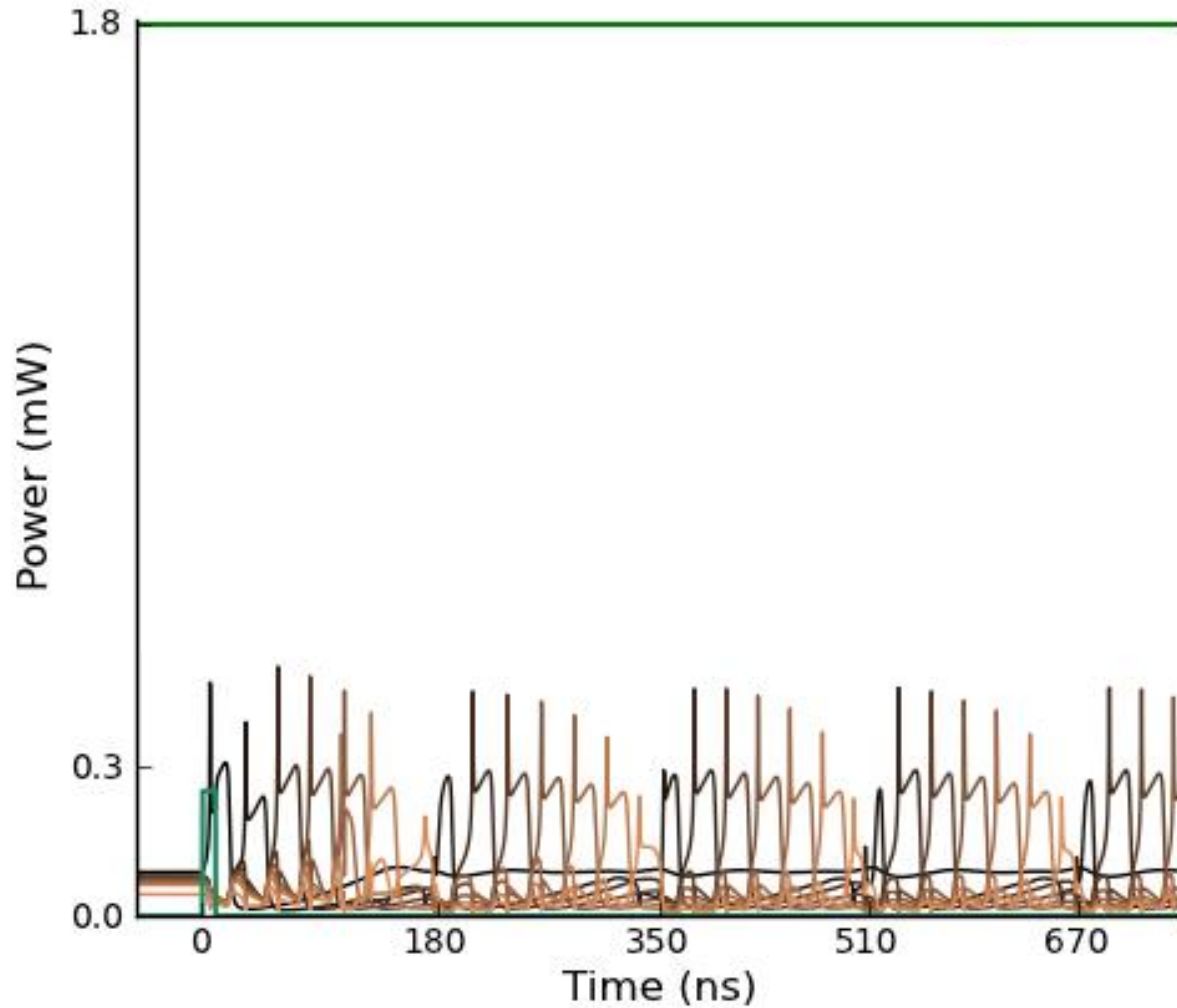
Making a loop => spike encoded memory/clock



If delay $>$ internal timescale neuron

=> Excitation loops through rings

The concept works! (loop from ring 2-8)



Conclusions

Neuromorphic computing
is interesting new paradigm
for photonics information processing