III-V-ON-SILICON WIDELY TUNABLE LASER REALIZED USING MICRO-TRANFER-PRINTING

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Abstract

We present a C-band widely-tunable III-V-on-silicon laser (50 nm tuning, 5.2 dBm maximum power, 300 kHz minimum linewidth) realized through a micro-transfer-printing approach, in which III-V SOAs are pre-fabricated on a III-V substrate transferred using an elastomeric stamp to the silicon photonic circuit defining the laser cavity.

1 Introduction

Silicon photonic integrated circuits (ICs) are of great interest to realize high-speed optical transceivers with applications ranging from intra-data center interconnects [1] to long-haul communication [2]. This stems from the fact that the circuits can be realized in high volume and at low cost using the CMOS fabrication infrastructure on 200 mm or 300 mm wafers. The high yield and uniformity of the fabrication technology also allows realizing more complex photonic systems-on-chip, for applications in optical interconnects [3], optical sensors [4], bio-medical instruments [5], etc. However, the lack of an integrated gain element on the platform is limiting the extension of the platform to an even broader range of applications. Therefore, much research is geared to the integration of III-V semiconductor optical amplifiers and lasers on the silicon photonic platform. Different strategies can be envisaged to realize this. The most mature approach, pioneered by Luxtera, is to use a micro-packaged III-V diode laser that is pick-and-placed on the silicon photonic wafer using an active alignment step and which interfaces with the silicon circuit using a grating coupler structure [6]. While this approach allows for high-efficiency single wavelength lasers to be integrated, the sequential assembly process (similar to flip-chip integration of III-V diode lasers) makes it difficult to scale up. Also, the integration of III-V SOAs, requiring two optical ports, still needs to be demonstrated. In order to overcome these issues, III-V die-to-wafer and wafer-to-wafer bonding approaches are pursued, in which case a high-throughput integration of lasers, amplifiers and other III-V opto-electronic components can be realized through wafer-level processing of the bonded III-V films [7]. This approach comes however with its own set of drawbacks: the process disrupts the silicon photonic process flow as III-V dies need to be bonded after the front-end process and before the back-end-of-line process. Moreover, a compound yield issue may arise, as the III-V opto-electronic devices are only fabricated (and therefore tested) after the III-V material has been integrated. III-V hetero-epitaxial approaches suffer from similar issues, and using this approach still many fundamental challenges need to be overcome before it can become a commercial reality. In this work we present the use of a novel technique, micro-transfer-printing [8], for the integration of III-V opto-electronic components on a silicon photonic wafer. It combines the advantages of flip-chip integration (pre-fabrication and testing of the opto-electronic components on the III-V wafer, minimal disruption to the silicon photonic process flow) with the advantages of die-to-wafer bonding (high throughput integration, easy incorporation of two-port optical devices such as SOAs and modulators). The schematic of the integration approach is shown in Fig. 1.

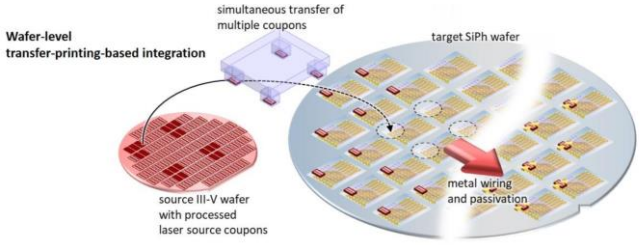

Fig. 1 Transfer printing process: overview of the transfer printing approach to populate a 200 mm/300 mm SOI photonic wafer with III-V components prefabricated on the III-V source wafer.

The process starts with the realization of the III-V opto-electronic component (in this paper semiconductor optical amplifiers) in a dense array on the III-V source wafer. As shown in Fig. 2, this is realized by incorporating III-V release layer (InGaAs or InAlAs) underneath the III-V device layer stack. After fabrication of the III-V opto-electronic components, the release layer is patterned and the devices are encapsulated with a dielectric material. By defining openings in that dielectric encapsulation the release layer can now be selectively etched (in the case of InGaAs or InAlAs using a $FeCl_3$:H_2O solution) leaving the III-V device free-standing on the III-V substrate, held in place using the photoresist tethers. Now the devices can be picked up using a poly-dimethyl-

siloxane (PDMS) stamp that is patterned to selectively pick a subset of III-V opto-electronic components from the III-V source substrate and print them on the silicon photonic target wafer. The printing can be realized using van der Waals forces (molecular bonding approach) or using an adhesive bonding layer (DVS-BCB in our case). Devices can be printed with high precision on the silicon photonic target wafer (better than +/-1.5 µm 3σ) through the use of pattern recognition. After the printing the encapsulation is removed and the devices are planarized and electrically connected to the surrounding circuit (not shown in Fig. 2).

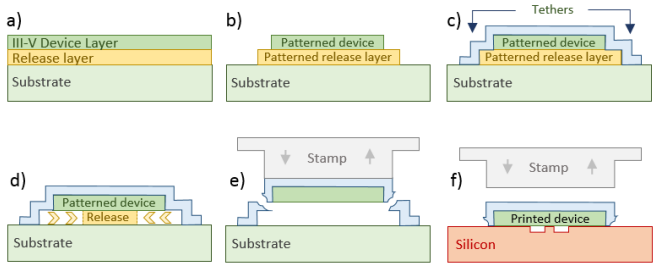

Fig. 2 Detail of the III-V source wafer preparation and transfer printing operation.

While we previously demonstrated this technique for the integration of III-V photodiodes on a silicon photonic integrated circuit [9], in this paper we demonstrate for the first time the realization of a III-V-on-silicon widely tunable laser realized using micro-transfer-printing, showcasing the power of this integration technique for incorporating III-V gain blocks on a silicon photonic circuit.

2. Tunable laser design

A schematic of the tunable laser design is shown in Fig. 3. It consists of a double-ring Vernier filter, with two micro-heaters (not shown in Fig. 3) for tuning of the laser wavelength, which forms the first mirror and a tunable broadband reflector as a second mirror (again the heaters used to tune this mirror are not shown for clarity). A (thermal) phase section to finetune the position of the longitudinal modes with respect to the Vernier filters is included as well. The III-V amplifier is micro-transfer printed to the silicon photonic IC using pre-defined alignment marks in the silicon device layer. The silicon waveguides are 400 nm thick (2 µm buried oxide layer thickness) and are etched 180 nm, after which they are planarized down to the silicon device layer using a SiO_2 chemical-mechanical polishing process. A DVS-BCB bonding layer with a thickness of less than 40 nm is used for the III-V integration. The silicon ring resonator structures have a radius of 25 µm and 27.5 µm, respectively, allowing to realize more than 40 nm tuning range. The loaded Q-factor of the ring resonators is approximately 34.5×10^3 and the drop port loss is 1.3 dB in the wavelength range of interest. The III-V epitaxial layer stack consists of 6 AlInGaAs quantum well active region sandwiched between a 260 nm thick n-InP layer and a 2 µm / 285 nm thick p-InP/p-InGaAs cladding layer. An adiabatic taper structure is defined on the III-V source substrate to allow for the broadband high-efficiency and alignment tolerant optical coupling between the silicon waveguide circuit and the III-V/Si optical amplifier. The taper structure is 200 µm long and starts from a taper tip of less than 0.6 µm to the amplifier mesa width of 4.5 µm.

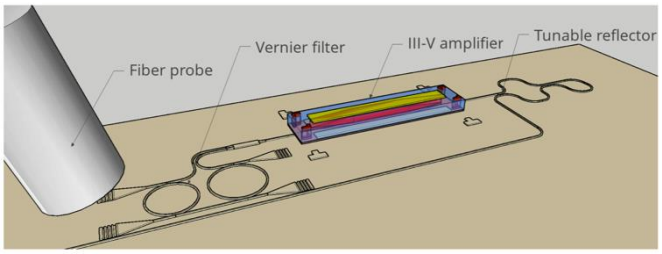

Fig. 3 Layout of the micro-transfer-printing-based widely tunable laser.

3 Tunable laser fabrication

The silicon photonic circuits to form the laser cavity were realized in imec's 200 mm pilot line. The processing consists of 193 nm deep-UV lithography, a 180 nm dry etch and SiO_2 deposition and planarization down to the silicon device layer. Then the wafer is diced and device integration is carried out on a die-level. A 1:4 diluted DVS-BCB:mesitylene solution is spin coated on the photonic circuits as an adhesive bonding agent to facilitate the micro-transfer-printing. The III-V process comprises the MOCVD epitaxial growth of the amplifier epi-layer stack on a release layer consisting of a 50 nm InGaAs to improve morphology of the n-doped InP and a 500 nm thick InAlAs release layer grown on the InP substrate. The III-V amplifiers are realized using standard III-V processing, using i-line contact lithography, a combination of dry and wet etching for the definition of the amplifier mesa and using a lift-off process for the Au-based metallization of the p- and n-contact. After device processing the devices are encapsulated using photoresist, which is patterned to locally expose the InAlAs release layer, which is subsequently selectively etched using $FeCl_3$:H_2O. This leaves the devices free-standing and anchored to the InP source substrate with the photoresist tethers. A picture of the III-V optical amplifiers on the III-V source wafer after etching the release layer is shown in Fig. 4, showing the III-V coupons with patterned amplifier, their metallization, the alignment markers incorporated to allow the subsequent alignment to the silicon photonic target wafer, the photoresist tethers and the patterned, underetched InAlAs layer. The III-V coupons measure 45 µm by 1255 µm, comprising 2 tapers of 200 µm and an amplifier waveguide of 760 µm. In a next step, the micro-transfer-printing operation is carried out. This is realized using an X-Celeprint micro-TP100 lab-scale printer, using a PDMS stamp with a post of 50 µm by 1400 µm, through which the device coupons are picked up, transferred above the silicon photonic target die, aligned using pattern recognition and printed. The whole printing cycle takes approximately 45 seconds. While in this first demonstrator a single SOA was transfer printed at a time, the technique can scale to several 10 s to 100 s of devices transferred in a single printing operation. Close to 100% transfer printing yield can be achieved by heating the target substrate to 70 °C. After transfer printing, the photoresist encapsulation is removed using O_2 plasma and the DVS-BCB is cured. Then devices are

planarized using DVS-BCB and electrically connected. At the same time also the Ti/Au heaters used for tuning the ring resonators and phase sections are processed. A microscope picture of an array of widely tunable lasers is shown in Fig. 5, showing on the left-hand side the micro-ring resonator filters and there thermal tuners, in the middle the transfer printed III-V SOAs and on the right-hand side the tunable reflector and phase section.

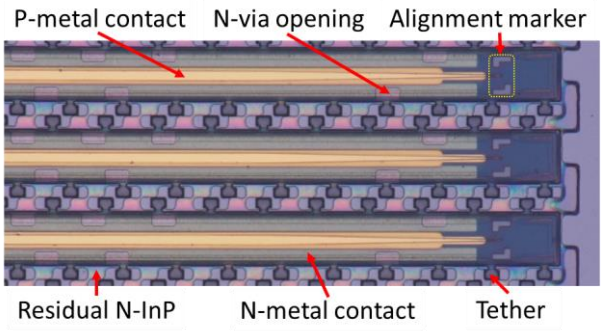

Fig. 4 III-V semiconductor optical amplifiers on the III-V source substrate after the release process.

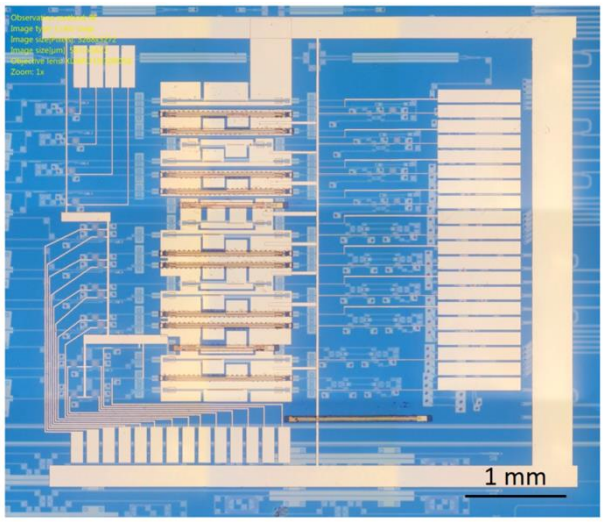

Fig. 5 Microscope image of the realized III-V-on-Silicon tunable laser array

4 Tunable laser characterization

The laser performance was characterized by mounting the sample on a temperature-controlled stage at 20 °C. The output is collected from one output port of the Vernier filter. The series resistance of the transfer-printed SOA is 15 Ω at a bias current of 110 mA. The threshold of the laser is 70 mA. By adjusting the power dissipated in the micro-heaters controlling the ring resonators a discrete tuning over 48 nm could be realized, as shown in Fig. 6(a). The waveguide-coupled output power varies between -1.8 dBm and 5.2 dBm over the entire tuning range. Fine tuning of the laser is realized by actuating both heaters of the ring resonator Vernier filter and the phase section simultaneously, as shown in Fig. 6(b). Linewidth measurements were carried out using a delayed self-heterodyne setup using a 200 MHz acousto-optic frequency shifter and a 5 km delay line. The linewidth is extracted by implementing a Voigt fitting to the frequency spectra of the beat notes. A minimum intrinsic linewidth (Lorentzian component) of 300 kHz is obtained at 1560 nm (center of the gain spectrum) and it remains below 1.5 MHz over the tuning range.

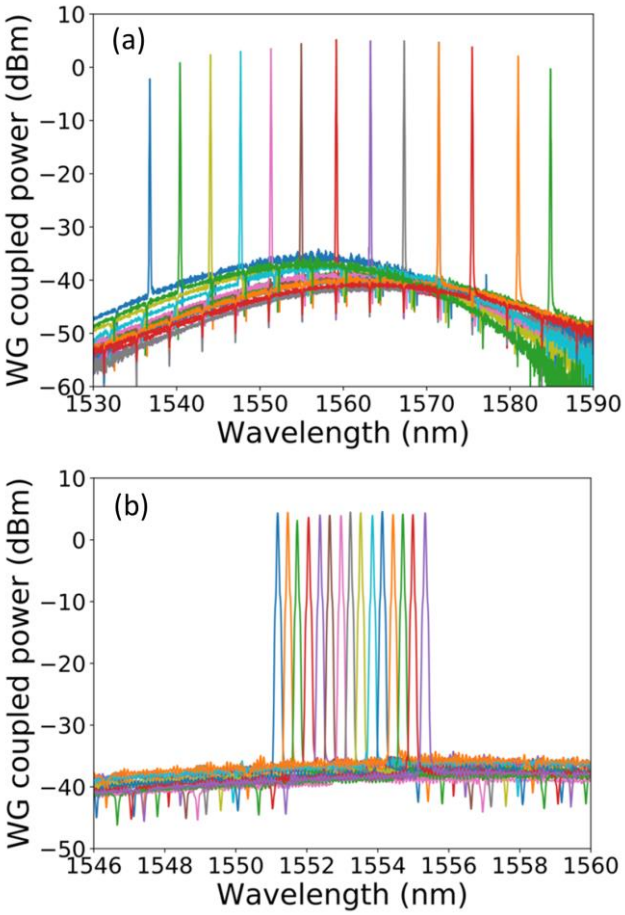

Fig. 6 Micro-transfer-printed III-V-on-silicon laser output characteristics: (a) coarse tuning (b) fine tuning.

5 Conclusion

In this paper we demonstrate for the first time the realization of a III-V-on-silicon widely tunable laser using the micro-transfer-printing of pre-fabricated III-V semiconductor optical amplifiers on a silicon waveguide circuit. We believe this integration approach combines the best aspects of flip-chip integration and die-to-wafer bonding and is therefore a very promising integration technique for the realization of III-V-on-silicon photonic integrated circuits in wafer scale.

6 Acknowledgements

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