APL Photonics

III-V-on-Si photonic integrated circuits realized using micro-transfer-printing

Cite as: APL Photonics 4, 110803 (2019); https://doi.org/10.1063/1.5120004
Submitted: 16 July 2019 . Accepted: 15 October 2019 . Published Online: 04 November 2019

Jing Zhang, Grigorij Muliuk, Joan Juvert, Sulakshna Kumari, Jeroen Goyvaerts, Bahawal Haq, Camiel Op de Beeck, Bart Kuyken, Geert Morthier, Dries Van Thourhout, Roel Baets, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Agnieszka Gocalinska, James O'Callaghan, Emanuele Pelucchi, Kevin Thomas, Brian Corbett, António José Trindade, and Gunther Roelkens

III-V-on-Si photonic integrated circuits realized using micro-transfer-printing

Cite as: APL Photon. 4, 110803 (2019); doi: 10.1063/1.5120004
Submitted: 16 July 2019 • Accepted: 15 October 2019 •
Published Online: 4 November 2019

Jing Zhang,[1,a)] Grigorij Muliuk,[1] Joan Juvert,[1] Sulakshna Kumari,[1] Jeroen Goyvaerts,[1] Bahawal Haq,[1] Camiel Op de Beeck,[1] Bart Kuyken,[1] Geert Morthier,[1] Dries Van Thourhout,[1] Roel Baets,[1] Guy Lepage,[2] Peter Verheyen,[2] Joris Van Campenhout,[2] Agnieszka Gocalinska,[3] James O'Callaghan,[3] Emanuele Pelucchi,[3] Kevin Thomas,[3] Brian Corbett,[3] António José Trindade,[4] and Gunther Roelkens[1]

AFFILIATIONS

[1]Ghent University—imec, Technologiepark-Zwijnaarde 126, 9052 Ghent, Belgium
[2]imec, Kapeldreef 75, 3001 Heverlee, Belgium
[3]Tyndall National Institute, University College Cork, Cork, Ireland
[4]X-Celeprint Limited, Cork, Ireland

Note: This article is part of the Special Topic on Hybrid Integration beyond Silicon Photonics.
[a)]jingzhan.Zhang@ugent.be

ABSTRACT

Silicon photonics (SiPh) enables compact photonic integrated circuits (PICs), showing superior performance for a wide variety of applications. Various optical functions have been demonstrated on this platform that allows for complex and powerful PICs. Nevertheless, laser source integration technologies are not yet as mature, hampering the further cost reduction of the eventual Si photonic systems-on-chip and impeding the expansion of this platform to a broader range of applications. Here, we discuss a promising technology, micro-transfer-printing (μTP), for the realization of III-V-on-Si PICs. By employing a polydimethylsiloxane elastomeric stamp, the integration of III-V devices can be realized in a massively parallel manner on a wafer without substantial modifications to the SiPh process flow, leading to a significant cost reduction of the resulting III-V-on-Si PICs. This paper summarizes some of the recent developments in the use of μTP technology for realizing the integration of III-V photodiodes and lasers on Si PICs.

I. INTRODUCTION

Silicon photonics (SiPh) is emerging as a promising platform for building complex and powerful photonic integrated circuits (PICs). Its high index contrast not only allows for ultracompact PICs but also results in an enhanced light-matter interaction enabling efficient active devices such as high speed modulators. The inherent advantage of complementary metal-oxide-semiconductor (CMOS) compatibility of SiPh processes allows for scalable and low-cost production of PICs on 200 mm or 300 mm wafers. Nevertheless, the complicated assembly of light sources with Si PICs leads eventually to a high product cost, impeding the use of Si PICs in a wider range of applications.

In the past years, great effort has been devoted to establishing a mature technology for realizing the cost-effective integration of III-V-on-Si lasers and other noninherent functionalities on Si PICs. Different approaches have been followed. Among the existing methods, the monolithic integration of III-V semiconductors on a Si substrate through heteroepitaxial growth is the ultimate integration approach.[1,2] However promising, this is still at an early stage, with much work to be done on the integration of these process modules in the SiPh process flow and demonstrating the reliability and performance of the resulting devices. From the hybrid integration approaches, flip-chip integration is mostly adopted in industry. This approach allows us to use the superior characteristics of readily fabricated devices such as III-V semiconductor lasers, amplifiers, and photodetectors (PDs) and allows for pretesting before assembly, enhancing the compound yield. The high alignment accuracy required in the flip-chip assembly process[3–6] makes it difficult, however, to scale up and reduce the cost of resulting PICs.

TABLE I. A comparison of different III-V-on-Si wafer-level heterogeneous integration approaches.

Technology	Integration density	CMOS compatibility	Efficiency of III-V material use	Alignment accuracy	Throughput	Cost	Maturity
Flip-chip	Low	Back-end compatible	Medium	Medium	Low	High	Mature
Heterogeneous bonding	Medium	Back-end compatible	Medium	High	High	Medium	Mature
μTP	High	Back-end compatible	High	Medium	High	Low	R&D
Epitaxial growth	High	Potentially front-end compatible	Very high	High	High	Low	R&D

Heterogeneous integration through die-to-wafer or wafer-to-wafer bonding has attracted a lot of attention in recent years to overcome this issue, as in this case the critical alignment of the III-V structure to the Si waveguide circuit is realized using wafer-scale lithographic processes. Some foundries are developing a CMOS process flow for the wafer-scale realization of III-V-on-Si PICs, where III-V dies are first distributed on a temporary carrier, e.g., a Si wafer, by a pick-and-place method and then integrated on the target SiPh wafer (after its front end processing) through wafer bonding, followed by a back-end process flow for the definition of the III-V structures and the back-end metallization stack.[7–9] In this case, the back-end process flow has to be modified to accommodate the III-V devices. In addition, the compound yield can be affected, as the III-V devices can only be tested after they have been integrated on the SiPh wafer. The simultaneous integration of different III-V materials/devices on a common substrate, while possible,[10] is also still challenging.

Micro-transfer-printing (μTP) is a novel integration technique developed by the Rogers group at the University of Illinois in 2004.[11,12] This technique allows for the manipulation of micrometer-sized thin films/thin film devices and enables the transfer of these thin film devices in a massively parallel manner (ensuring high throughput integration, as a single printing cycle only takes 30–45 s) from a source substrate to a target substrate with high alignment accuracy. By using this approach, the efficiency of the use of source materials can be significantly improved and different materials/devices can be intimately integrated on a common substrate. Moreover, this integration requires no modification of the SiPh back-end process flow, except for a local back-end opening where the devices need to be integrated. Similar to the flip-chip-like assembly, μTP allows for prefabrication and pretesting of the devices on its native substrate prior to their integration on a target Si PIC wafer. The technique in principle also provides the possibility of the reuse of the III-V substrate, which can again lead to a cost reduction. A comparison of the pros and cons of these aforementioned approaches is summarized in Table I. In this paper, we review our recent results on the heterogeneous integration of III-V lasers and photodiodes on Si PICs through the μTP approach. Other groups have activities along similar lines.[13–16]

II. CONCEPT OF THE μTP TECHNIQUE

The μTP process is schematically illustrated in Fig. 1.[17] A polydimethylsiloxane (PDMS) stamp with a post array (or a single post) whose size and pitch match those of the device array arranged on the source wafer is used to pick up and transfer these devices onto a target wafer. The stamp is fabricated through casting PDMS on a Si master mold and after releasing, laminating it on a glass carrier wafer. Over 300 000 printing cycles[18] have been demonstrated with such stamps. The release of the prefabricated devices from their native substrate is enabled by incorporating a sacrificial layer in the epitaxial layer stack between the device layer and the substrate, which can be selectively etched. As indicated in Fig. 1(b), devices are patterned on the III-V source wafer and are protected with an encapsulation layer (typically a photoresist layer in the case of III-V devices) with local openings to access the release layer, which is then underetched (using $FeCl_3$:H_2O in the case of InP-based epitaxy), leaving the released devices or material coupons anchored

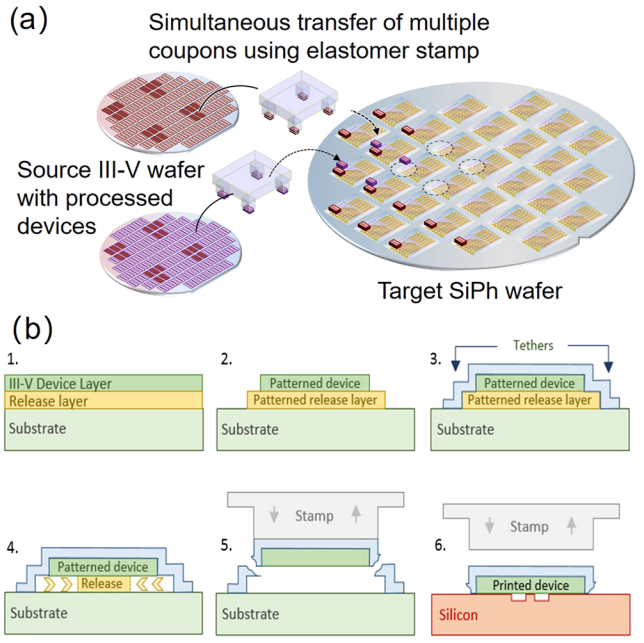

FIG. 1. Concept of μTP. (a) Schematic of μTP-based integration on 200 mm or 300 mm Si photonic wafers in a parallel manner and (b) prefabrication of III-V devices on their native substrate and the μTP integration sequence. Reproduced with permission from Roelkens *et al.*, in *2018 IEEE Optical Interconnects Conference (OI)* (IEEE, USA, 2018), pp. 13–14. Copyright 2011 IEEE.

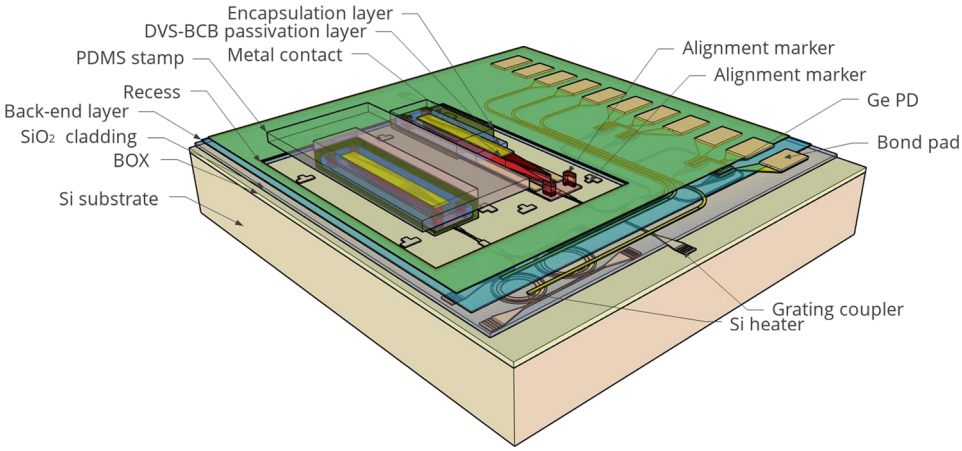

FIG. 2. An example of the integration of III-V-on-Si lasers on a complex Si PIC, only requiring a local opening of the back-end stack and a postprinting electrical connection between the III-V optoelectronic device and the Si PIC.

to the substrate by the tether structures while retaining registration. An example of a complex PIC that can be realized using this approach is schematically shown in Fig. 2, where two III-V-on-Si tunable lasers are cointegrated with microheaters and germanium (Ge) PDs by μTP of prefabricated III-V amplifier structures in a recess that was defined on the Si PIC.

The pick-up and printing operation are enabled by setting the peeling velocity of the stamp, due to the rate-dependent adhesion strength of the device(s) to the stamp.[19] In the pick-up step, the PDMS stamp is first aligned and laminated to the desired devices on the source wafer and is then pulled back at a high velocity. This results in a relatively high adhesion strength of the devices to the stamp, thereby breaking the tethers and attaching the devices to the stamp. The devices are then aligned to and automatically printed on the target wafer by laminating the stamp to the target wafer and slowly retracting the stamp. This results in a low adhesion strength between the devices and the stamp and leaves the device attached to the SiPh target wafer (either using van der Waals forces[20] or with an adhesive bonding agent[21]) together with the encapsulation layer. The alignment is enabled by locating the center of the codesigned fiducial marks on both the source device and target substrate—as seen through the transparent PDMS stamp—through a pattern recognition function. This way ±1.5 μm (3σ) alignment accuracy is achieved when printing devices in large arrays. We have observed in our experiments that better alignment accuracy can be achieved by reducing the size of the array. If deep submicron alignment accuracy is required one can make a compromise by μTP material coupons on the target substrate, followed by a contact UV lithography process,[22] similar to what is done in die-to-wafer bonding approaches. The final processing steps on the Si target wafer consist of removing the encapsulation, passivating the device, and electrically connecting the III-V optoelectronic components to the rest of the PIC.

III. μTP OF III-V PHOTODIODES ON Si PICs

High-performance PDs are essential elements in Si PICs. Different Ge PD structures with low dark current, high responsivity, high avalanche gain, and high bandwidth have been demonstrated. Nevertheless, in specific applications which, for example, require wavelength duplexing or polarization-independent optical detection or which are to operate outside the classical telecommunication wavelength window, III-V semiconductor photodiodes are required. As an example, a transceiver for Point-to-Point Fiber-To-The-Home (PtP FTTH) optical networks at the central office side is demonstrated. In this transceiver, an O-band III-V PD that was proposed for the reception of the O-band upstream data signal in a polarization-independent way was integrated on a SiPh fiber-to-chip grating coupler. Duplexing of the upstream (1310 nm O-band) and downstream (1550 nm C-band) signals is realized by choosing the cut-off wavelength of the III-V photodiode to be 1.37 μm.[23] Here, the μTP technique is used for the integration of such O-band III-V PDs on a SiPh platform for realizing a 4-channel PtP FTTH transceiver. The concept of the transceiver is schematically illustrated in Fig. 3, where microring modulators are used to imprint the downstream signal on the C-band optical carrier.

The epitaxial layer stack used in this demonstration consists of a 1 μm thick intrinsic InGaAsP absorbing layer with a cut-off wavelength of 1.37 μm sandwiched between p-doped and n-doped InP cladding layers. In addition, a 1 μm thick InGaAs layer was grown between the device layer stack and the InP substrate to enable releasing the prefabricated PDs. Figure 4(a) depicts the III-V source wafer

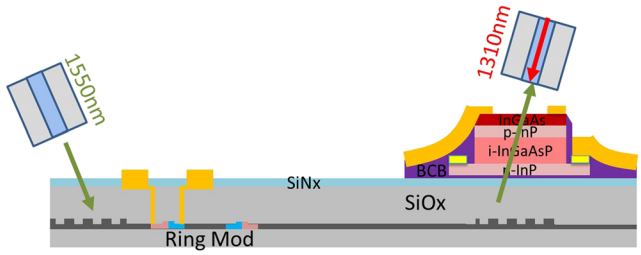

FIG. 3. Schematic cross section of a III-V-on-silicon full duplex transceiver using a III-V photodiode that detects O-band signals and is transparent for C-band signals. Reproduced with permission from Zhang *et al.*, Opt. Express **25**(13), 14290–14299 (2017). Copyright 2017 The Optical Society.

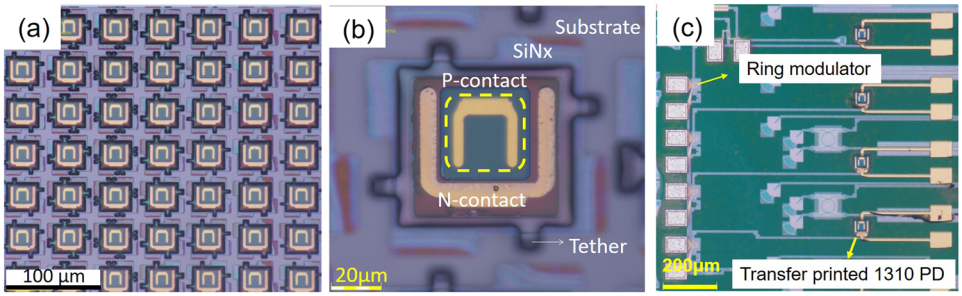

FIG. 4. The PDs before and after the μTP process. (a) Microscopic image of a prefabricated PD array on the III-V source wafer. (b) A zoomed-in image of one PD on the source wafer showing the design of the tether structures. (c) Final realized 4-channel transceiver with post-processed metal connections. Reproduced with permission from Zhang *et al.*, Opt. Express **25**(13), 14290–14299 (2017). Copyright 2017 The Optical Society.

with a dense square array of PDs with pitch of 100 μm. Figure 4(b) shows a zoomed-in image of a single device on the source wafer where the PD mesa is 40 × 30 μm^2, and the overall footprint of the device is around 65 × 65 μm^2. A U-shaped P-type metal contact was deposited on the top of the mesa, leaving a 17 μm wide aperture for the reception of the upstream and the transmission of the downstream signal from and to the same fiber, respectively. The fabricated O-band PD was released by etching the InGaAs sacrificial layer in an aqueous $FeCl_3$ solution (1 g:2 ml $FeCl_3$:H_2O) for 100 min at 5 °C. A detailed description of the fabrication process can be found in Ref. 24. In the printing step, the U-shape P-type metal contact and grating coupler itself were used as fiducial markers for the alignment by the pattern recognition software. Figure 4(c) shows the final realized 4-channel transceiver array. The responsivity of the integrated PDs for the O-band signal was measured to be 0.39–0.46 A/W, which is four orders of magnitude higher than that for the C-band signal, enabling the duplexing of both signals without substantial cross talk. 10 Gbps operation was successfully demonstrated for both up- and downstream data signals. A similar concept was also implemented for a C-band SiPh 4-wavelength channel receiver as shown in Fig. 5. In this case, a 1 μm thick intrinsic InGaAs layer instead of the InGaAsP layer is used for the C-band signal detection, while the rest of the layer stack remained the same. This receiver achieved 25 Gbps operation.[25] Moreover, parallel μTP using a stamp with 4 posts was demonstrated, resulting in a device printing yield of 98.8% (83 over 84 printed devices).[26] The resulting PIC with integrated PD array is shown in Fig. 6. Uniform performance was observed in the characterization, where, for example, the PDs integrated on 1D grating couplers show a waveguide-referred responsivity of 0.553 A/W at 1570 nm with a standard deviation of 0.033 A/W. Other than these classic III-V photodiodes, GaAs metal-semiconductor-metal (MSM) PDs and Ge PDs were also successfully integrated on a target wafer of interest (comprising passive SiN and Si waveguide circuits, respectively).[27,28]

IV. μTP INTEGRATION OF ETCHED-FACET LASERS ON Si PICs

Several different approaches are currently being considered for the integration of laser sources on SiPh PICs through μTP. One approach that is similar to the coupling scheme used for flip-chip integration is shown in Fig. 7, where a prefabricated etched-facet Fabry-Pérot laser is transfer-printed into a predefined recess on the SiPh target wafer with the bottom of the trench reaching the Si substrate. By properly designing the III-V epitaxial stack and the dimensions of the laser waveguide cross section, the laser output directly couples to the Si PIC through a codesigned spot-size-converter defined in the 220 nm thick Si device layer.[29] The III-V epitaxial layer stack used for this demonstration consists of 4 InGaAsP quantum well/barrier pairs (6 nm/12 nm) sandwiched between two 50 nm

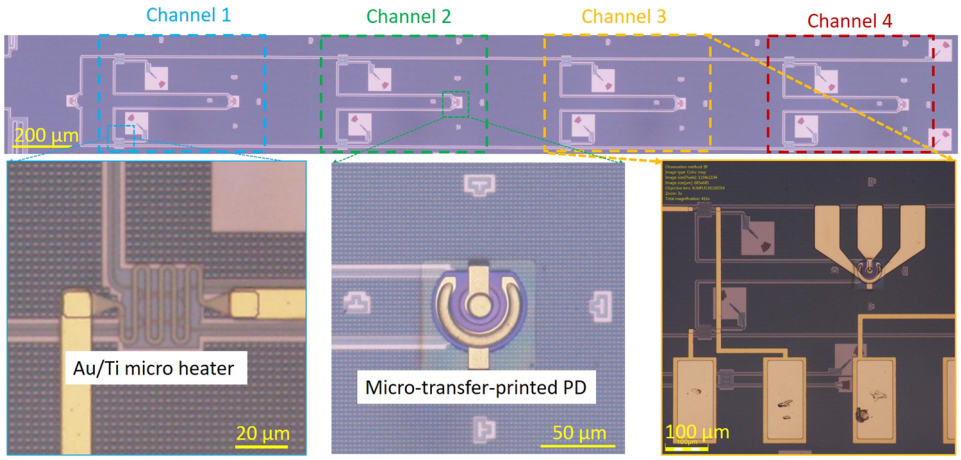

FIG. 5. Microscope image of the passive 4-channel polarization multiplexed receiver circuit with a zoomed-in view of a tunable ring filter, a PD transfer-printed on a 2D fiber grating coupler and the third channel of the receiver after the PDs have been integrated.

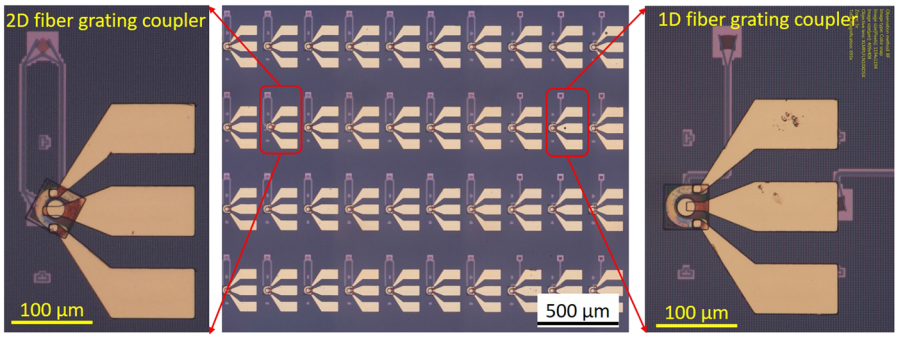

FIG. 6. Microscope image of the µTP C-band III-V PD arrays (with 40 out of 84 devices shown in this image) after the metallization process, showing well-aligned printing on both the 2D and 1D fiber grating couplers. The only failed device showed a rotation of the PD during the printing.

thick InGaAsP separate confinement heterostructure layers. A so-called Si trident taper structure which, as shown in Fig. 7, effectively expands the mode size in the lateral dimension is used to interface with the laser. A 1950 nm thick *n*-InP cladding layer and 100 nm undoped InP layer are used to level the III-V active region with the Si device layer. A 500 nm thick InGaAs sacrificial layer is incorporated beneath the InP bottom cladding layer to release the prefabricated devices.

As the laser cavity has to be formed on the III-V source wafer by etching the facets, a dry etch process was used in the laser definition to have a smooth and vertical sidewall. A gold deposition on the etched rear facet was used to enhance the reflectivity. The footprint of the coupon is $50 \times 400\ \mu m^2$. Note that the etching of the InGaAs release layer in a $FeCl_3$ aqueous solution is anisotropic.[30] Therefore, to accelerate the undercut and obtain a flat bottom surface (given the finite selectivity in etching InGaAs with respect to InP), the coupons are usually arranged at a 45° or 135° angle with respect to the cleave directions of the III-V wafer. Otherwise, a pyramid-shape bottom surface will be formed after the long release etch, as shown in Fig. 8, hampering the printing on the flat Si substrate.

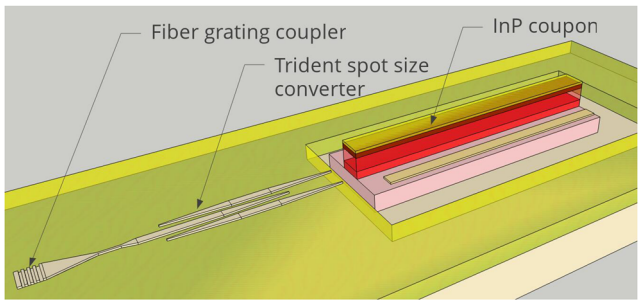

FIG. 7. Schematic of the µTP etched-facet Fabry-Pérot laser integrated in a recess on a Si PIC.

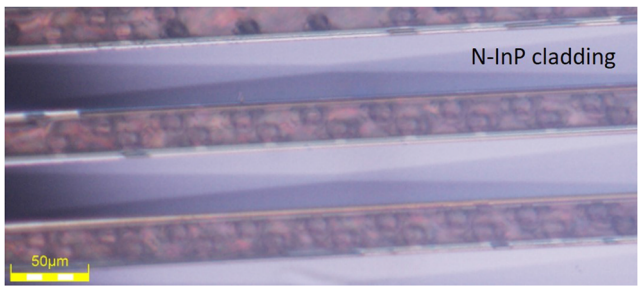

FIG. 8. Microscope image of the bottom surface of released coupons with its long side perpendicular to the major flat of the wafer, showing a pyramid-shape, related to the long anisotropic underetch and the finite selectivity of etching between InGaAs and InP.

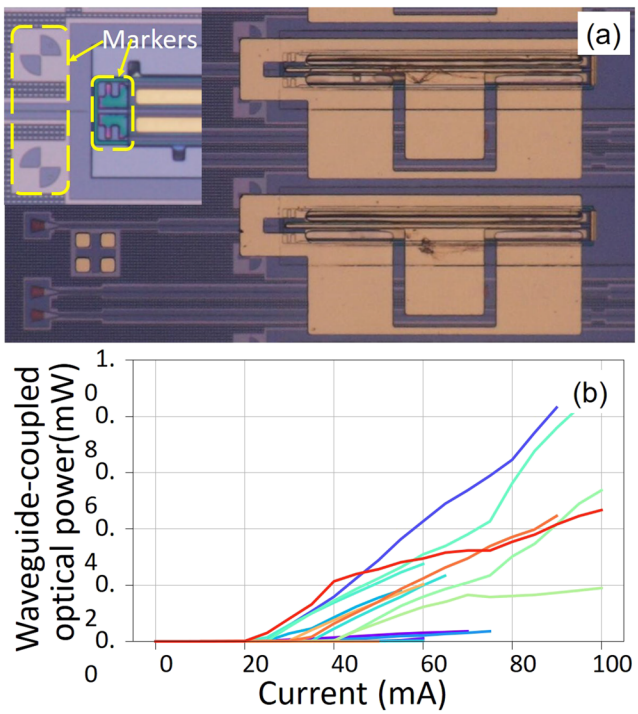

FIG. 9. Microscope image of the fabricated devices (after postprocessing the electrical contacts on the target wafer) with an inset (zoomed-in image) showing the codesigned alignment marks on both target SOI wafer and source coupon. (b) Measured waveguide-coupled power at 20 °C. Reproduced with permission from Juvert *et al.*, Opt. Express **26**(17), 21443–21454 (2018). Copyright 2018 The Optical Society.

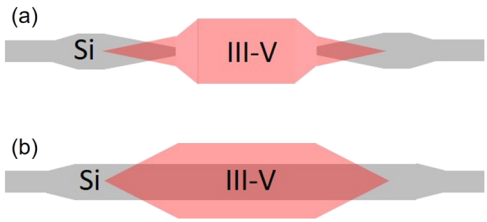

FIG. 10. Schematics of (a) the proposed alignment-tolerant adiabatic taper structure and (b) the classic piecewise linear taper structure.

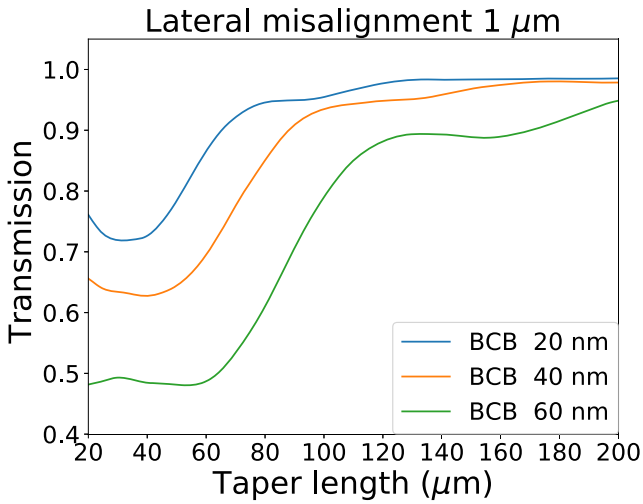

FIG. 11. Simulated coupling efficiency (1.55 μm—TE polarization) as a function of the taper length for a taper structure with 1 μm lateral misalignment.

In this proof-of-concept demonstration, the devices were printed one by one onto the target SiPh chip without using an adhesive bonding agent. The direct attachment of the III-V device to the Si substrate provides an enhanced thermal dissipation due to the high thermal conductivity of Si.[31] Figure 9(a) shows a microscope image of the resulting PIC with integrated lasers,[29] where the inset depicts the codesigned marks on the III-V laser coupons and the Si photonic target wafer used for the alignment through pattern recognition. 17 out of 20 devices were printed on the target

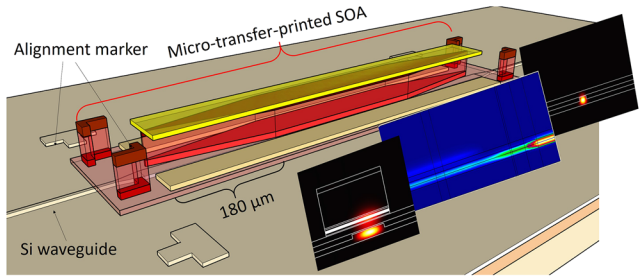

FIG. 12. Mode propagation through the 180 μm long taper structure with a 20 nm thick BCB bonding layer.

PIC with a resulting absolute alignment accuracy within 1 μm. All of the integrated lasers exhibited lasing and milliwatt-level waveguide-coupled optical power was successfully demonstrated, as shown in Fig. 9(b). However, the spread on the laser characteristics shows that there is still room for improvement in the laser and coupling uniformity.

V. μTP INTEGRATION OF III-V-ON-Si EVANESCENT LASER STRUCTURES

A. Alignment-tolerant adiabatic taper structure

An alternative option for laser realization is evanescent coupling of the III-V gain waveguide to the Si waveguide circuit using an adiabatic taper structure. This, however, typically requires thicker Si waveguides (400 nm or above) in order to achieve the phase match condition and thus allows for an efficient mode conversion between the III-V/Si and Si waveguide. Here, a waveguide platform consisting of a 400 nm thick crystalline Si device layer on a 2 μm thick buried oxide layer is used. The waveguide circuits are defined by a single 180 nm etch step using dry etching and planarized using a SiO_2 chemical mechanical polishing process down to the Si device layer. The linear III-V/Si taper structures that have been widely used in evanescently coupled III-V-on-Si devices realized through die-to-wafer bonding require a stringent alignment accuracy (typically less than 300 nm), however.[32] In order to accommodate the alignment accuracy provided by the μTP system, we designed a coupling taper structure that can tolerate up to 1 μm lateral misalignment. Figure 10 schematically illustrates the difference between

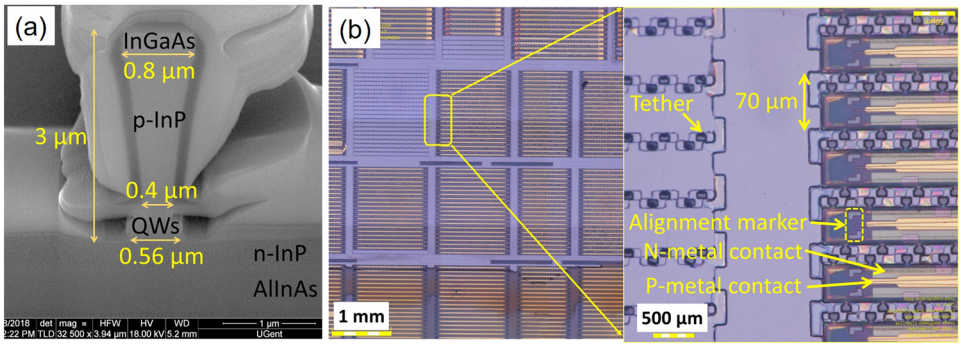

FIG. 13. (a) Focused ion beam cross section image near the III-V taper tip, showing a 560 nm wide active region. (b) Microscope image of the prefabricated SOA array on its native InP substrate.

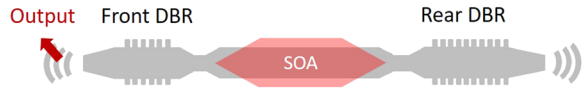

FIG. 14. Schematic of the III-V-on-Si DBR laser based on a micro-transfer-printed prefabricated SOA.

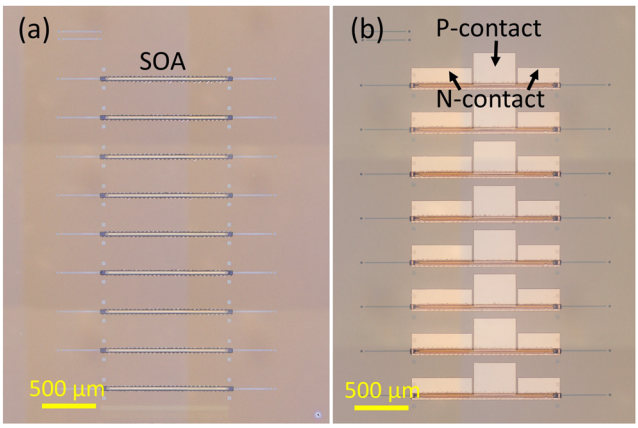

FIG. 15. Microscope image of a target Si PIC with an array of micro-transfer-printed prefabricated SOAs, (a) prior to and (b) after the metallization.

the new alignment-tolerant III-V-on-Si taper structure and the classic design. The hybrid waveguide section consists of a 4.5 μm wide III-V waveguide and an underlying 2.5 μm wide Si waveguide with a thin benzocyclobutene (BCB) bonding layer. The use of such a wide Si waveguide results in a strong confinement of the mode in the Si. In this way, the disturbance to the guided optical mode induced by any misalignment of the III-V taper structure is significantly reduced, at the expense of a reduced confinement in the III-V active region (1.43% per quantum well in the traditional taper structure vs 0.75% per quantum well in the alignment tolerant scheme). The optical mode in the III-V/Si taper is converted to the fundamental mode in the underlying Si waveguide through a linear III-V taper structure. Then, the broad Si waveguide is narrowed down and connected to a 650 nm wide single TE mode waveguide. The structure also shows potential for high saturation power semiconductor optical amplifiers (SOA) due to the reduced confinement in the active region.[33,34]

Figure 11 shows the calculated coupling efficiency (TE polarization—1.55 μm wavelength) as a function of the length of the III-V taper structure for different BCB bonding thicknesses with a given lateral misalignment of 1 μm. The III-V taper tip width was set to be 400 nm, while it was found by simulation that even an 800 nm wide taper allows for complete mode conversion. The length of the linear III-V taper structure was set to be 180 μm to enable a highly alignment-tolerant and process-variation-tolerant coupling.

Figure 12 shows the optical mode conversion over the taper structure, where the lateral displacement is set to be 1 μm. The III-V taper tip is 400 nm wide, the III-V taper structure is 180 μm long, and the BCB bonding layer is 20 nm. As expected, the hybrid mode converts to the fundamental Si mode along the taper structure.

B. Prefabrication of μTP-compatible SOAs on their III-V substrate

The III-V epitaxial layer stack used for the integration of C-band SOAs/lasers consists of a 60 nm/200 nm intrinsic InP/*n*-InP bottom cladding, a 6 quantum well AlInGaAs active region and a 2 μm/285 nm thick *p*-InP/*p*-InGaAs top cladding. As demonstrated in Ref. 35, InAlAs is more suitable for use as the release layer. It provides a higher etch rate, an improved selectivity to InP, and an isotropic etching behavior in $FeCl_3$ based etchants, and a 500 nm thick layer is adopted for the release of the devices. The definition of the SOA follows the standard processing steps that were developed for the heterogeneous integration of III-V-on-Si devices based on die-to-wafer bonding. In order to obtain a "V" shape mesa cross section and thus a narrow taper tip, an HCl-based wet etching of the *p*-InP was used and the taper structure was oriented along the [011] crystal axis.[22] Figure 13(a) shows the resulting 'V' shape InP mesa with a 400 nm wide bottom at the taper tip. To enable autoalignment in the μTP through pattern recognition, a pair of "L"-shaped fiducial marks was defined at the coupon ends during the *p*-InP mesa definition. The release was performed in a 3 °C aqueous $FeCl_3$ solution, and it took about 80 min due to the high etch rate of InAlAs. Figure 13(b) shows a microscope image of the released III-V SOA array on the source wafer.

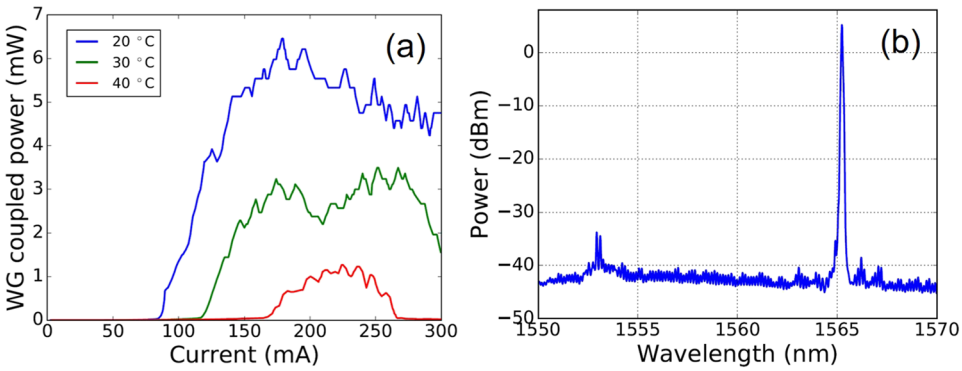

FIG. 16. Performance of the fabricated DBR lasers. (a) P-I curve at different temperatures. (b) Representative DBR laser spectrum.

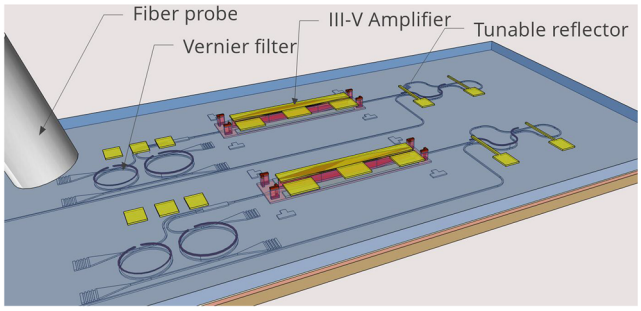

FIG. 17. Schematic of the μTP-based III-V-on-Si widely tunable laser.

C. μTP integration of III-V-on-Si DBR lasers

Distributed Bragg Reflector (DBR) lasers are demonstrated using the proposed tapered III-V SOA structure. The schematic layout of the DBR laser is illustrated in Fig. 14. The waveguide circuits were fabricated using an e-beam lithography process and a 180 nm single etch step into the 400 nm thick Si device layer. SOAs with an overall length of 1360 μm, including the taper structures, were micro-transfer-printed on the target PIC using a 20 nm thick BCB bonding layer. The laser cavity is 1800 μm long, formed by a pair of sidewall-corrugated DBRs[36] (period 247 nm, 900 periods, and 600 periods for the rear and front DBR, respectively). All of the coupons were successfully printed on the target PIC, as shown in Fig. 15(a), followed by final metallization through a standard lift-off process. The series resistance of the fabricated devices is about 6 Ω. A waveguide-coupled power over 5 mW is obtained at 20 °C, as shown in the Power vs Current (P-I) measurement in Fig. 16(a). The laser spectrum recorded at a bias current 290 mA is illustrated in Fig. 16(b), showing up to 40 dB side mode suppression ratio.

D. μTP integration of widely tunable III-V-on-Si lasers

In our earlier work, III-V-on-Si widely tunable lasers have been demonstrated on a 400 nm SiPh platform through die-two-wafer bonding technology,[37] in which case the optical mode was fully transferred from the Si device layer to the III-V amplifier. The laser exhibited a 40 nm tuning range in the L-band and milliwatt-level waveguide-coupled output power. To facilitate the μTP-based integration of such a widely tunable laser, a 2 μm wide waveguide is now incorporated underneath the amplifier. As discussed above, this relaxes the alignment requirements at the expense of a reduced confinement of the optical mode in the gain region. The laser has a 1.16 mm long linear gain region, as depicted in Fig. 17 along with two mirrors consisting of a tunable double-ring Vernier filter and a broadband tunable reflector (implemented using a Mach-Zehnder

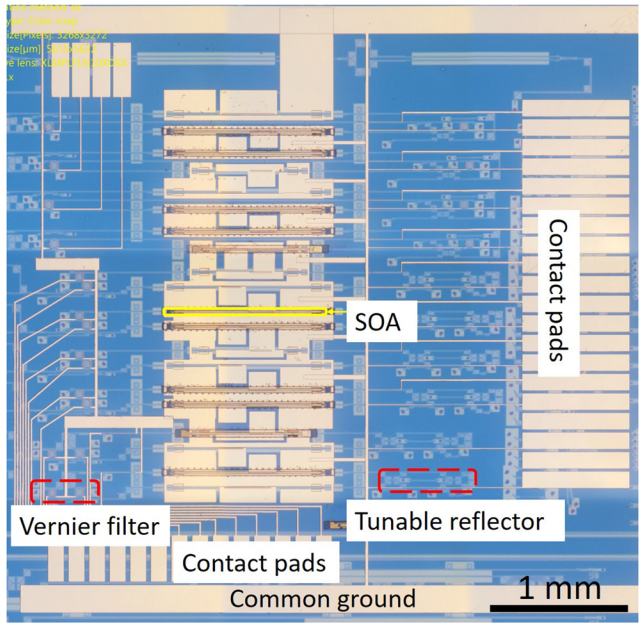

FIG. 19. Microscope image of the fabricated devices after the final metallization process.

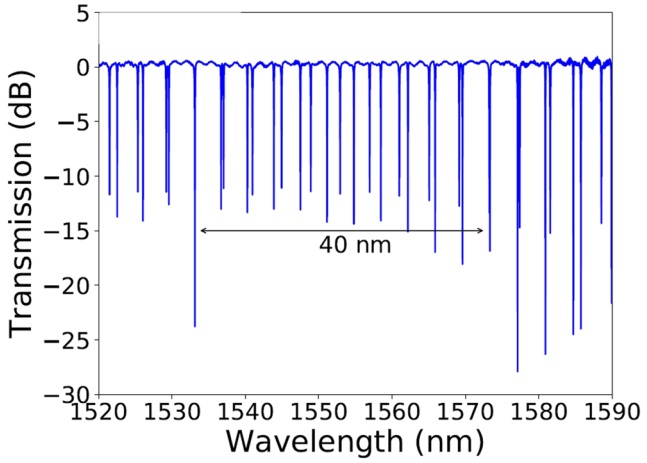

FIG. 18. Transmission of a cascade of two ring resonators with 25 μm and 27.5 μm radius, respectively, showing a combined FSR of about 40 nm.

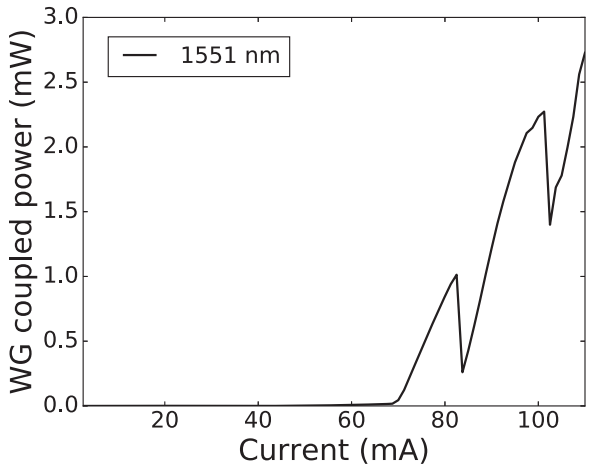

FIG. 20. P-I curve of the fabricated tunable laser.

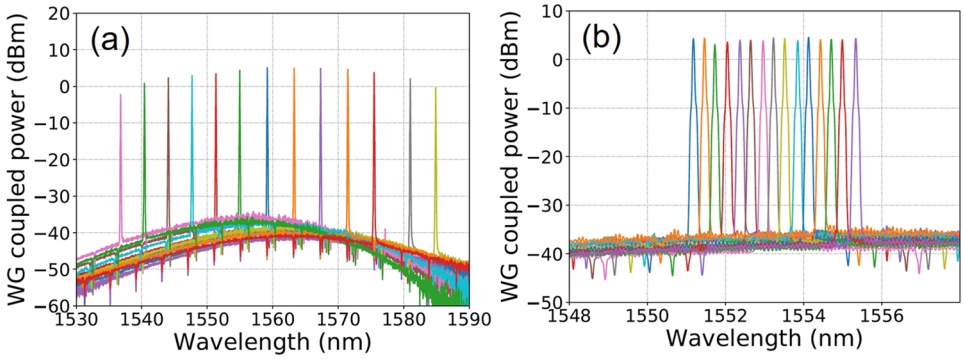

FIG. 21. Tuning behavior of the fabricated widely tunable laser. (a) Discrete wavelength tuning over a range of 48 nm by tuning one ring resonator. (b) Fine wavelength tuning filling the FSR of the ring resonator by tuning both ring resonators together.

interferometer and a loop mirror). Microheaters (not shown in the schematic) are integrated post transfer-printing on the ring resonators, the phase section, and the tunable reflector for laser tuning purposes. The overall cavity length is about 3.2 mm long, which results in a longitudinal mode spacing around 60 pm at a resonance of the Vernier filter. The ring resonators have a radius of 25 μm and 27.5 μm, respectively, leading to a combined Vernier FSR over 40 nm in the 1560 nm wavelength range, as a transmission spectrum through the Vernier filter shows in Fig. 18. The gap between the bus waveguide and the ring resonator waveguide (both are 650 nm wide) is 400 nm, which results in a loaded Q-factor of 34.5×10^3 and a drop port loss of 1.3 dB. In the fabrication, 1160 μm long SOAs (including a pair of 180 μm long taper structures and a 800 μm straight SOA waveguide section) were micro-transfer-printed to form the active region of the laser cavity using a 40 nm BCB bonding layer. Figure 19 shows an array of tunable lasers after postprocessing. The series resistance of the micro-transfer-printed SOAs is 15 Ω. A representative P-I curve obtained at 20 °C is shown in Fig. 20, which reveals a threshold of 70 mA and waveguide-coupled output power over 2 mW at a bias current of 110 mA. The abrupt changes in the output power are attributed to mode hops in the laser emission during bias current tuning, as is typical in a long laser cavity. This can be overcome by introducing a phase section in the laser cavity. A wide wavelength tuning over 48 nm is achieved by adjusting the thermal dissipation in the microheaters, as the recorded spectra in Fig. 21 illustrate.

VI. CONCLUSION

μTP is a powerful approach to integrate a variety of optoelectronic components, realized in dense arrays on a III-V source wafers, on SiPh target wafers. Devices include essential III-V SOAs, lasers, and photodiodes enabling advanced Si PICs. The technique is very well suited to massively parallel integration of these devices. In fact, nearly every material system/device that can be released from the substrate on which it was fabricated can be μTP. This creates opportunities for efficiently integrating other optical functions such as optical isolators, electro-optic modulators, and even electronic driver circuits (when realized on an SOI substrate) on the Si photonic platform. It can enable more complex PICs in nontelecom wavelength ranges such as the visible (VIS), near-infrared (NIR), and the mid-infrared (MIR), based on passive Si waveguide platforms such as SiN (VIS/NIR) and Ge-based (MIR) waveguide circuits and different III-V semiconductor technologies for light generation, modulation, and detection. The demonstrations presented in this paper are mostly based on the transfer printing of individual devices on target photonic dies. In order to introduce this technology to industry, wafer-level integration in a massively parallel way has to be investigated.

ACKNOWLEDGMENTS

This work was supported by the Methusalem funding of the Flemish Government, by the H2020 projects TOPHIT, TeraBoard and CALADAN, the ECSEL project MicroPrince, the INTERREG France-Wallonia-Flanders project SAFESIDE, and by the Irish Photonic Integration Centre.

REFERENCES

[1] Q. Li and K. M. Lau, "Epitaxial growth of highly mismatched III-V materials on (001) silicon for electronics and optoelectronics," Prog. Cryst. Growth Charact. Mater. **63**, 105–120 (2017).

[2] J. C. Norman, D. Jung, Z. Zhang, Y. Wan, S. Liu, C. Shang, R. W. Herrick, W. W. Chow, A. C. Gossard, and J. E. Bowers, "A review of high-performance quantum dot lasers on silicon," IEEE J. Quantum Electron. **55**, 1–11 (2019).

[3] H. Lu, J. S. Lee, Y. Zhao, C. Scarcella, P. Cardile, A. Daly, M. Ortsiefer, L. Carroll, and P. O'Brien, "Flip-chip integration of tilted VCSELs onto a silicon photonic integrated circuit," Opt. Express **24**, 16258 (2016).

[4] A. Moscoso-Mártir, F. Merget, J. Mueller, J. Hauck, S. Romero-García, B. Shen, F. Lelarge, R. Brenot, A. Garreau, E. Mentovich, A. Sandomirsky, A. Badihi, D. E. Rasmussen, R. Setter, and J. Witzens, "Hybrid silicon photonics flip-chip laser integration with vertical self-alignment," in *2017 Conference on Lasers and Electro-Optics Pacific Rim* (Optical Society of America, 2017), p. s2069.

[5] S. Tanaka, S.-H. Jeong, S. Sekiguchi, T. Kurahashi, Y. Tanaka, and K. Morito, "High-output-power, single-wavelength silicon hybrid laser using precise flip-chip bonding technology," Opt. Express **20**, 28057 (2012).

[6] B. Snyder, B. Corbett, and P. O'Brien, "Hybrid integration of the wavelength-tunable laser with a silicon photonic integrated circuit," J. Lightwave Technol. **31**, 3934–3942 (2013).

[7] B. Szelag, K. Hassan, L. Adelmini, E. Ghegin, P. Rodriguez, S. Bensalem, F. Nemouchi, T. Bria, M. Brihoum, P. Brianceau, E. Vermande, O. Pesenti, A. Schembri, R. Crochemore, S. Dominguez, M. C. Roure, B. Montmayeul, L. Sanchez, and C. Jany, "Hybrid III-V/Si DFB laser integration on a 200 mm fully CMOS-compatible silicon photonics platform," in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 24.1.1–24.1.4.

[8] X. Luo, Y. Cao, J. Song, X. Hu, Y. Cheng, C. Li, C. Liu, T.-Y. Liow, M. Yu, H. Wang, Q. J. Wang, and P. G.-Q. Lo, "High-throughput multiple dies-to-wafer bonding technology and III/V-on-Si hybrid lasers for heterogeneous integration of optoelectronic integrated circuits," Front. Mater. **2**, 1–21 (2015).

[9]G. Roelkens, A. Abbasi, P. Cardile, U. Dave, A. D. Groote, Y. D. Koninck, S. Dhoore, X. Fu, A. Gassenq, N. Hattasan, Q. Huang, S. Kumari, S. Keyvaninia, B. Kuyken, P. M. L. Li, M. Muneeb, D. Sanchez, H. Shao, T. Spuesens, A. Subramanian, S. Uvin, M. Tassaert, K. V. Gasse, J. Verbist, R. Wang, Z. Wang, J. Zhang, J. V. Campenhout, Y. Xin, J. Bauwelinck, G. Morthier, R. Baets, and D. V. Thourhout, "III-V-on-silicon photonic devices for optical communication and sensing," Photonics **2**(3), 969–1004 (2015).

[10]T. Komljenovic, D. Huang, P. Pintus, M. A. Tran, M. L. Davenport, and J. E. Bowers, "Photonic integrated circuits using heterogeneous integration on silicon," Proc. IEEE **106**, 2246–2257 (2018).

[11]E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers, "A printable form of silicon for high performance thin film transistors on plastic substrates," Appl. Phys. Lett. **84**, 5398–5400 (2004).

[12]M. A. Meitl, Z. T. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. A. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," Nat. Mater. **5**, 33–38 (2006).

[13]B. Guilhabert, J. McPhillimy, S. May, C. Klitis, M. D. Dawson, M. Sorel, and M. J. Strain, "Hybrid integration of an evanescently coupled AlGaAs microdisk resonator with a silicon waveguide by nanoscale-accuracy transfer printing," Opt. Lett. **43**, 4883 (2018).

[14]R. Katsumi, Y. Ota, A. Osada, T. Yamaguchi, T. Tajiri, M. Kakuda, S. Iwamoto, H. Akiyama, and Y. Arakawa, "Quantum-dot single-photon source on a CMOS silicon photonic chip integrated using transfer printing," APL Photonics **4**, 036105 (2019).

[15]J.-B. Park, K. H. Lee, S. H. Han, T. H. Chung, and M. K. Kwak, "Stable and efficient transfer-printing including repair using a GaN-based microscale light-emitting diode array for deformable displays," Sci. Rep. **9**, 11551 (2019).

[16]B. Gai, J. F. Geisz, D. J. Friedman, H. Chen, and J. Yoon, "Printed assemblies of microscale triple-junction inverted metamorphic GaInP/GaAs/InGaAs solar cells," Prog. Photovoltaics: Res. Appl. **27**, 520–527 (2019).

[17]G. Roelkens, J. Zhang, A. De Groote, J. Juvert, N. Ye, S. Kumari, J. Goyvaerts, G. Muliuk, S. Uvin, G. Chen, B. Haq, B. Snyder, J. Van Campenhout, D. Van Thourhout, A. J. Trindade, C. A. Bower, J. O'Callaghan, R. Loi, B. Roycroft, and B. Corbett, "Transfer printing for silicon photonics transceivers and interposers," in *2018 IEEE Optical Interconnects Conference (OI)* (IEEE, USA, 2018), pp. 13–14.

[18]D. Gomez, K. Ghosal, M. A. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond, D. Kneeburg, A. Fecioru, A. J. Trindade, and C. A. Bower, "Process capability and elastomer stamp lifetime in micro transfer printing," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)* (IEEE, 2016), pp. 680–687.

[19]X. Feng, M. A. Meitl, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Competing fracture in kinetically controlled transfer printing," Langmuir **23**, 12555–12560 (2007).

[20]J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, "Wafer-scale integration of group III-V lasers on silicon using transfer printing of epitaxial layers," Nat. Photonics **6**, 610–614 (2012).

[21]A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. Bower, D. Delbeke, R. Baets, and G. Roelkens, "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters," Opt. Express **24**, 13754 (2016).

[22]J. Zhang, B. Haq, J. O'Callaghan, A. Gocalinska, E. Pelucchi, A. J. Trindade, B. Corbett, G. Morthier, and G. Roelkens, "Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser," Opt. Express **26**, 8821 (2018).

[23]D. Vermeulen, T. Spuesens, P. De Heyn, P. Mechet, R. Nötzel, S. Verstuyft, D. Van Thourhout, and G. Roelkens, "III-V/silicon-on-insulator photonic integrated circuit for fiber-to-the-home central office transceivers in a point-to-point network configuration," in *36th European Conference and Exhibition on Optical Communication* (2010), pp. 1–3.

[24]J. Zhang, A. De Groote, A. Abbasi, R. Loi, J. O'Callaghan, B. Corbett, A. J. Trindade, C. A. Bower, and G. Roelkens, "Silicon photonics fiber-to-the-home transceiver array based on transfer-printing-based integration of III-V photodetectors," Opt. Express **25**(13), 14290–14299 (2017).

[25]G. Muliuk, K. Van Gasse, J. Van Kerrebrouck, A. J. Trindade, B. Corbett, D. Van Thourhout, and G. Roelkens, "4 × 25 Gbps polarization diversity silicon photonics receiver with transfer printed III-V photodiodes," IEEE Photonics Technol. Lett. **31**, 287–290 (2019).

[26]G. Muliuk, J. Zhang, J. Goyvaerts, S. Kumari, B. Corbett, D. Van Thourhout, and G. Roelkens, "High-yield parallel transfer print integration of III-V substrate-illuminated C-band photodiodes on silicon photonic integrated circuits," Proc. SPIE **10923**, 1092305 (2019).

[27]G. Chen, J. Goyvaerts, S. Kumari, J. V. Kerrebrouck, M. Muneeb, S. Uvin, Y. Yu, and G. Roelkens, "Integration of high-speed GaAs metal-semiconductor-metal photodetectors by means of transfer printing for 850 nm wavelength photonic interposers," Opt. Express **26**, 6351–6359 (2018).

[28]N. Ye, G. Muliuk, J. Zhang, A. Abbasi, A. J. Trindade, C. Bower, D. Van Thourhout, and G. Roelkens, "Transfer print integration of waveguide-coupled germanium photodiodes onto passive silicon photonic ICs," J. Lightwave Technol. **36**, 1249–1254 (2018).

[29]J. Juvert, T. Cassese, S. Uvin, A. de Groote, B. Snyder, L. Bogaerts, G. Jamieson, J. V. Campenhout, G. Roelkens, and D. V. Thourhout, "Integration of etched facet, electrically pumped, C-band Fabry-Perot lasers on a silicon photonic integrated circuit by transfer printing," Opt. Express **26**(17), 21443–21454 (2018).

[30]R. Loi, J. O'Callaghan, B. Roycroft, C. Robert, A. Fecioru, A. J. Trindade, A. Gocalinska, E. Pelucchi, C. A. Bower, and B. Corbett, "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates," IEEE Photonics J. **8**, 1 (2016).

[31]B. Corbett, R. Loi, J. O'Callaghan, L. Liu, K. Thomas, A. Gocalinska, E. Pelucchi, A. J. Trindade, C. A. Bower, G. Roelkens, and B. Roycroft, "Transfer-printing for heterogeneous integration," in *Optical Fiber Communication Conference (OFC) 2019* (Optical Society of America, 2019), p. M2D.1.

[32]M. Lamponi, "Hybrid III-V on silicon lasers for telecommunication applications," Ph.D. thesis, Université Paris Sud - Paris XI, 2013.

[33]K. V. Gasse, R. Wang, and G. Roelkens, "27 dB gain III-V-on-silicon semiconductor optical amplifier with >17 dBm output power," Opt. Express **27**, 293–302 (2019).

[34]M. L. Davenport, S. Skendžić, N. Volet, J. C. Hulme, M. J. R. Heck, and J. E. Bowers, "Heterogeneous silicon/III-V semiconductor optical amplifiers," IEEE J. Sel. Top. Quantum Electron. **22**, 78–88 (2016).

[35]J. O'Callaghan, R. Loi, E. E. Mura, B. Roycroft, A. J. Trindade, K. Thomas, A. Gocalinska, E. Pelucchi, J. Zhang, G. Roelkens, C. A. Bower, and B. Corbett, "Comparison of InGaAs and InAlAs sacrificial layers for release of InP-based devices," Opt. Mater. Express **7**, 4408 (2017).

[36]S. Dhoore, G. Roelkens, and G. Morthier, "III-V-on-silicon three-section DBR laser with over 12 nm continuous tuning range," Opt. Lett. **42**, 1121–1124 (2017).

[37]J. Zhang, L. Yanlu, S. Dhoore, and G. Morthier, "Unidirectional, widely-tunable and narrow-linewidth heterogeneously integrated III-V-on-silicon laser," Opt. Express **25**, 7092 (2017).