# Parameter extraction, variability analysis and yield prediction of the photonic integrated circuits.

**Umar Khan**[1,2], **Yufei Xing**[1,2], **and Wim Bogaerts**[1,2]

[1] *Photonics Research Group, Ghent University-IMEC, Ghent, Belgium*
[2] *Center of Nano and Biophotonics, Ghent, Belgium*
*umar.khan@ugent.be*

**Abstract:** We discuss the complete workflow from the extraction of behavioral and fabricated geometry parameters using optical measurements to a decomposition of spatial variability and ultimately to the layout-aware yield prediction of *photonic integrated circuits* (PIC). © 2019 The Author(s)

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## 1. Introduction

Silicon photonics is becoming more commercially viable with an increasing complexity of *photonic integrated circuits* (PIC). The high material contrast between the core and the cladding of the *silicon-on-insulator* (SOI) waveguides enables increased complexity by facilitating the sub-micrometer waveguides with high packing density. This high material contrast, on the other hand, makes silicon photonic devices very sensitive to fabrication imperfections. For example, a small variation in the dimensions (line-width, thickness) of the waveguide in a resonant structure may shift the resonance wavelength to an unacceptable value resulting into a lower overall yield of the circuit. The sensitivity to fabrication imperfections becomes a significant challenge with increasingly complex circuits as performance degradation propagates and accumulates to the circuit level. Therefore, it is necessary to make variability analysis and yield prediction an essential part of the standardized design flow.

## 2. Parameter extraction & spatial variability

It is essential to extract the compact model parameters of fabricated circuits to start the variability analysis and to get input data for performance evaluation [1]. The most basic photonic component (i.e. a waveguide) can be modeled using the effective index and group index. Even extracting effective and group indices from a fabricated device are not straightforward. Effective and group indices from fabricated circuits can be extracted using a low and a high order *Mach-Zehnder interferometer* (MZI) structures [2] or using a compact circuit called folded two-stage MZI [3]. This folded two-stage MZI and its circuit model are shown in Fig. 1. It can be noticed that directional couplers (DC) are used as splitters and combiners to also extract the coupling coefficients of the DCs along with the effective and group indices of the straight waveguides. Fabricated devices were measured and fit to the circuit model to extract the model parameters mentioned in Fig. 1(b).

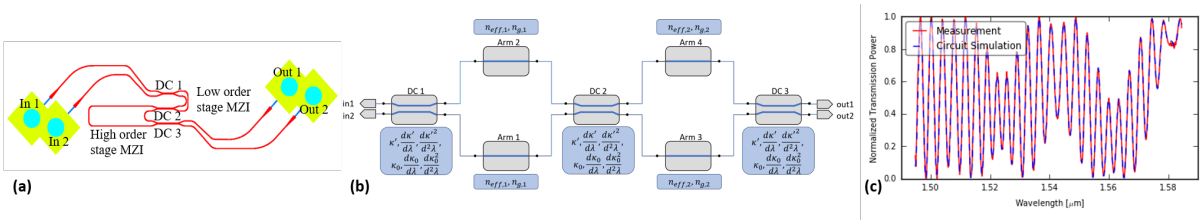


Fig. 1. (a) The folded two-stage MZI used to extract the compact model parameters from optical measurements. 117 copies of the folded two-stage MZI were distributed over the die to have a good idea of the fabrication variation. (b) The circuit model of the device. The model parameters for each component are labeled. (c) The measured spectrum is fitted to the circuit simulations to extract the model parameters.

It is important to find out the fabricated geometry of the waveguides over the wafer in order to map the fabrication imperfections to performance degradation. The metrology measurements like *scanning electron microscope* (SEM) or *atomic force microscope* (AFM) are time-consuming, expensive and/or destructive. Moreover, metrology measurements are not that accurate (measurement errors in nanometers) and do not provide enough sample points to perform the variability analysis. So, it is required to extract the model parameters from the optical measurements and then accurately map them to accurate geometry variations. It has been demonstrated that waveguide geometry (line-width and thickness) can be extracted from the effective and group indices using a numerically developed geometrical model [2]. The approach provides the sub-nanometer precision of geometry extraction for the waveguide fabricated using a foundry process line, which helps to identify process variations and non-uniformity across the device layer. The extracted effective and group indices are translated into the geometric parameters and wafer maps are generated for both line-width and thickness of the waveguides. The generated wafer maps using two-stage MZI circuits over the wafer are shown in Fig. 2.

## 3. Layout-aware yield prediction

It can be noticed in the generated wafer maps that line-widths and thicknesses vary with a radial pattern. So, devices in the center of the wafer will be affected differently by the variability than those at the edges. Also, devices located very close to each other on the wafer should be more correlated than devices placed far from each other. Monte-Carlo simulations can be performed to find out the performance of the devices due to the variation in the fabricated geometry. For accurate yield prediction, location-dependency of variations as depicted in the wafer maps should be taken into account. To make realistic predictions, we incorporate information of the spatial variations into the Monte-Carlo method. In a circuit simulator as CAPHE, maps of global variations (e.g., linewidth and thickness deviations from the nominal value) can be 'projected' onto the actual layout of a circuit which is positioned on different wafer sites [4]. Knowing the sensitivity of parameters to geometry variations, we can propagate these variations to the circuit level and simulate the response. These Monte-Carlo simulations taking into account the width and thickness variations over the wafer give an indication of the device performance. The yield of the circuits over the wafer is calculated based on these Monte-Carlo simulations.

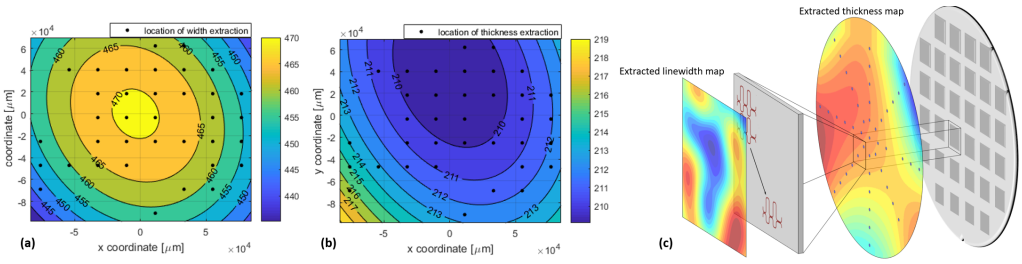


Fig. 2. Extracted wafer maps for the (a) width and (b) thickness. Layout-aware yield prediction is performed using the Monte-Carlo simulations based on the extracted width and thickness maps shown in (a) and (b).

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