Alignment-tolerant taper design for transfer printed III-V-on-Si devices

(Student paper)

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ABSTRACT

In this paper, we present the design of a 1.0 μm misalignment-tolerant taper for the evanescent coupling of light in a III-V-on-silicon opto-electronic device realized on an SOI waveguide platform with 400 nm thick Si device layer. The designed taper is also fabrication tolerant and is suitable for the transfer-printing-based integration of pre-processed III-V devices on Si photonics waveguide circuits. The design procedure is flexible and can take into account the limitations in critical dimensions imposed by the fabrication process.

Keywords: III-V/Si integration, Transfer Printing, Adiabatic taper

1 INTRODUCTION

Micro-Transfer printing is an emerging technique for the integration of III-V epitaxial layers and pre-processed devices on Si photonic circuits [4][2]. This technique is highly modular in terms of the integration of different III-V epitaxial layer structures / devices. Moreover, it allows for efficient III-V usage and massively parallel integration [1]. A key building block that needs to be realized by III-V semiconductors on a silicon waveguide circuit is a semiconductor optical amplifier. By locally removing the back-end stack of the silicon photonic integrated circuit, SOAs - pre-processed on the native substrate - can be transfer printed on top of the silicon device layer and evanescently-coupled to the underlying silicon waveguide circuit. The process of transfer printing and the resulting photonic integrated circuit is shown in Fig. 1 (a) and (b) respectively.

The idea is to process the epitaxial layer structure grown on its III-V native substrate, while incorporating a sacrificial layer between the device layer stack and the substrate. By encapsulating the devices and etching the sacrificial layer, the devices are released from the III-V substrate and can be picked up from the source wafer and printed on the silicon photonic target wafer using a PDMS stamp. Like in any other hybrid integration technique, integrating preprocessed devices using transfer printing requires high alignment accuracy. State-of-the-art transfer printing tools have an alignment accuracy of 1 to 1.5 μm 3σ, depending on the size of the array of devices that are being transferred [1]. Therefore, the adiabatic taper that is commonly used to couple light between the silicon waveguide and the III-V-on-silicon device must have a high alignment tolerance. In this paper, we present the design of such an adiabatic taper structure.

2 DESIGN AND SIMULATION

Designing of an optimal III-V-on-silicon taper structure can be realized using the formalism described in [3], where a two-mode coupled-waveguide system is assumed. In this formalism the shape of the shortest adiabatic taper structure can be found by solving (1),

$$\gamma = tan[sin^{-1}(2\epsilon^{\frac{1}{2}} \int_{z_0}^{z} \kappa(z`)dz`)] \tag{1}$$

where $\gamma \equiv \frac{(\beta_2-\beta_1)}{2\kappa}$, $\frac{\beta_2-\beta_1}{2}$ is the mismatch of the propagation constants between the individual uncoupled waveguide modes, ϵ is the fraction of power in the unwanted mode, κ is the coupling strength between the two

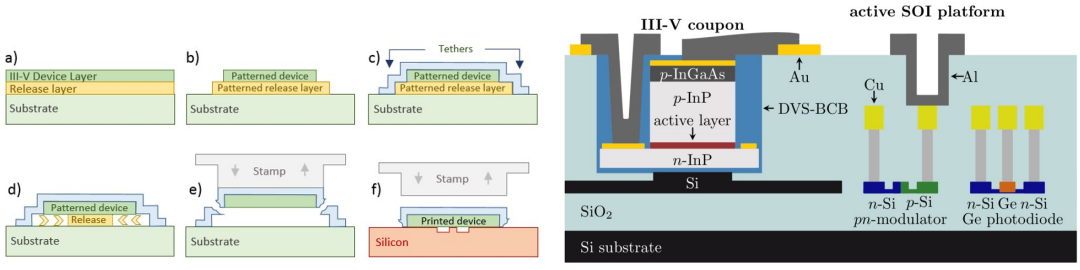

Figure 1. (a) Transfer printing process flow, (b) Transfer printed III-V coupon on SOI

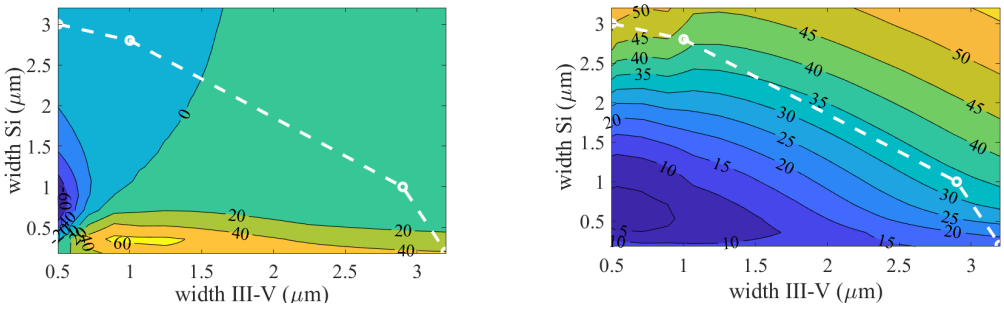

Figure 2. (Left) Calculated values of γ for several waveguide width combinations of III-V and Si, (Right) Calculated values of κ in mm^{-1}

waveguide modes ($\kappa_{mp} = \frac{k_0^2}{2\beta} \int \int_{-\inf}^{+\inf} (n'^2 - n_p^2) F_m * F_p dxdy$, where F_m and F_p are the normalized eigen modes of the each uncoupled waveguide and must be normalized such that $\int \int_{-\inf}^{+\inf} |F_m(x,y)|^2 dxdy = 1$, where n' is the refractive index profile of the coupled waveguide system, n_p is the refractive index profile of the uncoupled waveguide and β is the propagation constant of the coupled mode). Equation 1 gives us the optimal γ distribution along the length of the III-V and silicon taper structure, assumed to be along the z-axis. Subsequently, it can rewritten by assuming κ to be linearly varying between two consecutive points along z as

$$z_N = \frac{sin(tan^{-1}\gamma_N)}{\epsilon^{\frac{1}{2}}(\kappa_{N-1} + \kappa_N)} - \frac{2}{\kappa_{N-1} + \kappa_N}[\sum_{i=0}^{N-1} A_i] + z_{N-1}] \tag{2}$$

where $z = z_N$ is a point N along the length of the taper that begins at $z = z_0$, $A_i = \frac{1}{2}(\kappa_{i-1} + \kappa_i)(z_i - z_{i-1})$ and γ_N is the value of γ at $z = z_N$. In order to design the taper structure κ and γ were calculated for all possible width combinations of III-V and silicon waveguide, assuming a lateral misalignment of 1μm as the worst case. A standard III-V epitaxial stack used for evanescently-coupled optical amplifiers and lasers was used [4]. The device cross-section printed on SOI spin coated with BCB is shown in Fig. 1(b). The DVS-BCB adhesive bonding layer thickness is assumed to be 60 nm for all calculations. The map of γ and κ is shown in Fig. 2. When γ is greater than 10, the III-V waveguide is wide and the Si waveguide is narrow, and light is mostly confined in the III-V waveguide and when γ is less than -10, the light is predominately confined in the Si waveguide. The zero contour line is the phase matching line and corresponds to III-V and Si widths at which the optical modes are phase matched. Now, we have the freedom to choose any set of III-V and Si width pairs from the contour map such that γ values goes from negative to positive crossing the zero line to realize a transition from the silicon waveguide to the III-V waveguide. Each chosen trajectory will correspond to a new taper structure. If, however, we choose the widths pairs that correspond to higher κ values, the taper coupling length can be shortened. After the selection, the values of γ and κ are inserted in (2) and their location along the propagation direction z is calculated, thereby defining the taper geometry .

However, there is one more criterion that the adiabatic Si and III-V taper should follow in order to avoid power coupling into higher order modes. The local half angle of the Si and III-V taper must follow $\theta < \frac{\lambda_0}{2Wn_{eff}}$. This means that the tapering should be slower than the diffraction of the fundamental mode of each waveguide. After taking into account both the aformentioned adiabacity criteria and choosing a set of III-V and taper width pairs, shown by the dashed white line in Fig. 2, the taper shape calculated from (2) was exported into a 3D EME solver and the power coupling between Si and III-V was simulated. The taper shape and the simulated coupling with respect to lateral misalignment is shown in Fig. 3. The III-V waveguide width varies from 0.51 μm to 3.2 μm whereas the silicon tapers from 3 μm to 0.2 μm. The taper is 225 μm long. The coupling efficiency drops to -3 dB at 1.2 μm lateral misalignment.

During the processing, the width of the taper structure can vary, therefore, the design should have, besides good alignment tolerance, also a good fabrication tolerance. In particular, the isotropic etching of the QWs can lead to a width of the QWs narrower than designed. The effect of the variation of the III-V layer stack width including QWs and QWs width alone, while the tapers are 1 μm misaligned, is shown in Fig. 4(a) and Fig. 4(c). The coupling efficiency doesn't changes rapidly in case of widening of the taper and QWs as compared to narrowing. Moreover, the coupling efficiency decreases less than 1 dB for a reduction of the width by 250 nm from the design width. The coupling efficiency changes much more rapidly if the thickness of n-InP and BCB is reduced shown in Fig. 4(c) and Fig. 4(d), respectively. This is due to the change in κ between the III-V and Si waveguide. The impact of a layer thickness increase is less than in case of a decrease.

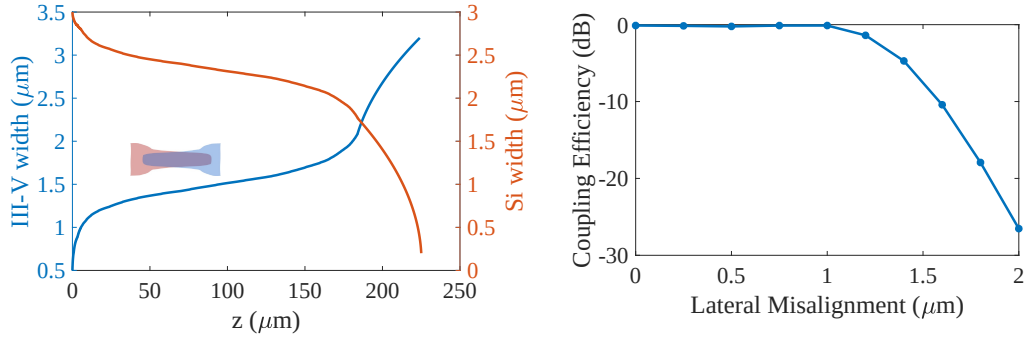

Figure 3. (Left) III-V and Si taper structure geometry, (Right) Simulated coupling efficiency plotted against lateral misalignment for the designed taper

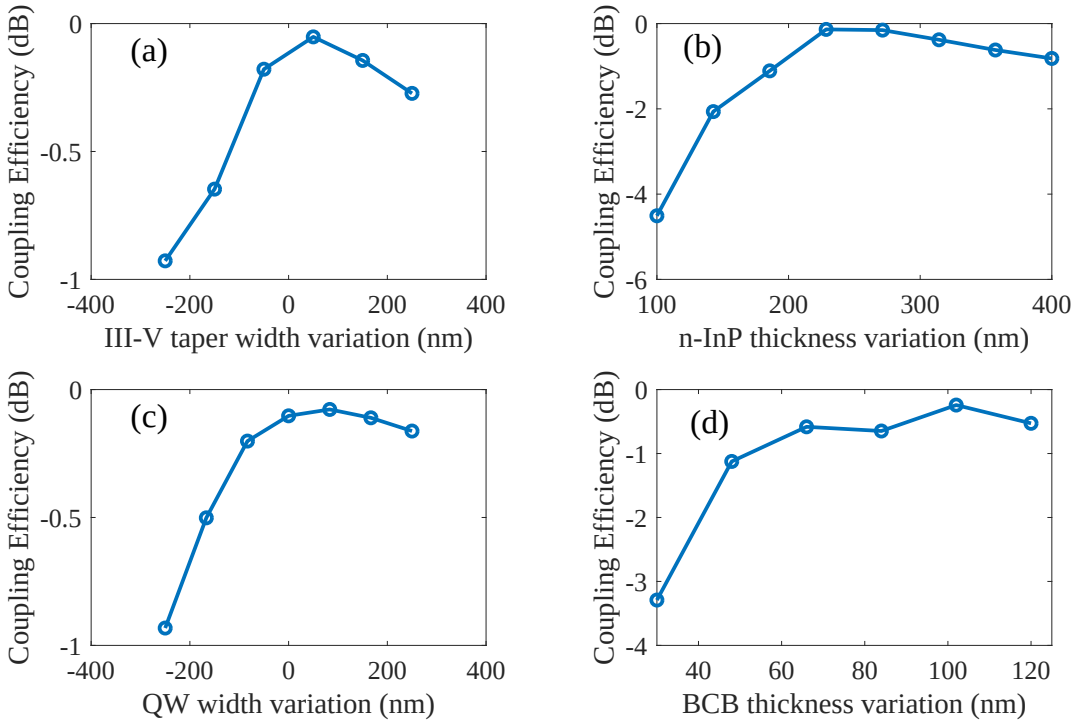

Figure 4. Effect on coupling efficiency with 1 μm misaligned III-V and Si taper of (a) III-V taper width variation, (b) n-InP thickness variation, (c) QW width variation, and (d) BCB thickness variation

CONCLUSION

In this paper, we present an alignment tolerant adiabatic taper structure for transfer printing preprocessed III-V SOAs evanescently coupled to Si photonic integrated circuit. The adiabatic taper structure has an alignment tolerance of 1 μm and is compact (225 μm).

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