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Predicting Yield of Photonic Circuits With Wafer-scale Fabrication Variability

(Invited Paper)

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***Abstract*—We present a workflow for variability analysis and yield prediction of photonic integrated circuits affected by fabrication variations. The technique combines synthetic wafer maps with layout-aware Monte-Carlo simulations. We demonstrate this on different layout configurations of linewidth-tolerant Mach-Zehnder interferometers.**

I. Introduction

Photonic integrated circuits (PIC) integrate many optical functions onto a chips, for use in fiber optics communication, sensing, spectroscopy and life science applications. One technology to implement PICs is *silicon photonics*, which uses silicon to implement submicrometer optical waveguides that can be fabricated on wafer-scale with high-end CMOS manufacturing technologies [1]. PIC technology is gradually pushing photonic design from components, which require full-vectorial electromagnetic modelling, to circuits, which rely on compact models to approximate the behavior. Like in electronics, photonic circuit design enables an increase in functionality by designing complex interconnected components, without the need for full physical modeling [2].

Because silicon waveguides have a very high refractive index contrast between the core and the cladding, they are very sensitive to nanometer-scale variations. Even with the best fabrication technology, it is not possible to control the dimensions to that level over large circuits, and between wafers and fabrication batches. As a result, components will experience geometric variations, resulting in functional variation across a circuit. This variation can result in circuits not performing as intended, and therefore impact the fabrication yield.

It is important that this is taken into account during the circuit design, so designers can predict the yield of their circuits after fabrication. Especially as designers are relying more and more on standard building blocks in the process design kits (PDK) of fabrication services [3], variability analysis and yield prediction at the circuit level becomes increasingly important.

However, such a functional analysis should still take into account the actual circuit layout. The fabrication induced variability is generated during various fabrication steps, and as a result there are fluctuations across the wafer on different length scales. A representative model of these contributions is needed, which can then be used in combination with the actual circuit layout to assess the impact on the performance.

In this paper, we will discuss our flow for variability analysis and yield prediction. First, we build a hierarchical model of variability across a wafer, separating die-level and wafer-level components. Using those models, we then run Monte-Carlo simulations on circuits to assess the impact of these variations. We illustrate how this approach can be used to choose between different circuit layouts to minimize the effect of variations.

II. Wafer-scale Variability Models

While photonic building blocks in a circuit are usually quite compact, silicon photonic circuits can scale up to centimeters in footprint. As a result, within a single circuit we can expect deviations from the nominal geometry, and therefore the functional parameters of the circuit building blocks. These variations come from the fabrication flow, which uses processes such as lithography, layer deposition, plasma and wet etching processes, and chemical-mechanical polishing (CMP). Even with state-of-the-art technology, all of these steps will impose different variational patterns over a wafer. For instance, a lithography step is repeated over a wafer using the same photomask, but there might be fluctuations in the light source or the photoresist thickness. In contrast, plasma etching is performed on an entire wafer, but might imprint a radial

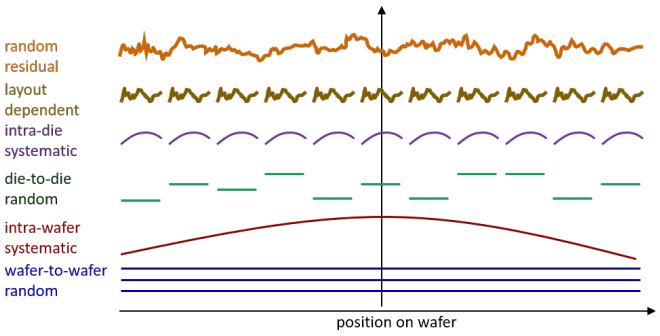

Fig. 1. Hierarchical model of variability contributions across the wafer.

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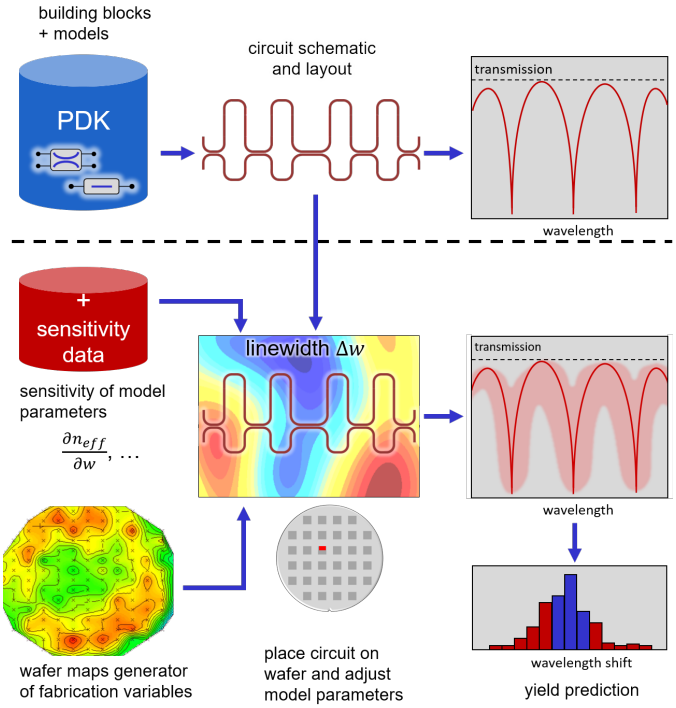

Fig. 2. Workflow for evaluating the layout-dependent variability of PICs.

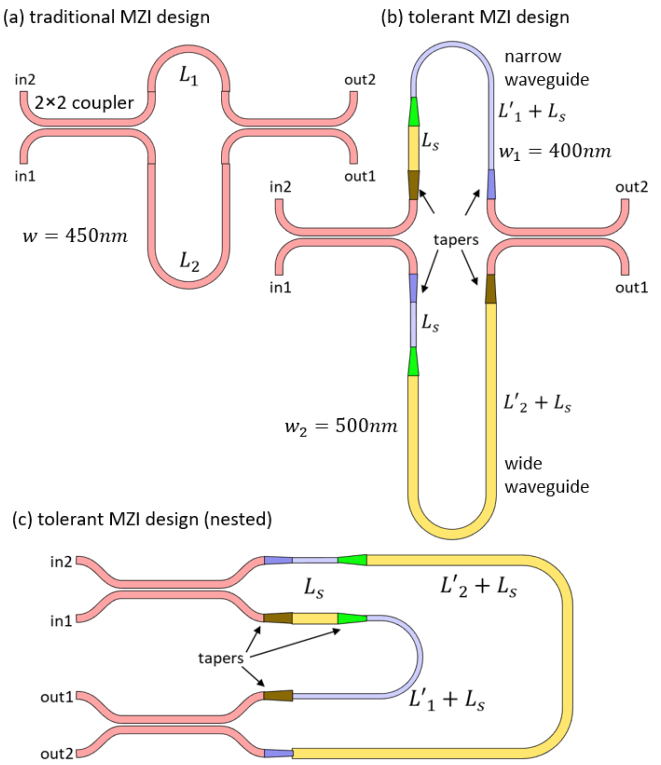

Fig. 3. Three designs for a Mach-Zehnder interferometer (MZI). (a) Using a single waveguide linewidth, (b) using two waveguide linewidths to make it tolerant to linewidth variations, and (c) the same design, but folded to nest the waveguides.

pattern due to uneven plasma composition. Also, local pattern density variations in the layout affect the plasma chemistry and thus the geometry. As lithography and etching are the most important process steps in defining silicon waveguides, it is clear that the waveguide geometry is subject to variability on different length scales.

Therefore, we construct a hierarchical model of the variability. Figure 1 shows how we can break down the variability into wafer-scale and die-level systematic contributions and random residues. On top of that, there are layout-related contributions, e.g. due to local pattern densities.

To extract these contributions for e.g. linewidth and thickness deviations, we experimentally extract those quantities from fabricated wafers. We do not measure the linewidth directly, because the accuracy is limited to a few nanometer; instead, we measure the transmission of dedicated waveguide test circuits, and map the variations of the functional parameters onto the geometric variations, such as linewidth and thickness [4]. Given the extreme sensitivity of the optical waveguides, this is a much more accurate extraction method. The resulting maps of linewidth and thickness are then broken down into their systematic and random components [5], and subsequently converted to a model that can generate representative maps for yield prediction.

III. Yield Prediction

These wafer maps of fabrication-related variables can be used as input to predict the performance of circuits over the wafer(s). The most straight-forward approach is to use Monte-Carlo simulations. The flow we use is depicted in Fig. 2 [6].

Starting from a component library in a process design kit (PDK), we create a circuit layout which we then simulate in a circuit simulator. For this, we use the IPKISS toolset by Luceda Photonics, which comes with the built-in circuit simulator Caphe. This gives us the nominal behavior of the circuit.

To model the effects of fabrication variability, we extend the circuit models in the PDK with a sensitivity matrix, listing how the circuit parameters will change when external variables, such as linewidth and thickness, deviate from their nominal value. Because the design framework is written in Python, this sensitivity can be provides as simple values or Python functions that calculate the values on the fly.

Using the wafer models described in II, we know the local deviation from the nominal linewidth, and using the actual circuit layout, we can now calculate how all the circuit parameters deviate from from their nominal value. We can then perform a Monte-Carlo simulation of the circuit by placing it on many locations on the wafer (dies) and on multiple wafers.

IV. Example

As an example of the use of location-aware yield prediction, we model a device that is already designed to be tolerant to linewidth variations. As described in detail in [7], a Mach-Zehnder interferometer (MZI) can be made tolerant to variations by using different waveguides in both arms.

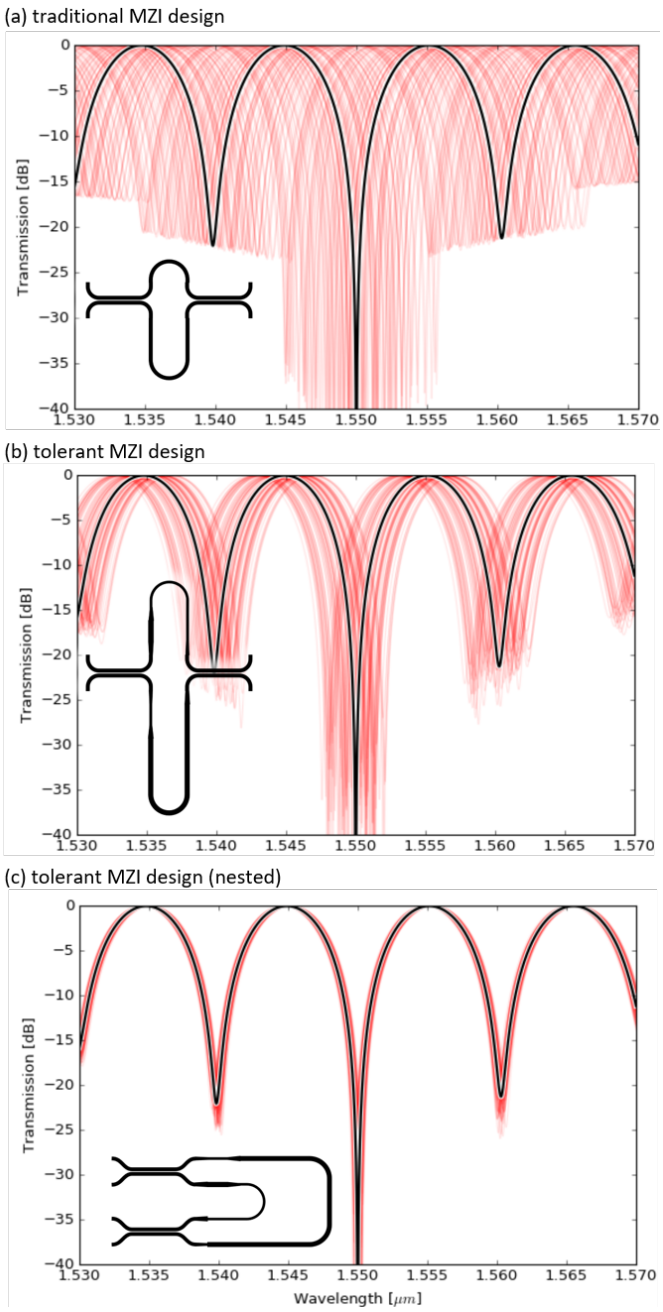

Fig. 4. Monte-Carlo transmission simulations of the MZI circuits in Fig. 3. (a) the non-tolerant design experiences large wavelength shifts, (b) the tolerant design with opposite waveguides compensates global variations, while (c) the nested waveguides make the design less sensitive to local variations.

This results in a larger circuit, but the different sensitivity of the two waveguide types can compensate a global drift in wavelength. Figure 3 shows three designs for an MZI with the same functional specifications. The first uses a single type of waveguide and is not expected to be tolerant to linewidth variations, while the second and third design are designed to be tolerant to linewidth variations and use two different types of waveguides, but with a different layout: One circuit has the two waveguides on opposing sides, while the other design nests the waveguides inside each other.

We modelled the response of these circuits over a wafer with long-range (¿ 1 cm) linewidth variations with 10 nm amplitude, plus short-range (100 μm) variations with an amplitude of 2 nm. Figure 4 shows the transmission simulations of 150 locations on this wafer. The non-tolerant design experiences dramatic shifts in the wavelength response due to the linewidth variations. this is less pronounced in the tolerant designs, but we still see a significant difference between the two circuit layouts, even though they are both designed with the same procedure and are both expected to show the same tolerance. The difference comes from the local variations in linewidth. The design procedure assumes that both arms in the MZI experience the same deviation in linewidth. this compensates for long-range fluctuations. However, if the arms are located far apart, they will experience different local deviations. As a result, the layout with the opposing arms fares much worse than the layout with the nested arms. This shows that layout-awareness for circuit variability analysis and yield prediction provides insight that cannot be obtained with pure stochastic methods that are not layout aware.

V. Conclusions

We have shown that layout-aware variability analysis gives deeper insight into the mechanisms behind circuit yield. For this, good models of wafer-scale variability are required, capturing the fluctuations at different length scale. Using a sensitivity matrix, these maps can be projected onto the actual circuit layout and fed into a Monte-Carlo simulator, which results in a map of the circuit yield.

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