CHAPTER THREE

Transfer Printing for Silicon Photonics

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1. INTRODUCTION

While photonics is a key enabling technology for multiple applications, unlike for electronics, the photonic devices for each application are generally customized with the key components being singly packaged. A laser is a vital component in many applications but since, for different applications, the laser emission may be required to be at a wavelength within the UV to the far IR range, this results in a special material structure and the laser generally being a stand-alone component. This singulation of

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devices requires costly, complex assembly to achieve photonic subsystems. Integration of photonic components is the clear solution. This is not so straightforward due not only to the wide range of materials needed but also to the wide variety of desired photonic functions.

Communications provide an example where it is imperative to reduce costs to allow the continued scaling of information flow. Data flow has been exponentially increasing for decades and while higher costs have been tolerated for high bandwidth internet communications this is not the case as photonics is replacing electrical signaling at shorter distances in fiber-to-the-home, in data centers and ultimately for chip-to-chip communications. The occurrence of the low loss window for silica fiber in the 1300–1550 nm wavelength range requires devices based on InP which provide the appropriate bandgaps for lasers, modulators, and detectors. These devices are the basis for all fiber-based long distance communications. InP wafers have only scaled slowly in size due to the challenges associated with creating the substrates. Currently most production is on 75–100 mm diameter substrates which are costly when compared with GaAs and especially silicon substrates. While this wafer size is adequate for the production of individual lasers and detectors it imposes a severe challenge for circuit integration since photonic device sizes are relatively large and the device arrangements are complex. The optimal device structures are distinct for different photonic functions often requiring epitaxial overgrowth steps and thereby affecting yield. Thus, the number of functional circuits per wafer is low. While excellent progress has been made with photonic integrated circuits (PICs) using InP platforms for telecommunications (Nagarajan et al., 2010); these are expensive to produce with only a handful of foundries producing InP PICs. The scalability of this approach for low-cost photonics is ultimately limited.

The most successful large-scale integration approach for photonics is based on silicon starting from wafers with diameters from 200 to 300 mm using highly mature technological processes that are precise on the nanometer scale. Several of these platforms are available from large, state-of-the-art foundries with established design rules for external designers. Nevertheless, these platforms are not complete without an active gain providing element which is the best supplied from III–V materials. This chapter will discuss the current state of development for microtransfer printing (μTP) as an effective technology for the scalable heterogeneous integration of different materials (particularly III–V semiconductors) and devices onto these silicon platforms. The technique involves the formation and registration of thin coupons of a material structure, releasing these coupons from their source wafer,

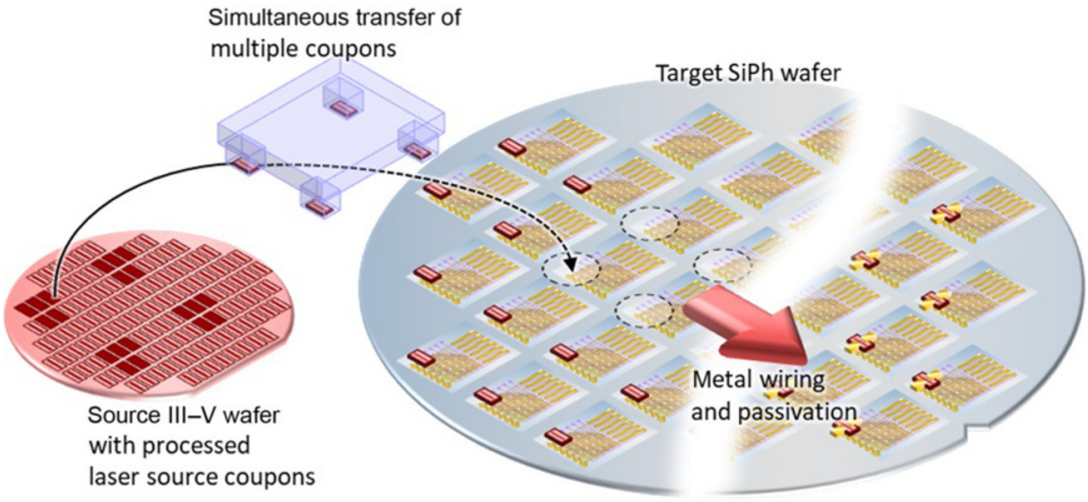

Fig. 1 Heterogeneous integration concept for the transfer of III–V components (materials or devices such as lasers) from a source wafer to a target silicon photonics (SiPh) wafer.

the sequential, parallel transfer of stamp-selected arrays of the coupons, and their bonding to selected matching locations on the target silicon substrate as shown schematically in Fig. 1.

1.1 Silicon Platforms

The silicon-on-insulator (SOI) technology has matured over the last 20 years to be a scalable platform for photonics (Reed and Knights, 2004). It takes advantage of the enormous development in technology for electronics and imposes the learnings on design rules and circuit verification. It relies on a thin layer of silicon surrounded by SiO_2 acting as a waveguide layer. The thickness of the Si is commonly 220 nm though other examples work with silicon layer thickness up to 4000 nm where coupling to external lasers and fibers is more straightforward. The accessible wavelengths are from 1.1 to 4 μm with the principle interest being for datacenters and communications around 1550 and 1300 nm. However, the same waveguide technology can be used for many other applications such as LIDAR, gas sensing, and medical devices (Wang et al., 2017).

The light source or an optical amplification function has yet to be monolithically integrated on silicon on a wafer scale. While recent advances have been demonstrated with selective area epitaxy and quantum dot growth on silicon (Liu et al., 2014), these approaches have yet to be proven in photonic circuits. In the meantime, the laser light has to be provided to the silicon waveguides from a separate InP (or GaAs)-based material structure.

Laser light can be coupled to these silicon waveguides using the following three general techniques. Grating coupling requires alignment and fixation of optical fibers or external lasers. Recently, fully formed VCSELs have been directly integrated on the wafer using flip chip technology (Lu et al., 2016). Edge coupling between a gain chip and the waveguide can be designed for broadband connection. By controlled etching of trenches in the SOI wafer and combined with accurate flip chip of InP reflective amplifier chips high-performance external cavity lasers have been achieved on large cross-section (3 μm) SOI waveguides (Zilkie et al., 2012) and small cross-section SOI waveguides (Guan et al., 2018). Hybrid lasers allow for a more scalable integration. In these lasers, there is an evanescent optical connection between the Si waveguide and a III–V gain element. The integration uses bonding of centimeter-sized dies up to full III–V wafers to the SOI wafer. This bonding approach has been well studied (Roelkens et al., 2010) and successfully commercialized. It does however limit the complexity of the SOI wafer as the surface needs to be flat (planarized) over the large area being bonded. It is also relatively inefficient in the use of costly III–V material especially if the component need is sparse.

More advanced SOI technologies have demonstrated modulators using lateral p–n junction, carrier accumulation/depletion with metal-oxide-semiconductor capacitor structures and the Franz–Keldysh effect in Ge grown on silicon. High bandwidth detectors have been widely used by local deposition of high-quality Ge. Yet these functions could be provided with higher performance by III–V materials if they could be integrated in a sensible manner. So while the gain providing components are uniquely provided by III–V materials there are many opportunities for the integration of other established photonic components based on InP, GaAs, and GaSb materials. It may also be possible to introduce desired novel functions based on optimized nonlinear materials such as $LiNiO_3$ or $BaTiO_3$. Furthermore, it could even be possible to integrate compact electrical circuits using III–V or Si technology for very high bandwidth electrical drivers and amplifiers. The power for optical circuits could be remotely delivered through fibers if an efficient power converter element was integrated on the circuit. Thus, a technology where different components can be heterogeneously cointegrated is highly desirable. This can be delivered through μTP.

The second set of platforms is based on the use of Si as a simple substrate but using well-established materials with wafer scale deposition

and etching processes. Waveguide systems based on doped silica waveguides, silicon nitride (SiN), and polymers are well established. These waveguide materials allow accessing a wider range of wavelengths particularly in the visible region. As there is minimal absorption by water in the visible region, this opens up many applications in life sciences especially in combination with microfluidics. Foundry processes for SiN are available. They provide relatively compact circuits with low waveguide loss allowing for larger propagation lengths and larger circuits. Refractive index control—as needed for tunable functions—can be provided by integrated heaters. The gain element is lacking and, as above, multiple active components spanning a wider material range including GaAs and GaN integrated at low cost are desirable.

The ultimate integration is the combination of photonics with the most advanced CMOS electronics. Electrical signal interconnections limit the bandwidth performance of modern electronic processing systems. Higher bandwidth can be achieved if photonics can be closely integrated with the electrical functions such as the processor or memory. However, such integration must not compromise the advanced and highly specialized electrical circuitry. The CMOS chips can be integrated on a silicon platform for waveguide interconnections or the waveguides can be directly integrated with the CMOS. In both cases the challenge of integrating the laser remains.

In summary, to obtain the most versatile, functional optical circuits require the integration of diverse materials and devices (Table 1).

Table 1 Platform Technologies Requiring Light Source Integration

Si Platform	Waveguide Form	Wavelength	Applications
Silicon-on-insulator	220 nm SOI	1100–4000 nm	Data communications
	Thick SOI		Computer interconnect
			Sensors
			Phased arrays
Si substrates	Polymer	300–3000 nm	Sensors
	Doped SiO_2		Biomedical
	SiN_x		Computer interconnect
CMOS electronics	Advanced technology nodes	800–1600 nm	Short reach, high bandwidth, and high density interconnect

2. TRANSFER OF EPILAYERS AND MICROTRANSFER PRINT

The III–V epilayers contain all the functionality required for device operation and so their separation and transfer have been long practiced. Epitaxial lift-off using an ultrathin AlAs release layer is well established for GaAs-based photovoltaics. Photonic recycling in thin structures results in enhancement of the open circuit voltage and record performance for single junction cells has been achieved with this approach (Kayes et al., 2011). Additionally, the cost of the substrate can be recovered and so epitaxial lift-off is now implemented commercially by a number of companies. Nanomembranes created especially for group IV materials is an active field of research (Rogers et al., 2011). Through the release and transfer of very thin structures, it is possible to apply stress profiles to Si materials in a manner that would not otherwise be possible (Scott and Lagally, 2007). These techniques use large areas of material without specific focus on alignment to the target substrate. Bonding of III–V material structures to a target substrate (e.g., SOI) followed by substrate removal and device fabrication is a very successful approach to the integration of active III–V materials with silicon waveguides (Roelkens et al., 2010) and is dealt with in another chapter in this volume. The μTP is an alternative approach to integration and this chapter will present the characteristics of the technique and its advantages.

μTP starts with the formation of arrays of islands of material (termed coupons hereafter) from a source wafer. These coupons, of appropriate dimensions, that can be actual processed devices, are tethered to the substrate, holding them in place while they are released from the source wafer by the selective etching of a buried layer (or the substrate) in the structure. Following this, a sequential, parallel, pickup, and transfer of stamp-selected arrays of the suspended coupons to selected matching locations on a target substrate is performed. The target substrate may be prepatterned but is locally flat for the receiving coupon. The process sequence for the transfer of a single coupon is indicated schematically in Fig. 2.

Note that the technique transfers the coupons in an "epitaxial-side-up" configuration in contrast to a wafer bonding approach. The primary requirement for bonding to the new substrate is that the mating surfaces are locally flat. This can be achieved by spin coating the surface of the target substrate with a thin layer of polymer which can also assist the adhesion of the coupons.

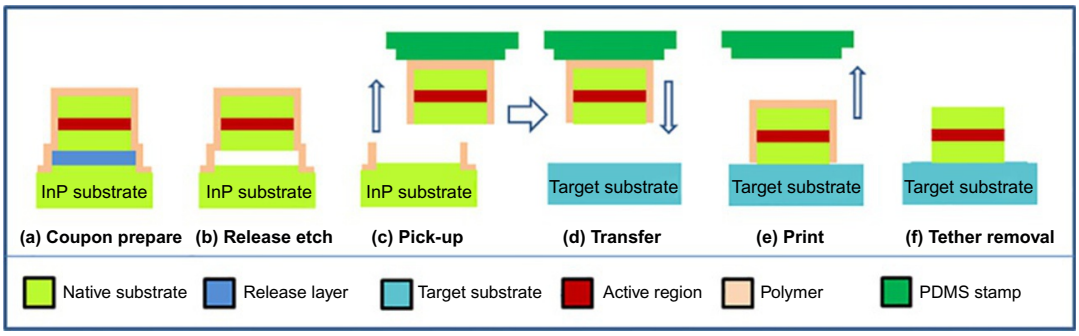

Fig. 2 Schematic of the microtransfer print process indicating the preparation, pickup, and transfer of a single coupon from a source substrate (InP) to a target substrate.

A direct bond can also be achieved between the mating surfaces through van der Waals forces. These are particularly enabled for very flat, thin, and small dimensioned coupons. Transfer print has been demonstrated for multiple materials including silicon, III–V materials and devices (GaAs, InP, InAs, GaN), graphene, and dielectrics. One example of the integration of large numbers of different components on a single substrate is for large area displays. Separate red (GaAs), green, and blue (GaN) micro-LEDs together with a silicon control circuit have been integrated for each pixel in the display (Bower et al., 2017) with thousands of devices being transferred per step. The magnification afforded by the printing of small devices on a large pitch makes possible the very effective use of the source material.

The important features of μTP for silicon photonics are:

- The highest quality source materials, as used for conventional devices, are used. The proviso is that a release layer and associated layers for waveguiding and height control are included. The technique is independent of the diameter of the source substrate and can print to large diameter target substrates.
- It makes efficient use of expensive materials. More devices per unit area can be obtained as the individual devices can be placed within 10–20 μm of each other on the source wafer since space for full bond pads is not required to be on the device.
- The devices can be prefabricated to allow manufacture in an optimum environment and to allow evaluation of their performance prior to transfer and identify known good die. In that case it is probably necessary that bond pads are provided for the device assessment.
- Accurate registration of the coupons on the target wafer is obtained by the use of fiducial markers on the source and target. A positional accuracy of ± 1.5 μm at 3σ can be obtained in high throughput, large area

operation though accuracy better than ±0.5 μm is achievable in individual coupon placement. Precise (lithographic) alignment to underlying waveguides can be obtained by postprocessing the associated waveguides on the transferred coupon.
- High throughput is obtained through wafer scale transfer of 2D arrays of devices in parallel. The step and repeat cycle takes <40 s.
- Multiple source materials can be selected in sequence. Thus lasers, amplifiers, modulators, detectors, and electronic components can be transferred. These devices can be transferred adjacent to each other thus allowing arrays of complex photonic circuits to be realized on the target wafers.
- The μTP approach allows the material to be transferred to structured substrates such as fully processed target wafers once the target area is locally flat.

2.1 Background to the Microtransfer Technique

A major advance in printing was made at the University of Illinois with the demonstration of kinetically controlled adhesion between an elastomeric stamp, an object, and a substrate (Meitl et al., 2006). Together with a technique where coupons of silicon could be held in place, and therefore registered, by silicon tethers which fractured in a controllable manner (Menard et al., 2004) allowed their transfer in a controllable, massively parallel manner with micron scale accuracy from a source wafer to a separate target substrate.

There are a number of excellent reviews on the technique and its general applications (Carlson et al., 2012; Yoon et al., 2015). The technique utilizes the viscoelastic properties of elastomeric materials and the associated motion-dependent adhesion properties. A master stamp is prepared with the array pitch required and is replicated with polydimethylsiloxane (PDMS) rubber. The stamp contains posts with dimensions corresponding to the desired size of coupons to be transferred. The stamp is retained on a transparent rigid support plate allowing the use of a vision recognition system for accurate transfer of the devices. The stamp is brought in contact with the coupons. A fast pulling motion is used to break the tethers at engineered locations picking up the selected coupons which are now adhered on the stamp posts. The coupons can be transferred and printed with the selected pitch/repetition to the target substrate and the stamp released by a slow movement. The stamp can be utilized repeatedly to consume all the

devices/coupons from the source wafer. The coupons can be transferred to multiple different target substrates.

Transfer printing has been demonstrated for many different devices in different configurations. Silicon solar cells with thickness of 10–20 μm and lateral dimensions of 50–100 μm × 1.4 mm have been transferred to glass and other substrates (Yoon et al., 2015). LEDs have been transferred to rigid and flexible substrates (Kim et al., 2011; Trindade et al., 2015). Near record efficiency solar cells have been achieved through stacking (Sheng et al., 2014). A five-junction solar cell comprised of a triple-junction GaAs-based cell mechanically stacked on a dual-junction GaSb/InGaAsSb cell was reported (Lumb et al., 2017) with an implied cell efficiency of 44.5%.

Many works have shown transfer of devices to flexible substrates.

μTP was first commercialized for the production of concentrator photovoltaic cells. Large-scale transfer tools were developed to achieve the production of the large volumes of multijunction cells which were transferred to metal substrates where world record performing solar modules were demonstrated (Furman et al., 2010). X-Celeprint (x-celeprint.com) is developing and licensing patented μTP technology.

2.2 Preparation of Devices for Microtransfer Print to Si Photonics

The μTP technique is implemented for Si photonics by the preparation of arrays of coupons on the source material that are then encapsulated and released from their native substrate by the selective etching of a sacrificial layer while the devices are held in place using a tethering system. Following transfer of the coupons, postprocessing on the target wafer may be required (Fig. 3). The entire process needs to be properly designed at the outset as there are several sequences possible. A key aspect to consider is the final coupling between the device and the waveguide. Butt coupling, evanescent coupling, and grating coupling to devices have all been implemented each with a specific relative positional tolerance requirement. The structuring of the material into devices (etching, contacts, etc.) can be performed in advance of the coupon preparation. This allows for the source wafers to be processed in a specialist foundry on the relevant wafer size without

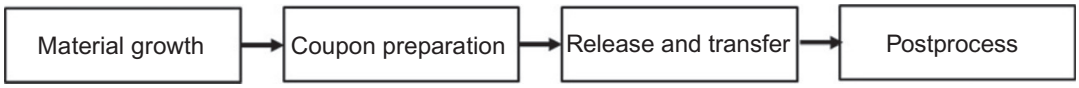

Fig. 3 Overview of process flow for the heterogeneous integration of diverse materials by microtransfer print.

limitations in the process technology and the devices to be optimally manufactured. In addition, this strategy allows for the devices to be tested in part or in full before transfer. This approach relies on the position tolerance of the transfer process and postprocessing steps to connect the devices. If the material alone is transferred then the alignment can be lithographically defined posttransfer. This approach requires foundry compatibility with the process technologies needed for the newly introduced materials and for the processing to take place on the new larger target wafers. The decision as to the best approach may also be determined by the density of transferred coupons.

Other considerations relate to the stress introduced though the process steps which are more significant due to the thin coupons used. They need to be managed in order to achieve the flattest coupons and thus the highest bonding yield and printing accuracy. The dimensions of coupons depend on the device type where, for example, long and narrow coupons are needed for laser or gain or waveguide-coupled elements. The target location is considered in relation to the optical, electrical, thermal, and mechanical interfaces. The devices can range from 20 to 800 μm on a side for grating-coupled photodetector and photovoltaic cells, respectively. The TP technology may not be as advantageous for larger devices.

2.2.1 Materials to be Transferred for Photonic Devices

Epitaxial structures grown on GaAs, InP, GaN, GaSb are used to create devices at relevant wavelengths. In addition, Ge deposited on Si provides a route to high-speed photodetection. Other photonic materials can be deposited on appropriate temporary substrates. In all situations, the μTP process seeks the inclusion of a release layer which could be the source substrate itself. The thickness of the release layer is chosen to be in the range of 500–1000 nm influenced by the ultimate bowing of the coupons after release which in turn is dependent on the stresses introduced by the fabrication processes. The subsequent layers are designed for the final device.

2.2.2 Preparation of Coupons

At a minimum it is necessary to etch mesas to define the coupons and to provide access to the release layer. The sidewalls of the coupons may need to be encapsulated to protect the other layers of the structure from being etched during the release process. If the devices are preprocessed then the various steps of etching waveguides, etching to buried contact layers,

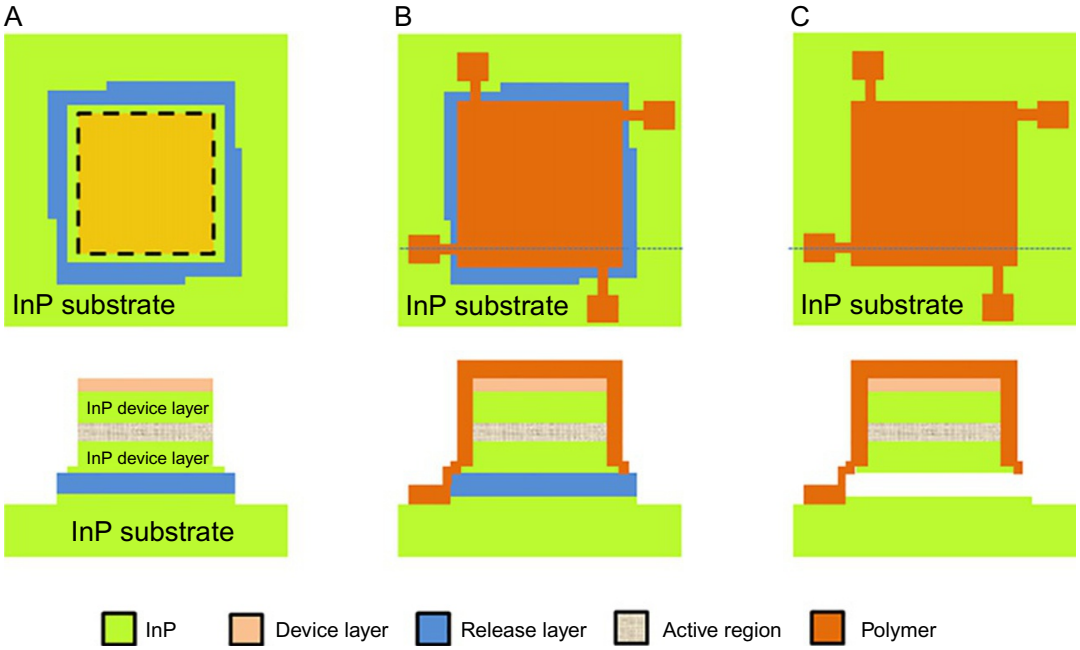

Fig. 4 Example process preparation of InP coupons for transfer (plan and cross-section at shown location). (A) Define respective mesas for the device and the release layer. (B) Resist tethering arrangement anchors the coupons to the substrate and prevents complete sealing of the release layer. (C) The release layer is etched resulting in suspended coupons.

formation of facets, deposition of dielectrics, and contact metallization are performed. Crucial to the eventual success is in managing the stresses in the coupons which can cause them to bend when released. Control can be achieved by deposition of layers with appropriate compensating stress. The overview of an example of the process sequence is shown in Fig. 4.

2.2.3 Tethering Systems

An anchoring system is needed to keep the devices stable and registered in place during their release from the source substrate. The anchor system must provide protection to the coupon, access for the etchant to the sacrificial layer, adequate adhesion to the substrate, stability during the undercut, rinsing, and drying steps and break easily and cleanly when the devices are being picked up. The material for the anchor system can be organic polymers such as standard photoresists that are shaped by lithography and made stiff by soft or hard baking. These materials can accommodate the height differences involved. Other choices for the anchor material are silicon dioxide, SiN, or the semiconductors themselves which can provide higher mechanical stability in a wider range of cases but can be more difficult to implement.

The engineering of a suitable anchor system strongly depends on the dimensions of the coupons, the materials involved, and the final application. Different tether shapes, dimensions, and configurations have been investigated for a range of photonics devices such as lasers, LEDs, photodiodes, and photovoltaic cells that have different thicknesses and lateral dimensions. It is possible to identify few general rules that usually can be applied to most of the anchor systems.

Resist anchors cover the coupon and are held to the substrate by a number of tethers. Some exposed regions on the sacrificial layer provide access for the etchant for the undercut to commence. The tethers are formed between these regions. The tethers are made by two main parts, a foot and a connection to the coupon. The foot should be large enough to provide adhesion to the substrate and not be peeled off during the pickup. Engineering of strong adhesion gradients along the narrowing tethers allows them to break in the desired location which is usually as close as possible to the coupon as this prevents flaps and debris which could affect the printing. The thickness of the polymer depends on the area of the coupons and the stiffness desired. The heat treatment of the resist alters its stress and mechanical properties. Finally, the number of tethers should be adjusted according to the perimeter of the coupon in order to withstand the capillary forces involved during the undercut.

An example of anchors for InP coupon transfer consists of 5 μm wide tethers arranged on a 40 μm pitch. The connection to the foot is kept of the same width for the first 1 μm to allow tolerance against misalignments during contact lithography without creating differences in the tether width, then is tapered down to 2 μm in order to allow a second breakage spot for the tether before encountering the foot which has to be the largest possible. The access regions protrude about 5 μm. The width of the tether foot is limited by this width. The feet can be enlarged to touch each other when 5 μm from the grating, this provides enough space for the etchant to access the sacrificial layer with proper transport properties. Coverage of the substrate and the free spaces between anchors of different coupons is recommended to reduce potential contamination by excess etched material. A third breakage point can be introduced along the foot by creating a slit. Also, V shapes at the meeting point between the connection and the foot can offer a higher gradient in the case of a tilted peeling of the tethers. Fig. 5 shows an example layout while Fig. 6 shows optical images of the tether system applied to the release of InP device coupons.

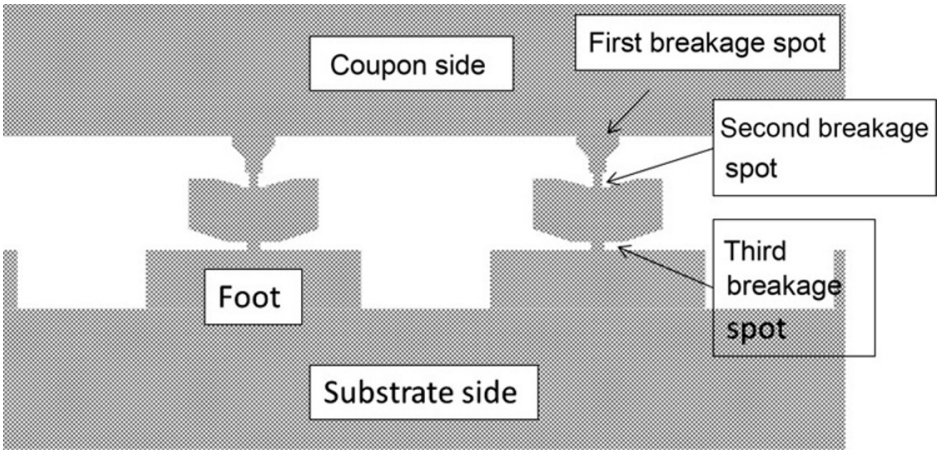

Fig. 5 Layout example of a tether retaining a coupon in place during and after undercut etching.

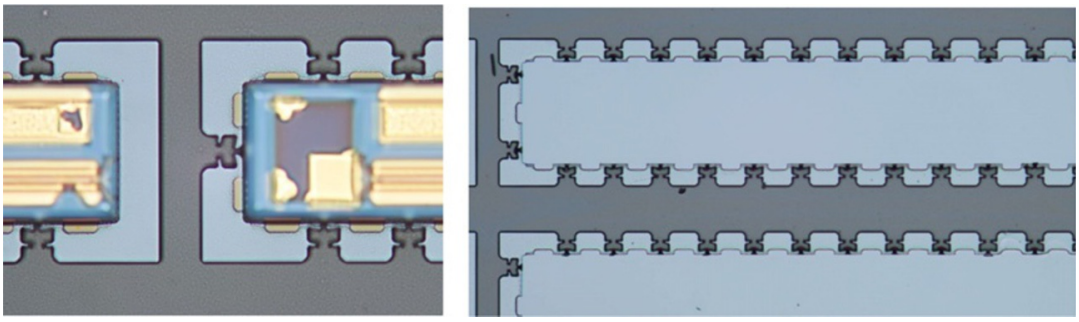

Fig. 6 Microscope image of resist tethering system showing devices held in place after release etch and before pickup (*left*) and after device pickup showing remaining InP stub and resist anchors (*right*).

2.2.4 Release Etching

The coupons can be released using dry or wet etching techniques. Dry techniques include the selective etching of Si and Ge in XeF_2 vapor which is selective against surrounding layers of SiO_2 and GaAs, respectively. More commonly, the coupons are released using wet chemical etching. Very high selectivity and very smooth etching are desired as otherwise the bottom surface of these coupons, i.e., the interface with the target substrate, will become shaped requiring thicker adhesives. Selective wet etchants are known for many material combinations (e.g., Hjort, 1996) and some examples are given in Table 2.

After release etching, the fragile coupons are typically rinsed in water and dried in air. The coupons can collapse during this stage, generally caused by internal stress, and resulting in unpickable coupons so stress management is of critical importance. Remarkably, there is no need for critical point drying

Table 2 Examples of Selective Etchants for Selected Layers Against Their Surrounding Combinations

Layer to be Etched	Surrounding	Etchant
InGaAs	InP	$FeCl_3$
InAlAs	InP	$FeCl_3$
InP	InGaAsP	HCl
InAlP	GaAs	HCl
$Al_xGa_{1-x}As$ $(x > 0.5)$	GaAs	HF, HCl
SiO_2	Si	HF (liquid or vapor)
Si	SiO_2	Tetramethyammonium hydroxide (TMAH), KOH $XeFe_2$
Ge	GaAs	$XeFe_2$

which is probably due to the fact that the selective etchants used leave the adjoining surfaces hydrophobic. It is also noteworthy that coupons of several hundred microns in dimensions can be undercut with submicron thick release layers and be easily picked up to die to the tethering process. After the removal of all coupons, it is potentially possible to recover the substrates for reuse.

We now discuss the development of a release layer for InP-based epitaxial structures which are the mainstay for the highest performing devices in the 1300–2200 nm wavelength range. The lattice-matched heterostructures provide many combinations of layers which can be selectively etched with the interface between -As and -P containing layers being attractive due to a selection of potential etchants. A release layer of InGaAs was shown to be effective for the realization of multilayer air–InP reflector structures (Kusserow et al., 2008). While many acid mixtures provide selective etching the highest selectivity was obtained using $FeCl_3$:H_2O (2:1) at temperatures below ambient. The optimum temperature is in the range of 5–8°C since the etch rate decreases and precipitation occurs as the temperature is lowered below 1°C.

The selectivity between InGaAs and InP is high for the ⟨010⟩ direction which is at 45 degree to the wafer flat (011). This requires the coupons be orientated along those directions for the shortest release time and thus the highest selectivity. However, ridge waveguides should be oriented along/perpendicular to the major flat for taper formation in InP using existing

wet chemical processes. This results in release times of many hours, consequent dishing (nonflat profiles) of the released surface, and limiting the width of the coupon. A solution is found through the use of InAlAs as a release layer (O'Callaghan et al., 2017). InAlAs etches at a faster rate in the same $FeCl_3$:H_2O mixtures, and the etch rate has a low dependence on the crystal direction. Fig. 7 shows optical microscope images comparing partly underetched circular mesas that used 500-nm thick InAlAs layers and InGaAs layers, respectively. No crystallographic dependence for the etching of InAlAs could be observed, while there is substantial dependence in the case of InGaAs. The quality of the bottom surfaces of the coupons can be assessed by atomic force microscopy and white light interferometry. It is found that the growth conditions during the switch from an As layer to a P layer play a role in the smoothness of an InAlAs–InP interface and that an interface layer of InGaAs assists in achieving a smoother interface. The best smoothness was obtained with a 50-nm InGaAs thick layer (Fig. 8). Using this release bilayer structure enables the orientation of coupons along any chosen crystal axis without penalty and leads to flatter surfaces after the release of wider coupons.

A similar approach can be used for the release of GaAs structures using a AlGaAs or AlInP release layer.

An interesting, if unwanted, result can arise if the layers to be released are thin and are strained by, for example, a protection dielectric layer such as SiN_x. The effect in question occurs as the etch release comes to it last stage

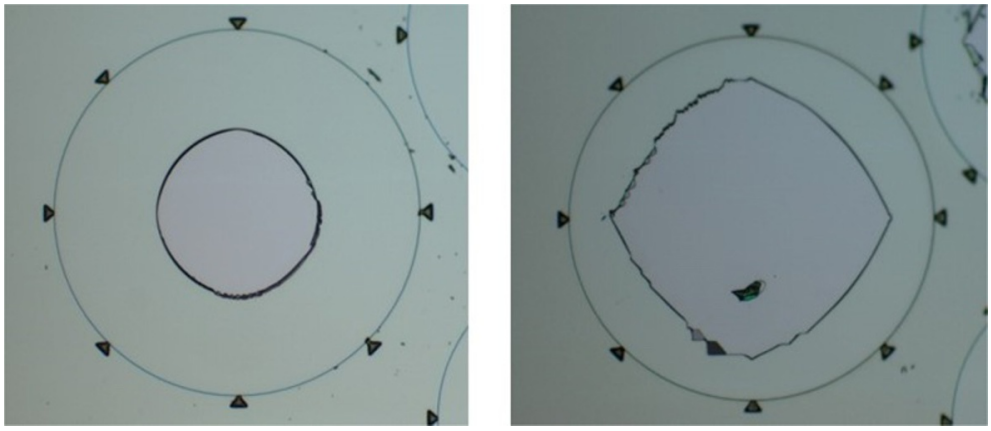

Fig. 7 Microscope images of release process for 300 μm diameter circular mesas at midstage following tape-removal of the undercut section. *Left* shows the residual mesa resulting from a 500-nm thick InAlAs release layer where it is evident that the undercut process has only a minor crystallographic dependence and *right*, the residual mesa with a 500-nm thick InGaAs release layer where strong crystallographic dependence is evident. In addition, the etch rate for the InAlAs is many times as that for the InGaAs.

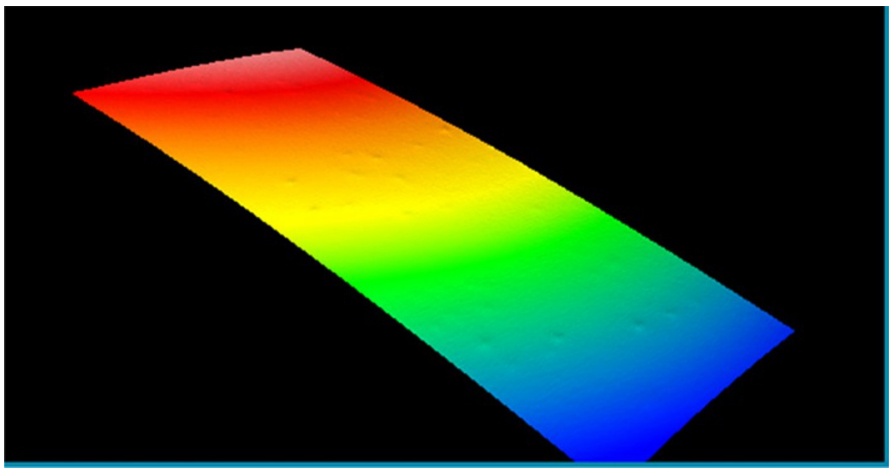

Fig. 8 White light interferogram of the bottom side of an InP coupon after release etching of an InAlAs/InGaAs bilayer.

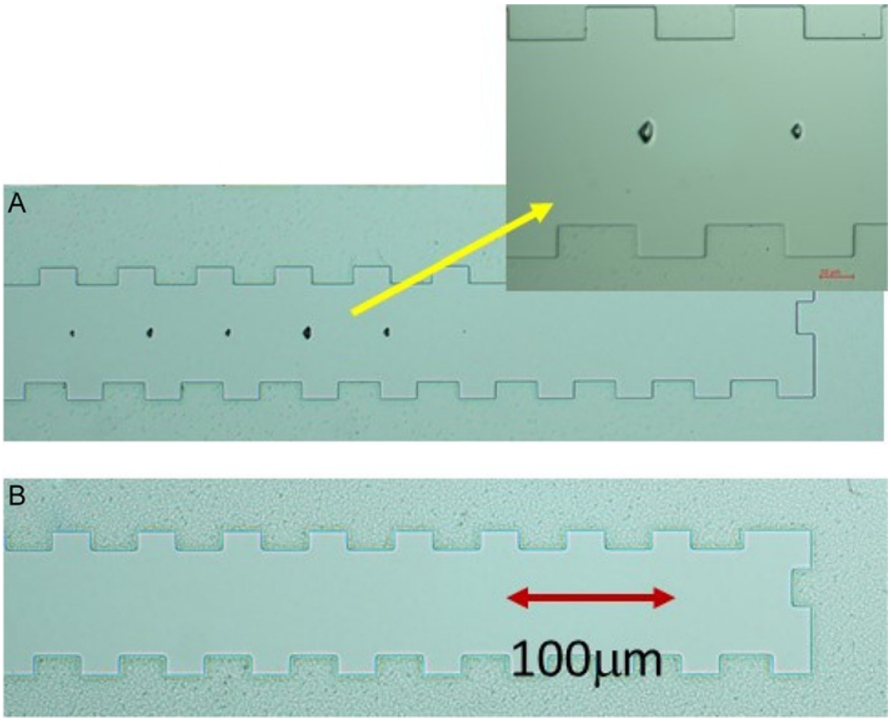

Fig. 9 Optical images of stress induced pillars created after etching with a stressed layer on the coupon (A) and its resolution with a stress managed layer (B).

and pinches off the final part of the release layer. At that stage, there is considerable stress on the coupon at these points which can lead to breaks in the coupon and ingress of the etchant to unwanted locations. In an example of resultant pillars shown in Fig. 9, the upper sample had a thick stressed SiN layer whereas the lower sample had the SiN mask removed and no defects were present. Both samples were etched in $FeCl_3$:H_2O 1:2 for 20 min at 1.5°C.

2.2.5 Transfer Process

A stamp created from PDMS with a single protruding post or an array of protruding posts separated by the required grid arrangement for the target wafer is used to pickup the devices. Note that the source wafer has a higher density of coupons than the target and is structured such that there are an integer number of coupons between those being picked by the stamp. In other words, there is a defined magnification between the source and the target. The grid spacing may be different in the two lateral directions. Picking of the devices is done by pulling back the stamp fast from the source wafer. It is essential that the target location be clean and flat and that the coupons themselves do not have any residue or debris from the tether breaking and undercut etching steps. Overpressure can be applied to the coupons. The coupons are not damaged by this process. The transfer is carried out in air. The coupons are released from the stamp by a slow peel motion. Generally the process is carried out at ambient temperature which is necessary to maintain registration over large areas. Release can be improved at higher temperatures at the expense of alignment and softening of the PDMS above 60°C. The adhesion of the coupons to the target depends on the properties of the mating surfaces. Polymers, including benzocyclobutene (BCB), polyimide, polyurethane, and intervia can be spinned on or spray coated on the target substrate to provide a flat adhesive layer. These polymers have excellent adhesive characteristics with low moisture absorbance, low curing temperature, and low stress. They can also act as a stress buffer. The choice of the adhesion layer thickness is determined by the need for evanescent coupling, the required thermal properties and the mechanical properties needed to accommodate stress. This results in thicknesses for the adhesive between 50 nm and 2 μm. The adhesion can be improved by oxygen plasma or thermal pretreatment and by curing of the polymer posttransfer. Direct, adhesive less, van der Waals adhesion can be achieved if the released surfaces are flat and smooth enough which allows for potential electrical connections and improved heat sinking of the devices.

Alignment accuracy requires high-contrast (metal) registration features on the source and target both within the field of view of the vision system. Positional accuracy of ±0.5 μm has been demonstrated (Ye et al., 2018a). After transfer, the tethers are removed by oxygen plasma in the case of resist. This allows the devices to be probed or to be connected up using standard process steps of planarization, via opening and metal deposition. The transferred coupons will withstand the thermal budget required which is typically <300°C.

3. EXAMPLES OF INTEGRATION

3.1 Etched Facet Laser on Si

Stand-alone lasers that are a few microns thick and that are transferred to a selected substrate are a basic example of the technology. The starting wafer to achieve such a device requires that an etch release layer and a lower cladding of sufficient thickness to isolate the laser mode from the target substrate to be included (Fig. 10). The width of the coupon is set by the etch selectivity. The lasers can be fabricated posttransfer (Justice et al., 2012) or pretransfer (Loi et al., 2016). The standard process steps of defining a ridge waveguide and p- and n-type ohmic contacts need to be supplemented by a means of making a resonator by using etched facets, using resonant or grating structures in the silicon waveguide circuit or within the III–V material. An etched facet was utilized where smooth and vertical facets can be obtained by inductively coupled plasma etching. A high reflection coating on the rear facet can be achieved by the angled evaporation of a reflective metal on a dielectric protection layer. The coupon is made longer to facilitate probing directly on the wafer. Additional steps as discussed earlier are implemented to allow the release of the laser coupons. The lasers are bonded directly to silicon and characterized in continuous wave (CW) mode. Fig. 11 shows the temperature-dependent light–current characteristics of the laser where improved temperature performance is obtained for the transferred lasers compared to the lasers on the source wafer due to the superior thermal conductivity of silicon (130 W/mK) over InP (63 W/mK).

Such laser (or gain) chips can be edge coupled to silicon waveguides as currently done using flip chip on silicon photonic platforms. μTP will allow multiple chips to be placed in close proximity. The laser chips have to be aligned with respect to waveguides where the reference height on the silicon

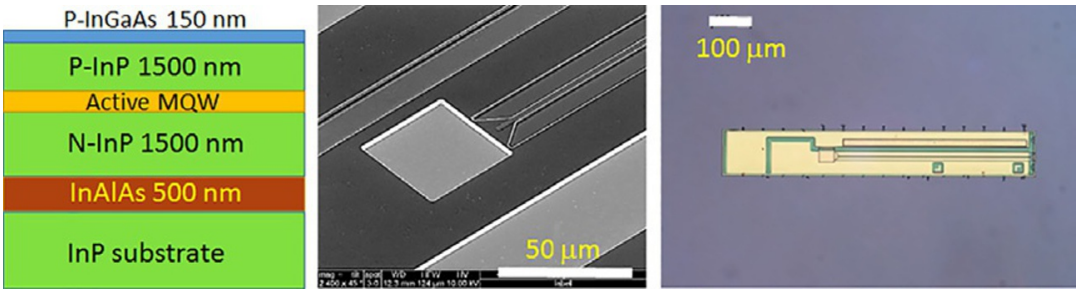

Fig. 10 Schematic layer structure for a 1550 nm emitting laser (*left*), scanning electron microscope image of an etched facet (*center*), and optical microscope image of transferred laser prior to tether removal (*right*).

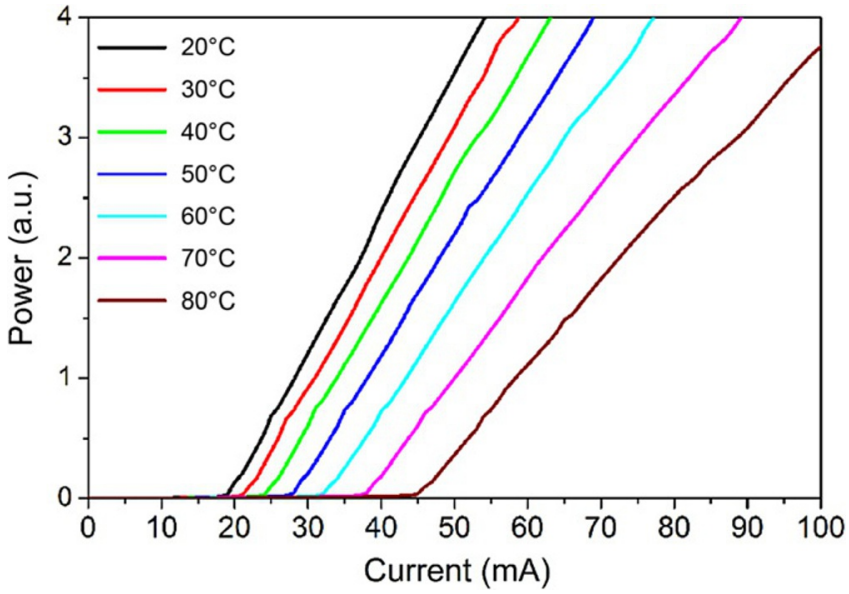

Fig. 11 Temperature-dependent light–current characteristics of 1550 nm etched facet laser transferred to Si.

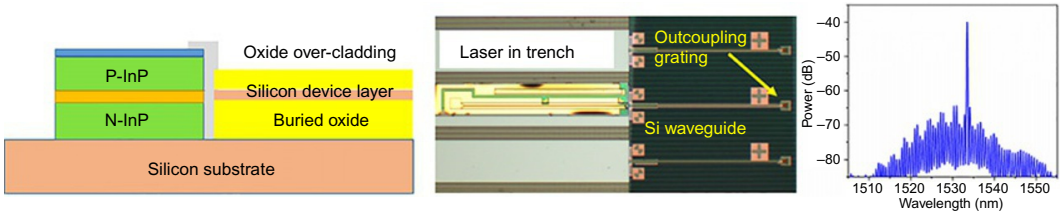

Fig. 12 Edge geometry for laser–waveguide coupling (*left*) using microtransfer printing, optical image of laser printed with respect to the waveguide (*center*), and outcoupled spectrum from grating (*right*).

photonics wafer is controlled by the thickness of the buried oxide layer. The laser waveguide height is then referenced with respect to this surface. The lateral alignment of the laser relies on high-contrast fiducials present on both the laser and the target substrate. Facets are etched in the silicon photonics wafers at the waveguide end using a chrome mask. To obtain the highest coupling efficiency, the laser mode field should be matched to that of the Si waveguide by using spot size converters. Fig. 12 shows an optical microscope image of the aligned laser that is recessed from the waveguide facet by ~3 μm. The spectrum from the laser when outcoupled using the fiber-to-chip grating coupler on the waveguide is shown.

3.2 Evanescent Laser on Si Using a Tapered Coupling

Evanescent coupling between a gain material and silicon waveguide containing a distributed feedback Bragg (DFB) reflector or a ring resonator-based

reflector is a second approach for creating an integrated laser. This has been widely implemented with die-to-wafer bonding using tapered waveguides on the silicon and III–V to achieve coupling. The same approach can be implemented with transfer printing noting that the interface to the silicon waveguide is grown on the III–V wafer immediately after the release layer. This allows for the growth of structures for electrically injected components in a p-on-n configuration which is often preferred over an n-on-p configuration required for wafer bonding due to the diffusion of the standard p-dopant (Zn) during wafer growth. The first demonstration of evanescent coupling to SOI waveguides using transfer printing was an optically pumped InGaAsP quantum well structure by De Groote et al. (2016). A thin BCB layer was used to adhere the coupons to the SOI waveguides and allowed for structuring of aligned tapered waveguides for optical coupling. The optically pumped LED showed a 3 dB bandwidth of 130 nm in line with devices realized using a traditional die-to-wafer bonding method. An electrically pumped DFB laser integrated on and coupled to a silicon waveguide circuit using transfer printing was realized by Zhang et al. (2018). Coupons of $40 \times 970\,\mu m^2$ of AlInGaAs gain material were picked from the growth wafer and transferred to SOI waveguides where a second-order grating had been defined with a period of 477 nm and a duty cycle of 75%. Postprocessing was used to define the III–V guiding region, the adiabatic taper structure for coupling to the silicon waveguide layer and the ohmic contacts (see Fig. 13A–C). The resultant laser had a threshold current of 18 mA and a maximum single-sided waveguide-coupled output power above 2 mW. Single mode operation around 1550 nm with >40 dB side mode suppression ratio was demonstrated as shown in Fig. 13D.

An alternative route for the laser is to define the feedback structure in the III–V structure. A 1D nanobeam laser based on a three quantum well InGaAsP gain structure was coupled to a silicon (SOI) waveguide with a coupling efficiency of 83% using transfer printing (Lee et al., 2017). The asymmetric photonic crystal laser was first created by etching nanoholes into the 280-nm thick structure. The 7–8 μm long nanobeams were tethered in place with the thin semiconductor itself during the undercut etching of an InP layer. The nanobeams were then transferred to a structured SOI wafer and placed to bridge a gap in the waveguide. The best positional accuracy was better than 0.3 μm and an angular misalignment of <1.3 degree. The experiment validated simulations that a very short (3.2 μm long) overlap was an efficient vertical coupler. When optically pumped with a 980 nm laser, lasing was obtained at a pump power of 0.2 mW and strong light

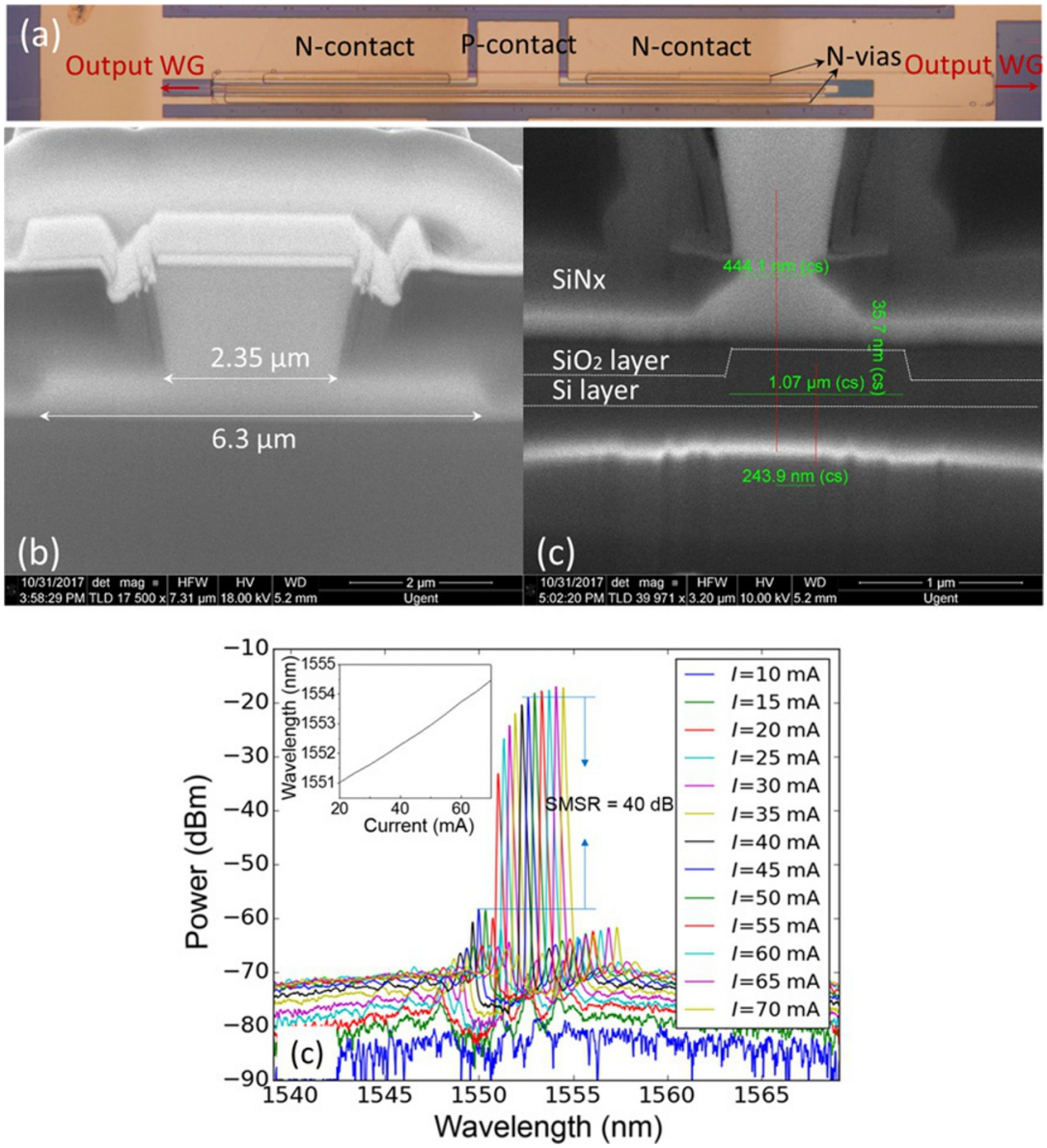

Fig. 13 (A) *Top*-view of the evanescently coupled III–V-on-silicon DFB laser; (B) cross-section of the laser mesa (B) and taper tip (C); (D) output spectrum of the laser as a function of bias current. *Reproduced with permission from Zhang, J., et al., 2018. Transfer-printing-based integration of a III–V-on-silicon distributed feedback laser. Opt. Express 28, 8821–8830.*

emission was measured at the end of the SOI waveguide with a narrow emission peak around 1550 nm.

Photonic crystal nanobeam structures were also fabricated in a 200-nm thick GaAs slab with six layers of InAs quantum dots (Osada et al., 2018). The structure was grown on a 1-µm thick $Al_{0.3}Ga_{0.7}As$ release layer. The nanobeam laser structures were released and transfer printed to SOI waveguides. Lasing emission at 1170 nm was measured under pulsed operation for a low pump power at a temperature of 8 K.

More complex components such as subcircuits can be integrated by evanescent coupling using transfer printing. A first exercise in proving the technique was coupling between a conventional SOI waveguide substrate and coupons containing comparable passive SOI waveguides which looped the light back to the conventional waveguides (Ye et al., 2018a). The coupons were encapsulated in amorphous silicon and used narrow triangular-shaped Si tethers. Stress control was vital to prevent coupon collapse during the HF release etch of the underlying SiO_2. The coupling interfaces were designed to be tolerant of misalignments of ± 1 μm. Adiabatic tapers show a loss per interface of 1.5 dB at 1310 nm while directional couplers showed a loss of only 0.5 dB at 1600 nm. Following that work, the authors demonstrated the integration of waveguide-coupled germanium photodiodes onto passive silicon waveguide circuits (Ye et al., 2018b). In the process Ge p–i–n photodetectors were fabricated on SOI wafers. The coupons (310 μm × 50 μm) contained a trident coupler designed for evanescent coupling with the target SOI. The responsivity of the transferred detector was 0.66 A/W with a bandwidth of 14 GHz. The device was used to show 40 Gb/s transmission. This strategy opens many possibilities for subcircuit integration.

3.3 Grating Coupling Photodiodes on Si/SiN

A third way by which components can be coupled with the Si or SiN waveguides is by using grating coupling. The integration of III–V photodiodes on a silicon-based PIC can be realized by transfer printing substrate illuminated p–i–n or metal–semiconductor–metal (MSM) photodetectors on a grating coupler structure defined in the silicon or SiN waveguide layer. This was recently demonstrated by Chen et al. (2018) where GaAs MSM photodetectors were defined on the GaAs wafer, on top of an $Al_{0.9}Ga_{0.1}As$ release layer. After device encapsulation the release layer is etched using HCl. The released devices were transfer printed to a SiN waveguide circuit containing grating coupler structures to interface with the GaAs MSM device. Microscope pictures of stand-alone surface-illuminated MSM detectors and waveguide-coupled bottom-illuminated devices are shown in Fig. 14. The dark current is 22 nA for a 70 μm × 70 μm device, while it is 7.2 nA for a 30 μm × 30 μm device at 2 V bias. For 850 nm wavelength the responsivity is about 0.1 A/W. 20 GHz bandwidth is measured and open 40 Gbps eye diagrams are realized.

A second example is the coupling light from the SOI to InGaAsP photodiodes with a bandgap absorption of 1370 nm (Zhang et al., 2017).

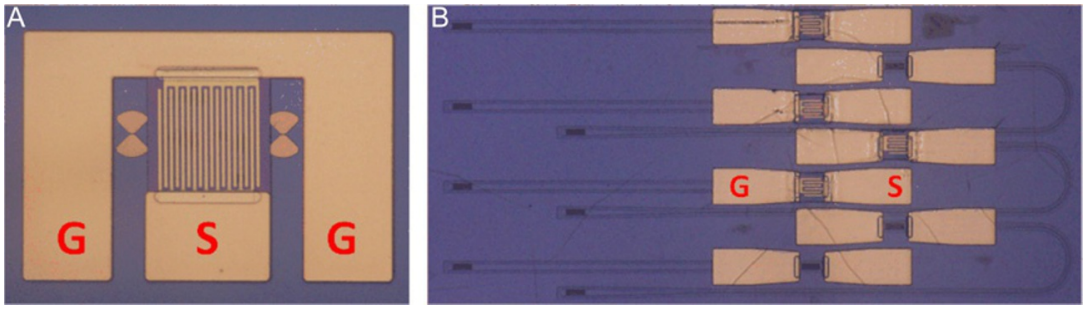

Fig. 14 Panel (A) surface-illuminated 70 μm × 70 μm MSM photodetector; (B) *bottom*-illuminated waveguide-coupled MSM detectors. *Reproduced with permission from Chen, G., Goyvaerts, J., Kumari S., Van Kerrebrouck, J., Muneeb, M., Uvin, S., Yu, Y., Roelkens G., 2018. Integration of high-speed GaAs metal–semiconductor–metal photodetectors by means of transfer printing for 850 nm wavelength photonic interposers, Opt. Express 26, 6351–6359. Copyright 2018 OSA.*

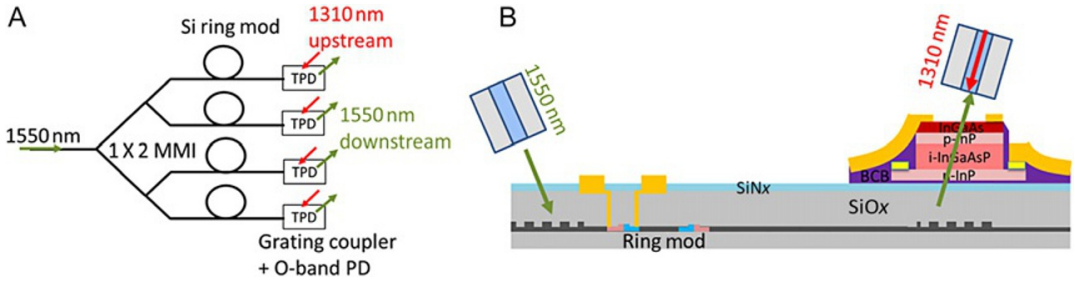

Fig. 15 (A) Schematic layout of the III–V-on-silicon FTTH transceiver array and (B) schematic cross-section of one transceiver. TPD: transparent photodetector. *Reproduced with permission from Zhang, J., et al., 2017. Silicon photonics fiber-to-the-home transceiver array based on transfer-printing based integration of III–V photodetectors. Opt. Express 25, 14290. Copyright 2018 OSA.*

The circuit for a four channel transceiver is shown in Fig. 15 where fiber delivered 1550 nm "downstream" signals are transmitted through the transfer printed 50 μm × 50 μm photodiodes and coupled to a second fiber. That fiber delivers "upstream" signals at 1310 nm. A ring resonator circuit is used to select the downstream wavelengths. The response of the photodiodes at 1310 nm is 0.39–0.49 A/W while at 1550 nm the response is <0.03 mA/W. The 11.5 GHz bandwidth photodiodes were capable of receiving 10 Gb/s signals across the O-band.

3.4 Other Laser Cavity Structures Enabled by Transfer

Microring lasers transferred to glass (Corbett, 1998) and to the end of an optical fiber (Corbett et al., 2002) were demonstrated to lase under CW optical pumping around 1500 nm wavelengths. The microrings with outer diameters of 5.8 μm, width of 1 μm, and a thickness of 0.41 μm

contained four quantum wells. The threshold pump power for CW operation was 80 μW. Recently Fan et al. (2017) introduced an intermediate polypropylene carbonate intermediate layer between the devices and the PDMS stamp as a thermal release layer for the transfer of GaAs-based nanoring devices emitting in the 1 μm wavelength range. 100-nm thick AlAs etched in dilute HF served as the release layer for the nanorings. GaAs-based quantum dot-based microring lasers tethered in place by the material itself were transferred to a silver-coated silicon wafer were shown to lase in a plasmonic mode under pulsed operation (Tamada et al., 2017).

A very exciting prospect is the realization of compact VCSEL-like structures. An optically pumped laser emitting around 1450 nm consisting of two high index contrast photonic crystal silicon membrane reflectors with a III–V InGaAsP quantum well heterostructure as the gain medium was realized by transfer printing (Yang et al., 2012). Subsequently, bandedge lasers consisting of a transfer printed active region printed on photonic crystal feedback structures have been realized on both SOI and Si. A threshold of 320 W/cm^2 was achieved for a device emitting at 1540 nm. Such design permits a large mode volume while retaining a single spatial mode.

3.5 Interconnection on Silicon

Polymeric based waveguides are useful for light signaling in datacenters and in high-performance computers at length scales where silicon is too expensive. The light can be coupled to and from silicon waveguides using adiabatic tapered coupling schemes (Dangel et al., 2018). Polymer platforms have also been developed (Zhang et al., 2015) and they need hybrid integration of active components to advance the functionality. μTP can assist with the heterogeneous integration of such components. An example of a simple optical interconnect consisting of an LED and photodiode connected by a polymer waveguide is shown in Fig. 16. LEDs are preferred due to the lack of a threshold current. Wavelength around 1.55 μm is initially selected to avoid any absorption in silicon circuits. The optical interconnect is realized by prefabricating the LED and photodetector and then transfer printing the devices to defined alignment locations on the target silicon substrate. The circuit is designed to operate as a low power stand-off optical switch and with 300 μA in the LED a photocurrent signal of 0.3 μA is obtained in the photodiode.

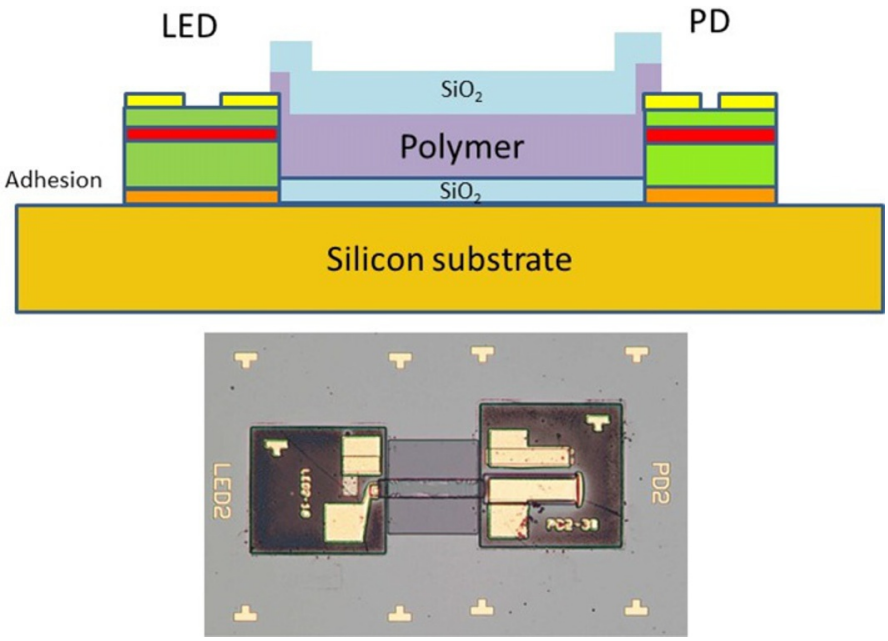

Fig. 16 *Upper* is a schematic cross-section of the optical link containing transfer printed LED and PD while *lower* is the realized connection.

4. CONCLUSIONS

μTP is emerging as a versatile technique for the heterogeneous integration of active and passive components on silicon. It enables the close integration of unique materials not possible by other means. The use of the technique requires engineering of the integration strategy, careful preparation of the starting wafers, and optimization of technological processes for accurate, stress-free transfer of materials, and devices. Alignment is a key issue of silicon photonics and can be addressed through postprocessing of the coupons or by the design of tolerant coupling structures. While many examples of its use for silicon photonics have been shown here it is noted that the work is very recent and is still in an early stage of development. Many more devices can be envisioned to be integrated such as optical isolators, filters, and electronics. The close proximity of the driving electronics can improve signal delivery and reduces the size of bond pads thereby reducing capacitances and allowing higher bandwidth.

Array selection is ideally suited to the production of large numbers of circuits on each wafer thus allow photonic circuits to be produced at low cost for consumer applications. Initial studies have shown that the transferred components pass the challenging reliability specifications. μTP has been used

to produce devices in commercial volumes. The technique is now being made available through semiconductor foundries (see microprince.eu).

There are many applications with a need for diverse devices to be cointegrated on a common platform. μTP is an important technology for the development and implementation of new integration concepts.

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