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III-V selective area growth and epitaxial functional oxides on Si: from Electronic to Photonic devices

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This review paper presents the challenges for the monolithic integration on silicon substrate by heteroepitaxy of III-V semiconductors selective area growth as well as epitaxial functional oxides. The heteroepitaxy of these materials on a common Si platform would allow the integration of new functionalities and advanced devices in both electronic and photonic areas.

I. Introduction

The semiconductor ICT industry continues its never-ending pursuit of new approaches for fabricating integrated circuits, to reduce fabrication cost and improve device performances. In this paper, we will present and review the current challenges for the integration onto silicon substrate of new materials such as III-V semiconductors and epitaxial functional oxides that can potentially be used in future generation of electronic and photonic devices. Regarding electrons-based devices ie. logic devices, recently, there has been an increase of interest in the integration of alternative channels with higher mobility than silicon, offering the possibility to further boost the performances of next Fin-Field-Effect-Transistors (FinFET) and Vertical-Field-Effect-Transistors (VFET) generations. In that context, due to their potential intrinsic properties (1), the heterogeneous integration of III-V semiconductors, such as InP and/or InGaAs compounds epitaxially grown by Metal Organic Vapour Phase Epitaxy (MOVPE) onto both 300mm standard Si(001)-oriented and Si(111)-oriented substrates, have been attracting much attention as building blocks for future FinFET and VFET devices, respectively. Concerning photons-based devices integrated on Silicon substrate, we will mainly focus in this paper on two specifics applications. First, the light source or LASER (Light Amplification Source of Emission of Radiation) device, which is made of direct band gap InP or InGaAs semiconductors grown selectively in trenches also by MOVPE and secondly optical modulators devices based on epitaxial ferroelectric material such as $BaTiO_3$ perovskite oxide grown on Si(001) substrate by molecular beam epitaxy (MBE).

II. Experimental

The III-V heteroepitaxy has been performed in a 300 mm production AIXTRON Crius MOVPE reactor, equipped with a vertical showerhead injector shown on Figure 1(a). The group-III precursors used was trimethylindium (TMIn), trimethylgallium (TMGa), trimethylaluminium (TMAl), and the group-V sources are tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP). During the growth, the reactor pressure can

vary from low pressure below 20 mbar up to high pressure above 500 mbar with a H_2 total flow of 48 slm as carrier gas.

The $BaTiO_3$ epitaxy were carried out using a Riber 200 mm molecular beam epitaxy cluster as shown on Figure 1(b). The BTO layer was grown on a 200mm Si(001) substrate via a monocrystalline $SrTiO_3$ buffer layer. Ba,Sr and Ti were evaporated using two standard Knudsen effusion cells and an electron beam gun, respectively. A remote plasma source was used for the generation of atomic oxygen. Ba/Ti and Sr/Ti stoichiometry was achieved by calibrating the metal fluxes using a quartz crystal microbalance, and an excellent stability of the Ti flux was achieved using an real time flux measurement from a mass spectrometer with a feedback loop on the source power during the growth.

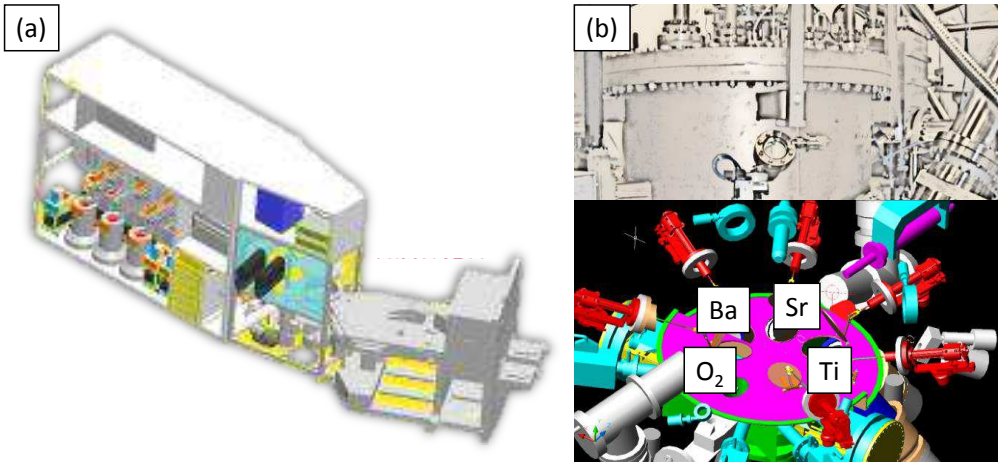

Figure 1. (a) Schematic of the 300mm MOVPE tool installed in imec clean room used for the III-V selective area growth.(b)Schematic of the 200mm MBE oxide reactor with the different sources used for epitaxial oxide growth.

III. Electronic (logic) devices

In the following part, epitaxial challenges for the monolithic integration of high mobility channels onto silicon substrate will be reviewed for next generation of FinFET and VerticalFET devices. In this context, Indium Gallium Arsenide compound semiconductor ($In_xGa_{1-x}As$), with high Indium concentration ($x > 0.5$) is considered as a candidate of choice for n-type channel due to its intrinsically superior electron mobility and high saturation velocity (2,3,4). However, the integration of III-V compounds on Si substrates is still a challenge since many years, due to the large lattice mismatch and the polar (Si) / non-polar (III-V) interfaces resulting in the generation of crystalline defects in high density. The resultant defects such as misfit / threading dislocations, twins, stacking faults and anti-phase boundaries, would strongly degrade the final device performances. Several options have been considered to obtain high quality single crystal III-V compounds on Si with low defect density: strain relaxed buffers (5,6), epitaxial lateral overgrowth (7,8), rapid melt growth (9), the defect confinement technique (10,11) and the selective area growth (12). In our case we will mainly concentrate on the use of the selective area growth approach which has attracted great interest due to the possibility of obtaining high quality III-Vs on Si. The main concept is based on patterning active regions before the epitaxy step with nanometer-scaled Si opening areas where the III-V semiconductor will be grown.

A. III-V FinFET devices

Regarding III-V FinFET devices, the III-V semiconductors are grown usign Selective Area MOVPE in trenches. For this, standard SiO_2 STI patterning was applied on 300 mm on-axis Si (001) substrates to realize 250 nm deep trenches with trench widths ranging from 16 nm to 500 nm. On the mask, the average active area exposed to the III-V layers deposition was kept constant at 10% of the total Si wafer surface. The trenches are aligned along the [110] and orthogonal [1-10] directions. Silicon recess engineering obtained by wet Si etching using TMAH (5% @ 80˚C) will stabilize the {111} planes of Si in the bottom of the trenches. This allow to initiate the III-V growth from a V-grooved enclosure with an atomically smooth (111) surface (12,13). Ideally, trenches with a minimum aspect ratio between the width and the height higher than 2 is required to block part on the defect onto the oxide sidewall. The III-V compound semiconductor is then grown selectively on a (001)-oriented Si on axis substrate but while (111)-oriented defects are efficiently trapped perpendicularly to the trench as depicted on Figure 2(a), the key challenge of this technique resides in the impossibility to trap the (111)-oriented defects along the parallel direction of the trench as shown on Figure 2(b). This makes the selective area growth approach a completely different concept compared to notions such as defect confinement technique, aspect ratio trapping and necking effect. Thereby, in the case of selective area growth, epitaxial conditions and growth mode are key to obtain low defect density III-V on Si. The best option for the integration on Si of ternary InGaAs compounds would be to make use of InP binary semiconductor as a buffer for the lattice matched $In_{0.53}Ga_{0.47}As$ channel (14,15,16,17,18).

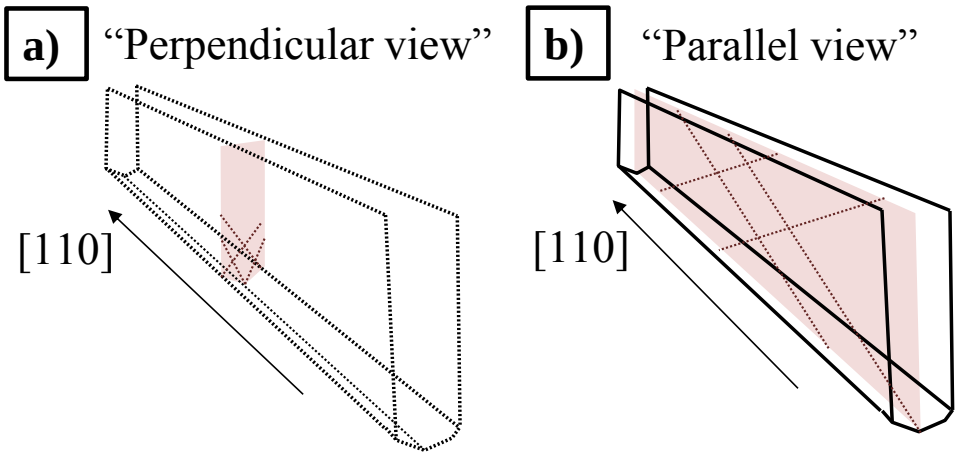

Figure 2. III-V selective area growth on Si(001) in trenches. (a) ***“Perpendicular view”*** *presenting an efficient trapping effect of (111)-oriented defects from the III-V/Si interface. (b)* ***“Parallel view”*** *where (111)-oriented defects are not trapped in the direction along the trench.*

We report then in a first part on the InP buffer heteroepitaxy on STI patterned Si wafers in scaled trench widths dimensions (W < 20 nm) which relies on a two-step growth. First, the native oxide from the bottom STI surface is thermally desorbed by a high temperature bake above 800°C in H_2 at low pressure. Then, the substrate temperature was cooled down to a lower temperature (T_G < 350°C) to initiate the nucleation layer epitaxy (12). Prior to the nucleation layer, the surface is exposed to

Arsenic under 550°C, at high pressure to form one monolayer of As-terminated surface which will promote the wetting of InP at low temperature. After the low temperature nucleation step, the temperature was ramped up to T_G = 550°C to obtain a high crystalline quality and uniform heteroepitaxy of InP layer (12) as presented on the figure 3 showing the scanning electron microscopy (SEM) images in (a) 20nm, (b) 40nm and (c) 100nm widths trenches.

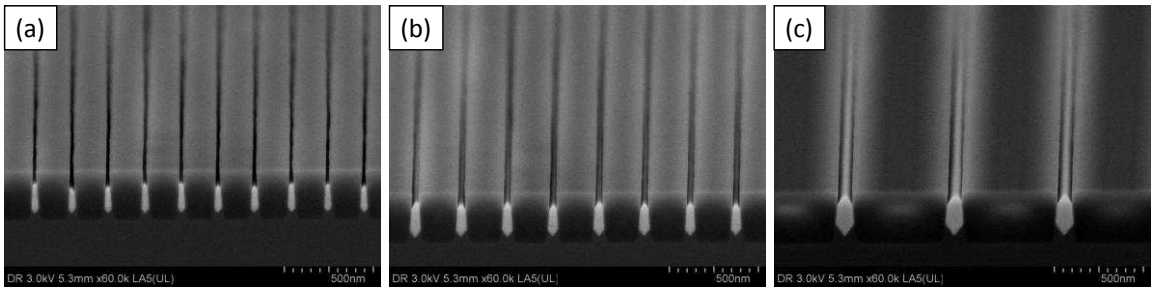

Figure 3. Tilted view SEM images after InP heteroepitaxy on patterned Si(001) in (a) 20nm, (b) 40nm, (c) 100nm widths trenches.

X-Ray Diffraction was performed on InP/Si heterostructures using *in-line* 300mm JVX 7300 X-Ray diffraction tool. Figure 4(a) is the ω-2θ scan recorded along the sample normal. The X-ray spectra of the InP/Si sample present an intense peak centred at ω-2θ origin for the (0 0 4) Bragg reflections of the Si(001) substrate and one other intense diffraction peaks centred at ω-2θ = - 10600 arcsec corresponding to the diffraction of the (0 0 4) planes of the 250-nm-thick InP layer. Furthermore, the ω-scans of the InP (0 0 4) Bragg reflections, used as a quality criterion for the InP crystalline perfection, are presented in Figure 4(b). The InP layer grown directly on Si presents a very narrow diffraction peak with $FWHM_{InP/Si}$ = 490 arcsec.

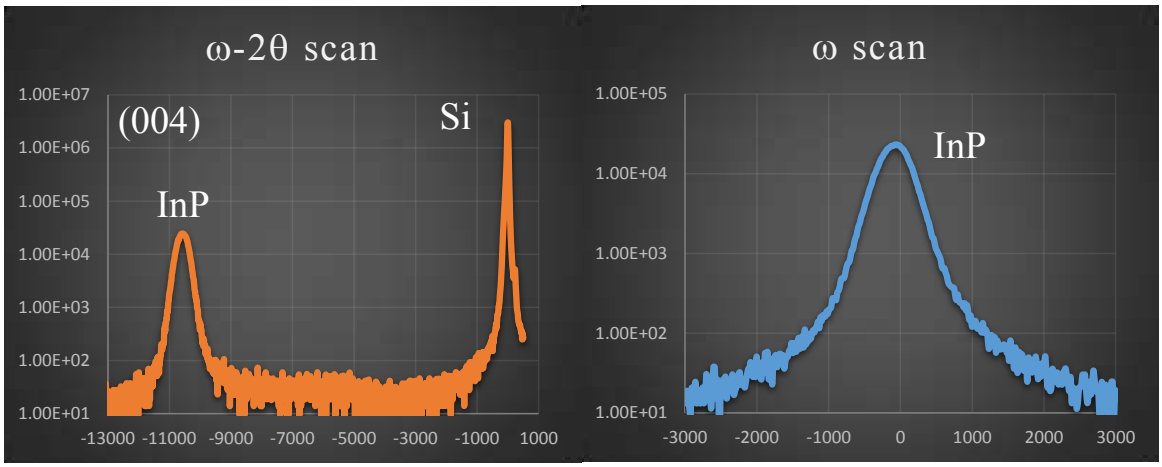

Figure 4. (a) X-ray diffraction ω-2θ scans along the Si (0 0 4) Bragg reflection and (b) X-ray rocking curve (ω-scans) along the InP (0 0 4) Bragg reflection of InP/Si heterostructure in patterned Si wafer.

The perpendicular and parallel view Transmission Electrons Microscopy (TEM) images of a 20-nm-width trenches is depicted on Figure 5. This TEM analysis confirms a high quality InP epitaxy on Silicon. On the perpendicular view relaxation defects are

clearly visible in the first 10nm of the InP/Si interface inside the {111} facet enclosure. Above the interfacial region, InP is fully relaxed and does not show particular crystalline defects. On the parallel view, at the bottom of the trench where is located the InP/Si interface, a Moiré region is clearly detected due to the interference between the electrons beams diffracted by the Si substrate and by the InP layer. The homogeneity of the Moiré fringes network attests the uniform plastic relaxation process of InP which is completely relaxed at the earliest stage of the growth. But in the TEM specimen some {111} oriented defects (stacking faults) which are in majority located at both edges of the trench, are clearly observable. However, the central region of the trench which is considered at the active region for the future device is mainly free of stacking faults.

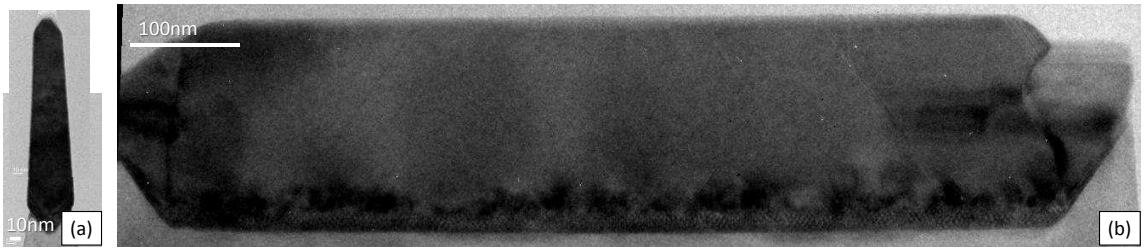

Figure 5. (a) Perpendicular and (b) parallel view TEM analysis of the InP/Si heterostructure grown in "V-grooved" for a 20-nm-width trench

On top of InP buffer layer, two alternative options can be used for the integration of InGaAs semiconductor on Si(001). Either the channel is grown in-situ right after the InP buffer epitaxy. For this a "TBP-to-TBAs" switch is performed at the same growth temperature than InP and the $In_xGa_{1-x}As$ layer is grown directly at the same temperature than the buffer film. The second approach to integrate InGaAs channel will be to grow InP above the oxide level, then to polish the overgrowth by CMP before the subsequent heteroepitaxy of InGaAs. In that approach the InGaAs growth will be initiated from a flat (001) InP surface compared to the {111} InP facet in the in-situ approach.

Finally, the electrical characteristics of different configurations and version of scaled III-V FinFET devices are discussed in the following references (19,20,21).

B. III-V Vertical-FET devices

Another approach for the further integration of III-V semiconductors onto silicon substrate, especially looking a vertical type of devices would be to grow III-V nanowires. In that case, the only solution to promote a vertical and uniform "bottom-up" growth would be to initiate the III-V NWs growth from (111)-oriented Si substrate. Furthermore, in order to prevent from any metallic contaminants which could perturb device operations, a catalyst-free approach is preferred. Then selective area growth of III-V nanowires can be achieved starting from pre-patterned holes in a 20nm-thick silicon oxide layer enabling the control of III-V NWs position onto the silicon substrate as shown on the Figure 6 (22). Because of the (111) orientation of the substrate, lattice misfit between III-Vs, which is one of the greatest challenges for III-V integration on Si, can be overcome. Moreover, the vertical geometry of III-V NWs is naturally suitable to fabricate the vertical gate-all-around devices, which would enhance device gate control ability and save space in future generation of logic circuits.

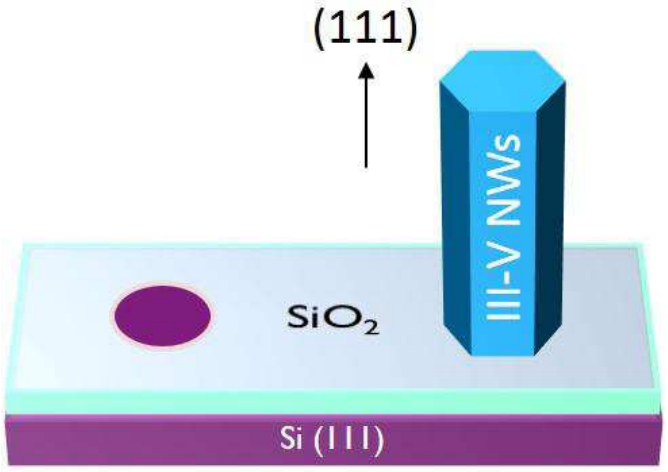

Figure 6. Schematic of selective area growth of III-V NWs on Si(111) from holes in oxide template.

In this part we will discuss the very first results of $In_{0.5}Ga_{0.5}As$ compound NWs growth in a production III-V MOVPE tool used in Silicon process line. As mentioned in the introduction, the selective area growth of III-V NWs is performed on (111)-oriented silicon substrate in order to control the vertical growth of $In_{0.5}Ga_{0.5}As$ wires presenting 8% lattice mismatch compares to silicon substrate. After holes patterning of diameter varying from 30nm up to 100nm on the 20nm-SiO_2/Si(111) substrate, a 60s diluted HF (0.7%) solution is used to remove a part of native oxide on exposed Si surface. The wafer is directly introduced in the MOVPE reactor followed by a high temperature step (above 800°C) at low pressure under H_2 to completely etch the remaining native oxide from the (111) silicon surface prior to the epitaxial growth. $In_{0.5}Ga_{0.5}As$ NWs growth was performed at a growth temperature of 600°C directly on the exposed Si(111) surface.

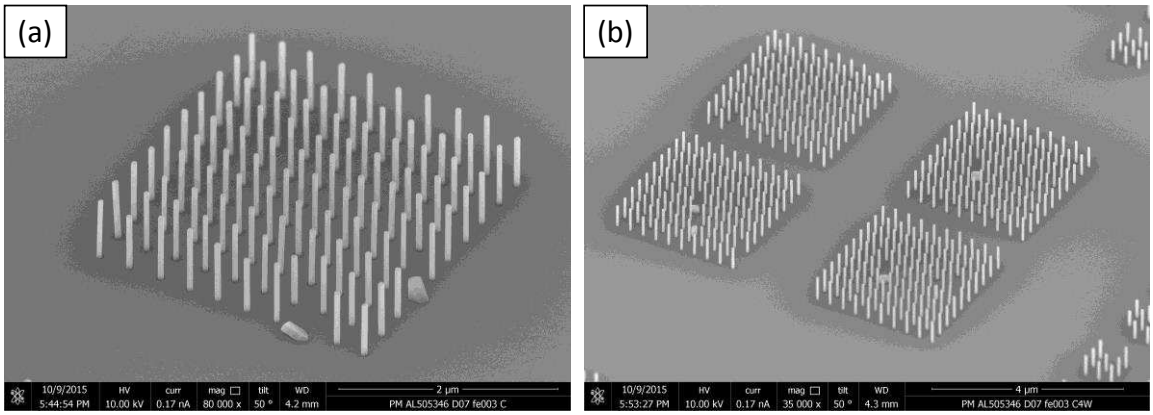

Figure 7. SEM images of $In_{0.5}Ga_{0.5}As$ NWs in (a) D=60nm contact area and (b) D=30nm device area.

Figure 7 show top view and tilted view in inset SEM images of the obtained $In_{0.5}Ga_{0.5}As$ NWs on Si(111) substrate. Two different locations on the mask with different pitch dimensions (a) D = 60 nm region and (b) D = 30nm region are presented. As seen on the SEM images, the $In_{0.5}Ga_{0.5}As$ NWs are only grown in the pre-defined holes and along the vertical (111) direction. The NWs diameter follow the initial scaled diameter of the patterned holes. As seen on the Figure 7, the yield of vertical $In_{0.5}Ga_{0.5}As$

NWs is very high (> 98%) confirming the well-controlled nucleation process during the selective area growth of typical hexagonal-shape $In_{0.5}Ga_{0.5}As$ NWs. This is also demonstrating the potential of this approach of future generation of vertical-based devices.

IV. Photonic devices

Owing to transistor scaling, the increasing level of chip density makes inter- or intra-chip data transmission by electrical wires more and more challenging. Si-based photonics interconnects are very promising to deliver the increasing bandwidths required at much shorter distances, lowering at the same time the power consumption. Therefore, silicon photonics devices such as light source (laser), and optical modulators have been recently developed.

A. III-V laser devices

Fully leveraging the well-established infrastructure initially developed for the electronic industry has been the main driving force for silicon photonics. While a clear solution for the long-awaited silicon integrated laser sources is still missing, the possibility of growing monolithically III-V materials directly on silicon enables to fully benefit from the economies of scale offered by processing in advanced CMOS foundries on large wafers. Given that III-V materials are well known to be efficient light emitters due to their direct optical band gap, silicon photonics could leverage from our III-V epitaxy know-how developed for next generation logic devices to complete its tool box.

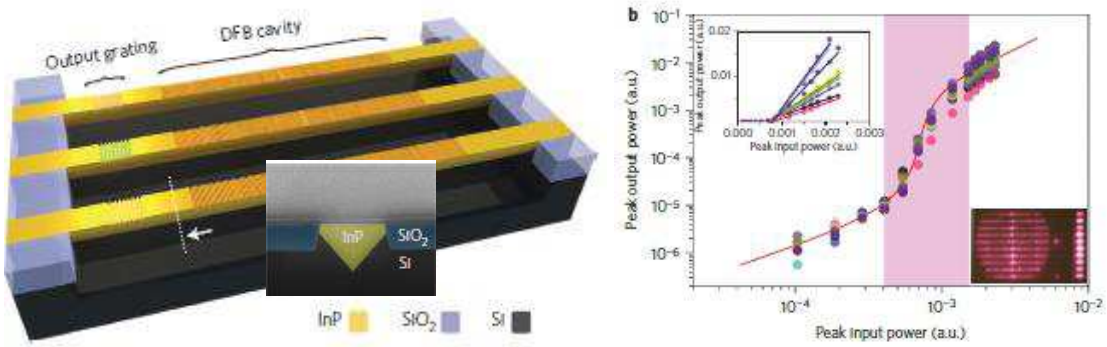

Figure 8. (a) Schematic plot of the InP DFB laser array integrated on silicon. Insert: SEM image of a InP-on-Si waveguide (b) Measured L–L curves of an array of ten DFB lasers. Inset: linear-scale version of the ten log-scale L–L curves presented in the main panel. Inset (bottom): camera-recorded photoluminescence image of ten working lasers under a large-area pumping condition.

In this work, we demonstrate wafer-scale growth of InP nanostructures by selective area growth but in the laser caser looking at much wider trench between 200nm and 500nm (23). The well-optimized epitaxial technology described previously which confines most of the defects within the first 10 nm at the interface of InP and silicon. Such buffer-less growth techniques has led to the recent demonstration of an InP DFB laser array as shown on the Figure 8 grown directly on silicon (24). The possibility of using well-established in-plane laser configuration and the top-down integration scheme

provide a route towards the monolithic integration of dense arrays of III–V laser sources with Si photonic circuits. The demonstration of a room temperature laser operation may pave the way to a monolithic solution to for realizing the integrated laser sources on silicon substrate.

B. BTO-based modulator devices

To achieve power-efficient Si-based optical modulators, ferroelectric $BaTiO_3$ has been viewed as one of the most promising Electro-Optical (EO) materials thanks to the huge Pockels coefficient (>1000pm/V) induced by its spontaneous polarization (25,26). However, the monolithic integration of BTO with Si is still challenging due to 4.4% lattice mismatch. In order to reduce the side impacts from the large lattice mismatch, Molecular Beam Epitaxy technique is used to firstly grow a $SrTiO_3$ buffer directly on Si(001) before the BTO hetero-epitaxy. The Si native oxide was thermally desorbed using the Sr-assisted desoxidation technique (27,28). After desoxidation and completion of the Strontium passivation layer, a bright (2×1) reconstruction of the Sr-Si(001) surface is obtained. A thin 3ML thick $SrTiO_3$ buffer is firstly deposited at low temperature and recrystallized above 550°C. BTO films were then grown under an atomic oxygen flux of $P(O_{ato})$~3.10^{-6} Torr at T_G = 650°C.

We first optimized the growth conditions of 0.5 ML SrO at the $SrTiO_3$/Si interface which is used to enable the in-plane lattice rotation of 45° between $SrTiO_3$ perovskites structure and Si substrates to reduce the effective mismatch below 2% between the different lattices (29). Then, optimal $BaTiO_3$ epitaxial conditions have been characterized physically and optically by various techniques as shown on the Figure 9. Figure 9(a) shows the RHEED pattern recorded after 15 nm of $BaTiO_3$ grown on 5nm-thick $SrTiO_3$ buffer on Si(001). The RHEED image exhibits streak diffraction lines, which attests for the good crystallinity of the entire heterostructure. On the figure 9(b) is shown the out-of-plane XRD 2θ/ω measurement recorded on the sample around the BTO/STO (002) Bragg reflections. The diffraction peak is intense and presents Pendellösung fringes around the $BaTiO_3$ reflection, attesting for the good crystallinity of the epitaxial oxide layers.

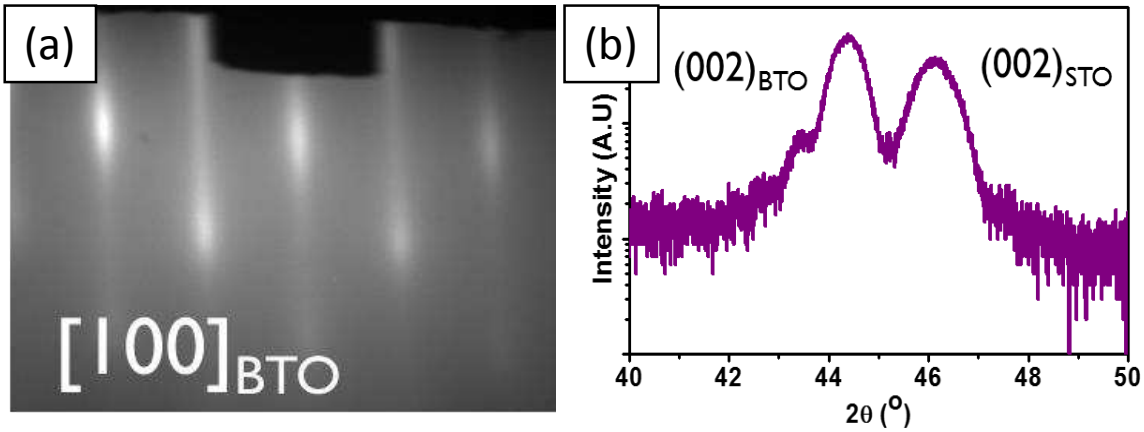

Figure 9. (a) RHEED pattern along [100] BaTiO3 azimuthal direction. (b) Out-of-plane XRD 2θ/ω measurement recorded around the BTO/STO (002) Bragg reflections

We will in the future discuss the ferroelectric properties as well as the optical properties of the epitaxial BTO on Si for next generation of optical modulators.

Conclusions

In conclusion, we have reported here on the monolithic integration of III-V semiconductors by MOVPE selective area growth and epitaxial oxides by MBE on silicon substrate. These material researches are focusing on the integration of new functionalities or advanced devices on a common platform. Both electronic and photonic devices are fabricated based on the developed epitaxial technology. The first part was dedicated to electronic (or logic) based devices made by where alternative high mobility III-V channels are grown selectively either in trenches on Si(001) oriented wafer for FinFET devices either from narrow holes on Si(111) oriented substrate resulting in thin free standing NWs for Vertical FET devices. In the second part of the paper, photonic devices such as light source (laser) based on III-V heteroepitaxy, and $BaTiO_3$ based optical modulators have been recently demonstrated. The effort in understanding material properties during the heteroepitaxy process and the low defective hetero-layers presented in this review confirms the potential of these different heterogeneous integration option for advanced III-V based logic devices and III-V / functional oxide photonic applications on a common Si platform.

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