Hierarchical Model for Spatial Variations of Integrated Photonics

Yufei Xing[1,2,*], Jiaxing Dong[1,2], Umar Khan[1,2], Wim Bogaerts[1,2]
[1]Photonics Research Group, Ghent University-IMEC, Ghent, Belgium
[2]Center of Nano and Biophotonics, Ghent, Belgium
Email: *yufei.xing@ugent.be

Abstract—The paper presents a hierarchical model that decomposes the spatial process variations of integrated photonics into different levels. We performed an analysis of automated wafer measurements and derived systematic intra-wafer variation and systematic intra-die variation of the wafer.

I. Introduction

In integrated photonics, variability is present at different levels (Fig. 1). Process conditions such as exposure dose, resist age, plasma density and CMP slurry composition lead to variations in device geometry such as linewidth, layer thickness, sidewall angles and doping profile variation. The geometry variation affects optical properties of a device such as its effective index, group index, coupling coefficients and centre wavelength. Variability on the device level propagates into circuits so that the optical delay has a random component and paths imbalance at the circuit-level, which degrades system performance such as increasing insertion loss, crosstalk, noise figures and power consumption.

Process variability can be environmental, temporal, or spatial. First two are often addressed by reliability models while the spatial variability requires a statistical model. The spatial variability is the device performance variation that depends on the distance between devices or device's location on the wafer.

II. Hierarchical Variability Model

A process-related device parameter has its variations from sources at different spatial levels. Lot-to-lot fabrications suffer a variation from tool drift, resist ageing, or a change of wafer supplier. Wafer-to-wafer variation is mainly led by tool priming, the difference in the layer thickness and non-uniformity in the chamber environment. Determining systematic signature of lot-to-lot and wafer-to-wafer variations
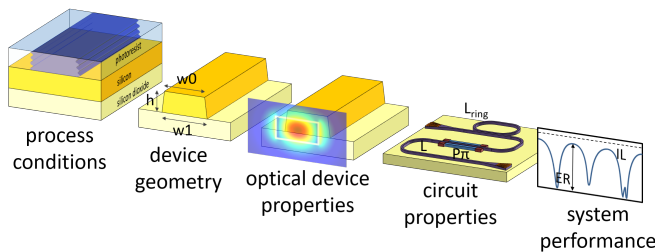

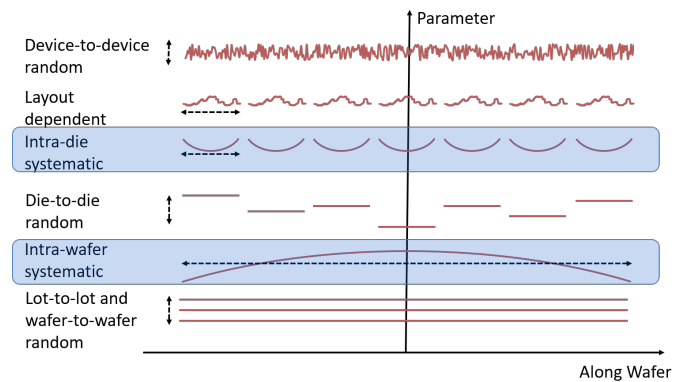Fig. 1. Describing variability presents at different levels

Fig. 2. Illustration of decomposing spatial variability of device parameter at different levels. The hierarchical model is based on Ref[1]. In this paper, we mostly focus on extracting intra-die and intra-wafer systematic variability.

requires long-term monitoring of lots of wafers. In practice, we assume variation above wafer-level is random and follows the normal distribution. Wafer-level non-uniformity can come from layer thickness, photoresist spinning effects and plasma distributions. The systematic intra-wafer variation varies slowly across the wafer and exhibits a symmetric radial pattern. Meanwhile, fluctuation in exposure dose and imaging focus add to the random die-to-die variation. On die-level, there is also a systematic variation that repeats on each die. Resources such as low-frequency change in layer thickness, local pattern density and error in the photomask lead to intra-die systematic variations. Besides, device-to-device random variation includes intrinsic randomness in layer thickness and waveguide sidewalls. In the end, devices with same design parameters but different layout designs may differ due to optical-proximity effect or strain-silicon effect.

Spatial variations from different levels have differed sources, and we assume they have relatively small interactions. Therefore, the total spatial variation can be decomposed into lot-to-lot, wafer-to-wafer, die-to-die and device-to-device variations with systematic and random components [1]. The addictive hierarchical model (Fig. 2) can capture components of variations, which facilitates characterising statistical data measured on-wafer that we present in the paper.

91

III. Experiment

To get process-related geometry parameters such as linewidth w, thickness t and behaviour parameters like effective index n_{eff} and group index n_g over the wafer, we distributed 44 copies of a pair of Mach-Zehnder interferometers on the die (Fig. 3) and measured 25 dies over a wafer using automated measurement. The wafer is fabricated by the IMEC multi project wafer (MPW) service. We fitted the measured spectrum of MZIs using Caphe circuit models [2] to accurately extract waveguide n_{eff}, n_g. From the two MZIs can map n_{eff}, n_g onto the geometry w, t from [3].

To decompose levels of variations, we use a two-step method. First, we separate the wafer-level variation. We take devices at the same location in a die over all of 25 dies on the wafer. We fit a parameter wafer map of w, t, n_g and n_{eff} of the waveguides using a second-order bivariate polynomial. The slow-varying curve matches the radial symmetric pattern of the intra-wafer systematic variation. The deviation of measured data from the parabola gives the random intra-wafer variation (die-to-die variation) of the device. The second step we separate the die-level variation. If we have parameter wafer maps for every device with the unique location on the die, the map by averaging all the device wafer maps gives the systematic wafer variation under the process variation (Fig. 4). Fig. 5 shows that the average offset between a device wafer map and averaged wafer map gives the systematic intra-die variation (systematic die-to-die variation) while the residue provides random die-to-die variation.

From decomposed variations, we observed that the waveguide thickness suffers significantly larger intra-wafer systematic variation (3.0 nm) than the intra-die systematic variation (0.7 nm). On the other hand, intra-wafer systematic linewidth variation (8.5 nm) and the intra-die systematic variation (5.0 nm) are more comparable. Since n_{eff} and n_g are related to both linewidth and thickness, their variations are affected by the fabricated geometry variations and present a very correlated variation pattern.

IV. Conclusion

The hierarchical model for spatial variations can serve as a simple but effective tool to decompose levels of process variations. The model helps to characterise variations of different sources and facilities yield prediction.
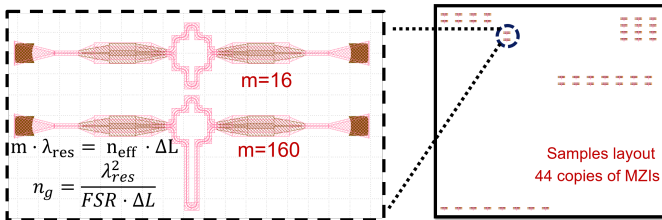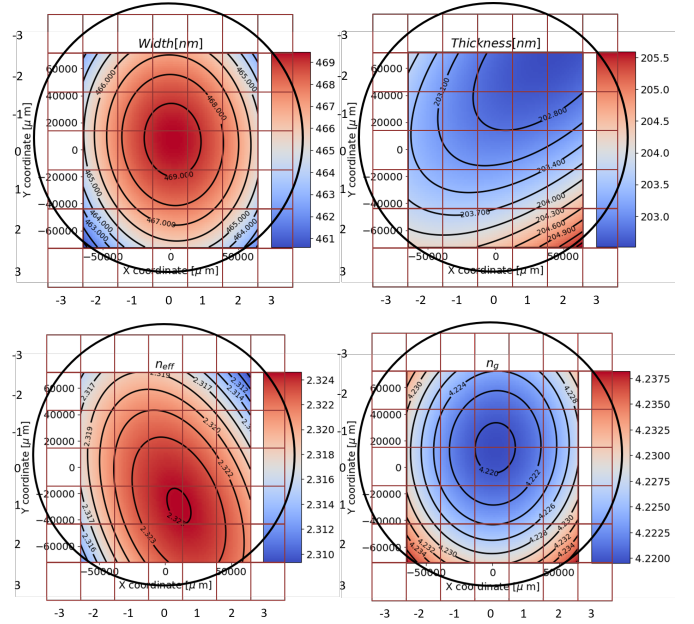

Fig. 4. The averaged map by averaging all the device wafer maps presents the systematic intra-wafer variation under the process variation. Red grid indicates dies on the wafer. Black circle is the boundary of the wafer. Top-left: width. Top-right: thickness. Bottom-left: n_{eff}. Bottom-right: n_g
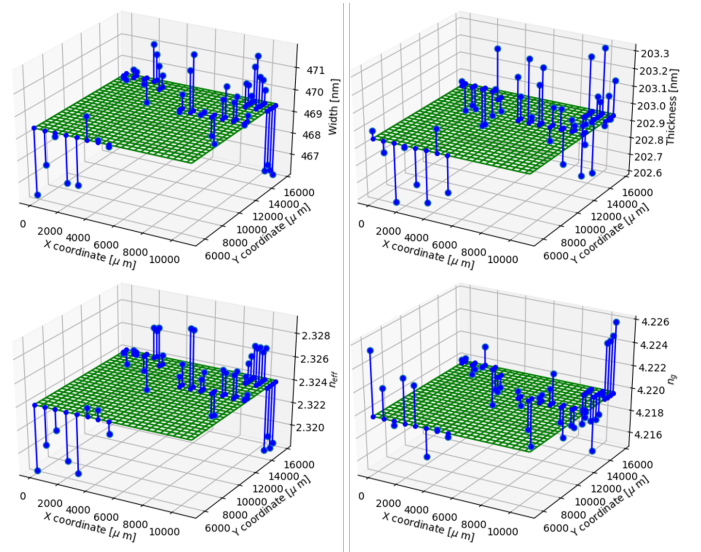

Fig. 5. The die map presents the systematic intra-die variation under the process variation. Clockwise from top-left: width, thickness, n_g, n_{eff}.

Fig. 3. Left: low-order and high-order MZIs we used for geometry extraction. Right: locations of two devices on a die.

$$m \cdot \lambda_{res} = n_{eff} \cdot \Delta L$$

$$n_g = \frac{\lambda_{res}^2}{FSR \cdot \Delta L}$$

m=16

m=160

Samples layout
44 copies of MZIs

References

[1] K. Qian, B. Nikolić, and C. J. Spanos, "Hierarchical modeling of spatial variability with a 45nm example," in *Design for Manufacturability through Design-Process Integration III*, V. K. Singh and M. L. Rieger, Eds., vol. 7275, 3 2009, p. 727505.

[2] A. Ruocco, M. Fiers, M. Vanslembrouck, T. Van Vaerenbergh, and W. Bogaerts, "Multi-parameter extraction from SOI photonic integrated circuits using circuit simulation and evolutionary algorithms," *Spie Opto*, vol. 9366, p. 936606, 2015.

[3] Y. Xing, U. Khan, Y. Ye, and W. Bogaerts, "Extracting Fabricated Geometry on Die-Level," in *2017 IEEE Photonics Scociety Benelux Annual Symposium, Netherlands*, 2017, pp. 148–151.