10. Reservoir Computing on an Active Silicon Photonics Chip Using Nonlinear Microrings Resonators

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The vast amount of data collected every day requires new paradigms for high-speed, energy efficient, information processing techniques. These challenges are addressed through the implementation of machine learning technique at the physical layer. Among the existing techniques, the implementation of reservoir computing on various hardware platforms, included photonics [1, 2], seems to be a very promising candidate for processing real-time data in optical fiber networks with rates exceeding 10 Gb/s.

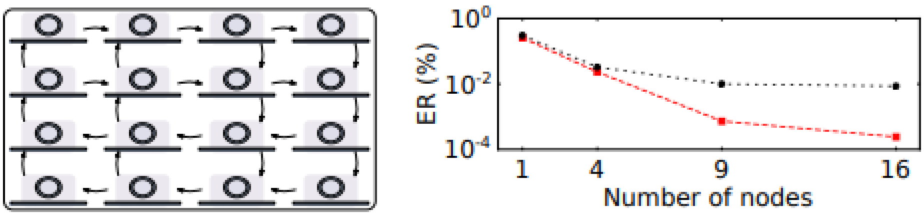

Figure 1: a) 4x4 topology of the photonics reservoir using nonlinear micro rings integrated on a silicon chip. (b) Error Rate for a 2-bits XOR task trained and tested on simulated data for different sizes of the reservoir at 10 Gb/s (black dots) and 20 Gb/s (red squares). The task is $x[k-1] \oplus x[k]$.

We present here a novel architecture depicted in Fig. 1(a). The design is similar to an existed chip presented by Vandoorne *et al.* [1], where we replace the passive nodes made of waveguides, splitters and combiners by nonlinear micro rings resonators [3]. Using numerical simulations, we demonstrate that a reservoir computer paradigm based on this type of integrated photonic chip can perform a typical XOR Boolean operation between two consecutive bits ($x[k-1] \oplus x[k]$ - thus requiring a memory depth of one) up to 20 Gb/s. Figure 1(b) shows the error rate for an increasing number of nodes of a reservoir computer with a swirl topology at two different bitrates : 10 Gb/s (black dots) and 20 Gb/s (red squares) for the typical XOR Boolean operation, trained using ridge-regression. Higher bitrates with similar - or better - performances are expected using larger networks based on micro-ring resonators.

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References

[1] K. Vandoorne, P. Mechet, T. Van Vaerenbergh, M. Fiers, G. Morthier, D. Verstraeten, B. Schrauwen, J. Dambre, and P. Bienstman, Nature Comm. **5**, (2014).