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High-alignment-accuracy transfer printing of passive silicon waveguide structures

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Abstract: We demonstrate the transfer printing of passive silicon devices on a silicon-on-insulator target waveguide wafer. Adiabatic taper structures and directional coupler structures were designed for 1310 nm and 1600 nm wavelength coupling tolerant for ± 1 µm misalignment. The release of silicon devices from the silicon substrate was realized by underetching the buried oxide layer while protecting the back-end stack. Devices were successfully picked by a PDMS stamp, by breaking the tethers that kept the silicon coupons in place on the source substrate, and printed with high alignment accuracy on a silicon photonic target wafer. Coupling losses of −1.5 +/− 0.5 dB for the adiabatic taper at 1310 nm wavelength and –0.5 +/– 0.5 dB for the directional coupler at 1600 nm wavelength are obtained.

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References and links

1. R. Soref, “Silicon Photonics Technology: Past, Present and Future”. SPIE Proceedings, **19**, 5730 (2005).
2. W. Bogaerts, S. K. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, and R. Baets, “Silicon-on-Insulator Spectral Filters Fabricated with CMOS Technology,” IEEE J. Sel. Top. Quantum Electron. **16**(1), 33–44 (2010).
3. L. Vivien, J. Osmond, J. M. Fédéli, D. Marris-Morini, P. Crozat, J. F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, “42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide,” Opt. Express **17**(8), 6252–6257 (2009).
4. W. M. J. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, “Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator,” Opt. Express **15**(25), 17106–17113 (2007).
5. D. Feng, W. Qian, H. Liang, C. C. Kung, Z. Zhou, Z. Li, J. S. Levi, R. Shafiiha, J. Fong, B. J. Luff, and M. Ashghari, “High-Speed GeSi Electroabsorption Modulator on the SOI Waveguide Platform,” IEEE J. Sel. Top. Quantum Electron. **19**(6), 34011710 (2013).
6. J. Verbist, J. Zhang, B. Moeneclaey, W. Soenen, J. Van Weerdenburg, R. Van Uden, C. Okonkwo, J. Bauwelinck, G. Roelkens, and X. Yin, “A 40 Gbaud QPSK/16-QAM integrated silicon coherent receiver,” IEEE Photonics Technol. Lett. **28**(19), 2070–2073 (2016).
7. X. Feng, M. A. Meitl, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, “Competing Fracture in Kinetically Controlled Transfer Printing,” Langmuir **23**(25), 12555–12560 (2007).
8. C. A. Bower, E. Menard, and P. E. Garrou, “Transfer Printing: An Approach for Massively Parallel Assembly of Microscale Devices,” in *Electronic Components and Technology Conference* (2008), pp. 1105–1109.
9. D. Moss, R. Morandotti, A. L. Gaeta, and M. Lipson, “New CMOS-compatible platforms based on silicon nitride and Hydex for nonlinear optics,” Nat. Photonics **7**(8), 597–607 (2013).
10. G. Muliuk, N. Ye, J. Zhang, A. Abbasi, A. J. Trindade, C. Bower, D. Van Thourhout, and G. Roelkens, “Transfer Print Integration of 40Gbps Germanium Photodiodes onto Silicon Photonic ICs,” in *ECOC* (2017), paper PDP.C.4.

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11. A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. Bower, D. Delbeke, R. Baets, and G. Roelkens, "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters," Opt. Express **24**(13), 13754–13762 (2016).
12. J. Zhang, A. De Groote, A. Abbasi, R. Loi, J. O'Callaghan, B. Corbett, A. J. Trindade, C. A. Bower, and G. Roelkens, "A Silicon Photonics Fiber-To-The-Home Transceiver Array based on Transfer-Printing-Based Integration of III-V Photodetectors," Opt. Express **25**(13), 14290–14299 (2017).
13. J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, "Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers," Nat. Photonics **6**(9), 610–614 (2012).
14. D. Gomez, K. Ghosal, M. A. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond, D. Kneeburg, A. Fecioru, A. J. Trindade, and C. A. Bower, "Process Capability and Elastomer Stamp Lifetime in Micro Transfer Printing," in *2016 IEEE 66th Electronic Components and Technology Conference* (2016), pp. 681–687.
15. Cognex Vision Pro ® Machine Vision, website: *http://www.cognex.com/products/machine-vision/visionpro-vision-software/*, accessed November 2017.

1. Introduction

Photonic integration is a rapidly evolving technology and finds applications in many different fields including telecommunication and sensing [1]. The use of silicon-on-insulator (SOI) provides a platform with high refractive index contrast and a CMOS compatible fabrication process, which results in potentially high-yield and low-cost, high volume fabricated devices. Over the years efficient passive components (e.g. waveguide structures and gratings [2]) and active devices (Ge photodiodes [3], Si [4] and Ge modulators [5]) have been developed on this platform, including their monolithic co-integration, demonstrating advanced optical transceivers [6]. However, a full process flow for monolithic integration involves more than 30 mask level processing steps in a fab, which impacts the turn-around time, and hence the photonic integrated circuit (PIC) product development cycle time.

A possible solution is to apply a novel integration technology called micro-transfer-printing (µTP or transfer printing [7] [8]). It is based on patterning dense arrays of devices on a source wafer and selectively picking and printing the devices on a target wafer with high yield using an elastomeric polydimethylsiloxane (PDMS) stamp, potentially in a massively parallel fashion. The concept is illustrated in Fig. 1.

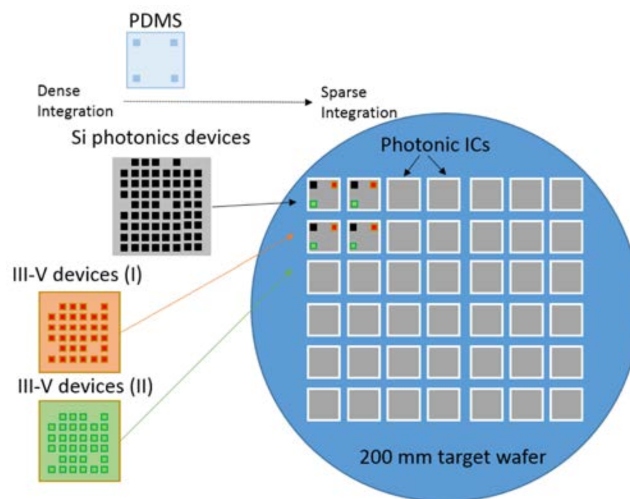

Fig. 1. Concept of transfer printing for photonic integrated circuit manufacturing.

Using such an approach, one can consider printing active devices, but potentially also passive devices, on a silicon photonics target wafer. This way, a new PIC device generation only requires the reiteration of the passive waveguide circuitry, substantially shortening the turnaround time. Moreover, active and passive device integration with other PIC platforms (e.g. silicon nitride [9]) now becomes feasible. We recently demonstrated the use of the technology to integrate waveguide-coupled Ge photodetectors on a silicon photonics platform

[10] using a divinyl-siloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding layer. The approach can also be applied to other types of source wafers, such as III-V semiconductors. This approach then also enables the wafer-scale integration of III-V opto-electronic components such as lasers and photodetectors on a silicon photonics platform. Some results have already been reported in [11–13].

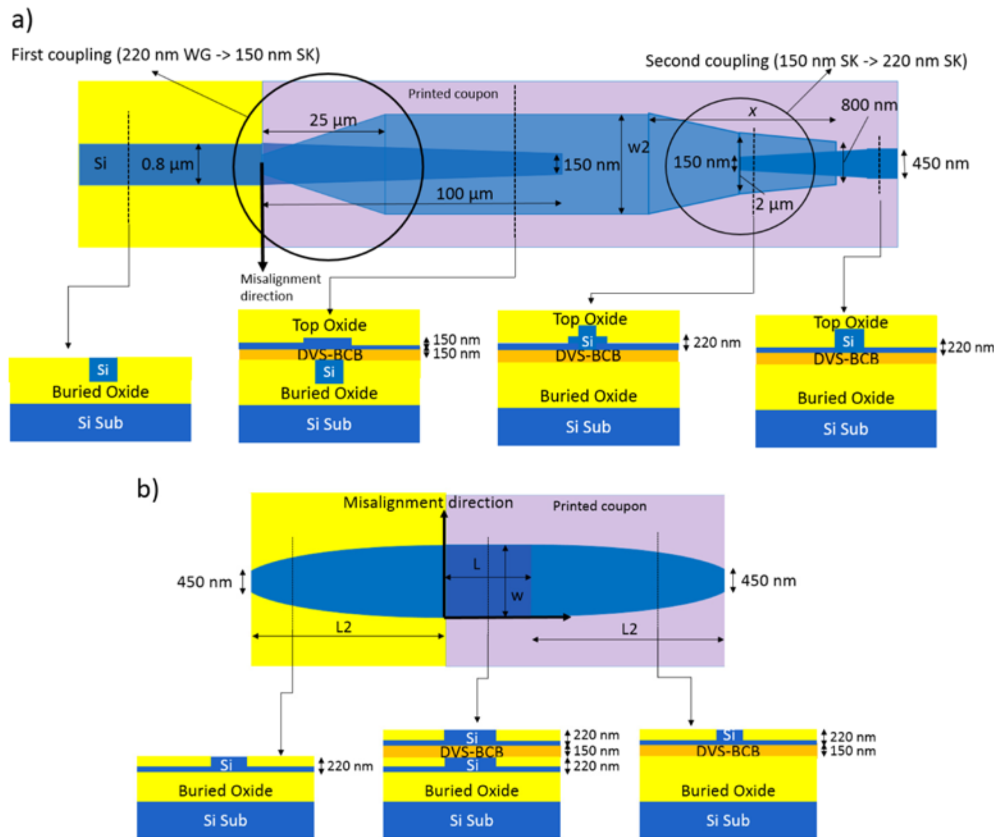

Fig. 2. Proposed adiabatic taper (a) and directional coupler (b) structure.

In this paper we present the development of the transfer printing of passive silicon devices on a passive silicon-on-insulator (SOI) waveguide circuit as a stepping stone towards the realization of 3D photonic integrated circuits and active/passive integrated waveguide circuits based on transfer printing. For this one needs to design alignment-tolerant optical interfaces that allow high-efficiency optical coupling between the target SOI waveguide structure and the silicon device coupon, in order to accommodate for misalignment during the printing. In section 2, these alignment-tolerant interfaces are discussed. Section 3 deals with the technological development of the release of passive silicon devices from their silicon handle wafer and their transfer-printing. In section 4 the measurement results of the optical coupling between the SOI target waveguide circuit and the silicon device coupon are discussed.

2. Device design

2.1 Alignment-tolerant coupling structures

When a silicon device is transfer printed on top of and coupled to an SOI target circuit, the point of interest is to develop a Si-to-Si coupling scheme which is compact (as short as

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possible) and broadband (efficient operation over the telecommunication wavelength range), while being alignment tolerant (efficient operation at ± 1 µm misalignment).

An adiabatic taper can be considered for this purpose. Such a coupling structure is schematically depicted in Fig. 2(a), including the DVS-BCB adhesive layer that will be used in the transfer printing experiments discussed later in the paper. A structure with a two-step transition is proposed. The first transition consists of coupling the transverse electric (TE) fundamental mode of a 220 nm fully-etched input waveguide on the target wafer to a 150 nm thick, 80 nm etched waveguide on the printed device coupon. The silicon waveguide on the target wafer tapers from 800 nm to 150 nm width over a length of 100 µm, while the waveguide on the silicon coupon tapers from 150 nm width to a width *w2* over a length of 25 µm. The second transition happens in the printed coupon, from a 150 nm thick and 80 nm etched silicon waveguide to a 220 nm thick and 150 nm etched silicon waveguide.

As a second option a vertical directional coupler structure can be considered as well as a Si-to-Si coupling scheme. Two identical waveguides placed in close proximity vertically can result in a complete optical power exchange between the two waveguides. We can implement this by using two identical 220 nm thick and 150 nm etched silicon waveguides, the schematics of which is depicted in Fig. 2(b). In this case the vertical directional coupler is implemented in waveguides with a width *w* that is substantially wider than a single mode waveguide, this in order to improve the misalignment tolerance. A parabolic taper structure with length *L2* can then be used to transition to a single mode 220 nm and 150 nm etched waveguide on both target and coupon.

The coupling efficiency of the adiabatic taper structure is simulated using a finite difference time domain (FDTD) software. The directional coupler structures were analyzed using eigenmode expansion simulations. A 150 nm thick DVS-BCB layer is assumed in the simulation. The coupling efficiency critically depends on the waveguide width *w2* and *w* for the taper structure and the directional coupler respectively, especially when the lateral misalignment tolerance is considered as shown in Fig. 3(a). A 1310 nm TE polarized input mode is assumed in these simulations. For the directional coupler structure a coupling length *L* of 20 µm was used.

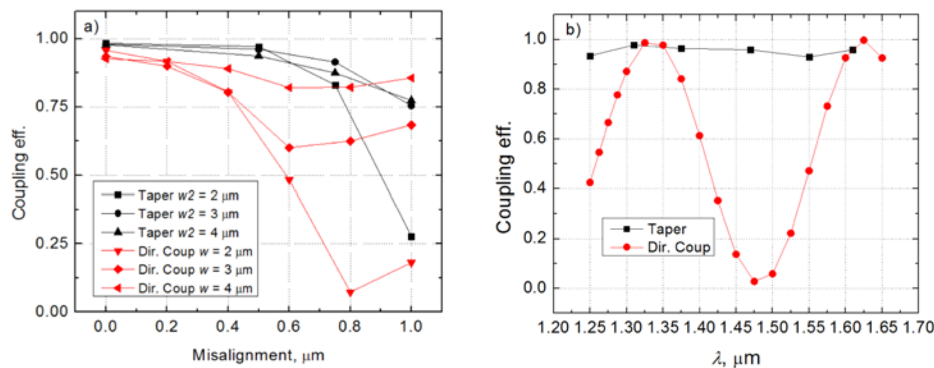

Fig. 3. (a) Misalignment simulations for both the taper and directional coupler structure, sweeping over taper and directional coupler widths; (b) Bandwidth simulations of adiabatic taper and directional coupler structures assuming perfect alignment.

For the adiabatic taper structure with a waveguide width *w2* of 4 µm one can achieve >75% coupling efficiency at ± 1 µm misalignment. In the case of a directional coupler structure, using a 4 µm wide waveguide, one can achieve about around 80% coupling efficiency at ± 0.6 µm. The efficiency slightly increases to 85% for lateral misalignment of ± 1 µm what can be explained by excitation of higher order modes that can combine for higher coupling efficiency at the fundamental mode. ± 1 µm longitudinal misalignment has no substantial impact on the coupling efficiency both for the parabolic taper and for the

directional coupler. The other fixed parameters were studied but have less influence on the device performance.

Bandwidth simulations [Fig. 3(b)] show that the adiabatic taper structure is optically broadband, covering all the telecommunication bands. For the case of directional couplers two bands couple efficiently for $L = 20$ µm (around 1330 nm and 1600 nm).

2.2 Layout of the silicon device coupons and target waveguide structures

Silicon device coupons and target waveguide structures were designed on imec's passive 220 nm silicon photonics platform, comprising a full (220 nm), shallow (70 nm) and socket etch (150 nm). The layout of the device coupons is schematically illustrated in Fig. 4. The design contains two couplers per coupon and a waveguide loop. For the experiments discussed in the remainder of the paper, an adiabatic taper structure with $w2 = 4$ µm and a directional coupler structure with $w = 4$ µm, $L = 20$ µm and $L2 = 70$ µm, because – as is clear from Fig. 3(a), this results in a coupling efficiency better than 75% even for the worst case misalignment of ± 1 µm.

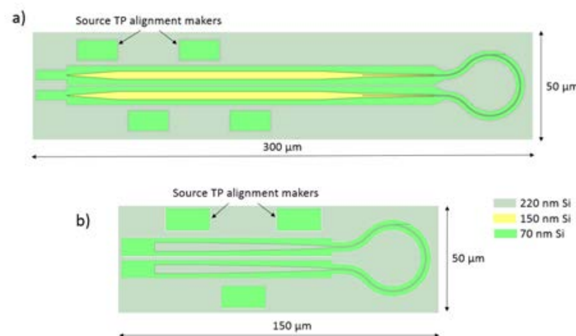

Fig. 4. Layout of passive device coupons: (a) adiabatic taper coupon; (b) directional coupler coupon.

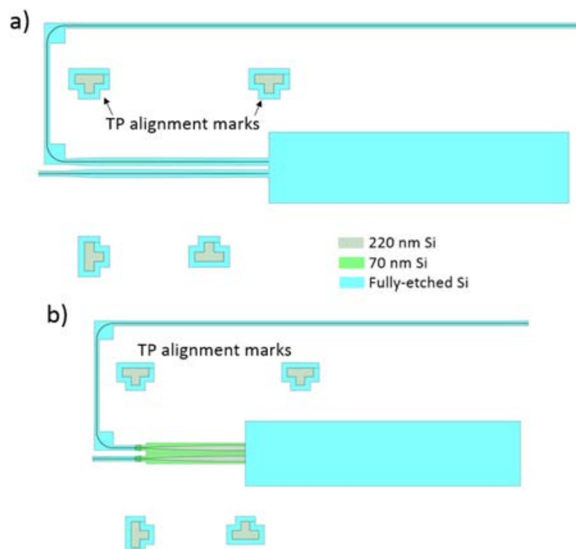

Fig. 5. Layout of silicon photonic target structures: (a) for the adiabatic coupling structure; (b) for the directional coupler structures.

The layout of the silicon photonic target waveguide structures is shown in Fig. 5. Using two grating couplers on the silicon target chip, one can couple the light in and out of the

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silicon device coupon to extract the coupling losses. To achieve precise alignment during transfer printing, it is crucial to add transfer printing (TP) alignment markers both on the silicon target waveguide structure as on the device coupon.

2.3 Layout of the tether structures

In order to make a device transfer printable, one has to release the device from the handle wafer. This is achieved by etching a release layer, while protecting the device. For the SOI devices, the release layer is the buried oxide (2 µm), which is etched using hydrofluoric (HF) acid (release process discussed later). In order to still keep the devices attached to the substrate after the etching of the release layer, tether structures are designed that keep the device coupons in place. Several tether shapes and pitches were evaluated. We conclude that triangular tether structures break at the narrowest points leaving no debris, nor contaminating the backside of the coupon during device pick-up and therefore work most efficiently for the considered silicon devices. The layout of the tether structures used in the experiments is shown in Fig. 6, both for a 300 µm long coupon (for the adiabatic taper structures) and for the 150 µm long coupons. The most optimal tether width is about 1.2 – 1.5 µm for efficient break avoiding any contamination, damage or debris on the source chip during device pick-up. The tether pitch is set 75 µm for the directional coupler and 100 µm for the adiabatic taper coupons. The tether pitch does not have a significant impact on coupon pick up yield.

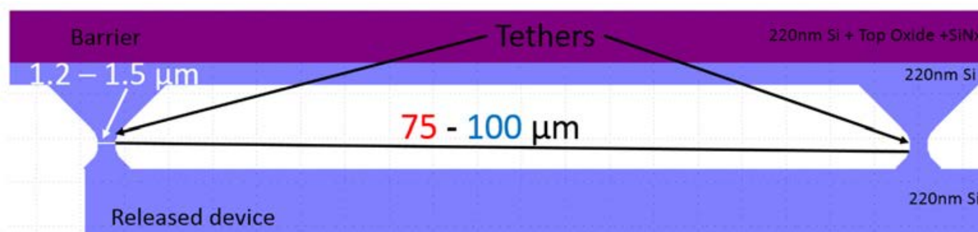

Fig. 6. Top view of silicon photonic tether structures.

3. Transfer printing process

3.1 Device release

As our silicon device coupons have a SiO_2 top cladding, this top cladding needs to be protected during the device release. Amorphous silicon (a-Si) can act as a good protection layer for this purpose. Depositing thick (~1 µm) amorphous silicon using plasma enhanced chemical vapor deposition (PECVD) at 180°C can effectively encapsulate the device. Moreover, using dry etching (SF_6:CF_4:H_2) one can uniformly remove the a-Si after release without damaging the device, nor the tethers. We used no full etch in the coupon area, therefore at the bottom side, the device coupons are protected by the silicon device layer, which is uniformly present over the entire coupon area.

After the release process is completed, silicon devices become thin suspended membranes attached to the surrounding silicon by the tether structures. This implies that stress inside the released device can cause bending of the coupons causing devices to collapse onto the substrate or the thin silicon device layer to break, causing penetration of HF into the top device layer. Therefore proper stress management is required. The stress in the top oxide cladding was measured to be 153 MPa compressive, while the stress in the a-Si encapsulation was measured to be 20 MPa compressive. In order to compensate for this compressive stress a tensile strain PECVD SiN_x is used. The used SiN_x has a tensile stress of 170 MPa. Thinning down the top silicon oxide layer to 100 nm, depositing 170 nm tensile strain SiN_x and using a 1 µm thick encapsulation layer allows for a proper release of the device.

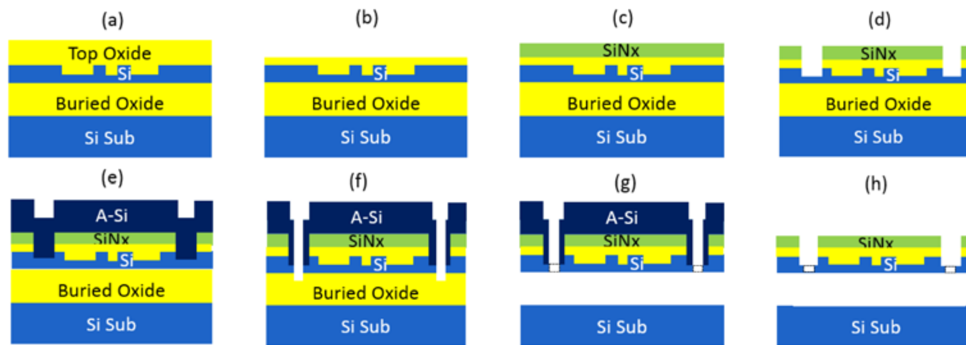

Fig. 7. Schematic representation of release process flow.

The complete process flow for releasing silicon passive devices is schematically displayed in Fig. 7. Devices were fabricated on a standard silicon-on-insulator (SOI) substrate with 1.1 μm top oxide cladding [Fig. 7(a)]. We start with thinning the top oxide to 100 nm using buffered hydrofluoric acid (BHF) [Fig. 7(b)]. 170 nm thick SiN_x (slightly thicker than needed in order to offer tolerance to over-etching in the following wet and dry etching steps) is deposited [Fig. 7(c)]. Rectangular coupons are defined by dry etching (SF_6:CF_4:H_2) the dielectric back-end and slightly etching into the 220 nm silicon device layer, [Fig. 7(d)]. Then 1 μm of a-Si protection layer is deposited at 180°C [Fig. 7(e)], which is then patterned. Tethers are defined using dry etching, thereby also exposing the buried oxide [Fig. 7(f)]. By dipping structures in 40% HF for about 13 minutes, the buried oxide is removed underneath the membrane rendering the passive silicon devices free-hanging, attached to the surrounding silicon by the tethers [Fig. 7(g)]. Finally, the encapsulating a-Si is removed using dry etching, slightly over etching into the top SiN_x layer [Fig. 7(h)].

3.2 Transfer printing process

The transfer-printing was implemented using an X-Celeprint micro-TP100 lab-scale printer. Coupons were picked and printed using an elastomeric PDMS stamp. The rigidity of the PDMS can be adjusted (by using the curing agent to polymer ratio) where the overall stamp stiffness/softness and adhesion will be influenced [14]. A softer stamp is more effective in devices with multiple height differences as the stamp surface has more embedded flexibility to mold to the existing topography. A stamp made stiffer can be just as effective at picking relatively flat coupons. The formulation for the stamps used in this work was 10:1 which is considered a mid-point between both stamp stiffness and adhesion and has proven quite effective in transferring the devices.

The process sequence is shown in Fig. 8. By laminating a structured PDMS stamp with a width of 60 μm and a length of 300 μm to the suspended silicon coupon and quickly moving it in the vertical direction, one is able to break the silicon tethers in the narrowest points and hence pick up the released coupon [Fig. 8(a)]. Printing is performed at room temperature by laminating the picked coupon against a DVS-BCB coated (previously soft-cured at 180°C) SOI target substrate [Fig. 8(b)]. By slowly moving the stamp up in the vertical direction the coupon remains attached to the SOI target wafer [Fig. 8(c)]. Finally, the DVS-BCB is cured at 280 °C.

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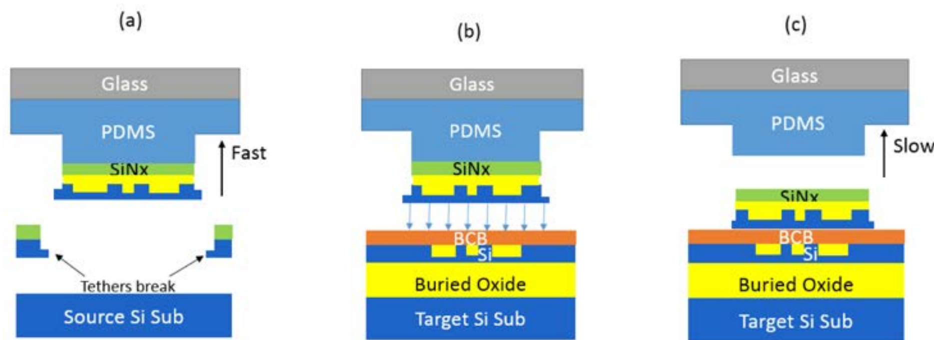

Fig. 8. Schematic representation of the transfer printing process.

In the current experiments, one coupon is printed at a time on a cm-scale target sample. The cycle time for printing is approximately 30 seconds. The approach is however directly scalable to massively parallel printing of 100s of devices. Alignment is performed using COGNEX image recognition software [15] and for this purpose markers were designed on the source coupon and on the target wafer, as shown in Fig. 4 and 5. One can train the software to identify these structures and align their geometric centers, eventually with an additional offset (a so-called off-center auto alignment method). By picking the coupon and bringing it in close proximity to the target wafer, the software can recognize both sets of markers and automatically align the coupon with respect to the target with high precision. Previously we demonstrated that alignment accuracy better than +/−1 µm can be obtained [10].

4. Experiments

In Fig. 9 we demonstrate transfer printing of two silicon coupons with passive optical coupling structures: the adiabatic taper structure for 1310 nm operation [Fig. 9(a)] and the directional coupler structure that operates at 1600 nm [Fig. 9(b)]. One can identify the tethers that broke during the pick process. Clean prints with no contamination on the target substrate are obtained.

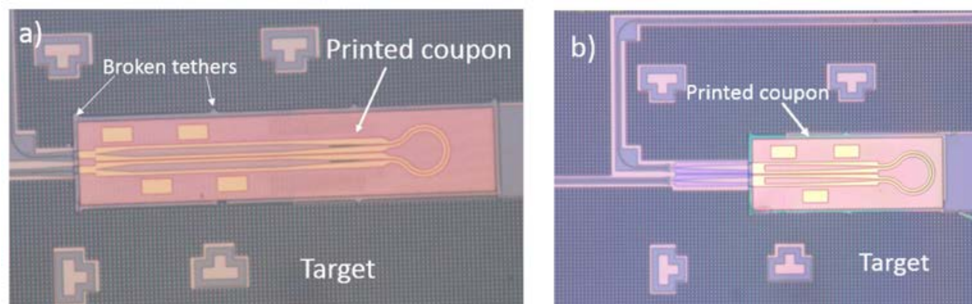

Fig. 9. Transfer printed coupons on the target waveguide circuit: (a) adiabatic taper coupon; (b) directional coupler coupon.

Transmission measurements were carried out by using a pair of single mode optical fibers connected to the grating couplers on the target waveguide circuit. Using a HP8153A power meter and a Santec TSL-510 O-band tunable laser and a Santec TSL-510 C-Band tunable laser the transmission of both types of coupons could be measured. Reference structures on the target waveguide circuit were used to calibrate out the grating coupler losses. The extracted coupling efficiency for a single adiabatic taper interface is extracted in Fig. 10(a). Coupling losses below 3 dB are obtained in the complete 1300 nm wavelength range with −1.5 +/− 0.5 dB coupling loss at 1310 nm.

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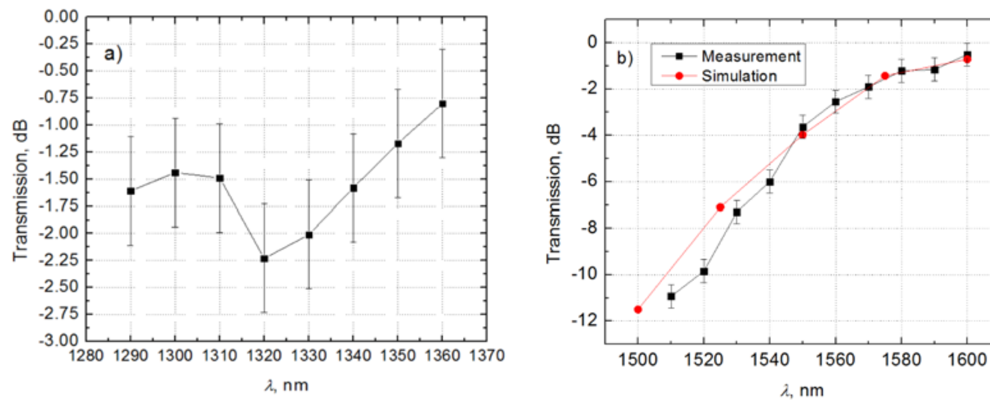

Fig. 10. Measurement results. (a) Adiabatic taper transmission per one coupler measured at 1290 – 1360 nm; (b) directional coupler transmission per one coupler measured at 1500-1600 nm wavelength range and compared with simulation results.

The coupling loss for the directional coupler structure is depicted in Fig. 10(b). Here one can see that we obtained a peak transmission at 1600 nm with a coupling loss of 0.5 +/– 0.5 dB per coupler. The measured coupling efficiency spectrum is in line with the simulation in Fig. 3b). Using focused ion beam (FIB) we evaluated the cross-section of the directional coupler interface and it is displayed in Fig. 11. From this figure we measure a DVS-BCB thickness of 140 nm as well as a lateral misalignment of 700 nm.

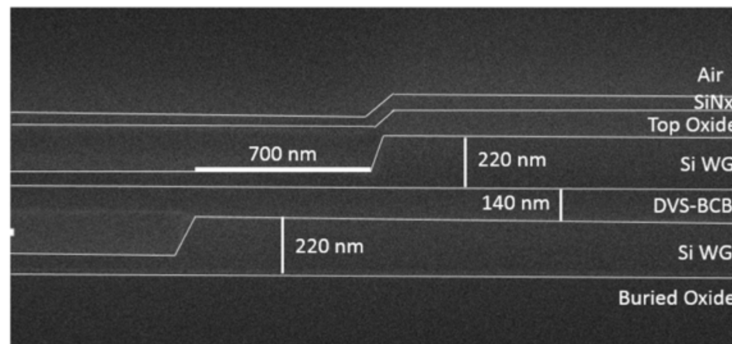

Fig. 11. Focused ion beam cross-section of transfer printed directional coupler interface.

5. Conclusions

For the first time, we demonstrate the transfer printing of passive silicon photonic devices on a silicon photonic target waveguide substrate. We designed compact alignment tolerant coupling schemes – an adiabatic taper and directional coupler structure - that both can efficiently operate at ± 1 µm misalignment in the 1310 nm and 1600 nm wavelength range respectively. A coupon release scheme was developed by under etching the buried oxide layer, while protecting the top device layers using amorphous silicon. Using an optimized tether design clean device picking and printing is demonstrated. The coupling loss of a single interface was –1.5 +/– 0.5 dB for the adiabatic taper coupler at 1310 nm and –0.5 +/– 0.5 dB for the directional coupler at 1600 nm. This demonstrates the high potential of the transfer printing technology for SOI photonic integrated circuit development and its potential to improve the turnaround time for fabricating such circuits.

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