Transfer Print Integration of 40Gbps Germanium Photodiodes onto Silicon Photonic ICs

Grigorij Muliuk[1,2,*], Nan Ye[1,2,*], Jing Zhang[1,2], Amin Abbasi[1,2] , Antonio Trindade[3] , Chris Bower[4] , Dries Van Thourhout[1,2] , Günther Roelkens[1,2]

[1] Photonics Research Group, INTEC Department, Ghent University-IMEC, Technologiepark 15, 9052 Zwijnaarde, Belgium. grigorij.muliuk@ugent.be
[2] Center for Nano- and Biophotonics (NB-Photonics), Ghent University, Belgium.
[3] X-Celeprint Limited, Cork, Ireland.
[4] X-Celeprint Inc., Research Triangle Park, NC, USA.
* equal contribution

Abstract *We demonstrate the integration of germanium photodiodes on SOI waveguides by transfer printing. Devices were printed with better than 1µm alignment accuracy. A waveguide-referred responsivity of 0.66A/W was measured at 1550nm and operation at 40Gbps is demonstrated.*

Introduction

Micro-transfer-printing (µTP or transfer printing), proposed by Rogers et al.[1] is an integration technology that relies on the use of a PDMS stamp to transfer materials or devices from a source wafer to a target wafer in a massively parallel way[2]. The key advantage of the technology for the field of photonic integrated circuits is that opto-electronic devices (either Si-based or III-V based) can be realized in dense arrays on their native substrate and cost-effectively integrated on passive target waveguide circuits. By structuring the PDMS stamp selected devices from the dense array can be printed in a single print cycle, thereby enabling to scale out the device array to e.g. a 200mm SOI wafer. This is particularly interesting for the development of scalable III-V-on-silicon integration[3] or the integration of Si/Ge photonic devices on passive waveguide circuits. While such Si/Ge active devices (photodetectors, modulators) can be integrated monolithically with passive silicon waveguide circuits, an important issue is the slow turnaround time for wafer fabrication, as the full flow comprises a > 30 mask level processing in a CMOS fab. Transfer printing on the other hand allows for a new product generation to only iterate the passive waveguide circuits and print the Si/Ge active devices (fabricated once in large arrays in a monolithic process). It also allows for the integration of Si/Ge-based opto-electronic components on other passive waveguide platforms, such as SiNx waveguide circuits, for which a monolithic integration approach is far less straightforward. In this paper we present the transfer print integration of waveguide-coupled Ge photodiodes (GePDs - fabricated on imec's iSIPP25G platform) on a passive SOI target waveguide circuit. In this paper we present the device design, as well as the developed release and transfer-printing processes, obtaining high alignment accuracy (better than 1 µm). We demonstrate a waveguide-referred responsivity of 0.66 A/W at 1550 nm and operation at 40 Gbps.

Device design

The p-i-n germanium photodiodes (GePD) were fabricated in imec's fully integrated Si Photonics Platform (iSIPP25G) along with Si modulators and various passive devices. Fig. 1 depicts the device coupon schematically. The Ge photodiode is interfaced with passive silicon waveguides (220 nm thick) on both sides of the device. The two silicon waveguides form the two prongs a trident taper structure that is used to optically couple from a tapered waveguide on the SOI target waveguide circuit (220 nm thick) to the device coupon, similar to the taper structures reported in other works[4]. Fig. 2 shows the simulation of the impact of the lateral misalignment of the coupon on the coupling efficiency of the trident taper structure, showing that a ±1 µm misalignment has a negligible impact on the coupling efficiency. The dimensions of the designed coupon are 310x50 µm. No large contact pads are defined on the device coupon in order to keep the dimensions small. This allows a very efficient use of the source material and the effective release of the coupon from the source wafer (see below). These

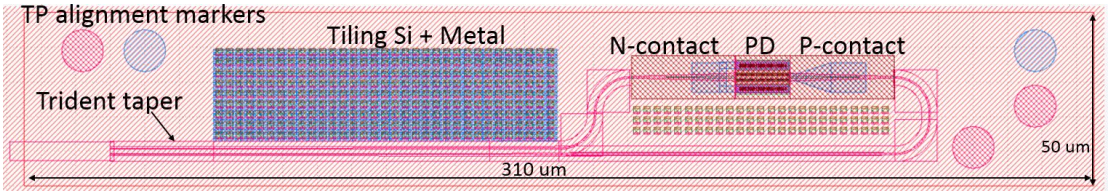


Fig. 1. Germanium photodiode coupon design

contact pads are to be defined after transfer printing to the target waveguide wafer, which can be realized on a wafer scale. Transfer-printing alignment marks are added to the coupon, which can be detected by pattern recognition software, to auto-align the coupon to the target waveguide structure.

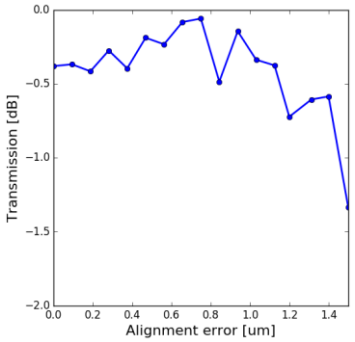


Fig.2. Impact of the lateral misalignment on the coupling efficiency of the trident taper structure.

Coupon release and transfer printing

The detailed process flow for coupon release and transfer printing is depicted in Fig. 3. On a standard iSIPP25G chip (Fig. 3 a) a 75 nm-thin mixed frequency SiNx is deposited for encapsulation of the back-end stack (Fig. 3 b). In a first lithography step 310x50 µm coupons are patterned by dry etching (CF_4:SF_6:H_2) in order to reach the 220 nm silicon device layer (Fig. 3 c). A pinhole-free 1um thick amorphous silicon (a-Si) protection layer is then deposited (Fig. 3 d), followed by lithography and dry etching to locally expose the buried oxide and shape the tether structures (Fig. 3 e) that will keep the coupon in place during the release. By immersing these structures in 40% hydrofluoric (HF) acid for about 11 minutes the buried oxide can be removed (release of coupons), keeping the thin silicon membranes (with back-end stack) free-hanging (Fig. 3 f). After removing the a-Si using dry etching (Fig. 3 g), the coupons are ready to be transfer printed. Fig. 4 a) shows a microscope image of the coupon after removing the a-Si encapsulation. The released coupon is supported to the barrier region by using about 1.2 µm wide triangular tether structures, which efficiently break during the transfer-printing pick process. The transfer-printing experiments are performed using an X-Celeprint uTP100 lab-scale printer. By laminating a structured viscoelastic PDMS stamp to the suspended coupon and quickly moving it in the vertical direction, one is able to pick up the released coupon (Fig. 3 h) by breaking the tethers. Printing is performed by laminating the picked coupon against a DVS-BCB (soft-cured at 180°C) coated SOI target substrate (Fig. 3 i). By slowly moving the stamp in the vertical direction the GePD coupon remains attached to the SOI target wafer (Fig. 3 j).

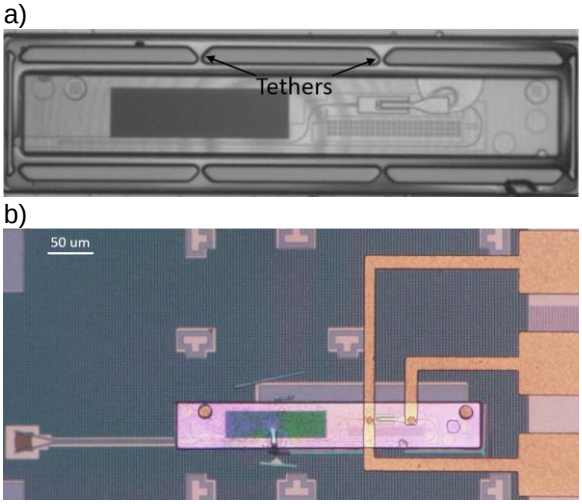


Fig. 4. (a) Microscope image of Ge PD coupon after release on the source wafer; (b) after TP on the target.

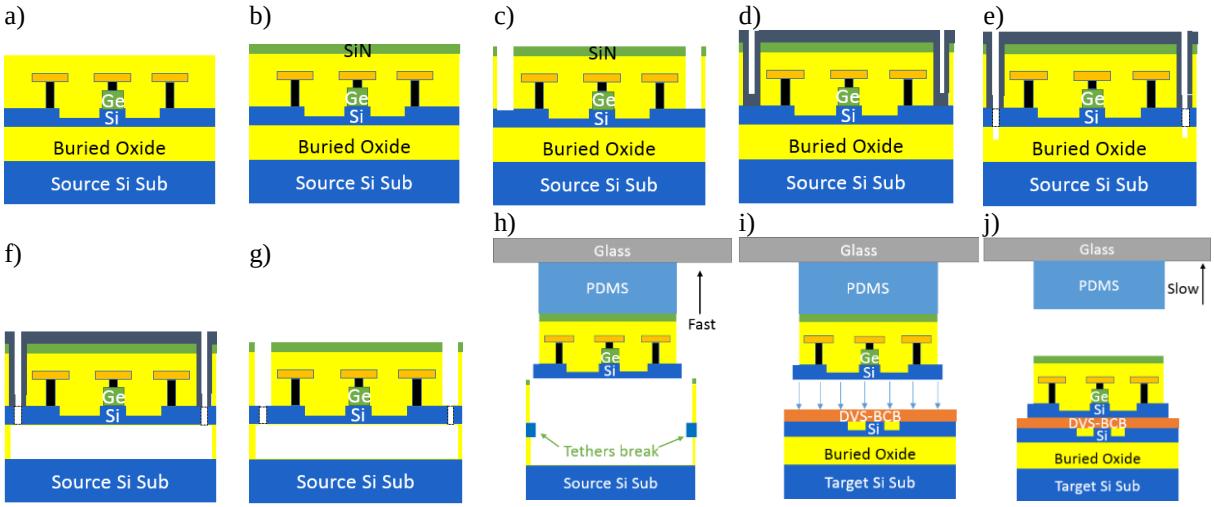


Fig. 3. Coupon release and transfer printing process

After transfer printing, the DVS-BCB was fully cured (at 280°C), the Cu M1 contacts of the PD opened and 1 µm thick Au metal electrodes were deposited to form contact pads. Fig. 4 (b) shows a Ge PD coupon transfer printed on the silicon target circuit, consisting of a single mode waveguide connected to a grating coupler. The alignment accuracy of this integration approach was assessed for 15 coupons, as shown in Fig. 5. An alignment accuracy of better than 1 µm is obtained.

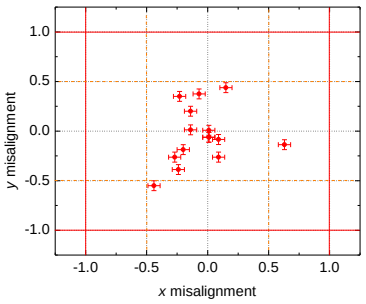


Fig. 5. Transfer printing alignment accuracy

Experimental results

Static I-V curves of the transfer printed devices were measured and compared with the devices on the source wafer. A good match between both curves was obtained (data not shown). A dark current of 12 nA at -1 V and series resistance of 29.6 Ohm was obtained. A waveguide-referred device responsivity of 0.66 A/W at 1550 nm is measured. The iSIPP25G photodetector responsivity was specified at 0.8 A/W, illustrating the high coupling efficiency to the printed device coupon. In order to verify the high-speed performance of the transfer printed device, small signal measurements were performed (Fig. 6). At -0.5 V bias, a 3dB bandwidth of 14 GHz is obtained.

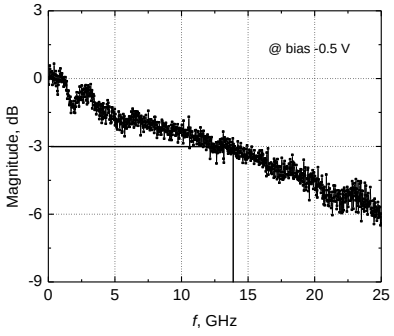
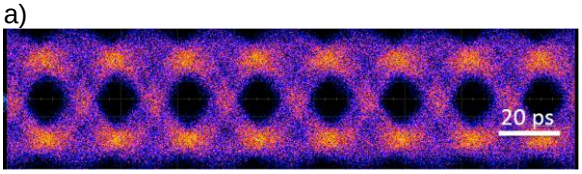


Fig. 6. Small signal measurement results

Large signal measurements were performed using a non-return-to-zero pseudo-random-bit-sequence (PRBS) with a pattern length of 2^7-1 at 40 Gbit/s generated using an arbitrary waveform generator driving a $LiNbO_3$ modulator. Open eye diagrams are observed for 40Gbit/s operation, as shown in Fig. 7(a). Bit error rate curves are depicted in Fig. 7(b). A raw bit error rate below $3.8*10^{-3}$ can be obtained, enabling error free operation using HD-FEC at 40 Gbit/s. No error floor could be observed.

a)



b)

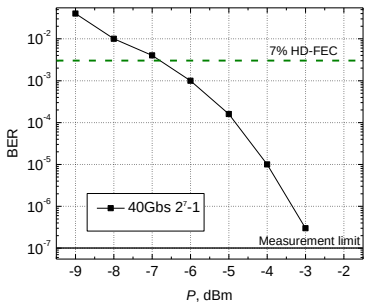


Fig. 7. (a) Eye diagram at 40 Gbit/s for a 2^7-1 PRBS sequence (b) Bit error rate curve at 40 Gbit/s for a 2^7-1 PRBS sequence

Conclusions

In this paper we demonstrate the transfer printing of high speed germanium photodiodes on a silicon-on-insulator passive waveguide circuit. Combining an alignment tolerant coupling structure with high accuracy transfer printing enables high efficiency coupling between the target waveguide and the device coupon. This demonstration paves the way to apply transfer printing for the realization of complex photonic integrated circuits on a wafer-scale, comprising potentially both Si/Ge and III-V opto-electronic components, in a cost-effective way and with a short turnaround time.

References

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