A 40-GBd QPSK/16-QAM Integrated Silicon Coherent Receiver

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***Abstract*— Through co-design of a dual SiGe transimpedance amplifier and an integrated silicon photonic circuit, we realized for the first time an ultra-compact and low-power silicon single-polarization coherent receiver operating at 40 GBd. A bit-error rate of $<3.8 \times 10^{-3}$ was obtained for an optical signal-to-noise ratio of 14 dB for QPSK modulation (80 Gb/s), and 26.5 dB for 16-QAM (160 Gb/s). We also demonstrate robust performance of the receiver over temperature and wavelength.**

***Index Terms*— Coherent receivers, electronic-photonic co-integration, optoelectronic devices, silicon photonics.**

I. Introduction

THE growth of internet traffic has led to a substantial amount of research towards high-speed coherent transceivers for long-haul networks. Coherent communication offers several advantages over traditional on-off keying schemes, including compensation of linear and non-linear fiber distortions and higher spectral efficiency thanks to phase-diversity and multilevel constellations (e.g. QPSK and 16-QAM) [1]. In the near future coherent transceivers are expected to become key components in metropolitan area networks and in the long term even in access networks [2], [3]. This will require a significant reduction in size, cost, and power consumption with regards to the current generation of coherent transceivers. The smallest version of these pluggable modules are envisioned as fully analog coherent frontends (e.g. ACO-CFPx modules), where the digital signal processer (DSP) is located on the motherboard. With the DSP outside the module, the coherent receiver accounts for a significant part of the power consumption and size of the transceiver.

Silicon photonics emerges as an ideal platform to implement such ultra-compact and low-power integrated coherent receivers (ICRs). These circuits can be fabricated on large 200 mm or 300 mm wafers in commercial CMOS foundries allowing for high-volume and low-cost photonic integrated circuits (PICs). Furthermore, the high index-contrast permits the realization of devices with very small footprint. Silicon ICRs with symbol rates up to 30 GBaud for QPSK and 28 GBaud for 16-QAM have been demonstrated using a single polarization receiver [4], [5] and using a polarization division multiplexed (PDM) receiver [6]–[9]. An alternative implementation with a 120° optical hybrid using a 3×3 multimode-interferometer (MMI) instead of the traditional 90° hybrid was demonstrated in [10]. Last year, [11] demonstrated a monolithic single-polarization ICR where the photonic devices were realized on the same chip as the transimpedance amplifiers (TIAs).

Recently, we reported a single-polarization silicon coherent receiver packaged with a 2-channel SiGe TIA-array in [4], where we discussed the design of the photonic and electronic ICs and demonstrated 28 GBaud capability.

In this letter we present new results on this ICR, demonstrating 40 GBaud operation for QPSK and 16-QAM modulation. We also evaluate the performance of the receiver over temperature and wavelength. The ICR achieves a bit-error ratio (BER) of 3.8×10^{-3} for an optical signal-to-noise ratio (OSNR) of 14 dB for 80 Gb/s QPSK modulation and 26.5 dB for 160 Gb/s 16-QAM modulation.

II. Design and Setup

The photonic integrated circuit (PIC) is realized in imec's iSiPP25G platform and is shown in Fig. 1. The circuit consists of two single-polarization grating couplers, a 2 by 4 multimode interferometer (2×4-MMI) acting as a 90° hybrid, and 2 pairs of balanced germanium photodiodes (Ge PDs) occupying an area of 0.3 mm by 0.7 mm. The grating couplers have an efficiency of −6.5 dB and a −1 dB bandwidth of 20 nm. The MMI was designed to have a phase error of less than 5° over the C-band [4]. The simulated common mode rejection ratio, taking into account typical fabrication tolerances, is better

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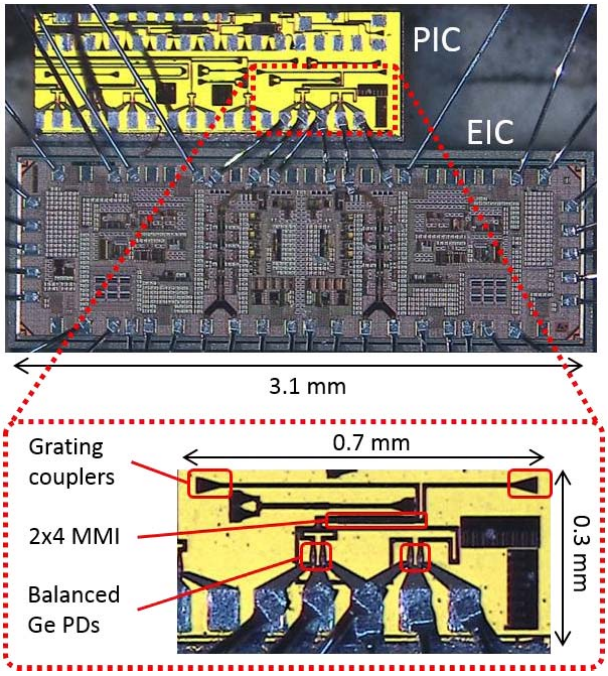

Fig. 1. Micrograph of the photonic integrated circuit (PIC) wirebonded to the electronic integrated circuit (EIC) together with a more detailed view of the PIC-layout. The PIC was kept larger than the dimensions of the coherent receiver for ease of dicing and assembly.

than −20 dB. A single Ge PD has a bandwidth above 50 GHz, an on-chip responsivity of 0.5 A/W, an external responsivity of ∼ 0.025 A/W, and a dark-current of < 15 nA at −1 V bias. The photodiodes are placed in a balanced configuration, which reduces the number of bondpads and prevents a large DC-current to enter the TIA, simplifying its design. This approach does, however, double the capacitance seen by the TIA, reducing the overall bandwidth. Nonetheless, the high individual bandwidth and low capacitance per photodiode will prove sufficient for 40 GBaud operation as we will demonstrate in section III.

The electronic chip consists of a 2-channel TIA array fabricated in a 0.13 μm SiGe BiCMOS technology with a f_T/f_{max} of 230/250 GHz. Apart from the decoupling capacitors, the TIAs also provide the biasing for the Ge PDs. The input stage of the TIA delivers a fixed voltage of 0.9 V across the bottom photodiode and a variable bias control output is set to 1.8 V, matching the voltage of the top photodiode to 0.9 V. This scheme has the benefit that it requires no negative supply voltage as in classic balanced configurations [5], [7]. Moreover, all electrical connections with the PIC are provided by the electronic IC.

Besides speed and power consumption, the TIAs were optimized for linearity to be able to handle multilevel constellations (e.g. 16-QAM) [13].

Both silicon coherent receiver and TIA-array were wirebonded and placed in a cavity of a high-speed printed circuit board (PCB) to minimize the length of the IC-to-PCB wirebond. The 2 × 2 differential outputs of the TIAs were routed symmetrically to 4 high-speed connectors. Due to the limitations of the measurement setup, all experiments were

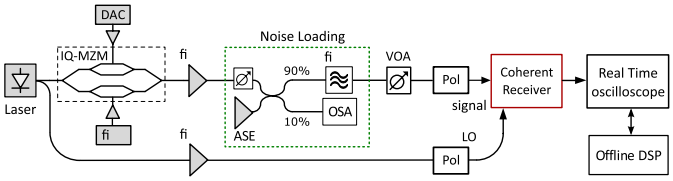

Fig. 2. Schematic of the characterization setup of the QPSK/16-QAM coherent receiver.

performed single-ended with one of each of the differential outputs DC-blocked and terminated with a 50 Ω resistor. This halves the maximal signal swing for a TIA-output from 400 mV to 200 mV peak-to-peak, which is still more than sufficient for the ADCs of the oscilloscope.

Fig. 2 shows the homodyne setup that was used to characterize the silicon coherent receiver, where light from a 1550.12 nm laser (linewidth < 100 kHz) serves as signal (TX) and local oscillator (LO). The signal part is fed to an IQ-Mach-Zehnder modulator (IQ-MZM) driven by two high speed DACs, and is modulated by a 2^{15}-1 symbols long pseudo random bit sequence (PRBS). As both the real-time oscilloscope and the DACs have a limited memory, the effect of longer PRBS on the receiver could not be investigated. Thanks to two 72 GSa/s high-speed DACs provided by MICRAM, we were able to significantly reduce the transmitter-based limitations from our previous experiments [4] and realize high quality transmission up to 40 GBaud. Amplified spontaneous emission (ASE) noise is added to the modulated light in a noise loading stage during OSNR measurements. A variable optical attenuator (VOA) controls the signal power to the receiver. The LO is amplified by a second EDFA to a desired power level. TE polarized light for both LO and TX is coupled through fiber-to-chip grating couplers to the silicon photonic IC with the aid of polarization controllers. A 50 GHz 160 GS/s real-time oscilloscope stores the two outputs of the TIA-array, carrying the I and Q components of the received signal, for offline processing.

III. Experiments

The bandwidth of the receiver system (i.e. PCB, silicon coherent receiver and TIA) was measured with a Lightwave Component Analyzer (LCA) and is shown in Fig. 3. The transimpedance (RF) of the TIA was swept over the range of possible values, i.e. $R_F = 400\ \Omega/\mathrm{N}$ with $\mathrm{N} = 1, 2, \ldots, 8$. As expected, the 3-dB bandwidth decreases inversely with increasing transimpedance. For the lowest R_F values the designed gain peaking becomes visible, extending the bandwidth even further. At lowest gain (i.e. lowest R_F) we reach a bandwidth of ∼30 GHz in good agreement with what was simulated in [4]. As the germanium photodiodes have a very high bandwidth and a slow roll-off [4], we believe that the ICR bandwidth is mainly determined by the TIA frontends. During the 28 GBaud experiments R_F was set to 133 Ω (resulting in 17 GHz bandwidth) for QPSK and 100 Ω (resulting in 22 GHz bandwidth) for 16-QAM transmission. To compensate for the higher data rate in the 40 GBaud experiments the transimpedance R_F was reduced to 80 Ω (resulting in 26 GHz bandwidth) for QPSK and 67 Ω (resulting

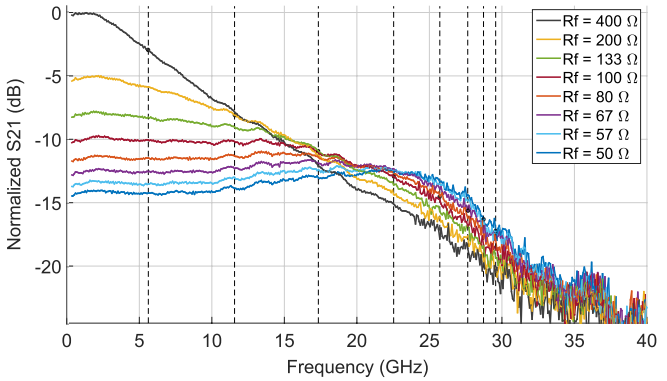

Fig. 3. Measured S21 of the coherent receiver with TIA for different transimpedance settings, i.e. R_F = 400 Ω/N with N = 1,2,..,8), normalized to the low frequency gain at the largest R_F setting. The dotted vertical lines indicate the 3-dB bandwidth corresponding to the decreasing R_F values.

in 28 GHz bandwidth) for 16-QAM. At a transimpedance of 133 Ω the input referred rms noise current of the TIA was 3.2 μA.

A. 40 GBaud QPSK and 16-QAM Operation

For BER measurements −8.3 dBm (QPSK) and −8.7 dBm (16-QAM) of fiber-coupled signal power were used, resulting in an on-chip power of −14.8 dBm and −15.2 dBm respectively. The fiber-coupled LO power was 10.7 dBm (on-chip power ∼4 dBm) for both modulations. These values were kept for all other measurements. The transimpedance of the TIA was set to 80 Ω for QPSK and 67 Ω for 16-QAM, as discussed above. No temperature control was used during these measurements.

Fig. 4 (a) shows the measured bit-error rate as a function of OSNR for both 28 GBaud and 40 GBaud operation. For 40 GBaud QPSK, operation below the soft-decision forward error coding (SD-FEC) threshold (BER of 1.9×10^{-2} for 20% overhead) is reached at an OSNR of 12.4 dB. The hard-decision FEC (HD-FEC) threshold (BER of 3.8×10^{-3} for 7% overhead) requires 14 dB OSNR. For 16-QAM this requires 22 dB and 26.5 dB OSNR, respectively. An example of the received constellation for QPSK (at 20 dB OSNR) can be found in Fig. 4 (b) and for 16-QAM (at 30 dB OSNR) in Fig. 4 (c). The ICR had a dynamic range of 6 dB measured at a BER of 1×10^{-3} for 28 GBaud 16-QAM.

The measured BER curve for 40 GBaud QPSK is in good approximation a ∼2.5 dB shifted version of the 28 GBaud curve. Theoretically a transition from 28 to 40 GBaud requires a 1.55 dB increase in OSNR [14], indicating that transmission at 40 GBaud adds approximately 1 dB to the OSNR penalty. For QPSK the penalty compared to the theoretical minimum, taken at SD-FEC level, amounts to < 2.5 dB for 56 Gb/s and < 3.5 dB for 80 Gb/s. As 16-QAM puts additional requirements on the receiver (e.g. linearity) the deviation from the theoretical OSNR limit is more pronounced at ∼4.5 dB (112 Gb/s) and ∼7 dB (160 Gb/s), respectively.

B. Temperature Dependence

We mounted the test PCB on a temperature controller and increased the temperature in steps of 10 °C from

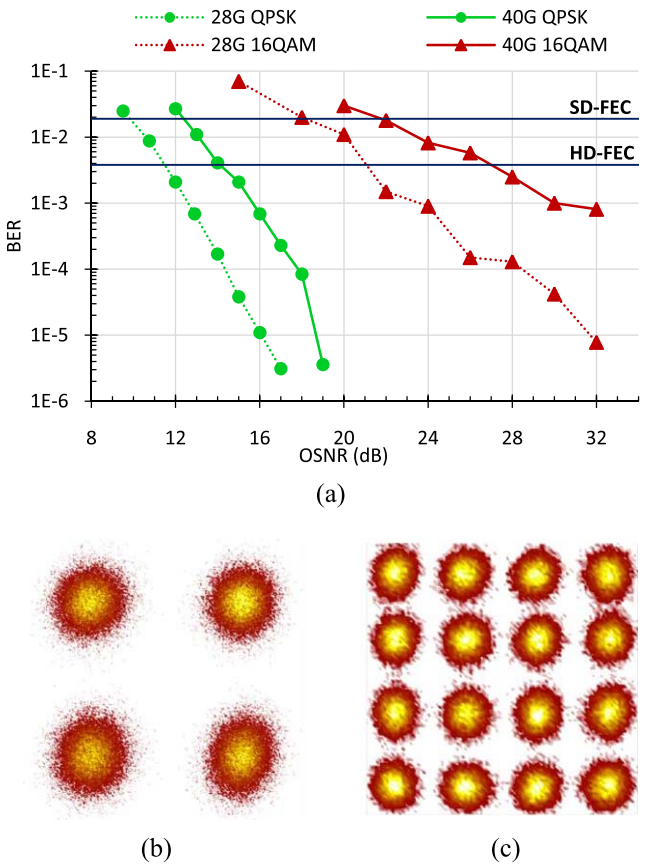

Fig. 4. (a) Measured BER versus OSNR (0.1 nm bandwidth). QPSK is shown as green and 16-QAM as red, 28 GBaud curves are dotted, 40 GBaud curves are full; Received constellations for (b) 80 Gb/s QPSK with 20 dB OSNR and (c) 160 Gb/s 16-QAM with 30 dB OSNR.

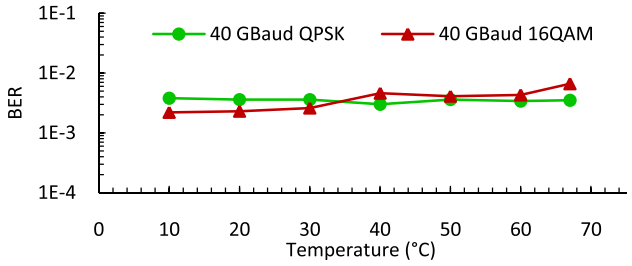

Fig. 5. Temperature dependence of coherent receiver in terms of BER for a fixed OSNR (corresponding to a BER of $\sim 3 \times 10^{-3}$ at room temperature) for 40 GBaud QPSK (green) and 16-QAM (red).

10 °C to 67 °C. We fixed the OSNR corresponding to a BER of 3×10^{-3} at room temperature and recorded the effect on the BER at different temperatures, as shown in Fig. 5. QPSK transmission shows no noticeable impairments, whilst 16-QAM has a small but constant rise in errors for increasing temperatures up to a BER of 6.5×10^{-3}, resulting in a maximal OSNR penalty of ∼2 dB at 67 °C. Up to 60 °C the penalty is limited to only ∼1 dB. As only the multilevel constellation seems to be affected, we suspect that the even higher on-chip temperature forces the TIA into a less linear operating point. This introduces slight saturation for symbols with the highest signal power (i.e. the four corner symbol in the 16-QAM constellation) and an increase in BER.

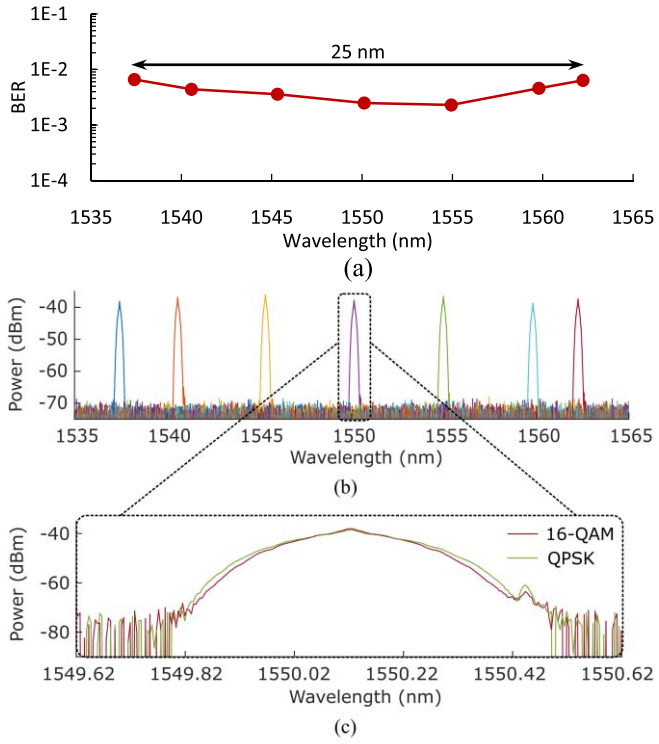

Fig. 6. (a) Wavelength dependence of the coherent receiver in the C-band in terms of BER measured over a range of 1550 nm ± 12.5 nm for 40 GBaud 16-QAM. (b) Optical spectra for each investigated channel. (c) Detailed example of an optical spectra for a carrier at 1550.12 nm.

C. Wavelength Dependence

To evaluate the wavelength dependence of the coherent receiver, we sent 40 GBaud 16-QAM symbols on different carriers in the C-band. The optical filter bank that was used in the noise loading stage had a limited frequency span, preventing us of covering the complete C-band. Operation over ∼25 nm centered around 1550.12 nm (λ_c) was studied as shown in Fig. 6. The OSNR was kept constant (corresponding to a BER of $\sim 2.5 \times 10^{-3}$ at 1550.12 nm) and no temperature control was used. Near the edges of the C-band the BER increases to 6.6×10^{-3} at the lowest and 6.4×10^{-3} and highest wavelength, corresponding to a maximal OSNR penalty of ∼2 dB compared to the center of the C-band. We attribute this to the limited optical bandwidth of the grating coupler having an excess insertion loss of 2.5 dB at $\lambda_c \pm 12.5$ nm. Replacing the grating couplers by edge couplers would provide a more broadband solution covering the whole C-band [9].

IV. Conclusion

We demonstrated for the first time a high-performance integrated silicon coherent receiver operating at 40 GBaud QPSK (80 Gb/s) and 16-QAM (160 Gb/s).

The ICR shows robust operation over almost 60°C range with no significant OSNR penalty for QPSK. For 16-QAM there is a ∼1 dB penalty for temperatures up to 60°C. The limited optical bandwidth of the fiber-to-chip grating couplers introduces an OSNR penalty of ∼2 dB for channels near the edges of the C-band, but this could be eliminated with edge couplers.

In [4], we showed that the presented receiver also featured an extremely compact PIC (0.3 mm × 0.7 mm) and low power consumption of the co-designed TIAs (310 mW) compared to the state-of-the-art silicon ICRs at 28 GBaud. At 40 GBaud 16-QAM the ICR has an energy consumption per bit of only 1.9 pJ/bit. With the addition of a polarization-beam splitter a 320 Gb/s PDM-ICR could be realized using two copies of the single-polarization receiver that consumes only 0.62 W (excluding the LO laser). Combining all these aspects, the ICR reported in this letter presents an important building block for future generation small form-factor pluggable modules (e.g. ACO-CFP4 or QSFP28), paving the way for low-power and low-cost silicon transceivers in metro and access networks at 200G and beyond.

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