Flip-chip assembly of VCSELs to silicon grating couplers via laser fabricated SU8 prisms

K.S. Kaur,[1,*] A.Z. Subramanian,[2,3] P. Cardile,[1] R. Verplancke,[1] J. Van Kerrebrouck,[4] S. Spiga,[5] R. Meyer,[5] J. Bauwelinck,[4] R. Baets,[2,3] and G. Van Steenberge[1]

[1]*Centre for Microsystems Technology, imec/Ghent University, Ghent 9052, Belgium*
[2]*Photonics Research Group, Ghent University-imec, Ghent 9000, Belgium*
[3]*Centre for Nano- and Biophotonics, Ghent University, Ghent 9000, Belgium*
[4]*Department of Information Technology Ghent University-iMinds-imec,Ghent 9000, Belgium*
[5]*Walter Schottky Institut, Technische Universität München, Garching 85748, Germany*
[*]*Kaur.Kamalpreet@elis.ugent.be*

Abstract: This article presents the flip-chip bonding of vertical-cavity surface-emitting lasers (VCSELs) to silicon grating couplers (GCs) via SU8 prisms. The SU8 prisms are defined on top of the GCs using non-uniform laser ablation process. The prisms enable perfectly vertical coupling from the bonded VCSELs to the GCs. The VCSELs are flip-chip bonded on top of the silicon GCs employing the laser-induced forward transfer (LIFT)-assisted thermocompression technique. An excess loss of < 1 dB at 1.55 µm measured from the bonded assemblies is reported in this paper. The results of high speed transmission experiments performed on the bonded assemblies with clear eye openings up to 20 Gb/s are also presented.

OCIS codes: (350.3390) Laser materials processing ; (130.6622) Subsystem integration and techniques ; (250.5300) Photonic integrated circuits; (140.7260) Vertical cavity surface emitting lasers; (130.3120) Integrated optics devices.

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1. Introduction

Silicon photonics has emerged as a mature technology platform for optical datacom and telecom applications. This is because by using the well-developed CMOS tools and fabs of the microelectronics industry, high quality photonic integrated circuits (PICs) can be fabricated with extremely good process control and yield. State-of-the-art passive devices such as waveguides with losses < 1 dB/cm [1], and high efficiency grating couplers [2], (coupling loss < 2.5 dB/coupler), and active devices such as high-speed modulators [3], are already available on this platform. In spite of all these advantages silicon remains an indirect bandgap material and as a result light generation in silicon is a huge challenge. Various approaches have been tried to generate light inside a silicon chip [4,5], or by direct epitaxial growth of III-V materials on Si [6], but a more widespread approach is to integrate light sources onto silicon chips by heterogeneous or hybrid integration. The heterogeneous integration involves bonding of III-V material stacks (e.g. InP), that are excellent light emitters, onto the silicon PICs. Several architectures for III-V-bonded-silicon lasers have been successfully demonstrated [7,8], but issues such as complicated process flow and poor yield still need to be resolved. The hybrid approach involves integration of a coherent light source to directly couple light into the silicon waveguide either via butt-coupling using edge emitting lasers or through GCs using VCSELs. The main advantage of this approach is that it allows for the selection of high power and state-of-the-art lasers before assembly. The VCSELs provide a simpler, less expensive and a compact packaging solution as compared to butt coupling that requires quite stringent alignment and is an expensive approach. The standard GC designs however require an off-normal incidence angle (typically 8-10 degrees [2],) to avoid second order Bragg reflections that lead to a poor coupling efficiency. This off-normal incidence condition makes the integration of VCSELs to silicon-on-insulator (SOI) chips a challenging task. Although complex designs of GCs adapted for perfect vertical coupling have been proposed and reported [9,10], they are hard to implement and their stringent design parameters push the limits of optical lithography. An alternative is to use the standard GCs and flip-chip bond the VCSELs on top at an angle but that again is a non-trivial and non-standard technology. Another way to address this problem is by incorporating micro-optical elements such as prisms on top of GCs. This approach not only allows hybrid integration using standard flip-chip technology but at the same time ensures good coupling efficiency by deviating the light falling at a normal incidence to the required angle for GCs. In a proof-of-concept experiment [11], fiber-to-fiber transmission was demonstrated using polymer (SU8 and PAK) prisms fabricated employing focused-ion-beam (FIB) and imprinting lithography on top of standard silicon GCs. However, FIB is an inherently time-intensive, expensive and non-flexible process. Besides, as the polymer prism is protruding out on the silicon chip it will be very challenging to pattern bond pads and realize VCSEL-to-silicon chip assembly using this method.

In order to overcome the pitfalls of the above approach, we present a novel laser-based, contactless and single-step process to fabricate polymer prisms on top of GCs. It is a simple, fast, flexible and wafer-scalable process. In this paper, we demonstrate for the first time, the integration of VCSEL chips to silicon GCs using SU8 prisms. The VCSELs were flip-chipped onto the SOI chips employing the laser-induced forward transfer (LIFT)-assisted thermocompression bonding technique [12]. We describe details of the technological approach and results of coupling efficiency measurements along with the high speed data transmission experiments performed on the bonded assemblies.

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2. Experiments and results

2.1 Flip-chip bonding of VCSEL to SOI

The waveguides and GCs used for the experiments were fabricated using deep UV lithography on 200 mm SOI wafers in a CMOS environment via ePIXfab [13]. The waveguides were completely etched and were 220 nm x 500 nm (height x width) in dimensions. The GCs were shallow etched by 70 nm at the input and the output end of the waveguide and were designed to have a period of 630 nm and a duty ratio of 50%. The entire structure was cladded by SiO_2 on top for reduced losses. The various steps involved in the process to realize the VCSEL to SOI assembly are depicted in Fig. 1. First of all the insertion loss of the SOI chips (GC-WG-GC) was measured prior to the prism fabrication to get the reference loss value. The GCs used for the experiments were designed for 10° operation in the C-band for TE polarization mode.

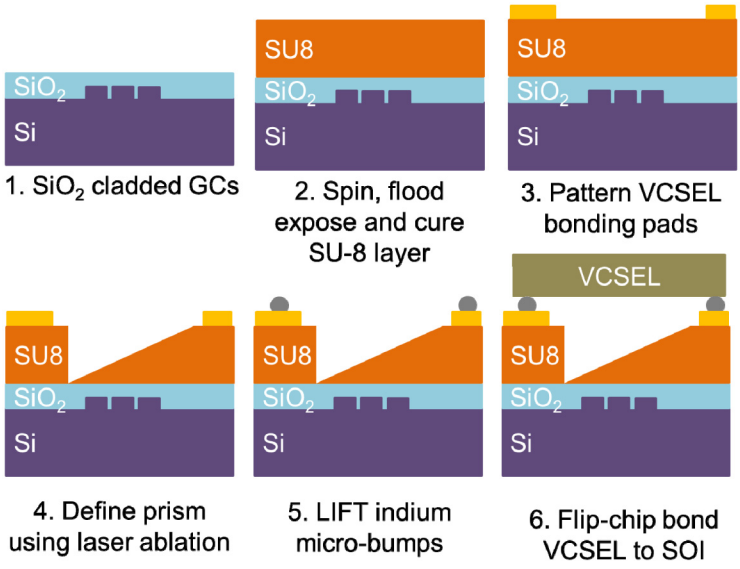

Fig. 1. Schematic for the process flow describing SU8 prism fabrication and VCSEL flip-chip integration on SOI GCs.

For the optical measurements, light from a tunable laser source was coupled in and out of the waveguide using single mode fibers (SMFs) at the input and output GCs at an angle of 10°. A 25 µm thick layer of SU8 was then spin coated on top of the SOI chip, followed by soft bake (1 min @ 65 deg, 10 min @ 95 deg), flood exposure (> 300 mJ/cm^2) and hard bake (1 hr @ 150 deg) steps to fully cure the SU8 layer. Next, the metal tracks for bonding and probing the VCSEL were defined on top of the SU8 layer by using image reversal lithography, evaporating a Ti/Ni/Au stack (20 nm/50 nm/300 nm) and doing lift-off. After metal tracks definition, the SU8 prisms with an angle of 24° were fabricated on top of the GCs using non-uniform laser ablation [14]. The optimum value for the prism angle was calculated to be 24° using Snell's law for a normal incidence on prism face such that it resulted into a 10° incidence angle onto the GCs. Laser pulses from an excimer laser (KrF, operating wavelength 248 nm, pulse duration 5-8 ns, pulse energy 570 µJ) were first passed through a triangular mask (1000 µm x 610 µm), and a demagnified image (factor of 12) of the mask was projected onto the SU8 coated sample. The sample was then scanned in a direction perpendicular to the incoming laser beam at a speed of 157 µm/s at 100 Hz repetition rate, in order to ablate a linear slope in the SU8 layer thereby, resulting in ~22 µm deep prism with 24° angle as shown schematically in Fig. 2(top). The simplicity of this technique lies in the fact that the prism angle can be tuned just by adjusting the laser energy and sample scan

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speed. Figure 2(bottom) shows the variation of the ablation depth and in turn the prism angle as a function of laser energy/scan speed obtained during the optimization cycle. Micro-bumps of indium metal with ~20 µm diameter and ~7 µm thickness were then printed on the VCSEL bonding pads employing the LIFT technique [12]. A commercial laser source Timebandwidth Duetto (12 ps, 355 nm) and a transfer fluence of 300 mJ/cm^2 was used for the LIFT experiments. The details about the LIFT printing of indium micro-bumps can be found in [12].

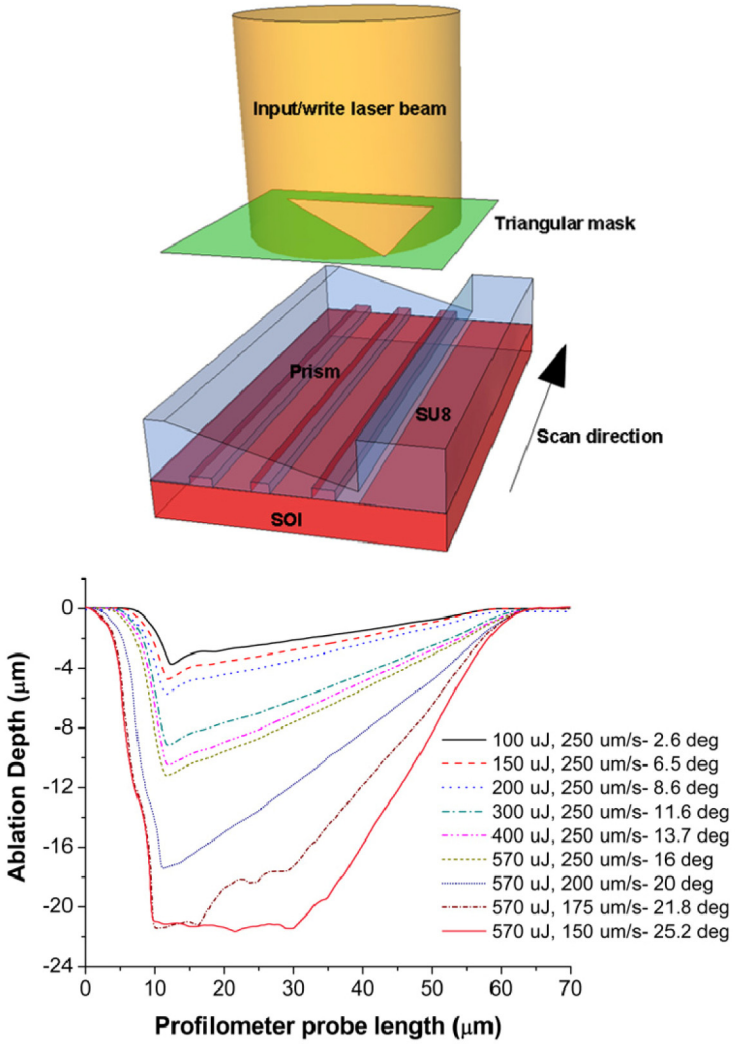

Fig. 2. (top) Schematic of non-uniform laser ablation technique for SU8 prism fabrication on top of GCs, and (bottom) Variation of SU8 ablation depth (prism angle) w.r.t laser energy/writing speed as measured by a profilometer.

The final step in the assembly was to flip-chip bond the VCSEL chips onto the GCs with SU8 prism fabricated on top. The 1.55 µm *n*-InP VCSELs used in these experiments were based upon a short-cavity design and had three compressively strained AlGaInAs quantum wells [15]. The VCSEL chips were diced using the Timebandwidth Duetto laser at a fluence of 3.3 J/cm^2 with a repetition rate of 50 kHz and dicing speed of 200 mm/s. Due to the soft nature of the VCSEL substrate (80 µm thick Au) it was practically not possible to use a commercial mechanical dicing tool as the substrate tend to bend and deform during the dicing

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thereby damaging the VCSELs. Hence laser dicing was employed as a non-contact method to dice the VCSEL wafer into single dies/arrays of VCSELs. Inset of Fig. 3(a) shows the optical microscope image of a typical laser-diced 1 x 2 VCSEL array chip. A semiautomatic flip-chip bonder from Tresky was used for thermocompression bonding of the VCSELs to the SOI chips. The bonding was done at an effective temperature of about 180° C, necessary to melt the indium bumps and to establish a mechanical and an electrical interconnection between the VCSEL and the SOI chip [12]. A typical bonded assembly comprising of bonding pads, prism, SOI chip and VCSEL is shown in Fig. 3(a).

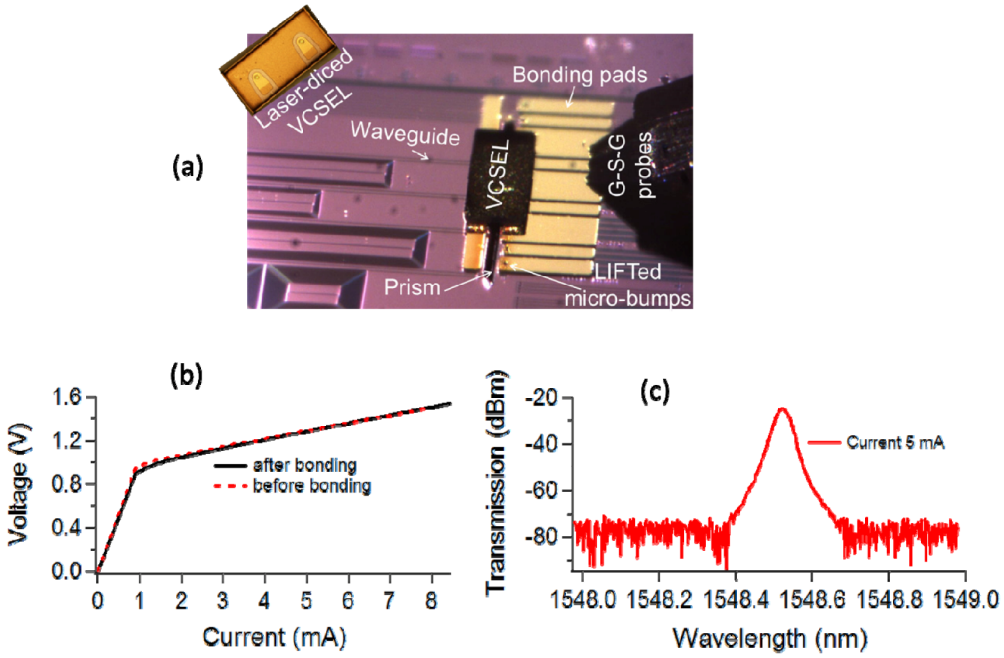

Fig. 3. (a) Optical microscope image of the final VCSEL-to-SOI chip bonded assembly, with inset showing a 1 x 2 laser-diced VCSEL chip; (b) I-V characterization curves for the VCSEL prior and post bonding and (c) Optical spectrum of the bonded VCSEL measured through the output GC of the waveguide.

2.2. Characterization of the bonded assembly

The samples were measured after each processing step (1-6 in Fig. 1) to evaluate the excess loss introduced by the processing to ensure an optimum coupling efficiency from the GCs. The loss values measured at various stages are listed in Table 1. Till step 3 the optical loss measurements were done with both the input and output fibers positioned at 10° angle from the normal to GCs, while from step 4 onwards, the input fiber was positioned along the normal (0°) and the prism refracted the incident light to an optimum 10° at the input GC. No significant shift in the GC efficiency was recorded at any stage of assembly process indicating that the process was optimum. Additionally, no extra loss was introduced by the laser ablation, thus indicating that the SU8 prisms have an optically smooth finishing. The typical fiber transmission curves recorded before and after prism fabrication are shown in Fig. 4. To get the statistical distribution for prism's performance, loss values were measured for 8 different samples and the values are plotted in the inset of Fig. 4. This confirms the reproducibility of the prism fabrication process. Before bonding, the VCSEL chips were characterized and they typically emitted –4 dBm @ 5 mA. After bonding the assemblies were first characterized electrically and Fig. 3(b) shows the typical I-V curve of the VCSELs post-bonding which matches well with the I-V curve of VCSELs pre-bonding. For the optical

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characterization, a driving current of 5 mA was applied to the bonded VCSELs and the emitted power was coupled into the SOI waveguide via SU8 prism and GC combination. After propagating in the waveguide the power was collected at the output GC by a SMF at 10° and was recorded by a power meter.

Table 1. Optical loss values measured at different stages of the VCSEL-to-SOI integration process.

Sample ID	Fiber-to-waveguide coupling efficiency without prism (10°, 1550 nm) (dB)	Fiber-to-waveguide coupling efficiency with prism (0°, 1550 nm) (dB)	VCSEL-to-waveguide coupling efficiency (@ 5mA) (dB)	Total excess loss (prism + bonding) (dB)
S1	- 18.5	- 19	- 20	- 1.5
S2	- 17	- 17.5	- 17.7	- 0.7

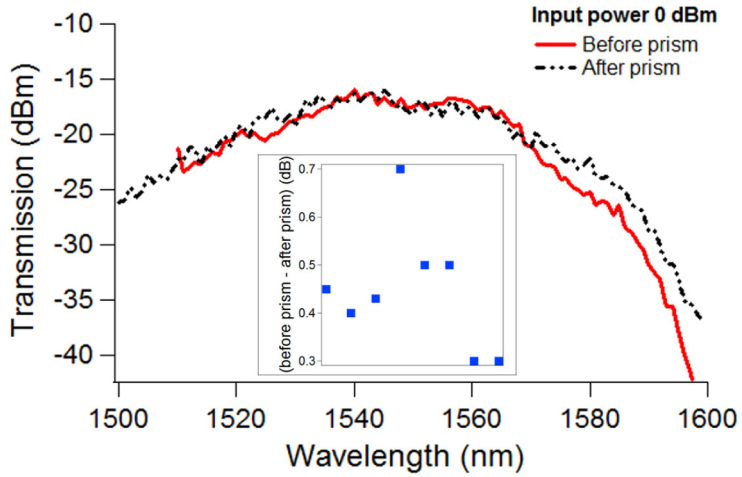

Fig. 4. Comparison between the transmission curves recorded before and after SU8 prism fabrication on top of SOI GCs. The inset shows a plot, indicating the statistical distribution of the prisms' performances at 1550 nm over 8 different samples.

Few devices were tested and for the best case the transmitted power collected at the output was up to −21.7 dBm at 1548.5 nm (peak wavelength of VCSEL) for a driving current of 5 mA. This resulted in a total excess loss of < 1 dB introduced by the whole assembly process as shown in Table 1. The main contributing factor for the excess loss is attributed to the misalignment during bonding as the flip-chip process involved passive alignment of the VCSEL and SOI chip. Figure 3(c) shows the optical spectrum (for sample S2) measured at the output of the waveguide using an optical spectrum analyzer with a resolution of 0.05 nm and a dynamic range of 40 dB, at a driving current of 5 mA. The spectra were continuously recorded over a period of 45 minutes for different current values and no significant effect of back-reflection from the prism (no shoulders around the main peak) was observed.

To further check the reliability and the performance of the process, non-return-to-zero (NRZ) transmission experiments till 30 Gb/s were performed on the bonded assemblies by direct modulation of the VCSELs. The experimental configuration used is shown schematically in Fig. 5(top). A pseudorandom binary sequence with a word length of 2^7- 1 and a bit rate of 30 Gb/s was generated from a commercial pattern generator. The synchronization for the pattern generator was done with an external clock generator set to 30 GHz. The output of the pattern generator was a single-ended NRZ signal with a swing of 450

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mV peak-to-peak. Using a bias tee this data signal was superimposed on a DC bias current of 5 mA. The current was applied to the VCSEL through RF probes as shown in Fig. 3(a). The optical signal generated by the VCSEL was coupled into the SOI waveguide and was collected at the output by a SMF at 10° angle. The optical signal was then pre-amplified with an erbium-doped fiber amplifier (EDFA) and the amplified signal was sent through a tunable optical filter (TOF) with 3 dB bandwidth of 0.3 nm. The TOF was used to reduce amplified spontaneous emission noise from the EDFA. The amplified and filtered optical signal was then detected with the lighwave converter (HP 11982A). It combines a PIN photodetector (PD) with an electrical low-noise preamplifier. The electrical signal at the output of the PD was then captured by the sampling scope, which displayed the eye-patterns. The eye-patterns of the electrical signals after the PD for bit rates of 10, 15 and 20 Gb/s are shown in Fig. 5(bottom). The optical extinction ratio measured for the recorded eyes was 6.5 dB. Clear and wide open eye patterns for 10, 15 and 20 Gb/s represent an error free transmission. At 30 Gb/s, the bandwidth limitation of the setup started to appear.

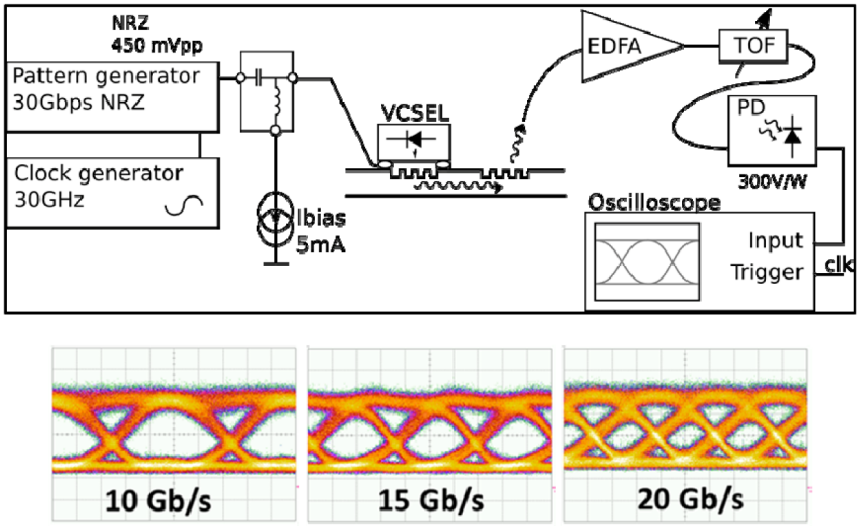

Fig. 5. Illustration of the experimental set-up used for performing NRZ transmission measurements on flip-chip bonded assemblies (top) and eye diagrams recorded for the bonded VCSELs at 10, 15 and 20 Gb/s (bottom).

3. Conclusions

In conclusion, flip-chip bonding of VCSEL chips to SOI GCs using SU8 prisms was successfully demonstrated in this paper. The step-by-step process for the SU8 prism fabrication on top of GCs employing non-uniform laser ablation followed by LIFT assisted thermocompression flip-chip bonding of VCSEL chips was presented. An excess loss of < 1 dB @ 1.55 µm was measured for the bonded assemblies. Clear open eyes recorded till 20 Gb/s for the bonded samples confirm the suitability of this approach for high speed data transmissions. The simplicity, cost-effectiveness, flexibility and wafer scalability makes this method an attractive solution for VCSEL-to-SOI integration.

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