Fabrication and characterization of CMOS-compatible integrated tungsten heaters for thermo-optic tuning in silicon photonics devices

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Abstract: We present fabrication and characterization of tungsten (W) heaters for thermo-optic tuning on silicon-on-insulator (SOI). The wafer-scale fabrication of these thermal tuners was done using standard complementary metal-oxide-semiconductor (CMOS) back-end fabrication materials and processes. Static and transient characterizations of heaters are presented.

OCIS codes: (250.5300) Photonic integrated circuits; (160.6840) Thermo-optical materials; (220.4241) Nanostructure fabrication; (130.4815) Optical switching devices.

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1. Introduction

The high thermo-optic coefficient of silicon (1.8×10^{-4} K^{-1}) makes performance of silicon photonic devices extremely susceptible to temperature variations [1]. This sensitivity can be both a challenge (operational tolerances) as well as strength (efficient tuning) [2,3]. Novel design and material approaches have already shown that the unwanted impact of thermal sensitivity can be mitigated [4,5]. On the other hand, the high thermal sensitivity has been exploited for low-frequency modulation and thermo-optic tuning since the early days of silicon optoelectronic devices. Operational simplicity and relatively cheap fabrication make resistive heaters still very attractive for thermo-optic tuning in active as well as passive devices, and for low speed switching [6–8]. Resistive heaters are traditionally defined as metal lines on top of passive waveguide devices, with an intermediate buffer layer of dielectric or polymer. There are two popular techniques to make such overhead heaters: *Lift-off* (metal electroplating or deposition on patterned resist, followed by resist removal) [4,9,10], and *deposition-pattern* (patterning deposited or electroplated metal and etching away non-essential metal) [11,12]. Alternative, non-overhead heaters have been implemented in silicide [13] or doped silicon [14] on one or both sides of the waveguide. While such heaters can be integrated in the processes of the silicon waveguides, they impose limits on the waveguide geometry and density and take up chip real-estate that could be allocated to waveguides. Overhead heaters do not impose such restrictions.

In this work, we present overhead tungsten (W) heaters for thermo-optic tuning. These overhead heaters are fabricated entirely using CMOS fabrication technology and they are fully compatible with standard complementary metal-oxide-semiconductor (CMOS) back-end metallization (contact via, damascene metal interconnects, bond-pads etc.) processes. This is an important consideration from the point of view of process development, contamination (no new materials), and introduction of the devices in an industrial manufacturing environment. Fabrication and characterization results of this technology were first reported by us in 2012 [15]. Here we elaborate on material selection, device design, fabrication process, and characterization results of second generation devices with similar technology.

2. Material choice

The choice of materials for overhead heater is limited to those available in the fab at the relevant point in the process flow. This limits us to conductors used in the *middle-of-line* and *back-end-of-line*. The two key materials available are W (used for contacts) and copper (Cu) (used for interconnects). Other conductive materials include titanium, tantalum etc. However, these materials are mostly used as thin films for diffusion barriers, and the processes cannot necessarily be used to deposit patterned heater lines of sufficient thickness [16].

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Resistivity and melting point of W (8 μΩ-cm and 3417 ºC respectively) are higher than that of Cu (1.68 μΩ-cm and 1083 ºC respectively) [16], which means that W heaters not only require lower driving current to achieve a certain level of power dissipation, but also can be operated at higher temperature. Also, as the heaters will be electrically contacted by Cu lines, the higher resistivity of W will ensure that most heat dissipation of the current is in the W line, and not in the Cu feed lines. W is usually deposited through chemical vapor deposition (CVD), which has superior conformal step coverage compared to electroplating, which is used for depositing Cu. Hence, heater lines in etched trenches with lower critical dimensions and higher aspect ratio are possible. Therefore, we chose W for fabricating overhead line heaters for thermal tuning in silicon photonics devices with a CMOS like layer stack.

3. Device design

Thermo-optic tuning is usually characterized by measuring the resonant wavelength shift in integrated optical filters. Upon heating, the effective index of the waveguide changes because of the thermo-optic effect which, in turn, changes the effective optical path length. This heat induced change in optical path length can be translated into a phase shift as:

$$\Delta\varphi = \frac{2\pi L \Delta n_{eff}}{\lambda} \tag{1}$$

λ is the wavelength of the signal, L is the length of the heated waveguide and Δn_{eff} is the change in effective index. This temperature induced phase shift can be calculated by measuring optical intensity at filter output. Ring resonators were used for our first demonstration of W heaters [15]. However there are many other parameters influencing the performance of ring-resonators including the coupling efficiency, quality factor etc., which makes it difficult to disentangle the heater performance from the ring output during thermal tuning. Therefore, for the follow-up experiment we chose an asymmetric Mach-Zehnder interferometer (MZI) as test device. MZI arms were sufficiently separated to minimize crosstalk and the waveguide of the heated arm was kept straight and parallel to the heater. A four-probe layout was used to drive the heater and to measure heater resistance accurately.

4. Fabrication

Device fabrication was done at the 200mm CMOS pilot line of imec (Leuven). Only CMOS fabrication tools and processes were used for the fabrication. 200mm silicon-on-insulator (SOI) wafers used for device fabrication had 220nm crystalline silicon (Si) on top of 2μm buried silicon dioxide (SiO_2) and thick Si substrate.

4.1. Front-end and contact module

Imec's Silicon-Photonics Platform (iSiPP) has standard processing modules for fabricating passive photonic devices on SOI wafers. 193nm lithography and inductively coupled plasma reactive ion etching (ICP-RIE) were used for fabricating waveguides and grating couplers [17]. Active devices, such as modulators (see Fig. 1(b)), require ion implantation steps, annealing and nickel-silicidation (NiSi), again executed using standard CMOS modules [18]. A blanket layer of SiO_2 was deposited using CVD serving as a waveguide cladding as well as inter-metallic dielectric for metal lines. This layer was planarized using a timed chemical-mechanical polishing (CMP) step. Contact holes were etched by a capacitively coupled plasma reactive ion etching (CCP-RIE) stopping on the NiSi. Contact metallization uses a damascene process: A titanium/titanium nitride (Ti/TiN) contact-barrier layer is deposited, and subsequently W is deposited using a CVD process, filling the etched holes. Subsequently, the W is polished using CMP down to the level of the oxide cladding.

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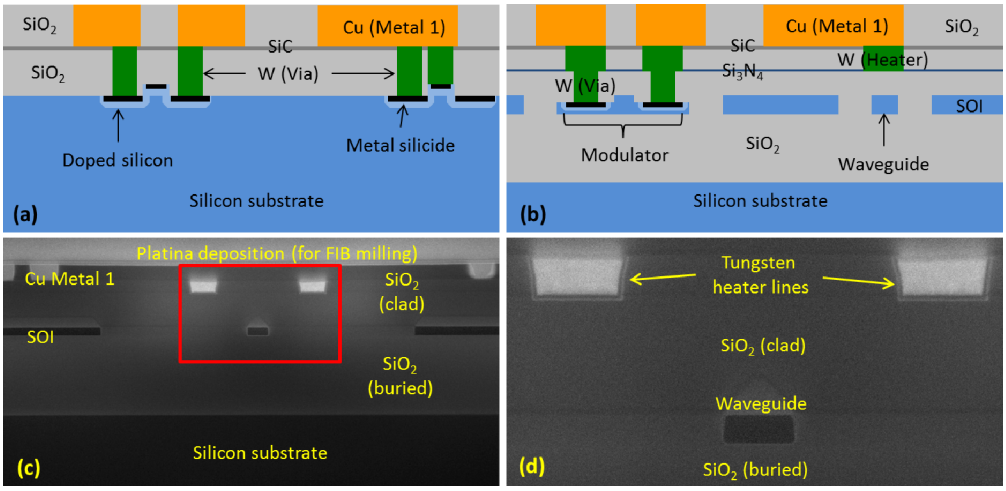

Fig. 1. Cross sections of (a) Typical CMOS stack with front-end and back-end. (b) SOI-photonics stack with modulator and W heater. (c) SEM image of SOI-photonics device cross section. (d) W heaters and waveguide.

4.2. Heater module

The heater fabrication builds on top of the W contact module, using the same processes. First, a stack of Si_3N_4, SiO_2 and SiC is deposited. The purpose of the Si_3N_4 layer is to act as an etch stop for the heater etch while the SiC acts as a CMP stop for the heaters. Similar to the contact via module, 248nm lithography is performed to pattern the heater layer, followed by a CCP-RIE etch in two steps: first the SiC is etched, and subsequently the SiO_2, stopping on the Si_3N_4 layer. Barrier layers and W are deposited next, and a CMP step removes excess W and planarizes the top surface, preparing it for back-end metallization. This heater module is inserted between the standard contacting procedure and the Cu back-end metallization.

4.3. Back-end metallization

Typical CMOS uses many layers of Cu or aluminum (Al) based metallization. In this case, we used only a single metal interconnect layer, which was formed using a standard Cu damascene process for 130nm CMOS technology. For reference, some wafers were passivated with a thin layer of SiC to prevent Cu oxidation, while others were processed further to perform Al passivation on top of Cu probe pads. This completes the full stack as depicted in Fig. 1(b), which is very similar to a typical CMOS stack shown in Fig. 1(a). Figures 1(c) and 1(d) show scanning electron microscope (SEM) images of cross section of a device with full stack.

5. Simulated performance

For simulations, Finite-Element-Method based multi-physics modelling was performed. Figure 2(a) shows the cross section of the model and the temperature distribution during heater operation. Thermal insulation was kept as a boundary condition for sides. Since silicon substrate can be treated as a heat sink, constant temperature was kept as bottom boundary condition. Natural convective cooling was chosen as the boundary condition for the top. Heat sources were located in the W lines. 2D simulations were performed for the benchmark heater length of 200µm, width of 0.6µm and three different offsets from the center symmetry axis. The length of the heated waveguide is assumed to be approximately the same as the length of the heater.

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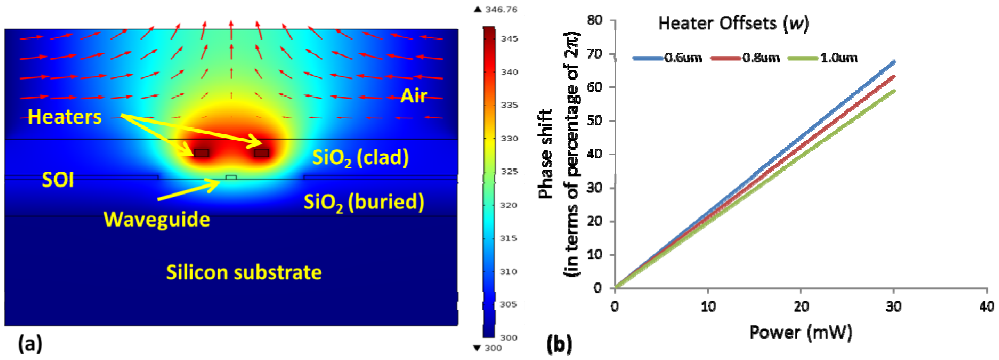

Fig. 2. (a) Simulated temperature profile of device cross section model. (b) Simulated phase shift versus applied electrical power for different heater offsets 'w', defined as the horizontal distance between inward edges of heater line and the waveguide.

The temperature dependence of the refractive index, n, can be written as:

$$n = n_0 + \alpha(T - T_0) \tag{2}$$

n_0 is refractive index at temperature T_0 and α is the thermo-optic coefficient. Since α for Si (1.8×10^{-4} K^{-1}) is considerably higher than that of SiO_2 (1×10^{-5} K^{-1}), the shift in refractive index of Si due to a change in temperature is the same as the shift in effective index of the Si wire waveguide. Hence, Eq. (1) and Eq. (2) are used in the simulation model to plot power versus phase shift performance for heaters with different offsets, shown in Fig. 2(b). From the graph, it is estimated that the power required for a π-phase shift (P_π) for heaters with lateral offset 0.6μm, 0.8μm and 1.0μm is 22.19mW, 23.70mW and 25.43mW respectively.

6. Characterization methodology

6.1. Electric characterization

The resistance of the Cu lines that connect the probes to the W heaters cannot be ignored, because it is comparable to the resistance of the heaters. Hence, both two-wire (2W) and four-wire (4W) measurements were carried out to determine the current-voltage (IV) characteristics of the fabricated heater lines. Figure 3(a) shows the resistance of a 0.6μm wide wire for different lengths. The average line resistivity was calculated to be 1.10 Ω/μm. Figure 3(b) highlights the significance of using the 4W method. Also, it is evident that the heater resistance is almost constant, suggesting little effects of the temperature coefficient of resistivity for W.

6.2. Optical characterization

For optical characterization, light at a single wavelength was injected into the MZI and the output was recorded using an optical power meter. Insertion loss of the MZI with W heaters was found to be around 1.8dB, compared to around 1dB for the MZI without W heaters. Since the MZI was designed with an additional delay in one arm, its response is wavelength dependent and shifts with changing temperature. We operated the device at a wavelength slightly longer than a wavelength for total destructive interference (and hence, minimum power output). Upon heating one arm, the optical path length difference increases, which induces a red-shift in the transmission spectrum. At our operation wavelength, this induces a change in power between minima and maxima as the waveguide temperature rises, as shown in graphs in Fig. 3(c). A shift from minimum optical power output to maximum power output corresponds to a shift from zero phase difference to 180º phase difference (or π-shift). A sinusoidal function was used for curve fitting and to extract P_π as shown in Fig. 3(c). For the

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heater of wire width 0.6µm and length 200µm, P_π has been measured to be 23.38mW, 24.99mW and 27.77mW for offsets of 0.6µm, 0.8µm and 1.0µm respectively.

These values compare well with recently published results for CMOS compatible heaters, where P_π have been reported as 12.7mW for doped Si heaters [8], 20mW for silicide heaters [13], and 25.0mW for metal heaters [14]. Thermal isolation of heated section can reduce P_π by more than an order, as shown by us in [19]. However, such techniques require further processing which is not within the scope of this paper.

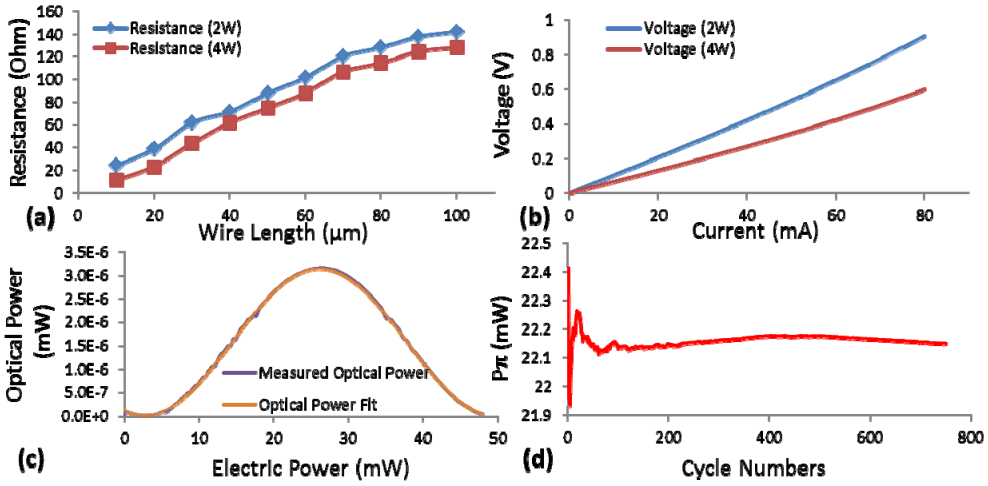

Fig. 3. (a) Length versus resistance plot for 0.6µm wide heater wire. (b) IV characteristics of a heater during operation. (c) Output optical power of MZI versus applied electrical power. (d) Variation of power efficiency over multiple cycles.

For dynamic measurements, the operating wavelength was adjusted to match the minimum in optical power output. The voltage was increased until the first maximum was achieved. We then applied a square wave between this voltage and zero voltage using a function generator. The power output over time was recorded using an oscilloscope referenced to the function generator, and exponential fits on the rising and falling power provides time-constants for heating and cooling, respectively. The time constants for heating and cooling were found to be 38µs and 45µs respectively. To test the reliability of the W heaters over multiple heating cycles, a heater was repeatedly heated and cooled, and the power required to cause a π - shift was recorded for each cycle. In this way, 750 cycles were run, over which very little change in P_π was observed as shown in Fig. 3(d). The maximum shift in P_π and line resistance from their initial values was found to be only 0.3mW and 0.03Ω/µm respectively which is equivalent to changes less than 1.2% and 2.5%, respectively, compared to their original value.

7. Summary

To summarize, we presented detailed fabrication and characterization results of W heaters designed for thermo-optic tuning of SOI devices. We demonstrate how CMOS back-end fabrication processes and materials have been adapted to fabricate these heaters. This method is especially advantageous for thermal tuning in SOI devices with multi-layered metal stacks, because any incompatible material or fabrication process can hamper fabrication of metal layers using CMOS fabrication technologies. Furthermore, since this fabrication process is wafer-scale, it is highly beneficial for high volume production and device uniformity. The characterization results demonstrate state-of-the-art efficiency as well as reliability.

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