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Design Challenges in Large-Scale Silicon Photonics

(Invited Paper)

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Abstract—**We discuss the challenges in the design flow of complex silicon photonic circuits. The treatment of multi-physics, variability, parasitics at both layout and circuit level is not straightforward. Also, layout automation and verification will need significant developments on existing electronic and photonic design methods.**

I. Introduction

Silicon photonics is gaining rapid adoption by industry and is quickly being developed into a technology for real products. A high refractive index contrast and electronics manufacturing techniques enable new levels of complexity in photonic circuits. However, this introduces significant challenges at the design level. In this paper, we will take a closer look at some of these challenges. These include multi-physics, signal handling, variability, parasitics, and design verification. Apart from these fundamental challenges, there is a need for an effective design flow, with efficient information exchange between the different stages in the design process.

II. Integrated design flow

In a photonics design flow, the designer has to go through several stages. Photonics is still very much rooted in the physical domain, where geometries are optimized for a specific optical function. This is often where the design flow starts TODAY: constructing the atomic building blocks. We can expect that this part of the design flow will shift increasingly to the fab, who will provide validated building blocks in a component library. Still, there will always be a need for design capabilities at the physical level.

The core activity will be in circuit design, where the designer composes circuits from building blocks, and simulates them using abstract behavioral models, rather than direct electromagnetic simulations. Photonic circuit design is still a relatively immature process, and some of the challenges are discussed further.

From the circuit simulation, a physical layout should be derived. This can be done manually, but semi-automatic placement and routing tools should take over for complex circuitry. Finally, the design is verified against the requirements of the fabrication process and at the functional level.

This is not a linear flow. The user will move back and forth in the design flow to optimize physical properties of building blocks or fix design errors in the circuit and layout. An integrated flow where transitions between between design steps is largely automated is therefore desirable. This is an area where EDA has paved the way, and where some early photonics solutions are appearing [1], [2], [3].

III. The Challenges

A. *multi-physics*

Silicon photonic devices often require direct physical modeling, as many approximations do not hold well in high-contrast structures. In addition, the electrical and thermal properties of silicon often dictate a multi-physics approach. There are several tools that support the joint physical simulation in multiple domains. However, at the circuit level the multi-physical aspect of photonics introduces a significant challenge. Most photonic applications require electrical control so electrical/photonic cosimulation is an essential requirement. Also, thermal sensitivity and the use of active thermal control introduces the thermal domain in the circuit-level simulation. Beyond this, additional physics could be relevant for specific applications: mechanical (MOEMS-based devices), fluidic and chemical (sensors) and RF (high-speed communications) are among those.

When looking at circuit simulation methods, we see that many systems fit into an *effort-flow* formalism, where a given effort (voltage, pressure, force) results in a given flow (current, flow, movement). Such systems can be captured in a SPICE model. However, there is no effort-flow equivalent in photonics, and this requires specific simulation algorithms [4] [5]. Also, for successful circuit simulation, good behavioral models are needed that capture the multi-physics behavior with sufficient accuracy to enable reliable circuit simulation.

B. *Time scales and signals*

Multiple physical domains operate at different time scales. While this can sometimes facilitate modeling (e.g. steady state in one domain) domains cannot always be be decoupled. At the circuit simulation level, this could imply that different signals should be handled on different time scales. Photonic signals present their own challenges: Depending on the application signals contain much more information than electrical signals coherent optical signals carry both an amplitude and phase at different wavelengths. Depending on the type of circuit the effects one wants to model, and the application, more or less information is needed. For instance, in point-to-point links, a simple *power* signal can suffice. But for interferometric structures and WDM systems, the phase, the wavelength and even the mode for each channel needs to be transmitted. Designing a spectrometer will require full-spectrum signals with a high resolution. This means that at each time step in a circuit simulation hundreds or thousands of numbers have to passed on every connection. It is not yet clear how this can be accomplished in a scalable way, and how this can be integrated with existing electronic circuit simulation tools.

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C. Variability

The high index contrast of silicon photonics makes the waveguide structures very sensitive to geometric variations, but also to effects during operation (temperature, stress). This inevitably leads to a distribution of device properties within a chip, but also from chip to chip, wafer to wafer and batch to batch. While this can be easily modeled at the component level, the difficulty is to predict how this affects a circuit, and eventually the yield, as illustrated in Fig. 1. Corner analysis in electronics cannot capture the multivariate effects in photonics. Today, no solutions exist that can effectively model variability in active/passive photonic circuits.

D. Parasitics

In high-contrast photonics every imperfection can give rise to scattering and reflections, which may cause light to travel where it is not supposed to be. Some of these mechanisms are illustrated in Fig. 2. This *parasitic* light can interfere with the main signal, and as many photonic applications use coherent light, such interference can be phase-dependent and difficult to control. Some parasitic effects, such as reflections, can easily be incorporated in an existing circuit model, but parasitics that do not propagate through the existing paths are much more difficult to capture.

E. Placement and Routing

When generating a circuit layout for fabrication, the blocks have to placed on the chip and connected by waveguides. This can be done manually, but complex circuits will require a (semi)-automated approach. This is already widely used in electronics, but photonics has different requirements. Most photonic technologies offer only a single interconnection layer, compared to many metal layers in an electronic IC. On the other hand, photonic waveguides can be engineered to tolerate some crossing. Global place-and-route algorithms for photonics are not yet well developed.

F. Verification

A final step in the design flow is verification: EDA verification methods are already being applied to silicon photonics for some time. However, electronic structures based on

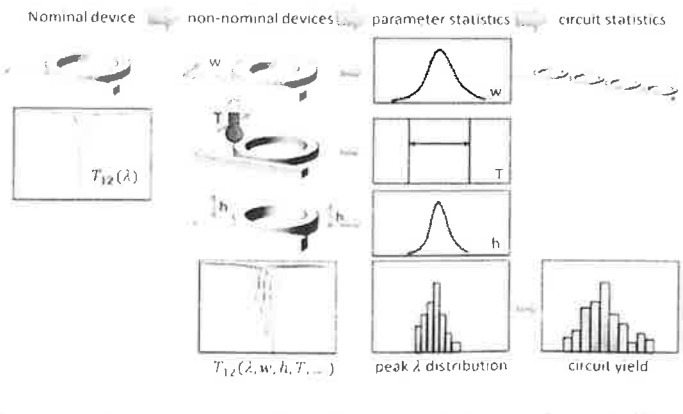

Fig. 1. Translating variability effects into yield predictions. Nominal components have a distribution of geometric and operation parameters, and this variability propagates to a functional variability at the circuit level. Depending on the specifications, this should be translated into circuit yield.

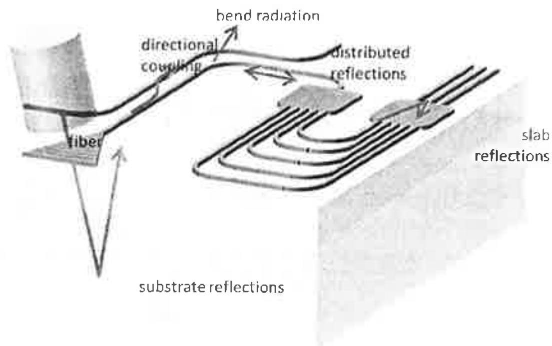

Fig. 2. High contrast photonic circuits will invariably suffer from parasitics: light which is reflected and scattered may interfere with the useful signals.

rectangular patterns differ significantly from waveguide-based devices with curvilinear shapes. Verification methods need to be tuned for this. In the first design rule checking (DRC), line widths, spacing, enclosures, but also bend radius, are inspected. The second verification step is more challenging. In Layout-versus-Schematic (LVS), the circuit layout is analyzed and an equivalent circuit is extracted, which is then compared to the original circuit design. This extraction is non-trivial, because photonics has different connection mechanisms than electronics. Waveguides can evanescently couple, and coupling can be wavelength dependent. Or vice versa, waveguides can be made to cross, with negligible crosstalk effects. At this point, there are no effective LVS solutions for photonic integrated circuits.

IV. Conclusion

The ability to silicon photonics to build large-scale integrated circuits introduces significant challenges in the design process. We discussed several in this paper. Today, there is no tool set that offers an integrated design flow that addresses these challenges in a satisfactory way. There are point solutions which solve partial problems, and we can expect more tools to emerge in the near future. Also, we need tighter integration of design flows between domains, especially between photonic and electronic design, as well as vertically between the physical and the circuit level.

Acknowledgment

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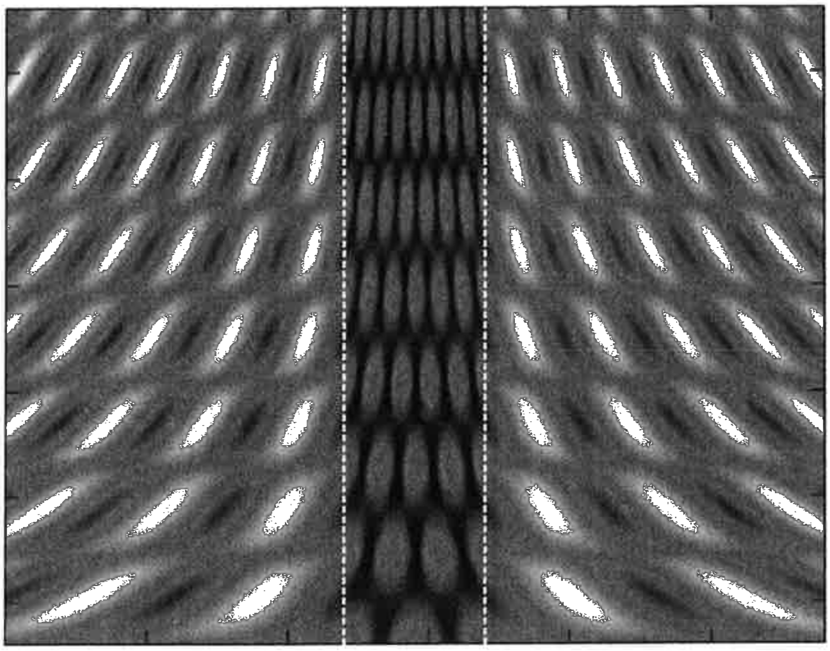

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