Compact Thermally Tunable Silicon Racetrack Modulators Based on an Asymmetric Waveguide

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***Abstract*— A compact wavelength-tunable 10-Gb/s silicon racetrack modulator with integrated thermo-optic heater is demonstrated by using a waveguide with an asymmetric cross section, combining the compact footprint of microdisk modulators with the design simplicity of regular racetrack or ring modulators. The outer perimeter of the asymmetric racetrack modulator is fully etched to maximize optical confinement, and the inner waveguide edge is shallowly etched to maintain an electrically conductive path to the embedded p-n diode and to control the propagation of the asymmetric optical mode and its coupling to the bus waveguide. The resistive heating elements based on highly doped Si strips are implemented at the outer edge of the modulator for thermo-optic control. The asymmetric modulators can be fabricated along with Si wire waveguides and shallowly etched fiber-grating couplers using a simple process flow involving just two Si-patterning steps. Devices with a bending radius of 10 μm and a novel "T"-shaped p-n diode layout have been fabricated, and exhibit electro-optic modulation and heater efficiencies of 28 pm/V and 42 pm/mW, respectively. At 10 Gb/s, a stable extinction ratio of 10 dB is demonstrated from a $2V_{pp}$ drive swing, which can be maintained over a wavelength range of 4.6 nm by thermally tuning the modulator. This is equivalent with a temperature variation of about 62 °C.**

***Index Terms*— Electro-optic modulators, integrated optics, optical resonators, thermo-optical effects.**

I. Introduction

REQUIREMENTS for modulators in silicon photonic interconnect systems include complementary metal oxide semiconductor (CMOS) compatibility, high extinction ratio (∼10 dB), low insertion loss, high modulation speed (>10 Gb/s), low power consumption, and thermal robustness [1]–[3]. Carrier-depletion ring modulators potentially possess all these merits, provided that its temperature sensitivity is compensated, either actively by integrated heaters [4], [5] or passively by a modified Mach–Zehnder interferometer(MZI) [6]. Since the diode capacitance of a carrier-depletion ring modulator is proportional to its perimeter, its power consumption can be reduced by miniaturizing the ring. For example, modulation energy and bit rate of7 fJ/bit and 25 Gb/s for a ring of 7.5 μm radius [4], and 10 fJ/bit and 12.5 Gb/s for a racetrack ring of 10.4 μm radius [7] have been demonstrated. In order to realize a small radius without causing too much bending loss, deeply etched rib waveguides are necessary [4], [7]. On the other hand, several passive optical devices use fully etched Si waveguides, while others such as fiber grating couplers and splitters are preferably implemented with a shallow etch to reduce the lateral index contrast [8]. This means that typical silicon photonic circuits with modulators require three etch depths in silicon. However, for some real cases only two etch depths are implemented to cut the fabrication cost, although this compromises the performance of relevant elements. In [9] the grating couplers which are designed to use the same etch depth as the deep-etched ring modulator exhibit high coupling loss, and thus become a bottleneck of the whole photonic link. In contrast the ring modulators in [10] adopt the same etch depth as the shallow-etched grating coupler. The insufficient etch depth constrains the ring radius to 40 μm. An alternative to reduce the bending radius is to use a micro disk which only requires a complete Si etch [11]. The drawback is the presence of high-order radial modes, and moreover, controlling the coupling strength and the resonance wavelength of a whispering-gallery mode is not as straightforward as the racetrack or ring resonator.

In this letter, we demonstrate a compact racetrack modulator with an asymmetric waveguide core and a specifically designed doping pattern. Using only two etch steps necessarily shared with passive components, we demonstrate the particular waveguide geometry combining advantages of the ring and the microdisk. Its fully etched outer wall provides a tight confinement similar to a microdisk, while the shallowly etched inner edge enables us to engineer the coupling and the resonance like a ring, facilitating the implementation of a wavelength-division multiplexed (WDM) transmitter. This scheme also enables a doped silicon heater in close proximity to the ring. Stable operation is demonstrated at 10 Gb/s over a wavelength range of ∼4.6 nm by thermally tuning the resonance wavelength.

II. Design and Fabrication

The three-dimensional (3-D) schematic diagram and the top view of our design are shown in Figs. 1(a) and 1(b). The modulator is fabricated on a 200-mm silicon-on-insulator (SOI) wafer with 2 μm buried oxide and 220 nm top

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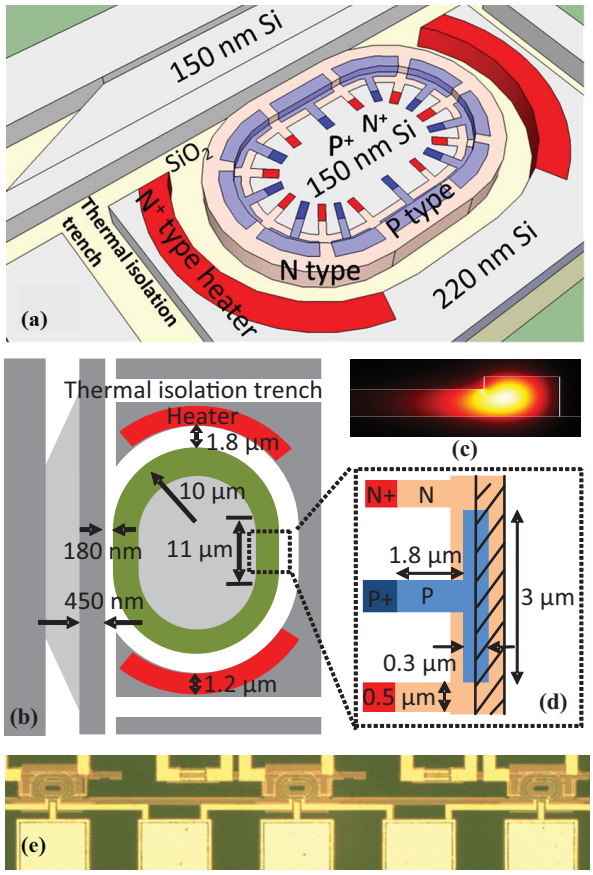

Fig. 1. (a) 3-D schematic diagram of the ring modulator based on the asymmetrical waveguide. (b) Top view: ring modulator. (c) Simulated optical intensity distribution of the fundamental mode in the asymmetric waveguide. (d) Top view: doping pattern where the shaded area delineates the waveguide position. (e) Microscope image of cascaded ring modulators with different circumferences to form a WDM transmitter.

c-Si layer. The outside of the ring is completely etched to expose the buried oxide layer, whereas the inside of the ring is shallowly etched by 70 nm, i.e., the optimal etch depth for the fiber grating coupler. The asymmetric waveguide core width is 450 nm. The bus waveguide has the same shape at the coupling section to maximize phase matching. The simulated optical intensity profile of the fundamental mode is shown in Fig. 1(c). The effective index and the group index of this mode are 2.56 and 3.88, respectively, at 1550 nm wavelength. In order to achieve critical coupling, a racetrack structure is utilized with a bending radius of 10 μm and a straight section length of 11 μm. The gap between the ring and the bus waveguide is 180 nm. The asymmetric bus waveguide is tapered to 450 nm strip waveguides by two adiabatic tapers of 10 μm each.

Unlike the regular rib-waveguide-based modulator where N^+ and P^+ contact regions are located at the opposite sides of the waveguide, the asymmetric waveguide design requires that both contact regions are situated on the inner side of the ring since the silicon outside the ring is completely etched. For this purpose, a particular doping pattern as shown in Fig. 1(d) is implemented within the asymmetric waveguide. The P-type silicon has a "T" shape and is surrounded by the N-type area. Doped bridges offer electrical paths from the P-N junction to the contact areas inside the ring. Their width and height are 1.8 μm and 0.5 μm, respectively. P-type strips inside the

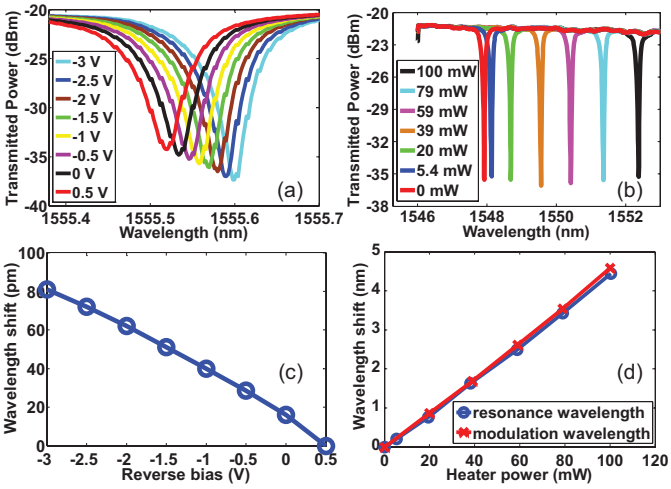

Fig. 2. (a) Transmission spectra of the ring for different reverse bias voltages. (b) Transmission spectra of the ring for different heater powers. (c) Resonance wavelength shift versus the reverse bias. (d) Shifts of the resonance wavelength and the modulation wavelength versus the heater power.

N-type background have a width and a height of 0.3 μm and 3 μm, respectively. The gap between two adjacent P-type strips is 0.5 μm, while the aggregate length of all P-type strips is 64 μm. The nominal doping concentration of the P-N junction is $1 \times 10^{18}/\text{cm}^3$, whereas the contact areas are heavily doped to $1 \times 10^{20}/\text{cm}^3$ to form an ohmic contact.

As there is no metal contact of high thermal conductivity outside the ring to dissipate the thermal flow, the heater can be implemented by the doped silicon in close proximity to the ring as shown in Figs. 1(a) and 1(b). Here, the heater was placed 1.8 μm away from the ring. Compared to the metal heater on top of the ring [5], or the doped silicon heater embedded inside the ring waveguide which shortens the modulation section length [4], this scheme neither requires any additional metallization steps nor impairs the modulation efficiency. The device was fabricated in the 200 mm CMOS pilot line of imec. A full description of the processing flow can be found in [12].

III. Static Measurement

The measurement is at first carried out in the DC regime. The transmission spectra under different reverse bias voltages on the P-N junction and different heater powers are shown in Figs. 2(a) and 2(b), respectively. The Q factor and the free spectral range (FSR) of the racetrack at 0 V bias are 13 100 and 7.3 nm, respectively. From these spectra we extract the resonance wavelength shift $\Delta\lambda$ vs. the reverse bias in Fig. 2(c) and vs. the heater power in Fig. 2(d). Provided a DC voltage swing from 0.5 V to -1 V, the maximum extinction ratio is 11 dB at 1555.56 nm accompanying with an insertion loss of 4 dB.

In Fig. 2(c), $\Delta\lambda$ is 81 pm for a voltage swing from 0.5 V to -3 V, which is equal to modulation efficiency $V_\pi L_\pi$ of 1.3 V·cm. If the voltage swings from 0.5 V to -0.5 V, the values of $\Delta\lambda$ and $V_\pi L_\pi$ are 28 pm and 1.1 V·cm, respectively. The modulation efficiency of our device compares favorably with the reported ring modulators based on deeply etched rib waveguides. The spectrum shifts for the same voltage swing from 0.5 V to -3 V are 77 pm for a modulator with a doped

silicon waveguide heater in [4], 58 pm for a modulator with a Ti heater in [5], 80 pm for a modulator with interleaved P-N junctions in [13], and 93 pm for the modulator in [7]. The comparison indicates that the DC modulation efficiency of our scheme is not inferior to deeply etched rib-waveguide-based modulators.

The resistance of the heater is measured to be 1500 ohm at room temperature. Its tuning efficiency is 45 pm/mW as shown in Fig. 2(d), which implies that 162 mW is required to shift the spectrum by a whole FSR. In contrast, the tuning power for one FSR is 66 mW for the ring with a doped waveguide heater in [4], and 46 mW for the ring with a Ti heater in [5]. The relatively poor efficiency originates from the low thermal conductivity of the 1.8 μm SiO_2 trench between the heater and the racetrack. We can improve the efficiency by reducing the width w of the doped silicon heater and the gap g between the heater and the ring, as well as by removing the undoped parts of the Si heater that act as an unwanted heat spreader. The horizontal temperature distributions along the waveguide center [the dashed line in Fig. 3(b)] are shown in Fig. 3(a) with a heater power of 50 mW for different values of w and g. Figure 3(b) depicts the two-dimensional temperature distribution for $w = g = 0.6$ μm. Our present design uses a 1.2 μm wide heater and a gap of 1.8 μm. As shown in Fig. 3(a), by shrinking the heater and the gap to 0.6 μm, the waveguide temperature rises by a factor of 2.2, which corresponds to a tuning power of 74 mW for one FSR. This is comparable with the heaters in [4], [5]. The optical intensity distribution in Fig. 1(c) indicates that a trench of 0.6 μm still provides sufficient lateral confinement. On the other hand, as shown in Figs. 1(a) and 1(b), the rectangular thermal isolation trenches are far from the heaters at the bottom of the arc, which impairs the effect of thermal isolation. As such, reshaping these thermal isolation trenches also helps improve the heater efficiency. With all these approaches, we expect that a heater power of <50 mW is able to tune the wavelength by one FSR. Further improvements include the backside substrate removal technique which can reduce the heater power by more than tenfold [14].

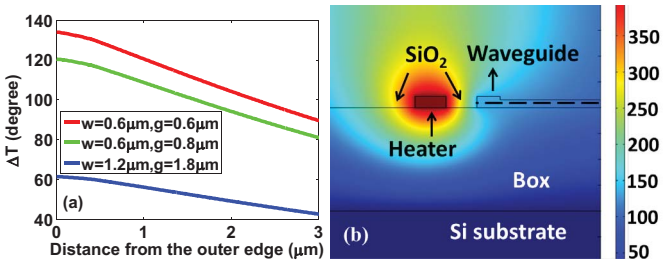

Fig. 3. (a) Horizontal temperature distributions along the center of the asymmetrical waveguide with a heater power of 50 mW. (b) Temperature profile for a waveguide cross section of $w = g = 0.6$ μm.

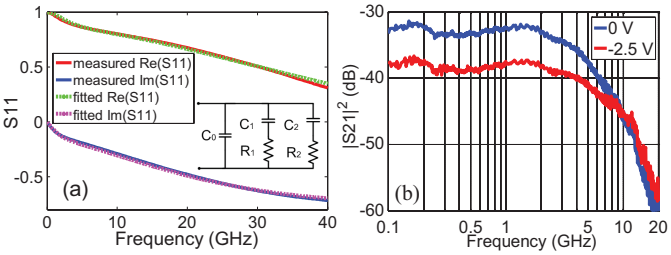

Fig. 4. (a) S11 parameter of the ring modulator with 0-V bias. (b) Frequency response of the EO modulation.

IV. Dynamic Measurement

The dynamic characterization includes the RF reflection coefficient measurement (the S11 parameter), the frequency response measurement of the electro-optical (EO) modulation (the S21 parameter), and the eye diagram measurement. The measured S11 is shown in Fig. 4(a) from 100 MHz to 40 GHz at 0 V bias, where the inset is the circuit used to represent the modulator. C_0 is the capacitance of the GSG pads, C_1 and R_1 represent the capacitance and the series resistance of the diode. Since both P^+ and N^+ contact regions locate inside the ring, there are PIN junctions between these contact regions. Two additional elements C_2 and R_2 are used to represent these PIN junctions as well as the parasitic effect of the buried oxide layer and the Si substrate [4]. We extract values of these elements from the S11 measurement result by curve fitting, which are: $C_0 = 30.6$ fF, $C_1 = 75.8$ fF, $C_2 = 19.8$ fF, $R_1 = 606$ Ω, and $R_2 = 83.3$ Ω. Dashed lines in Fig. 4(a) depict the fitted curves, which agree well with the measured data in the whole frequency range. Here we compare R_1 and C_1 with their theoretical expectation. At first, our C-V measurement preformed at 100 kHz shows that the diode capacitance per unit length is 0.44 pF/mm for the lateral PN junction-based modulators on the same wafer [12]. Since a P-type strip gives rise to two PN junctions on its left and right sides, we anticipate the diode capacitance per unit length of the doping pattern in Fig. 1(d) is roughly two times as high. Given the total length of all P-type strips is 64 μm, the final diode capacitance is around 56 fF. Secondly, the P-N junction is connected to the contact regions by doped bridges as shown in Fig. 1(d). A majority of total diode resistance comes from these narrow paths. According to the measured film resistance of doped silicon layer, bridge size and number, the total access resistance through these bridges is estimated to be 700 Ω. Therefore, the values of R_1 and C_1 extracted from S11 basically agree with the values expected from the physical structure.

In principle, the bandwidth of a ring modulator is limited by both photon lifetime and the RC constant. The ring quality factor of 13100 here leads to a photon lifetime limited 3-dB bandwidth of 14.8 GHz. It is much higher than the bandwidth of the circuit in Fig. 4(a). As such, the frequency response of the circuit dominates the EO modulation bandwidth. With the circuit, the 3-dB bandwidths of |S21| and $|S21|^2$, i.e., the optical and the electrical 3 dB bandwidths of the EO modulation, are calculated to be 6 GHz and 3.5 GHz, respectively. The measured frequency responses of $|S21|^2$ are shown in Fig. 4(b) from 100 MHz to 20 GHz for bias voltages of 0 V and −2.5 V. At 0 V, the 3 dB bandwidths are measured to be 5.9 GHz for |S21| and 4.1 GHz for $|S21|^2$, which generally agree with the prediction based on the measured S11 and the circuit in Fig. 4(a). A reverse bias of −2.5 V boosts the 3 dB bandwidths to 9.1 GHz for |S21| and 5.7 GHz for $|S21|^2$.

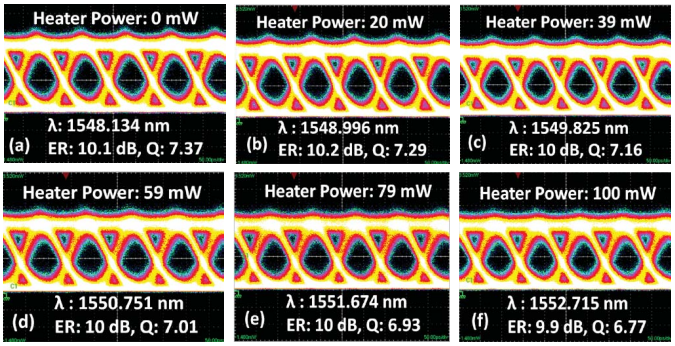

Fig. 5. Eye diagrams at different operation wavelengths and heater powers.

The modulation bandwidth here is mainly limited by the high diode resistance of 606 Ω which results from the narrow bridges connecting the PN junction and the contact regions. This can be relieved by expanding the width and shortening the length of these bridges, e.g., the diode resistance scales down to 210 Ω if we use bridges of 1 μm × 0.8 μm instead of 1.8 μm × 0.5 μm. This can significantly increase the modulation bandwidth. The optical intensity distribution in Fig. 1(c) indicates a bridge width of 1 μm is still long enough to isolate the optical mode from the contact regions of high loss. On the other hand, the PIN diodes between the P^+ and the N^+ contact regions can be removed by completely etching the silicon in between. In addition, our simulation confirms a bending radius of 5 μm with negligible bending loss, which implies the PN junction capacitor C_1 can be reduced as well. With all these measures, it is estimated that the final 3 dB bandwidth of $|S21|^2$ can exceed 11 GHz.

Eye diagrams are recorded under different heater powers by sending a 10 Gb/s non-return-to-zero (NRZ) pseudorandom binary sequence (PRBS) to the device through a high-speed GSG probe. The peak-to-peak voltage, pattern length, and bias voltage of the source PRBS signal are 2 V_{pp}, $2^{31}-1$ and −2.5 V, respectively. Due to the superposition between the input and the reflected RF signals, the practical voltage swing on the diode is around 4 V_{pp}. To measure eye diagrams, we could either adapt the heater power to the assigned operation wavelengths, or adapt the operation wavelength to the assigned heater powers. In other to compare the shifts of the optimal modulation wavelength and the resonance wavelength, we use the same heater powers used in Fig. 2(b), and then tune the wavelength to achieve the best performance. The corresponding eye diagrams are presented in Fig. 5, where a heater power of 100 mW tunes the operation wavelength by 4.581 nm (63% FSR). This indicates an average temperature rise of 62.6 °C according to $\Delta T = \Delta\lambda \cdot \lambda/(FSR \cdot L_r \cdot \partial n_{\text{eff}}/\partial T)$. Here n_{eff} is the effective index of the waveguide, and L_r denotes the perimeter of the racetrack ring. As the heater power goes up from 0 mW to 100 mW, the extinction ratio remains 10 dB, while the quality of the eye falls only slightly from 7.37 to 6.77 ($Q_{\text{eye}} > 6$ corresponds to a bit error rate of less than 10^{-9}). The dynamic ER falls to 8 dB if a PRBS signal of 1 V_{pp} is used to drive the modulator. Based on the circuit model in Fig. 4(a), the modulation energy consumptions are ∼230 fJ/bit and ∼50 fJ/bit for source PRBS signals of 2 V_{pp} and 1V_{pp}, respectively. With the current heater efficiency, the additional energy consumption caused by thermal tuning is as high as 16.2 pJ/bit at 10 Gb/s if the operation wavelength has to be shifted by a whole FSR. As discussed in Section 3, we can reduce the tuning power for one FSR to be less than 5 mW by optimizing the heater and removing the backside substrate. On the other hand, with the aforementioned approaches to increase the modulation bandwidth, we expect a bit rate of >20 Gb/s together with a modulation energy consumption of <20 fJ/bit. As such, the total energy consumption including modulation and thermal tuning will be well below 270 fJ/bit by improving the design.

V. Conclusion

We demonstrate an asymmetric racetrack modulator combining the compact footprint of microdisk modulators with the design simplicity of regular racetrack or ring modulators. The device can be fabricated along with optimized passive devices without introducing any additional Si patterning steps and enables straightforward implementation of integrated heaters based on doped Si strips. When driven by a 10 Gb/s PRBS signal of 2 V_{pp} swing, a fabricated device with a 10 μm radius exhibits a stable ER of 10 dB while a heater power of 100 mW tunes its operation wavelength over a range of 4.581 nm. By simply optimizing relevant design parameters, we expect that an improved device can finally operate beyond 20 Gb/s with a driving voltage of less than 1 V_{pp}.

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