Low-Power, 10-Gbps 1.5-Vpp Differential CMOS Driver for a Silicon Electro-Optic Ring Modulator

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***Abstract* - We present a novel driver circuit enabling electro-optic modulation with high extinction ratio from a co-designed silicon ring modulator. The driver circuit provides an asymmetric differential output at 10Gbps with a voltage swing up to 1.5V_{pp} from a single 1.0V supply, maximizing the resonance-wavelength shift of depletion-type ring modulators while avoiding carrier injection. A test chip containing 4 reconfigurable driver circuits was fabricated in 40nm CMOS technology. The measured energy consumption for driving a 100fF capacitive load at 10Gbps was as low as 125fJ/bit and 220fJ/bit at 1V_{pp} and 1.5V_{pp} respectively. After flip-chip integration with ring modulators on a silicon-photonics chip, the power consumption was measured to be 210fJ/bit and 350fJ/bit respectively.**

I. Introduction

Aggregate bandwidth requirements for I/O in advanced CMOS chips and stacked DRAM packages are expected to reach the level of multiple TB/s by 2018 [1]. Given the constrained I/O power envelope, the energy efficiency for an appropriate I/O solution will have to be on the order of 1pJ/bit or lower [2]. In addition, I/O bandwidth densities from the chip edge on the order of 1Tb/s/mm will have to be obtained. Meeting such challenging system level specifications is becoming increasingly more difficult using the traditional electrical solutions, and optical interconnects are increasingly being considered as a viable alternative to enable further I/O scaling.

Over the past ten years, tremendous progress has been reported on silicon-based photonics technology, including demonstrations of high-speed silicon modulators and Ge-based photodetectors [3]-[6]. Existing CMOS infrastructure can be leveraged for the fabrication of the silicon-based optical devices, promising high yields and low cost at high volumes. As a result, silicon photonics has become an attractive technology for realizing chip-scale optical interconnects.

However, enabling optical I/O scaling into the TB/s regime within the voltage constraints of advanced CMOS circuits will require the adoption and co-integration of the best-in-class silicon optical devices, combining low-loss optical channels with efficient electro-optic modulation and high photo-detection efficiencies at low applied voltages. In addition, the associated driver and amplifier CMOS circuits will need to be co-designed and optimized to obtain the desired link performance. Finally, co-integration of the silicon-photonics devices with advanced CMOS circuits will have to be realized with sufficiently low electrical parasitics.

An attractive approach for realizing the aforementioned requirements involves the 3-D flip-chip assembly through (micro-)bumping [7] of the CMOS logic die and/or DRAM stack onto a silicon-photonics optical chip (Fig. 1). Micro-bumping enables tight, hybrid integration of known-good dies fabricated with distinct optimized technologies within a single package and with acceptable electrical parasitics, enabling high bandwidth densities and high power efficiencies.

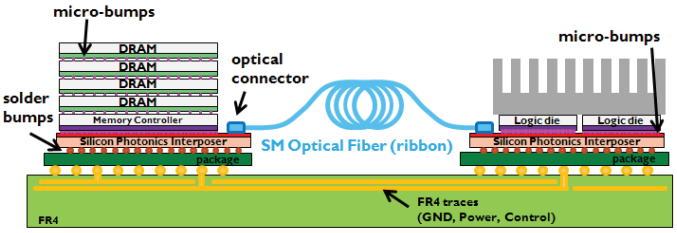

Fig. 1. CMOS logic to DRAM stack optical interconnect using a silicon-photonics interposer.

In this paper, we report on the design and implementation of a CMOS driver specifically developed for realizing a low-power silicon ring-based electro-optic transmitter with high optical extinction ratio and low insertion loss. The driver circuit provides an asymmetric differential output at 10Gbps with a programmable voltage swing from 1.0V_{pp} to 1.5V_{pp} from a single 1.0V supply.

In section II, the requirements for such ring-modulator driver are reviewed. Next, in section III, our approach for realizing such driver in 40nm foundry CMOS is presented in detail. Subsequently, the design of the transmitter CMOS test chip is described in section IV. The measurement results of the stand-alone CMOS test chip and first measurement results of a flip-chip assembly combining the CMOS chip with a silicon-photonics chip are then presented in section V, followed by a conclusion and outlook in section VI.

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II. Driver Circuit Requirements For Depletion-Based Silicon Ring Modulators

A schematic of a silicon-based single-wavelength optical link is depicted in Fig. 2. An external, fiber-coupled laser is used as an optical power supply, and is optically coupled to a silicon-photonics chip through a vertical fiber grating coupler [8]. On the photonics chip, the optical power can be split across multiple optical channels, each feeding through an on-chip waveguide into an electro-optic ring modulator. This modulator converts the electrical data stream originating from the sending CMOS chip into the optical domain, and is driven by a modulator driver on the CMOS chip. The modulated optical data stream is subsequently coupled into a second fiber, which connects the sending package to the receiving package. The optical data stream is then coupled to the photonics chip of the receiving package, using a polarization-diversity scheme [9], and fed into a Ge-based photodetector, which converts the optical data into a modulated current. Finally, the current-based data stream is converted into a digital data stream by a dedicated receiver amplifier.

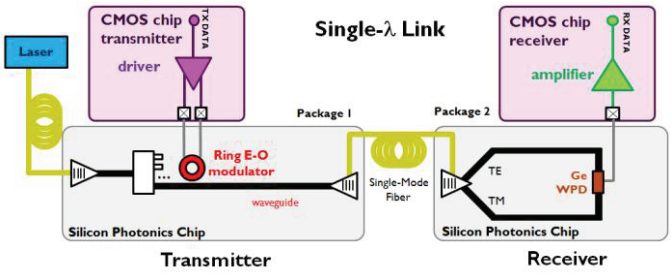

Fig. 2. Building blocks of an optical link.

In this paper, we focus on the transmitter part of the link, and we describe the co-design of a ring modulator and its driver circuit. In silicon electro-optic modulators, the free-carrier dispersion effect is exploited to realize an optical phase shift by adding or removing charge from the waveguide core [10], which is typically implemented through carrier depletion in an embedded a p-n junction. The resulting phase shift is translated into an optical intensity modulation by incorporating the phase shifter into an interferometric structure. Traditional Mach-Zehnder modulators typically require a phase shift in the order of 0.5-1 π in order to enable a high optical extinction ratio (ER) as well as a low insertion loss (IL) [11]. However, even in highly-confined silicon waveguides, the p-n diode required to obtain such a large optical phase shift typically represents a capacitive load of 1pF or more, and requires drive voltage swings of $2.0V_{pp}$ or more, which imposes a lower limit of ~1pJ/bit on the obtainable power efficiency of the transmitter. In contrast, silicon ring resonators based on the same p-n diode can enable high ER and low IL at a much lower capacitive load of less than 100fF and requiring less than $1.0V_{pp}$ swing, by exploiting the multiple roundtrips in the ring phase shifter at resonance. In rings with a sufficiently high quality factor, a shift of the resonant wavelength λ_r results in large ER at low IL, as shown in Fig. 3.

We have recently reported on the optimization of depletion-type 10Gbps silicon ring modulators using CMOS compatible voltage swings of $1.0V_{pp}$ [12]. Obtaining ultimate ER and IL requires a careful tuning of the optical quality factor and modulation efficiency $\Delta\lambda_r/\Delta V$. Both the ER and IL depend on the layout and doping level of the p-n diode as well as on the amplitude of the optical coupling between the ring and the bus waveguide, as illustrated in Fig. 3a. A typical, static modulation measurement of a 40μm radius ring modulator is shown in Fig. 3b. It can be seen that a voltage swing between -1.0V and 0V enables an ER >15dB, however at a large IL of ~8dB. By increasing the voltage swing to $1.5V_{pp}$ through a slight 0.5V forward bias, the ER is increased to >20dB and the insertion loss is reduced to less than 5dB. Further increasing the forward bias is not desired, as it would result in carrier injection into the diode, which is an intrinsically slow effect (<1GHz) [13].

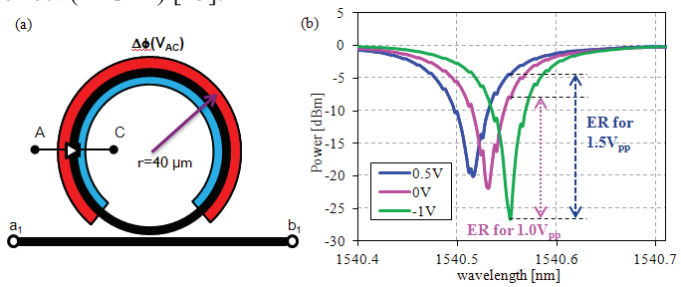

Fig. 3. (a) A schematic of the micro-ring modulator. (b) Measured and normalized transmission spectra for various applied voltages [12].

The depletion capacitance of the ring modulator was evaluated by measuring the S11 parameter and fitting an equivalent RLC circuit to the measured data. The measured and fitted S11 curves are shown in Fig. 4a, for frequencies up to 40GHz. A depletion capacitance of ~140fF was extracted, in addition to a ~10fF pad capacitance. In addition, an open eye diagram at 10Gbps was obtained by driving the modulator with a $1.0V_{pp}$ 2^{31}-1 PRBS data stream from a programmable pattern generator (Fig. 4b).

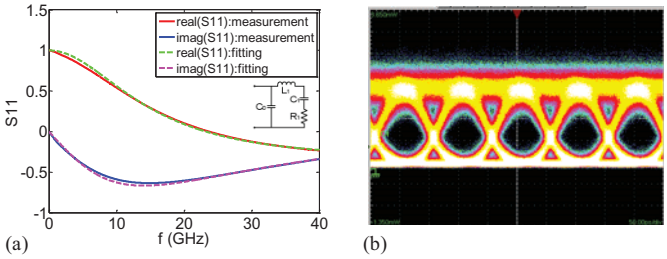

Fig. 4. (a) S11-parameter measurements of the ring modulator. (b) Measured 10Gbps eye diagram [12].

In addition to a low-capacitance optical modulator, a low-power optical transmitter also requires an energy efficient CMOS driver circuit. From the ring modulator description above, it is clear that the driver should provide a maximum (differential) voltage swing to maximize ER and minimize IL, while avoiding forward-biasing the diode above 0.7V to avoid carrier injection. The typical capacitive load represented by the ring modulator is in the range 50-200fF, depending on the ring radius and the diode configuration.

III. Driver Circuit Implementation

Different approaches for the driver design can be proposed in order to maximize the voltage swing across the modulator. In [14] and [15], a single-ended cascode driver stage with double, 1-V and 2-V power supply was implemented to obtain a $2V_{pp}$ voltage swing. Although excellent power efficiencies of 135fJ/bit and a $2V_{pp}$ swing were obtained for ~70fF load, the need for two power supplies increases the complexity of this implementation.

The driver presented in this paper operates from a single power supply. It comprises an asymmetric differential output to enable forward biasing of the ring modulator, maximizing the voltage swing applied to the modulator.

The block diagram of the differential driver design is shown in Fig. 5.

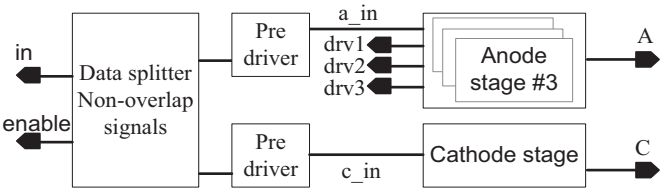

Fig. 5. A block diagram of the driver.

The anode and cathode of the diode are each driven separately from a dedicated stage. The cathode stage contains a set of inverters providing a full voltage-supply swing to the cathode of the diode, resulting in a reverse diode bias to the order of the supply voltage for loads up to around 400fF.

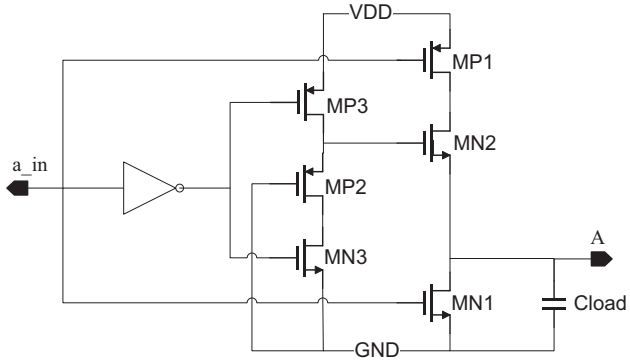

Fig. 6. A schematic of the anode stage of the driver.

The anode stage provides a forward bias to the diode by applying a fraction of supply voltage to the anode of the diode, which can significantly extend the modulation depth of the optical signal as explained in section II. To minimize the power consumption, the anode stage has been designed without a short-circuit path. The forward bias voltage is programmable via 3 switches as shown in Fig. 6, which allow controlling the anode drive strength according to the load capacitance. The obtained anode voltage depends on the state of the switches and on the load capacitance. Transistor MN2 works as a switch closing the charging path while MP1 is active. The width ratio of the transistors MN2 and MN3 determines how fast the gate voltage of MN2 decreases. Once MN2 is deactivated, the loading path is closed and the output voltage is fixed at a value always lower than the supply voltage, avoiding carrier injection into the diode. Each of the 3 circuits forming the anode stage has been designed with different transistor dimensions in order to reach the required output voltage for a given capacitive load. The fully activated anode stage is capable of driving a load capacitance up to 350fF with a 0.5V voltage swing.

Finally, the input data stream arriving at the driver is first going through a data splitter block for non-overlapping signals, which is feeding the data to the anode and cathode stage. This block has been included to limit the short-circuit current, which helps to further reduce the power consumption of the driver. A draw-back of this approach is that the data-splitter block reduces the maximum obtainable modulation speed to 10Gbps.

IV. Transmitter Test Chip Design

The CMOS transmitter test chip contains 4 configurable ring-modulator drivers as described in section III, an Phase-Locked Loop (PLL) used as an on-chip clock source, a 512-bit programmable shift register used as an on-chip pseudo-random bit-sequence (PRBS) data source (data can be provided externally), and a Network on Chip (NoC) to control each of the CMOS blocks. A schematic representation of the CMOS chip containing the driver circuit is shown in Fig. 7.

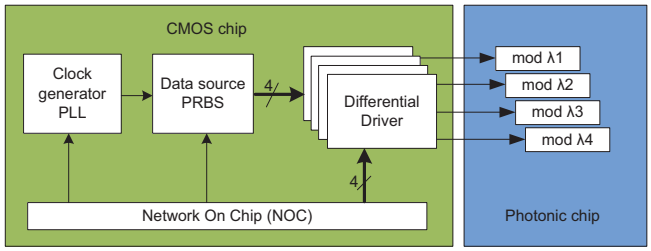

Fig. 7. A block diagram of the CMOS chip and the components for the optical transmitter demonstrator.

The flexible design of the CMOS transmitter chip allows covering a wide range of bit transmission rates (200Mbps up to 18Gbps) and different transmission modes, e.g. with or without additional forward biasing of the ring modulator. This flexibility allows exploring the most optimum optical transmitter configuration in terms of the power consumption of the modulator and the drivers, as well as the required laser power for a given BER.

A. On-chip data source - PRBS block

Besides the actual driver circuits, a high data rate digital data source has been integrated to simplify testing. The generated data sequence must be well known for bit-error rate measurement. A PRBS generator with a programmable 512bits shift register was developed. The pseudo random data generator is a programmable, 512-bit shift register which provides serial data for the drivers at speed up to 18Gbps. To achieve such a speed, 8x64-bit shift registers have been designed together with a high speed serializer (Fig. 8). The frequency divider provides a properly phase-shifted clock signal for the high-speed multiplexers and for each shift register.

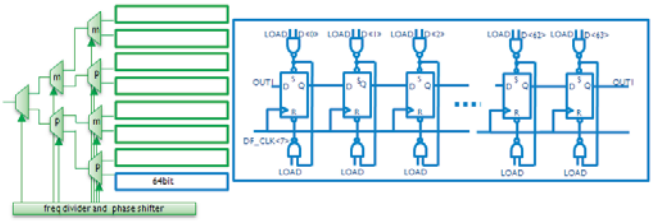

Fig. 8. A Block diagram of the 8:1 serializer with clock and 64-bit parallel-in/serial-out shift register.

B. PLL and NoC

To complete the transmitter test chip, a PLL with integrated VCOs provides a clock signal which can be programmed at frequencies from 100MHz up to 14GHz. Finally, the CMOS components on the test chip (PLL, drivers and shift register) are controlled through the NoC controller.

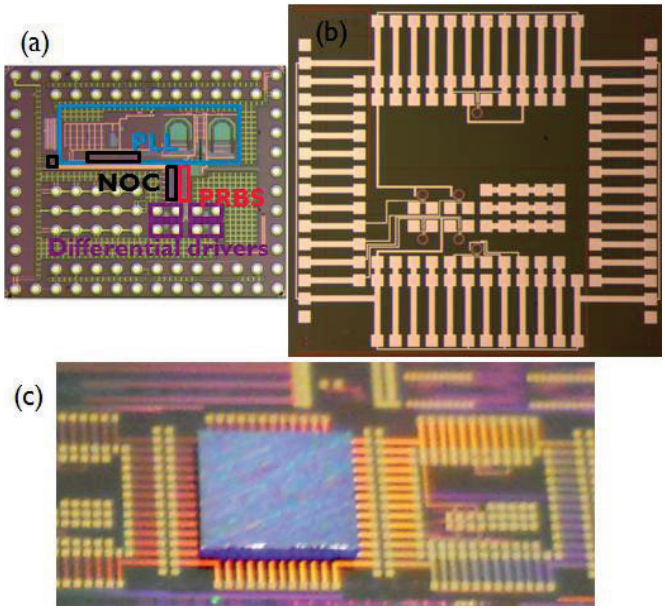

Fig. 9. (a) Fabricated CMOS test chip. (b) Co-designed photonic chip containing the silicon ring modulators. (c) CMOS transmitter chip flip-chipped on top of a photonic chip.

V. Measurement Results

A. Stand-alone CMOS test chip

Fig. 9a shows a microscope picture of the fabricated CMOS chip with the different components highlighted.

The CMOS chip was wire-bonded to a PCB for electrical measurement purposes. High speed signals, such as the reference clock for the PLL, the PRBS output and the outputs of the differential drivers, have been wired to the RF lines on the PCB. The Network on Chip was used to control CMOS components – to set or sweep PLL frequency and to program the shift registers (PRBS) to generate a continuous clock-like "1010..." data sequence.

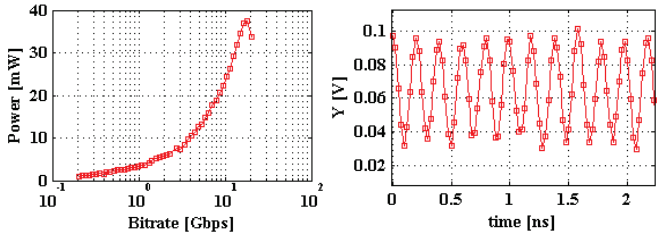

Fig. 10. Measured power consumption and output waveform of the PRBS block, programmed with clock–like data.

The output of the PRBS was measured with a high-speed logic analyzer and oscilloscope. Fig. 10 shows the measurement results of PRBS – the power consumption and the output waveform for clock-like data. The PRBS block is capable of feeding the drivers with data at a speed up to 18Gbps.

At bitrates above 2Gbps, a degradation in the amplitude of the output signal is observed, which might be explained by the high-frequency loss caused by wire bonds, PCB, cables and the instruments load.

A functional test and an IDDQ test have been performed on the drivers. The functionality of the driver has been verified by measuring the outputs of the cathode and the anode stage at 4Gbps. The measurement results show good agreement with post layout simulations, performed including the capacitive load of the bond pads load (100fF) (Fig. 11).

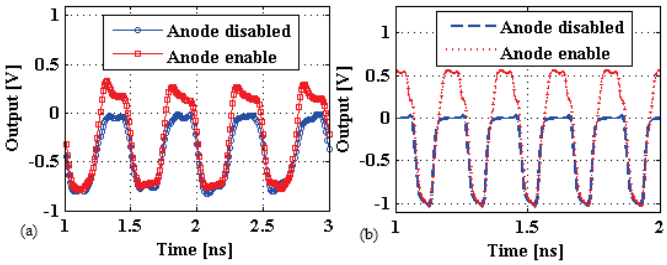

Fig. 11. Output waveform of the driver. (a) Measurement at 4Gbps.(b) Simulation at 10Gbps with enabled and disabled anode stage.

The power consumption of the drivers has been measured at different bit rates and supply-voltage levels. Based on the measured power consumption, the energy per bit has been calculated by dividing average power consumption by the bit rate.

The measured and simulated energy efficiencies of the driver with activated anode stage ($1.5V_{pp}$ swing) are shown in Fig. 12, for a clock-like data stream.

The measured energy consumption of the drivers loaded only with the bond pads on the CMOS chip matches very well with simulated results (PEX level), assuming a 100fF capacitive load of the bond pads . For bit rates below 10Gbps, the energy consumption per-bit is flat owing to dominant dynamic power consumption of the driver. At bit rates exceeding 10Gbps, the output signal of the driver no longer reaches the desired voltage swing, resulting in a reduced the power consumption, and an accordingly lower energy per bit.

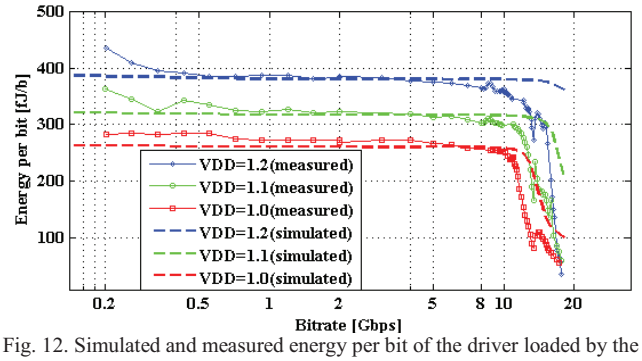

Fig. 12. Simulated and measured energy per bit of the driver loaded by the bond pads (100fF) for various supply voltages. A clock-like data stream is applied and the anode stage is disabled ($1.0V_{pp}$ swing).

For PRBS data, the dissipated energy per bit (E_{bit}) is equal to half of the energy for clock-like data presented in Fig. 12 because of equal probability of occurrence consecutive '00' and '11' in a bit sequence. As such, at 10Gbps, the energy efficiency E_{bit} for PRBS data is equal to 125fJ/bit when the anode stage is disabled and 220fJ/bit when the stage is enabled.

B. Transmitter package: CMOS driver flip-chip integrated with a silicon-photonics carrier chip

Next, a CMOS test chip was integrated by flip-chip assembly techniques with a specifically co-designed silicon-photonics chip containing 4 depletion-type ring modulators as described in section II. Conventional flip-chip techniques using eutectic solder bumps were employed, with 100-um wide bond pads on a 150-um pitch.

After flip-chip integration, preliminary electrical testing of the transmitter package was carried out by probing the CMOS chip through metal lines and contact pads on the photonics carrier die, using multi-contact wedge probes. The NoC, PLL and PRBS CMOS blocks could be successfully activated when probed though the flip-chip package. The power consumption of the drivers, now loaded with the actual silicon ring modulator (~140fF), was measured. The results are shown as energy per bit in Fig. 13.

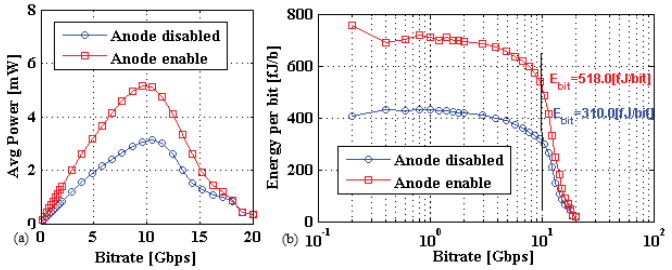

Fig. 13. Measurement results of the driver loaded with the micro-ring modulator for clock-like data: (a) Power consumption (b) Energy-per-bit.

The addition of the ring-modulator load resulted in an increase in the driver energy consumption of 85fJ/bit (140fJ/bit) for the disabled (enabled) anode stage, resulting in a total energy consumption of 220fJ/bit (350fJ/bit).

The measured power consumption of the flip-chip package also shows very good agreement with post-layout simulation, performed with total load of 250fF (CMOS pads ~100fF, ring modulator ~140fF and ~10fF for additional bumps parasitics) (Fig. 14). The maximum modulation speed of the driver is approximately 10Gbps at 1.0V supply and is in this design mainly limited by the data-splitter block of the driver as discussed in section III.

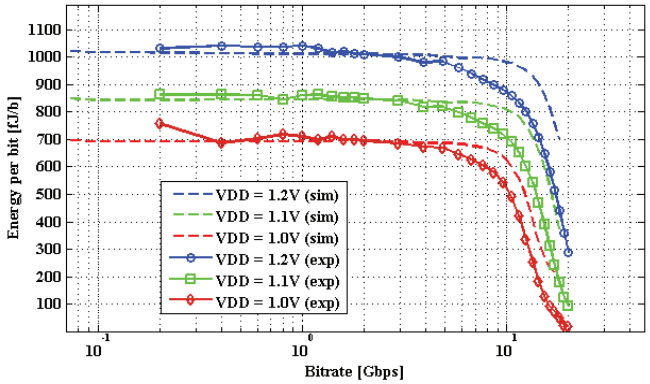

Fig. 14. Energy plot of the driver with anode stage enabled ($1.5V_{pp}$ voltage swing) with flip-chip package. Post layout simulation results (doted lines) with total load of 250fF.

VI. Discussion And Conclusion

Table 1 shows the energy consumption of our driver with and without the ring-modulator load, and compares this with previous results [14] and [15]. It can be seen that our driver has somewhat higher power consumption at $1.5V_{pp}$ swing as compared to the $2.0V_{pp}$ drivers presented in [14]. However, it should be noted that our driver was designed for driving a bigger ring modulator representing a higher load (up to 350fF), compared to the one presented in [14]. A reduction in power consumption can be obtained for driving smaller rings by reducing the size and strength of the driver's output stages.

TABLE I
Comparison of driver implementations.

Ref.	# Power Supplies	Load [fF]	Speed [Gbps]	Power [fJ/bit]	Swing (V_{pp})
[14]	2	~ 70	10	135	2.0
[15]	2	~ 70	5	320	2.0
This work	1	~ 100	10	125	1.0
				210	1.5
		~250		220	1.0
				350	1.5

A full electro-optic characterization of the transmitter package is pending. In these measurements, the optimum transmitter configuration will be evaluated, minimizing the overall power consumption of the transmitter (including laser power) for a given BER at a reference detector. Indeed, the increased driver power consumption when enabling the anode stage of the driver for obtaining higher ER at $1.5V_{pp}$ has to be compared and traded with the potential reduction in required laser power to achieve a similar BER of the full optical link.

The conventional flip-chip integration used in the current demonstrator doesn't allow us to obtain the ultimate transmitter power efficiencies due to the high capacitance

(~100fF) of the relatively large bond pads. State-of-the-art microbumping technology with bond pads as small as 15um are currently under development at imec, which, when combined with 10um radius ring modulators, will enable to reduce the total pad + driver load to below 50fF, resulting in a dynamic power consumption of the transmitter below 100fJ/bit.

Finally, it should be noted that an integrated heater element as well as an active feedback control loop will need to be added to thermally stabilize the ring modulator, as the ER and IL are highly sensitive to temperature variations [16]. The power consumption of these elements needs to be included to assess the total power consumption of the full electro-optic transmitter, in addition to the power consumption of the driver, the ring modulator and the laser diode.

In conclusion, we have presented the design and the electrical measurement results of a silicon ring-modulator driver with asymmetric differential output. The reconfigurable driver can provide a voltage swing from $1.0V_{pp}$ up to $1.5V_{pp}$ from a single 1.0V power supply, targeting high extinction ratios from depletion-type ring modulators. A 40nm CMOS test chip containing four driver circuits, an on-chip PRBS generator, and a PLL and was designed, fabricated and tested. The measured energy consumption for driving a 100fF bond-pad capacitive load at 10Gbps was as low as 125fJ/bit and 220fJ/bit at $1.0V_{pp}$ and $1.5V_{pp}$ respectively. The CMOS drivers were subsequently flip-chip integrated with a silicon ring-modulator chip, and preliminary electrical testing of the loaded drivers revealed a power consumption of 210fJ/bit and 350fJ/bit at $1.0V_{pp}$ and $1.5V_{pp}$ drive swing respectively. A substantial power reduction is possible in a future design by shrinking the ring modulator size, driver output stages and bond pads.

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REFERENCES

[1] I.A. Young, E.M. Mohammed, J.T.S Liao, A.M. Kern, S. Palermo, B.A. Block, M.R. Reshotko, P.L.D. Chang, "Optical technology for energy efficient I/O in high performance computing," Communications Magazine, IEEE, Volume: 48, Issue: 10, 184 - 191, Oct. 2010.

[2] D.A.B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proc. IEEE 97, 1166 – 1185, 2009.

[3] C.T. DeRose, C.D. Trotter, W.A. Zortman, A.L. Starbuck, M. Fisher, M.R. Watts, P.S. Davids, "Ultra compact 45 GHz CMOS compatible Germanium waveguide photodiode with low dark current," Optics Express, Vol. 19, Issue 25, pp. 24897-24904, 2011.

[4] G. Li, X. Zheng, Jin Yao, H. Thacker, I. Shubin, Ying Luo, K. Raj, J.E. Cunningham, A.V. Krishnamoorthy, "High-efficiency 25Gb/s CMOS ring modulator with integrated thermal tuning," Optics Express 19(21), 20435-443, 2011.

[5] A.V. Krishnamoorthy, Ron Ho, X. Zheng, H. Schwetman, Jon Lexau, P. Koka, G. Li, I. Shubin, J.E. Cunningham, "Computer Systems Based on Silicon Photonic Interconnects," Proceedings of the IEEE, 97 (7) 1337-1361, 2009.

[6] X. Zheng, D. Patil, J. Lexau, F. Liu, G. Li, H. Thacker, Y. Luo, I. Shubin, J. Li, J. Yao, P. Dong, D. Feng, M. Asghari, T. Pinguet, A. Mekis, P. Amberg, M. Dayringer, J. Gainsley, H.F. Moghadam, E. Alon, K. Raj, R. Ho, J.E. Cunningham, A.V. Krishnamoorthy, "Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver," Opt. Express 19, 5172-5186, 2011.

[7] W. Zhang, B.D.P. Limaye, A.L. Manna, P, Soussan, E. Beyne, "Ni/Cu/Sn bumping scheme for fine-pitch micro-bump connections," 61st Electronic Components and Technology Conference (IEEE 2011), pp. 109 – 113.

[8] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, R. Baets, "Grating Couplers for Coupling between Optical Fibers and Nanophotonic Waveguides," Japanese Journal of Applied Physics (invited), 45(8A), p.6071-6077, 2006.

[9] D. Taillaert, H. Chong, P. Borel, L. Frandsen, R.M. De La Rue, R. Baets, "A compact two-dimensional grating coupler used as a polarization splitter," IEEE Photonics Technology Letters, 15(9), p.1249-1251,2003.

[10] A. Soref, B.R. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electronics, QE-23 (1), pp. 123—129, January 1987.

[11] B.G. Lee, W.M.J. Green, J. Van Campenhout, C.L. Schow, A.V. Rylyakov, S. Assefa, M. Yang, J. Rosenberg, J.A. Kash, Y.A. Vlasov, "Comparison of Ring Resonator and Mach-Zehnder Photonic Switches Integrated with Digital CMOS Drivers," IEEE Photonics Society, 327 – 328, 2010.

[12] M. Pantouvaki, H. Yu, P. Verheyen, G. Lepage, W. Bogaerts, M. Moelants, J. Wouters, D. Radisic, A. Vandervorst, P. Absil, J. Van Campenhout, "Lateral versus Interdigitated Diode Design for 10 Gb/s Low-Voltage Low-Loss Silicon Ring Modulators," IEEE Optical Interconnects Conference, 2012.

[13] J. Rosenberg, W.M. Green, A. Rylyakov, C. Schow, S. Assefa, B.G. Lee, C. Jahnes, Y. Vlasov, "Ultra-low-voltage Micro-ring Modulator Integrated with a CMOS Feed-forward Equalization Driver," in OFC, OSA, OWQ4, 2011.

[14] F. Liu, D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H.F. Moghadam, Xuezhe Zheng, J.E. Cunningham, A.V. Krishnamoorthy, E. Alon, R. Ho, "10 Gbps, 530 fJ/b Optical Transceiver Circuits in 40nm CMOS," Proc. IEEE Symp. VLSI Circuits, 2011..

[15] G. Li, X. Zheng, J. Lexau, Ying Luo, H. Thacker, Po Dong, Shirong Liao, Dazeng Feng, Dawei Zheng, R. Shafiiha, M. Asghari, Jin Yao, Jing Shi, P. Amberg, N. Pinckney, K. Raj, R. Ho, J. Cunningham, A.V. Krishnamoorthy, "Ultralow-Power High-Performance Si Photonic Transmitter," OFC/NFOEC, 1-3, 2010.

[16] K. Padmaraju, J. Chan, L. Chen, M. Lipson, and K. Bergman, "Dynamic Stabilization of a Microring Modulator Under Thermal Perturbation," in Optical Fiber Communication Conference, OSA Technical Digest (Optical Society of America, 2012), paper OW4F.2.