Silicon-Photonics Devices for Low-Power, High-Bandwidth Optical I/O

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Abstract: Electro-optic transceivers integrated in silicon-photonics interposers are attractive for realizing low-power high-bandwidth Optical I/O for future advanced logic and memory. We review recent results obtained at imec on low-voltage silicon ring modulators and Ge photodetectors.
OCIS codes: (200.4650) Optical interconnects; (250.4110) Modulator; (250.0040) Detectors

1. Silicon-Photonics Interposer Technology for 3-D Optical I/O

Aggregate bandwidth requirements for I/O in advanced CMOS chips and stacked DRAM packages are expected to reach the level of multiple TB/s by 2018. Given the constrained I/O power envelope, the energy efficiency for a proposed silicon-based Optical I/O solution will have to be on the order of 1pJ/bit or better [1]. In addition, I/O bandwidth densities from the chip edge into optical fiber (ribbons) on the order of 1Tb/s/mm will have to be obtained, likely requiring the introduction of wavelength-division multiplexing (WDM) techniques.

Obtaining such power efficiencies and bandwidth densities within the voltage constraints of advanced CMOS circuits will require the adoption of the best-in-class silicon optical devices, combining low-loss optical channels with high modulation and photodetection efficiencies at low applied voltages. Although monolithic integration of photonics into the CMOS flow would arguably enable the highest integration density and best power efficiencies, co-integration of high-performance silicon optical devices becomes increasingly more challenging in advanced CMOS nodes, and it is not clear if sufficient compound yield can be obtained at low cost.
An attractive alternative for silicon-based Optical I/O involves the 3-D flip-chip assembly through microbumping [2] of a silicon-photonics interposer with the CMOS logic die and/or DRAM stack, as shown in Fig. 1. Microbumping enables tight, hybrid integration of know-good dies fabricated with distinct optimized technologies within a single package, with low electrical parasitics. The potential of tight-pitch microbumping for realizing silicon optical transceivers with sub-pJ/bit energy efficiency using has already been demonstrated in [3].
In this paper, we review the recent progress at imec on low-voltage, low-loss silicon ring modulators and Ge waveguide photodetectors and their co-integration on a silicon-on-insulator wafer for realizing a high-performance silicon-photonics interposer, as a first step to toward a competitive 3-D Optical I/O technology.

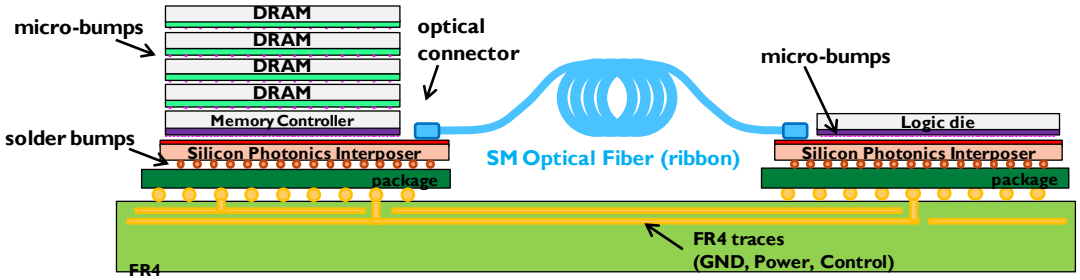

Figure 1: Concept of silicon-photonics interposers for high-bandwidth, low-power 3-D Optical I/O for advanced CMOS logic and DRAM stacks.

2. Low-loss, low-voltage silicon electro-optic ring modulators

Silicon ring optical modulators are attracting increasing interest for low energy, small footprint optical interconnects co-integrated with CMOS electronics. Key requirements for such devices are high extinction ratio (ER~10dB), low insertion loss (IL<1dB), high modulation speed (>10Gb/s) and low energy per bit (<50fJ/bit). Recently, 10 Gb/s and 25 Gb/s optical modulation has been reported in carrier-depletion ring modulators using a 1 V peak-to-peak driving voltage (V_{pp}) [4]. However, the obtained extinction ratios were limited to 5dB for insertion losses lower than 3dB. Such modulators are typically designed with the depletion area parallel to the waveguide (lateral diode design). Modulators with junctions perpendicular to the waveguide (interdigitated diode design) have been proposed to

increase the modulation efficiency and extinction ratio, however so far they required high voltage swings V_{pp}, incompatible with CMOS [5]. We have fabricated and compared the performance of two identical ring modulators, differing only in the diode design [6]. We find that the interdigitated design results in higher modulation efficiency, achieving a 7.5 dB extinction ratio for 3 dB insertion loss using 1 V_{pp}, as opposed to only 3 dB extinction ratio with the lateral diode design. Open eye diagrams were obtained at 10 Gb/s for both modulator types, as illustrated in Fig. 2c for the interdigitated design. Design improvements are expected to improve the modulation speed of the interdigitated modulator up to 25Gb/s. Modulation speeds up to 40Gb/s have already been demonstrated in Mach-Zehnder modulators with traveling-wave electrodes and the conventional lateral diode designs [7].

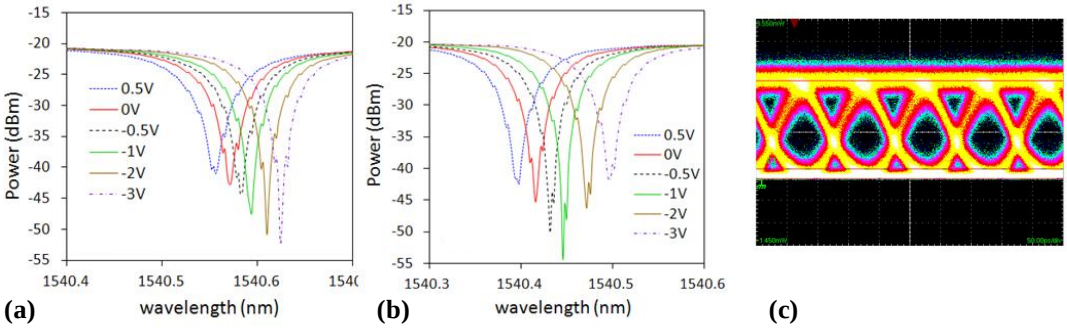

Figure 2: a) Static through-port transmission spectra showing the resonance wavelength shift vs. applied voltage for depletion ring modulators (40μm radius) with lateral (22pm/V) and b) interdigitated diode design (30pm/V). c) 10Gb/s eye diagram at 1.2V_{pp} for a ring modulator with interdigitated diode design [6].

As an alternative to depletion-type modulators, we also explore compact ring modulators based on an embedded metal-oxide-semiconductor (MOS) capacitor (see Fig. 3, [8]). Owing to the high efficiency of the embedded MOS-based phase shifter [6], a MOS ring modulator exhibits a resonance-wavelength shift of more than 130pm/V, as shown in Fig. 3e. An ER as high as 8dB was obtained together with an IL of only 3dB for a voltage swing of only 1.5Vpp in a MOS device with a relatively low optical Q of only 3500. Open eye diagrams were obtained up to 3Gb/s, limited by the RC cut-off frequency. Proposed design improvements will enable modulation speeds well beyond 10Gb/s in future devices, leveraging the intrinsically fast carrier-accumulation effect. As such, MOS-based ring structures offer a compelling platform for realizing robust, ultra-low voltage silicon modulators, likely surpassing the performance trade-offs that can be obtained with depletion-based ring modulators.

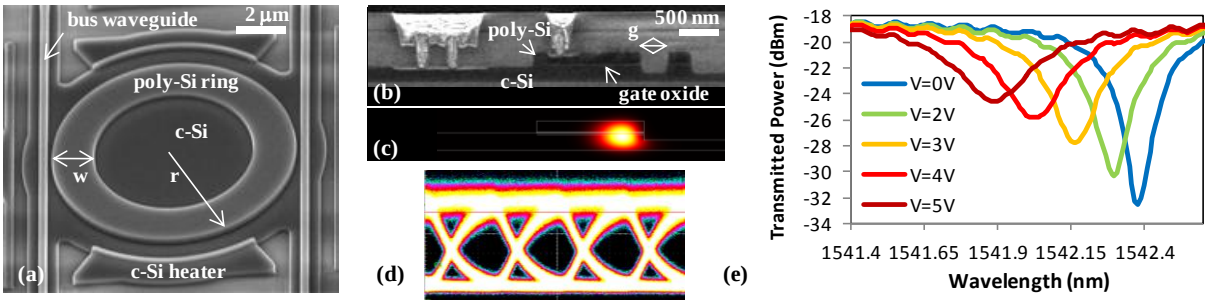

Figure 3: a) Tilted top-view SEM image of a MOS ring modulator, b) cross section SEM image of MOS structure, (c) simulated mode profile of the fundamental whispering-gallery mode, (d) 2Gb/s eye diagram for 1.5V_{pp} drive signal, and (e) static through-port transmission spectra for various applied voltages (136pm/V) [8].

3. High-responsivity Ge-on-Si waveguide photodetectors

Low-power silicon-based optical transceivers require the co-integration of high-speed Ge waveguide photodetectors with high responsivity and low dark currents on the same substrate as the silicon modulators. We have developed a process module for co-integrating Ge photodetectors with the MOS modulators described in section 2 [10]. The module involves selective Ge epitaxial growth by reduced-pressure chemical-vapor deposition, followed by a post-growth anneal to remove threading dislocations from the Ge. Subsequently, chemical-mechanical polishing is employed to flatten the Ge patterns. The existing topography in the underlying Si and poly-Si layers can be used to fabricate "inverted-rib" Ge waveguide structures by deliberate lateral overgrowth of the Ge (see Fig. 4a). Such laterally overgrown areas can be exploited to reduce the optical absorption at metal contacts, by providing lateral confinement away from the lossy metals for the optical mode propagating in the Ge waveguide.

Lateral p-i-n Ge waveguide photodetectors were fabricated with widths in the range 1.4μm to 3μm and lengths in the range 5μm to 50μm. The dark current was measured to be around 2μA at -1V at 25C (Fig. 4c). The photodetector responsivity at 1.5μm wavelength was measured to be around 0.72A/W for a 2μm-wide device, and up to 0.9A/W for a 3μm-wide device, both 20μm long. For the "inverted-rib" Ge photodetector, the responsivity was as high as 0.9A/W even for a 1μm-wide device, owing to the reduced impact from metal absorption losses. High-speed characterization was also performed for a 5x2μm^2 Ge PD. An open eye diagram was obtained at 10Gb/s for -2V (Fig. 4b).

Although the demonstrated levels for dark current and responsivity are slightly worse than some of state-of-the-art (stand-alone) Ge-on-Si photodetectors [11], this performance is already sufficient for realizing power-efficient receivers with -15dBm sensitivity [3]. In addition, it was found that the dark current depends only weakly on device length and temperature (4.5μA at -1V at 100C, Fig. 4c). As such, we believe that the dark current originates mainly from a parasitic edge effect, which can likely be mitigated in future designs.

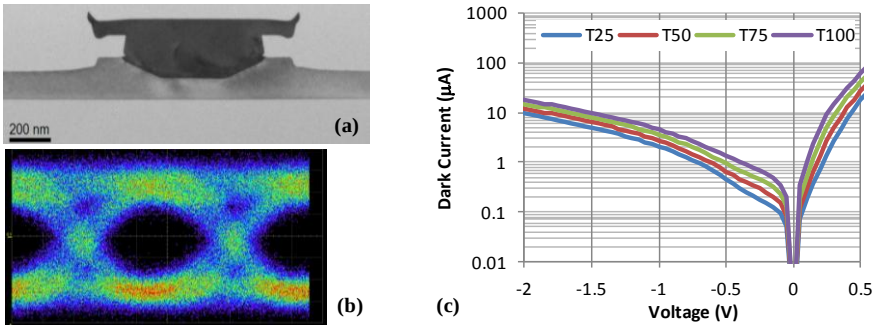

Figure 4: a) TEM image of a Ge waveguide photodectector with laterally overgrown contact areas (prior to contacting module), b) 10Gb/s eye diagram for a 5x2μm^2 Ge PD at -2V, c) dark current vs. voltage and temperature for a 10x2μm^2 Ge PD.

4. Conclusion

The adoption of silicon photonics as a technology for low-power high-bandwidth Optical I/O is contingent upon the co-integration of highly efficient silicon optical devices, including both voltage-efficient silicon modulators and highly responsive Ge photodetectors. Recent results on low-loss, low voltage depletion and accumulation ring modulators have been reviewed, as well as the co-integration with Ge photodetectors.

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