Low-Voltage, Low-Loss, Multi-Gb/s Silicon Micro-Ring Modulator based on a MOS Capacitor

Joris Van Campenhout, Marianna Pantouvaki, Peter Verheyen, Shankar Selvaraja[1,2], Guy Lepage, Hui Yu[1,2], Willie Lee, Johan Wouters, Danny Goossens, Myriam Moelants, Wim Bogaerts[1,2], and Philippe Absil

imec, Kapeldreef 75,3001 Leuven, Belgium

[1]Photonics Research Group, Dept. of Information Technology,Ghent University – imec, St.-Pietersnieuwstraat 41,9000 Ghent, Belgium

[2]Center for Nano- and Biophotonics (NB Photonics), St.-Pietersnieuwstraat 41,9000 Ghent, Belgium

jvcampen@imec.be

Abstract: Optical modulation with 8dB extinction ratio and 3dB insertion loss is achieved by applying a 1.5-V_{pp} drive voltage to a 10-μm ring with embedded MOS capacitor. Open-eye diagrams are obtained at 3Gbps.

OCIS codes: (230.4110) Modulators; (200.4650) Optical Interconnects

1. Introduction

A low-power, compact, high-speed silicon electro-optic modulator is a key device for realizing scalable, high-bandwidth optical interconnects for future high-performance computing systems [1]. The ideal optical modulator provides a high extinction ratio (ER) of more than 7dB together with an insertion loss (IL) below 1dB, with an energy consumption (E_{bit}) of less than a few tens of femto-Joules per bit at speeds of 10Gb/s and above, all obtained from an electrical drive signal that is directly generated by circuits implemented in advanced CMOS technologies (voltage swing of less than $1V_{pp}$).

Over the last several years, substantial progress has been made to reach these specifications, mostly by using silicon ring modulators with embedded p-n junctions operated in charge-depletion [2] or charge-injection mode [3]. While devices based on carrier injection exhibit a strong modulation efficiency enabling resonance-wavelength shifts on the order of 1nm/V, slow carrier diffusion and a high capacitive load require pre-emphasized drive signals for obtaining speeds above 1Gb/s [3], which increases complexity and power consumption. Ring modulators based on carrier depletion have demonstrated an electrical bandwidth in excess of 40GHz. However, even highly optimized depletion-based ring modulators exhibit a much smaller resonance-wavelength shift of only 40pm/V [2]. Consequently, the depletion-based ring modulators have to be designed with an optical quality factor Q in the order 15000 in order to reach an acceptable ER and IL when driven with only $1V_{pp}$ [1, 2]. As a result, very accurate temperature control of the ring temperature of better than ±0.1K will be needed in order to maintain the appropriate bias of the resonance wavelength with respect to the laser wavelength. In addition, the modulation speed is limited in these devices by the cavity photon lifetime.

In this paper, we demonstrate a compact, low-loss, low-voltage ring modulator based on an embedded metal-oxide-semiconductor (MOS) capacitor. Owing to the high efficiency of the embedded MOS-based phase shifter [4,5], the ring exhibits a resonance-wavelength shift as high as 130pm/V. An ER as high as 8dB is obtained together with an IL of only 3dB for a voltage swing of only $1.5V_{pp}$ and a relatively low Q of only 3500. Open eye diagrams were obtained at 3Gb/s. Design improvements will be proposed to obtain modulation speeds well above 10Gb/s in future devices, leveraging the intrinsically fast carrier-accumulation effect.

2. Modulator design and fabrication

The MOS-based ring modulator was fabricated on a 200-mm SOI wafer with 2-μm buried oxide and 220-nm top c-Si layer using processing modules from imec's Silicon-Photonics Platform (iSiPP), which also supports co-integration with advanced passive optical devices [6]. First, a local phosphorous implant to about $5\times10^{17}cm^{-3}$ was performed to obtain an n-type doped c-Si layer where the modulators will be fabricated. Subsequently, a 5-nm gate oxide was grown, followed by the deposition of a 160-nm amorphous Si layer. Then, a four-level patterning sequence involving 193-nm lithography and Si dry etching steps was carried out. First, the top a-Si layer was locally etched together with 70nm of the underlying c-Si to define the outer edge of the ring modulator and the bus waveguides. Subsequently, the top a-Si layer was locally etched to expose the c-Si layer in the center of the ring. Finally, two more patterning steps were carried out in which respectively 70nm and 220nm of the c-Si layer were locally etched to define fiber-grating couplers as well as strip access waveguides, followed by a spike anneal to crystallize the a-Si into poly Si. Then, the top poly-Si ring was implanted with boron ions to about $1\times10^{18}cm^{-3}$. Subsequently, local high-dose boron and phosphorous implants were carried out, followed by an activation anneal and a local CMOS-like silicidation module to define the ohmic contacts to the top poly-Si and underlying c-Si. Finally, W-based contacts were fabricated, followed by a Cu-based interconnect module.

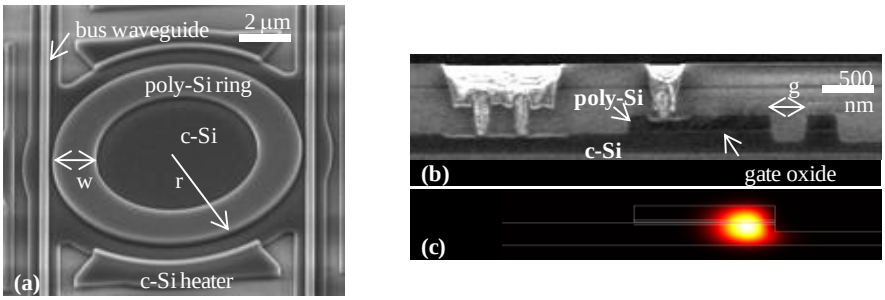

Fig. 1. (a) Tilted top-view SEM image of the ring modulator, (b) cross-sectional SEM image of the MOS structure, and (c) optical intensity of the fundamental whispering gallery mode (simulation)

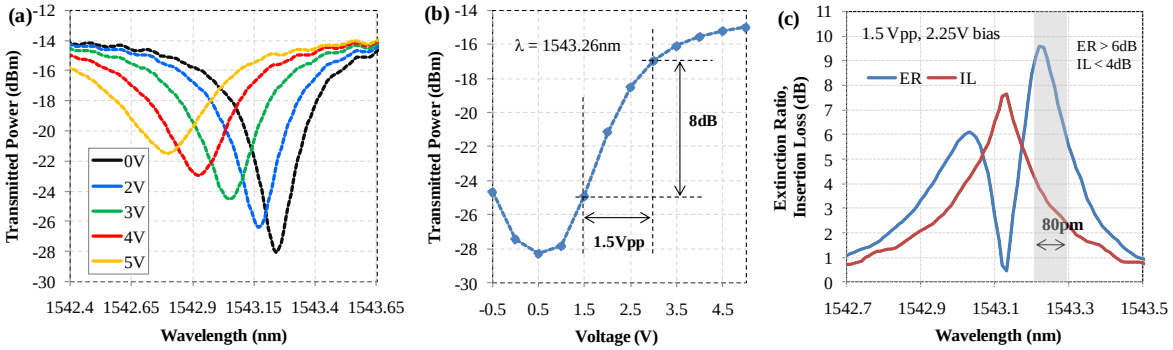

Fig. 2. (a) Through-port transmission spectra for various applied voltages, (b) transmission versus applied voltage at λ=1543.26nm, and (c) extinction ratio and insertion loss spectra for a 2.25-V applied bias and 1.5-V_{pp} voltage swing.

A tilted top-view SEM image of the modulator prior to the silicidation module is shown in Fig. 1a. The poly-Si ring has an outer radius of 5μm and an inner radius of 3.2μm. The resonator is implemented in a symmetric add-drop configuration with two 350-nm wide p-Si/c-Si bus waveguides, leaving a coupling gap of 200nm between the bus and the ring. The bus waveguides are connected to fully etched c-Si strip waveguides through low-loss taper structures. Shallowly etched gratings are implemented for coupling to fiber. Two n+-doped c-Si blocks at the outer edge of the ring can be used as resistive heating elements for thermal control of the modulator. A cross section of a fully fabricated (straight but representative) MOS structure can be found in Fig. 1b, showing the c-Si/poly-Si bus waveguide and ring with embedded 5-nm-thick gate oxide, as well as the silicide contacts and W/Cu metallization. The top contact to the poly-Si layer is implemented only near the inner edge of the ring, in order to avoid substantial metal-induced optical absorption losses of the fundamental whispering-gallery mode (WGM) of the resonator, which is confined near the outer edge of the ring as shown in Fig. 1c.

3. Electro-optic measurements

First, the static electro-optic response of the modulator is characterized by recording the through-port transmission spectra of the ring using a tunable laser, for various levels of applied electrical bias. The rings are operated in accumulation mode, with the p-type poly-Si biased at a higher voltage than the n-type c-Si layer. The resulting spectra are shown in Fig. 2a for applied biases of 0V through 5V. At 0V, the ring exhibits through-port extinction as high as 14dB, a Q of 3500, and a free-spectral range of 21nm. Applying a 2-V bias to the ring results in an 80pm blue shift of the resonance wavelength. For voltages above 2.5V, the resonant wavelength shifts at a rate of 130pm/V, for a total blue shift of 460pm at 5V. This is equivalent with a $V_\pi L_\pi$ efficiency of 0.24Vcm, which is close to the value reported in [5]. The maximum extinction of the through-port transmission drops with increasing bias, owing to the increased round-trip loss in the ring due to higher free-carrier absorption losses caused by the accumulated charge. For applied voltages below 5V, the leakage current flowing through the device is less than 1nA. As such, the DC power consumption of the device is negligible.

These static curves were subsequently used to identify the optimum bias conditions to achieve the highest ER and lowest IL at low V_{pp}. The transmission for λ=1543.26nm is plotted as a function of applied bias in Fig. 2b. An appropriate compromise can be found for a bias voltage of 2.25V and a voltage swing of 1.5V_{pp}, resulting in ER of 8dB and IL of 3dB. Furthermore, for this drive signal, ER>6dB and IL<4dB can be simultaneously obtained over an optical bandwidth as high as 80pm, as illustrated in Fig. 2c. Finally, the thermo-optic tuning efficiency of the doped Si heater was measured to be 270pm/mW.

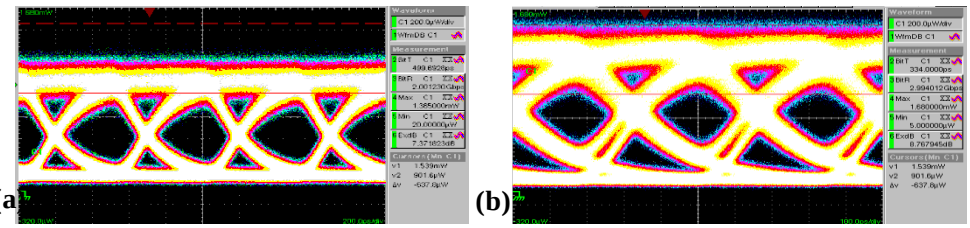

Fig. 3. (a) 2-Gb/s eye diagram recorded for 2.5V bias and 1.5V_{pp} swing, and (b) 3-Gb/s eye diagram recorded for 2.5V bias and 3V_{pp} swing

Subsequently, the high-speed performance of the MOS-based ring modulator was tested by applying an RF drive signal generated by a pattern generation to the chip using an unterminated RF probe, combined with a DC bias voltage using a bias tee. As the impedance of the ring MOS modulator is high, the effective voltage swing delivered to the device can be expected to be about twice as large as the one generated by the pattern generator due to the reflection of the RF wave. In the remainder of the paper, we will quote the estimated (doubled) effective voltage swing. Light from a tunable laser was coupled to the chip and the transmitted light signal was amplified by a C-band erbium-doped fiber amplifier, subsequently sent through a narrow-band optical filter and visualized on a high-speed sampling scope outfitted with a 20GHz optical module.

A typical eye diagram obtained by applying a 2.5V bias and a 2^7-1 PRBS 2-Gb/s data stream with 1.5V_{pp} effective voltage swing is shown in Fig. 3. A clear open eye is obtained, with an ER of 7.4dB. An open eye diagram can still be obtained at 3Gb/s as shown in Fig. 4, albeit after increasing the effective voltage swing to 3V_{pp}. Independent C-V measurements were performed at 100kHz on much larger MOS test capacitors, which yielded an accumulation capacitance of about 6.5±0.5fF/μm^2 for voltages above 2.5V, which is in good agreement with the theoretically predicted gate capacitance of 6.9fF/μm^2 for a 5-nm gate oxide. As such, the capacitance of the modulator is estimated to be around 320fF, and the power consumption at 1.5V_{pp} voltage swing can be estimated to be about 180fJ/bit. The frequency response is RC limited, with a 3-dB cut-off frequency off the electro-optic S_{21} parameter at about 1.7GHz, which can be explained by a device series resistance of 380Ω.

3. Discussion and conclusion

The modulation efficiency of 130pm/V obtained in the present MOS ring modulator is more than three times stronger than that of the highly optimized p-n depletion ring modulator described in [2]. In the current device with relatively low Q, this enables a high ER combined with low IL over an optical bandwidth as wide as 80pm, making the device tolerant to temperature fluctuations up to ±0.5K, which is a more than 3-fold improvement over the highly optimized depletion-based ring modulator. Alternatively, by lowering the optical coupling to the drop and bus waveguide to increase the quality factor, part of this thermal robustness could be traded for a further reduction of the required voltage drive swing, allowing the modulator to be driven with ultra-low voltage CMOS drive circuits with swing well below 1V_{pp}. Obviously, the operation speed of the MOS ring modulator will need to be improved to 10Gb/s and above for application in future high-bandwidth systems. Strong potential exists to reduce the device capacitance without affecting the modulation efficiency, as the WGM occupies only 25% of the gate area in the present device. In addition, the device series resistance can be lowered by optimizing the implant conditions. A combination of both design improvements is expected to yield an up to tenfold speed improvement, enabling 20Gb/s modulation.

In conclusion, a compact MOS-based ring modulator was demonstrated with more than three times stronger electro-optic modulation efficiency as compared to highly optimized depletion-based ring modulators. MOS-based ring structures offer a compelling platform for realizing robust, ultra-low voltage silicon modulators, likely surpassing the performance trade-offs that can be obtained with depletion-based ring modulators, owing to the high modulation efficiency of the embedded MOS-based phase shifter.

4. References

[1] X. Zheng, et al., "Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver," Opt. Express 19, 5172-5186 (2011)
[2] Po Dong, et al., "High-speed and compact silicon modulator based on a racetrack resonator with a 1 V drive voltage," Opt. Lett. 35, 3246-3248 (2010)
[3] J. Rosenberg, W. M. Green, A. Rylyakov, C. Schow, S. Assefa, B. G. Lee, C. Jahnes, and Y. Vlasov, "Ultra-low-voltage Micro-ring Modulator Integrated with a CMOS Feed-forward Equalization Driver," in OFC, OSA, OWQ4 (2011)
[4] A. Liu, et al, "A high-speed silicon optical modulator based on a metal–oxide–semiconductor capacitor," Nature 427, 615-618 (2004)
[5] http://www.ofcnfoec.org/osa.ofc/media/Default/PDF/2009/09-Dandrea.pdf
[6] D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible Silicon-On-Insulator platform," Opt. Express 18, 18278-18283 (2010)