Doping Geometries for 40G Carrier-Depletion-Based Silicon Optical Modulators

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Abstract: A comparison is preformed between carrier-depletion modulators with different doping patterns to reach low $V_\pi L_\pi$ = 0.62 V·cm at DC with interdigitated and lateral PN junctions respectively, but also show modulation at 35 Gbit/s (errorfree).
OCIS codes: (130.0250) Optoelectronics; (060.4080) Modulation

1. Introduction

As a key component in optical interconnect systems, integrated silicon modulators have experienced rapid progress during the last years [1]. Due to the weakness of intrinsic electro-optical effect, most silicon modulators rely on either the plasma dispersion effect or an electro-optic cladding material [2] to change the refractive index. In case of the plasma effect the free carrier density inside an optical waveguide is manipulated by an electrical signal. This can be implemented by carrier depletion, injection, or accumulation. Among these three mechanisms carrier-depletion modulator has advantages of both high operation speed and fabrication simplicity. However, it suffers from low modulation efficiency. To overcome this drawback, different doping patterns are chosen to improve the overlap between the optical mode and the carrier depletion region [3, 4]. Since reported devices have different waveguide dimensions, implantation doses and driving schemes, there is no comprehensive comparison between different doping patterns so far. In this paper, we make a systematic comparison between the two prevalent doping patterns: the interdigitated PN junction and the lateral PN junction (see Fig. 1). Modulators with these two doping patterns are fabricated (front end-processing in CMOS line of imec) and characterized in the same platform, then compared in terms of the loss, modulation efficiency and operation speed.

2. Device design and fabrication

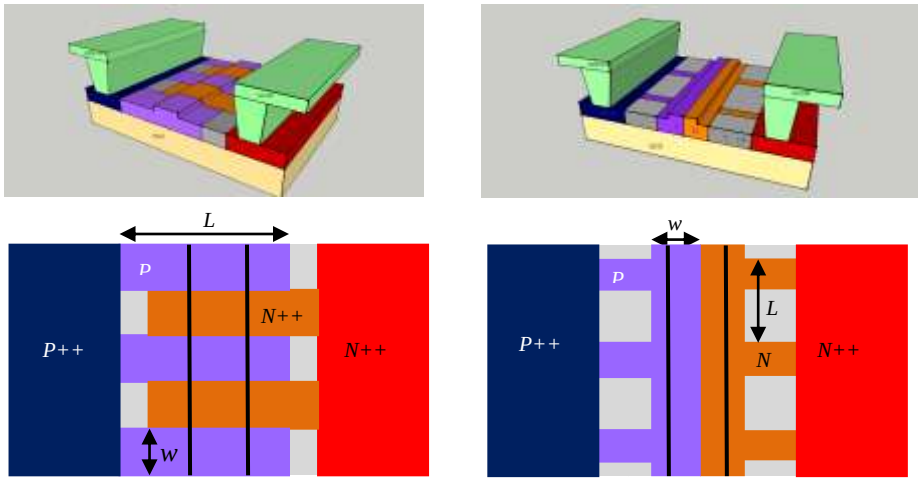


Fig. 1. 3D schematic figures and top views of phase shifters with two different doping patterns

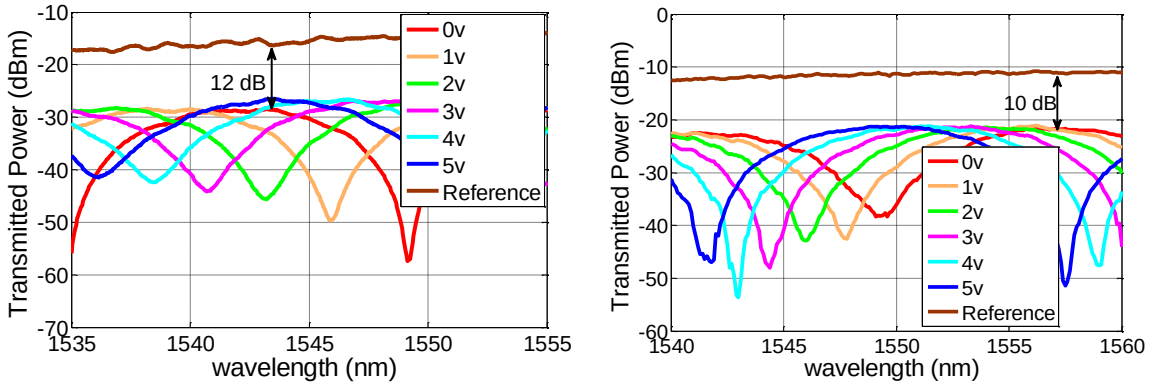
The basic device is an asymmetrical Mach-Zehnder interferometer which incorporates PN junctions in both arms so as to form two phase shifters. Schematic 3D views together with top views of phase shifters are displayed in Fig. 1 for two different doping patterns. The width and height of the shallow-etched waveguide are 500 nm and 220 nm respectively. The etching depth is 70 nm in order to be compatible with standard fiber grating couplers in the same

platform. For the phase shifter with interdigitated PN junctions, left side of Fig. 1, the overlap between the carrier depletion region and the optical mode is determined by the length *L* and the width *w* of the interdigitated arms. We sweep the two parameters so as to find the optimal values. The measurement result shows a periodic unit with *w*=250 nm and *L*= 2 μm exhibits the highest modulation efficiency. For the normal PN junction on the right side of Fig. 1, the carrier depletion region in the center of the waveguide and the highly doped contacting areas which reside 1 μm away from the waveguide sidewalls are connected by doped arms so as to reduce the unnecessary optical loss. The width *w* of the two doped strips which form the PN junction is 300nm. This is limited by the resolution of 248 nm lithography. The width of doping arms and their pitch are 400 nm and 1000 nm respectively. The filling factor of 40% here is based on a trade-off between the optical loss and the RC constant. Fiber-grating couplers are used to couple the light in and out.

The optical modulator was fabricated on a 200 mm SOI wafer with a 2 μm-thick buried oxide (BOX) layer and a 220 nm-thick crystalline silicon film. 193 nm optical lithography and silicon dry etching were used to define the optical waveguide. Then a layer of resist was spin-coated for the implantation mask. The implantation window was opened by 248 nm lithography. Subsequently ion implantation was carried out with a sweep of different doses, energies and tilt angles in the wafer matrix. Silicidation was followed by wafer dicing. The diced sample was spin coated with a BCB layer. After via etching through the BCB, a Pt/Au electrode was patterned by lift-off technology and annealed.

3. Characterization and performance comparison

The transmission spectra of asymmetrical MZ modulators at different reverse bias points are presented in Fig. 2 for the two doping patterns. Spectrums of the straight waveguides are displayed together as a reference. Phase shifters for both modulators are 3 mm. Coplanar waveguide electrodes (CPW) are placed to drive the modulator. The width of the signal metal is 6 μm, while the gap between the signal and the ground is 3.5 μm. The nominal doping concentration is 2e18/cm^3 for both P and N type silicon. We deduce the figure of merit $V_\pi L_\pi$ from the peak shift and the free spectral range (FSR) in Fig. 2. The modulation efficiency corresponding to a reverse bias from 0V to 1V is 1.4 V·cm for the lateral PN junction, while that for the interdigitated PN junction is 0.62 V·cm.



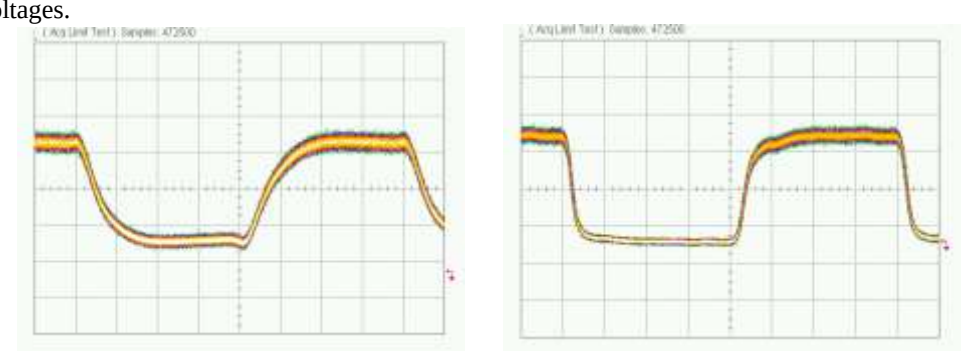
(a) (b)

Fig. 2. Transmission spectrums at different bias voltages of two different doping patterns: (a) interdigitated PN junction (b) lateral PN junction

The first adverse effect of enhancing the modulation efficiency with the interdigitated PN junction is an insertion loss increment of 2 dB. One more serious penalty is a slowdown of the response speed. This point is shown in Fig. 3 which displays the responses of modulators to a square wave signal with a peak to peak voltage 8 V and period of 0.64 ns. The DC reverse bias voltages are 6.0 V for the interdigitated PN junction and 5.7 V for the lateral PN junction which make sure that devices are always reverse biased. The 90% to 10% fall time and the 10% to 90% rise time of the response are used to characterize the modulation speed. In Fig. 3 the fall and rise times are equal for each doping pattern due to educated balancing between the bias point of the MZM and the changing capacity of the depletion region during modulation. The response time of the interdigitated PN junction is at least two times longer than that of the lateral PN junction. This value coincides with their modulation efficiencies. The modulation efficiency of interdigitated PN junction is 2.25 times the efficiency of lateral PN junction. This implies approximately the same ratios between their capacitances and between response times.

Figure 4 presents an eye diagram of the lateral PN junction based modulator by driving it with a 25 to 40.5 Gbit/s pseudorandom bit sequence (PRBS) with a 2^7-1 pattern length. The PRBS signal is boosted to a peak-to-peak voltage of 8 V by an electrical amplifier before it is sent to the modulator. The operation wavelength 1555 nm was

fixed and hence bias voltages are tuned for the optimal operation point. Clear eye opening is achieved with an extinction ratio of 11.7 dB at 25 Gbit/s and error free operation (BER smaller than 2e-10) is possible up to 35 Gbit/s. At 40.4 Gbit/s the BER is 2e-3 and just below the current Forward Error Correction (FEC) limit. In contrast, the interdigitated PN junction based modulator does not work at 25 Gbit/s but might be suitable for application relying on low driving voltages.



(a) (b)

Fig. 3. Time responses to a square signal of two different doping patterns: (a) interdigitated PN junction (b) lateral PN junction

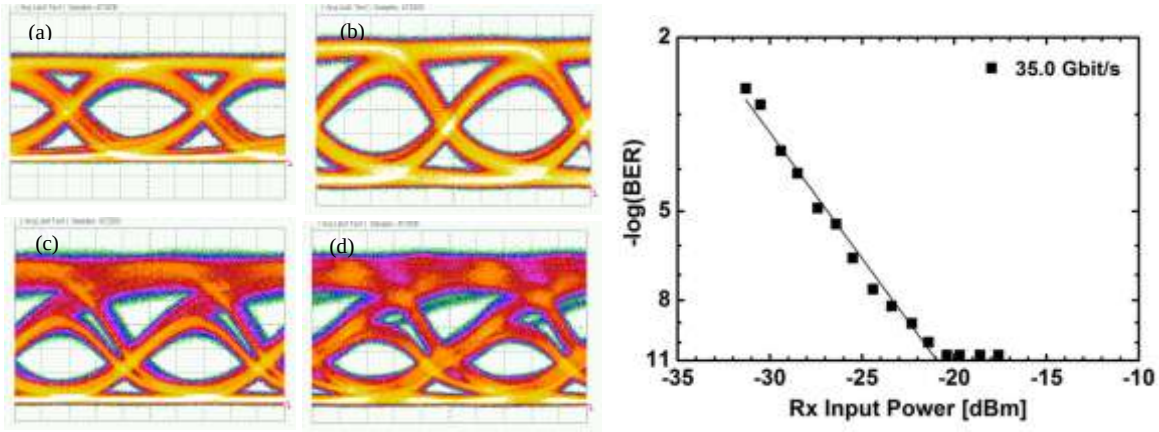


Fig. 4 Eye diagrams (a) 25 Gbit/s, (b) 28 Gbit/s, (c) 35 Gbit/s, (d) 40 Gbit/s and BER of the lateral PN junction based modulator at a bit rate of 35 Gbit/s

4. Conclusion

We compare the performance of carrier-depletion-based modulators with different doping patterns. The results illustrate the conflict between the operation speed and modulation efficiency and give design indications. Compared with the lateral PN junction, the interdigitated PN junction increases both the modulation efficiency and the response time. According to the intended application the proper doping pattern can give 40 Gbit/s data transmission.

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