INVITED PAPER

An optically pumped nanophotonic InP/InGaAlAs optical amplifier integrated on a SOI waveguide circuit

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Abstract   A small footprint integrated optical amplifier on Silicon-on-insulator is proposed in this article. By choosing to use optical pumping to drive the device, electrical contacting is avoided and the active waveguide can be made as thin as 100 nm, maximizing the optical confinement in the quantum well layers. Furthermore, the optical pumping is done through the silicon waveguide layer to optimally use the pump light. This leads to a compact device with high gain. We show 8 dB gain in pulsed regime in a 100 μm long device using a peak pump power of only 4.5 mW, while a comparable gain using an electrically pumped device would require an order of magnitude higher power consumption. This is an important step towards a CMOS-compatible optical amplifier for intra-chip optical interconnects.

1 Introduction

The current tendency in high performance computing is directed towards parallelism on all levels. As the number of processor cores, executional units and transistors increases, the amount of data that needs to be sent across a chip increases as well. Electronics are reaching their data transfer limits however, so an alternative solution needs to be found. An integrated optical solution could provide for the necessary bandwidth for next-generation computing (Miller 2000). However, to make an optical solution viable, its fabrication needs to be CMOS compatible to ensure inexpensive integration with the electronics circuits. The Silicon-on-insulator (SOI) waveguide system would therefore be an excellent candidate. Furthermore,

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the high index contrast waveguides that can be achieved, show low loss and allow very tight bends, reducing the footprint of the photonic circuit (Bogaerts et al. 2008). However, to allow the realization of an integrated optical transmission system, also active components are required. Due to silicon's indirect band gap, creating these components remains a challenge on SOI. Several approaches exist to address this (Jalali and Fathpour 2006), however currently the most successful demonstrations are based on heterogeneous integration of an active III–V layer stack on top of the SOI waveguide circuit (Jain et al. 2011; Roelkens et al. 2010; Park et al. 2007). This can be achieved either by direct die-to-wafer bonding (Augendre et al. 2010) or adhesive die-to-wafer bonding, using DVS-BCB as an intermediate adhesive between the SOI circuit and III–V layers (Roelkens et al. 2006). However, in these devices the active III–V waveguide is at least 500 nm thick, to ensure efficient current injection in the device. This limits the maximal confinement of light one can achieve in the active layers, reducing the maximal gain and increasing the necessary device length, thereby increasing the power consumption. However, if optical excitation of the semiconductor gain medium were used instead of electrical pumping, it would be possible to dramatically reduce the thickness of the active III–V waveguide, as current injection and ohmic contact layers would no longer be required. As a result, one can leverage the high index contrast between the III–V and the surrounding air and DVS-BCB cladding to create III–V membrane waveguides with a much higher confinement in the active layers. This stronger confinement can bring the design advantage of higher optical gain with lower total power consumption, a very relevant consideration for advanced on-chip optical interconnects. In this approach, a chip architecture is supposed in which an external pump is coupled to the chip as an external optical power supply. Due to recent advances in fiber-to-chip coupling, a coupling loss of less than 1 dB can be achieved (Shoji et al. 2002) and using a commercially available pump laser, a wall-plug efficiency of 16 % can be expected (Kimura et al. 2000), making this a viable approach. In this article we propose and demonstrate a 100 nm thick membrane waveguide which is optically pumped through the underlying silicon waveguide layer.

2 Device layout

The device structure is schematically shown in Fig. 1a. It consists of two silicon access waveguides which are coupled to a III–V membrane waveguide by two inverted taper couplers. These couplers are designed to support an adiabatic transition of the fundamental TE mode in the silicon waveguide to the fundamental TE mode in the III–V membrane waveguide, for DVS-BCB layer thicknesses below 150 nm. The couplers consist of a linearly tapered 220 nm thick silicon wire of 12 µm long below the III–V waveguide, starting from a width of 700 nm and tapering down to a width of 100 nm. The III–V waveguide is a strip waveguide with a width of 2 µm and a thickness of 100 nm, which was found to be the optimal thickness to reach maximal confinement in the active region, independent of the number of quantum wells the region consists of. To maximize the possible gain, the active region consists of four compressively strained (0.85 %) AlGaInAs quantum wells of 7 nm thick with five tensile strained AlGaInAs (0.55 %, Q1.3) barriers of 10 nm, which is the highest number of quantum wells possible in a 100 nm thick wire. This quantum well stack is sandwiched between two 10 nm InP cladding layers and has a bandgap wavelength of 1.6 µm. In Fig. 1b, the mode profile in the membrane waveguide is shown for a wavelength of 1,550 nm, clearly displaying the high light intensity in the active layers. In this structure, a confinement of 0.22 can be achieved in the quantum wells, while in a previously demonstrated integrated electrically pumped amplifier the confinement is only 0.03, where consequently a device
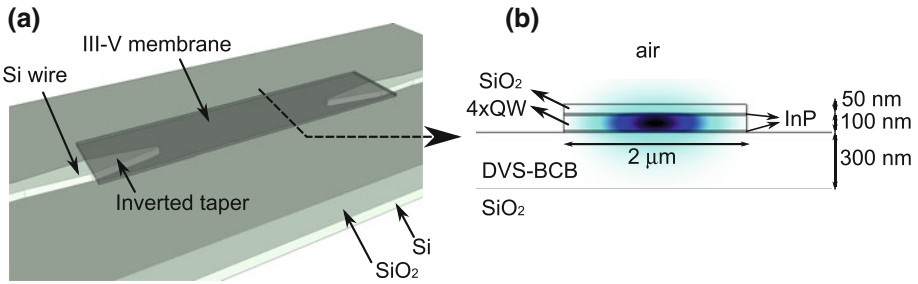
Fig. 1 a Schematic view of the device. It consists of two silicon access waveguides, a membrane III–V waveguide and two intermediate tapering sections. **b** The mode profile in the III–V membrane waveguide

length of 1.3 mm is necessary to reach 13 dB of gain (Park et al. 2007). Thanks to the very high confinement in the membrane waveguide this device length could be reduced by a factor of 7, leading to a significant power reduction. This also has a drawback however: the output power will saturate faster than in a design with low confinement. The device is coupled to optical input/output fibers through two grating couplers, which have a coupling loss of 5 dB per coupler and a bandwidth of 70 nm (Taillaert et al. 2006).

3 Fabrication

Fabrication of the SOI waveguide circuit was done using 193 nm deep UV lithography and dry etching on a 8 inch SOI wafer in a CMOS pilot-line (Epixfab 2004). After dicing of the wafer, the seperate dies are cleaned for 15 minutes in a Standard-Clean-1 solution at 75C. In the mean time, the III–V dies are prepared for bonding by removal of the InP/InGaAs sacrificial layer pair, using a $3HCl:H_2O$ solution and $1H_2SO_4:1H_2O_2:18H_2O$ solution respectively. After this, a diluted DVS-BCB solution (1BCB:5Mes) is spincoated on the SOI die at 5,000 rpm. After the evaporation of the mesitylene, the dies are brought into close contact and cured at 250°C for 1 h. Then, the InP substrate is removed using a combination of mechanical grinding and wet etching using a $3HCl:H_2O$ solution until the InGaAs etch stop layer is reached. After removal of the etch stop layer using a $1H_2SO_4:1H_2O_2:18H_2O$ solution, a 50 nm thick SiO_2 hard mask is deposited. This hard mask is patterned using contact lithography. Dry etching the hard mask and the III–V stack leaves the III–V membrane waveguides. Figure 2a shows a top down microscope image of the fabricated device. Figure 2b shows a transmission electron microscopy image of the quantum well layer stack bonded to the SOI waveguide circuit. From this figure, it can also be seen that the DVS-BCB bonding layer has a thickness of only 260 nm in the etched parts of the 220 nm thick silicon layer, which means that the bonding layer thickness is only 40 nm at this location. Typically the thickness stays within a range of 50 nm using a thin bonding layer recipe, and therefore the DVS-BCB thickness is within the margin to have good coupling in the inverted taper couplers.

4 Characterization

4.1 Continuous wave experiment

To measure continuous wave (CW) gain, a pump-probe experiment was performed. A pump beam at a wavelength of 1,545 nm was combined with a probe beam using a 99/1 combiner and sent through the device. By comparing the probe transmission through the device with
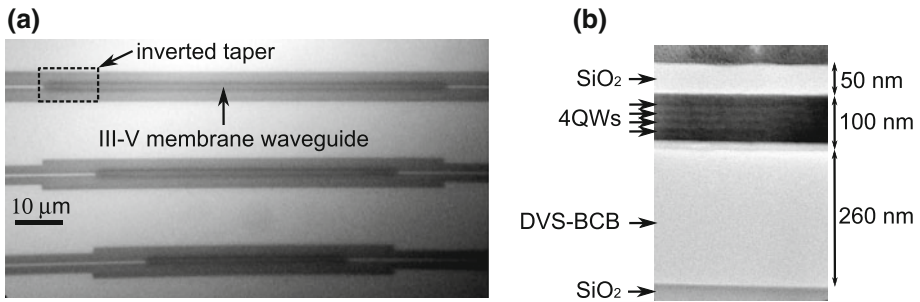
(a)

inverted taper

III-V membrane waveguide

10 μm

(b)

SiO₂ → 50 nm

4QWs → 100 nm

DVS-BCB → 260 nm

SiO₂ →

Fig. 2 **a** Optical microscopy image of the fabricated devices. **b** Transmission electron microscopy image of the III–V waveguide in the fabricated device
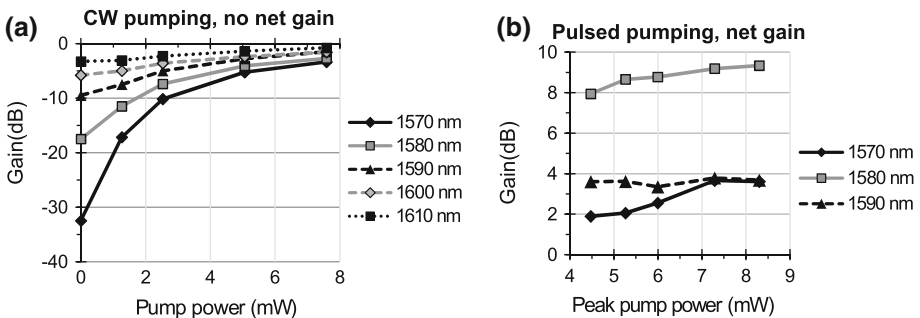

(a) CW pumping, no net gain

Gain(dB)

- 1570 nm
- 1580 nm
- 1590 nm
- 1600 nm
- 1610 nm

Pump power (mW)

(b) Pulsed pumping, net gain

Gain(dB)

- 1570 nm
- 1580 nm
- 1590 nm

Peak pump power (mW)

Fig. 3 **a** Measured CW gain in a 100 μm long device. **b** Net gain achieved a 100 μm long device for a pulsed pump. In both experiments the pump was at 1,545 nm and the pump power shown in the *graph* is the on-chip power, calculated by subtracting the 5 dB grating coupler loss from the measured pump power before the chip. The different curves correspond to different probe wavelengths

the transmission through a reference silicon waveguide, the net gain in the III–V membrane waveguide can be extracted. In the experiment, both the pump power and the probe wavelength are varied. The results for a 100 μm long device are shown in Fig. 3a. When the pump power is increased, the absorption of the probe decreases as expected and eventually starts saturating. However, the point where we have net gain is not reached. This lack of net gain can be attributed to thermal effects, degrading the device performance primarily caused by a smoothing of the Fermi-Dirac distribution of holes and electrons (Van Campenhout 2007). This has two effects: next to a direct reduction of the gain peak, it also reduces the absorption of the pump beam, leading to a lower amount of generated carriers for a certain pump power. This effect can be seen in Fig. 3a by extrapolating the absorption at 1,545 nm at high pump powers. Both non-radiative recombination of the generated carriers (predominantly surface recombination) and free carrier absorption of the probe and pump beams are a cause for the heating of the device.

4.2 Pulsed experiment

To test our hypothesis that thermal effects cause the lack of gain, we have also performed a pulsed experiment. In this experiment, the CW pump laser is replaced by a directly modulated distributed feedback laser which also operates at 1,545 nm and produces pump pulses of 0.3 μs long with a period of 10 μs. This low-duty cycle pump signal avoids thermal effects, as the device's thermal time constant was determined to be 3.7 μs. To boost the pump power,
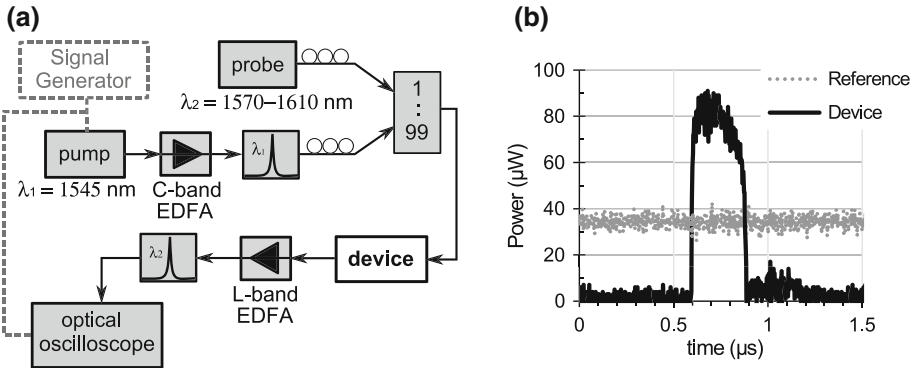
(a)

(b)

Fig. 4 **a** Measurement setup for the pulsed experiment. **b** Trace of the resulting pulse profile (*black*) and the trace of the transmission through the reference waveguide. This measurement is for a 1,570 nm probe beam and a peak pump power of 7.29 mW which yields a net gain of 3.7 dB. The *dashed line* shows the transmitted power through the reference waveguide

the pulses are sent in a C-band erbium doped fiber amplifier (EDFA) and afterwards filtered by a band pass filter to avoid that the amplified stimulated emission (ASE) of the EDFA would pump the device. The pump is sent together with a CW probe beam in the device. Because of the pulsed character of the pump signal, the CW probe signal is amplified only during the duration of the pump pulse. After transmission through the device, the probe is amplified using a L-band EDFA and filtered in a band pass filter, which also removes the remaining pump. The resulting signal is then measured using an optical oscilloscope, which was referenced to the zero level before measurement. The setup is shown in Fig. 4a and one of the measured probe traces is shown in Fig. 4b. The variation on the trace during the pump pulse is caused by an imperfect pump pulse shape and therefore the net gain is extracted by averaging the measured power over the peak $0.1\,\mu s$ of the pulses and subtracting the average of the trace measured through the reference waveguide. The achieved net gain is plotted in Fig. 3. From these results, it is clear that thermal effects must be the cause for the lack of gain in CW regime. A gain of 8 dB is achieved in pulsed regime for a peak pump power of only 4.5 mW, while in CW regime the device doesn't reach transparency for a comparable power. Taking into account a wall-plug efficiency of the pump laser of 16 % and a coupling loss of 1 dB, the total power required to drive the III–V membrane waveguide is found to be 35 mW, considerably lower than the required power in the electrically pumped amplifier integrated on SOI reported in (Park et al. 2007), which is estimated to be more than 150 mW. Furthermore, it seems that the gain is already saturated for the lowest used pump power at 1,590 nm, while it is still increasing a little for the shorter wavelengths. This increase is quite small however, because of absorption saturation of the pump beam. To increase the gain even more, one should move to a shorter pump wavelength, but in the current setup the limited bandwidth of the grating couplers limits the separation between pump and probe wavelength.

4.3 Thermal analysis

To achieve CW gain, the thermal performance of the device needs to be improved. To evaluate the current design, the thermal resistance of the device was simulated using COMSOL (Fig. 5a). It seems that the device has a thermal resistance of 9 K/mW. This high value can be attributed to both the low thermal conductivity of the 260 nm thick DVS-BCB bonding layer (0.3 W/(m K)) and the $2\,\mu m$ thick buried oxide layer (1.27 W/(m K)) which forms the
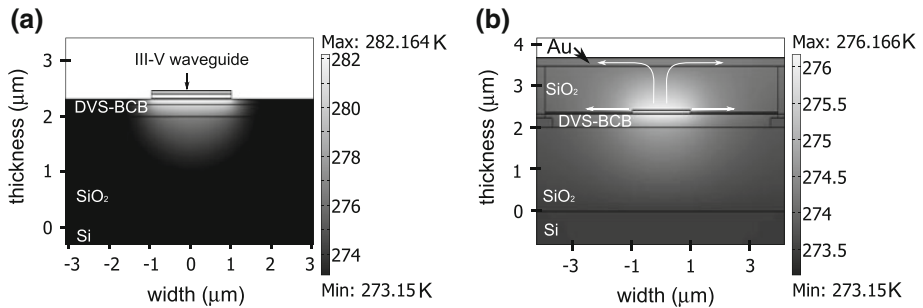
Fig. 5 **a** Thermal simulation in COMSOL of the fabricated device for a heat dissipation of 1 mW. **b** Thermal simulation in COMSOL of an improved design with shallow etch and heat spreader for a heat dissipation of 1 mW

cladding for the silicon waveguides (Van Campenhout 2007). Furthermore, the heat is dissipated in a small volume, which has a small contact area with the SOI die. As we cannot change the bonding material and buried oxide thickness easily, we can only improve the thermal behaviour by increasing this contact area. There are two strategies to do this: first of all, the III–V membrane waveguide could be shallow etched instead of completely etched. This allows for a heat flow towards the shallow etched parts of the III–V waveguide. At the same time, this also decreases the scattering loss in the waveguide and the amount of non-radiative recombination due to a reduction of surface recombination. If the shallow etch is deeper than 40 nm, the reduction in confinement in the active region is furthermore limited to 0.01. A second strategy is the use of a thick SiO_2 overcladding with a highly conducting metal layer on top, which acts as a heat spreader. The simulation shows that the combination of these strategies, using gold as a heat spreader, reduces the thermal resistance of the structure by a factor of three to 3 K/mW (see Fig. 5b).

4.4 Conclusion

In summary, we have proposed to use thin III–V membranes to create an efficient integrated optical amplifier on SOI. The first fabricated devices show no CW gain however, which seems to be caused by thermal effects. The measured net gain of 8 dB in pulsed mode at a peak pump power of only 4.5 mW shows the potential of this device. To address the thermal quenching of the gain, we have proposed to use a shallow etched waveguide instead and to add a heat spreader on top. In future work, we will implement these solutions and use horizontal couplers instead of grating couplers to be able to pump the devices at shorter wavelengths as well.

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