Ultra-high Speed, All-optical Wavelength Converters Using Single SOA and SOI Photonic Integrated Circuits

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Abstract
We report a new family of ultra-fast all-optical wavelength converters. The device architecture employs a single SOA and filtering elements integrated in silicon-on-insulator substrates. These schemes enable high-integration density and low power consumption.

Introduction

Recently monolithic integration of all-optical wavelength converters (AOWC) in InP has been pushed to the edge with the fabrication of dense AOWC arrays [1]. These components prove the feasibility of practical, chip-level photonic routing systems and integration efforts are focused on addressing key issues like yield, volume and cost. Hybrid integration is one way to address these issues due to the use of low cost substrates and the optimum utilization of the available 2" InP wafers. In this context, the first hybrid integrated arrays of AOWCs have been reported in the European project MUFINS [2]. The devices are fabricated in a 3-step process by mounting prefabricated SOA chips on silicon submounts and eventually on silica-on-silicon substrates. Using this technique a quad array SOA-MZI AOWC was fabricated employing 8 active elements on-chip and consuming 12 W of electrical power. However, the low index contrast waveguides have a great impact on the chip size, whereas the scaling of the SOA-MZI structures is limited by overall power consumption and thermal management requirements.

The advent of silicon as a flexible integration platform is now providing a promising alternative. The low-cost and large size silicon wafers combined with the high index contrast of silicon-on-insulator (SOI) material could lead to a new generation of scalable and ultra-compact integrated AOWCs. In this rationale, the purpose of this paper is to introduce two new schemes capable of WDM-enabled AOWC that make use of a single semiconductor optical amplifier (SOA) followed by optical filters with comb-like spectral response integrated on SOI substrates. Firstly, we demonstrate experimentally 160 Gb/s AOWC employing a cascaded delayed interferometer (DI) structure implemented using SOI 4μm rib waveguide technology. Secondly, we present the design of 160 Gb/s AOWC employing 3rd order micro-ring resonators (MRRs), as well as the fabrication of the MRRs in 220nm SOI nanowire technology. Both schemes are promising candidates for fully integrated AOWCs operating at bit rates above 100Gb/s and consuming less than 1 W of electrical power.

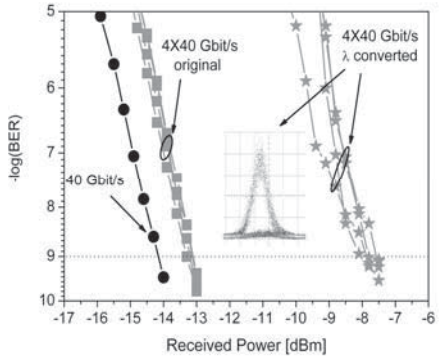

Figure 2. SOI-DI AOWC concept: a)-c) eye diagrams at SOA output, SOI chip output and 40 Gb/s demultiplexed channel.

SOI-DI AOWC

Figure 1 shows the SOI-DI AOWC concept and the experimental results. A data stream of 160 Gb/s RZ data at

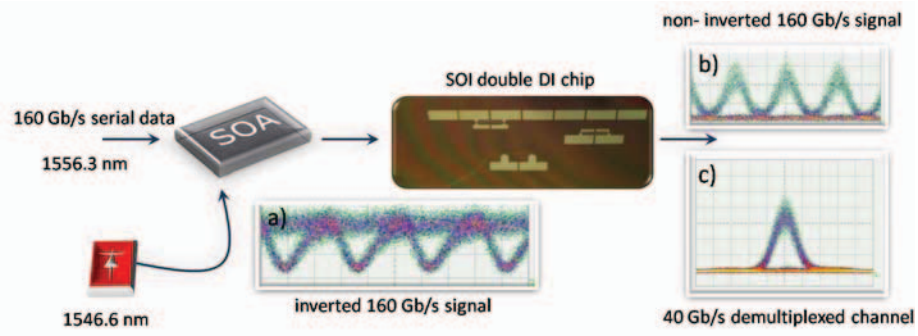

Figure 1. SOI-DI AOWC concept: a)-c) eye diagrams at SOA output, SOI chip output and 40 Gb/s demultiplexed channel.

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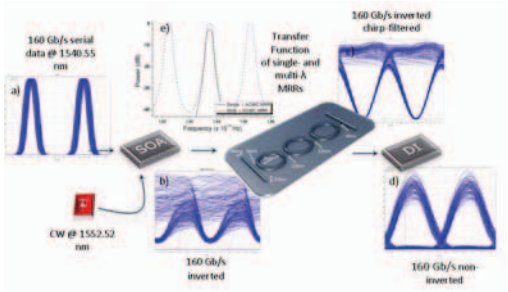

Figure 3. MRR-assisted AOWC concept: a)-d) eye diagrams at input, SOA output, MRR output and DI output, (e) Transfer functions of designed MRRs

1556.3 nm is injected into a single SOA together with a CW light at 1546.6 nm. The XPM effect results to a wavelength converted inverted signal at the output of the SOA (fig. 1a). This signal passes then through the SOI chip. This consists of two cascaded DIs implemented on a 4 um SOI substrate with differential delays of 1 and 2 ps, yielding a free spectral range (FSR) of 8 and 4 nm respectively. The response of the first SOI-DI is detuned with respect to the CW wavelength so that blue-chirp filtering takes place. The second DI is used to invert the polarity of the RZ pulses and finally an inverted wavelength converted signal is obtained at the output (figure 1b and 1c). Bit error rate curves are depicted in figure 2. All the channels achieved error-free operation with an average optical receiver power of -7.5 dBm associated to an average power penalty of 5.5 dB. This penalty is due to a reduction of the signal-to-noise ratio introduced by the light coupling in the unpackaged SOI chip. Signal-to-noise ratio can be improved by using a pigtailed device, leading to reduced penalties.

MRR-assisted AOWC

Figure 3 shows the MRR-assisted AOWC concept and the modeling results. A 160 Gb/s data stream enters the SOA and due to the slow recovery time of the amplifier, a closed eye diagram is obtained (figure 3b). 3rd order MRRs designed for optimum chirp filtering and enabling single- or WDM-enabled AOWC, are cascaded to accelerate the effective recovery of the system. Hence the wide eye openning of figure 3c) is obtained. With a 2ps DI following the MRR, a non-inverted 160Gb/s AOWC signal is observed (Figure 3(d)). The transfer function of both designed MRRs is depicted in figure 3(e) and both have resonance peaks with 180GHz 3dB bandwidth, at least 40dB extinction ration and Free Spectral Range of 3.397THz and 1.5THz for single and WDM-enabled AOWC, respectively. The values of the single-λ MRR correspond to commercially available bandpass filters used in previous 160 Gb/s AOWC experiments [3]. Table 1 summarizes the parameters of the designed MRRs.

Table 1: Parameters of designed MRRs for 160Gbps AOWC

Parameter	Single Lambda WC	Multi Lambda WC
Type of resonator	Ring	Racetrack
Free Spectral Range	3.397THz	1.5THz
Ring Radius	3 μm	-
Radius of the bending section of the racetrack	-	5μm
Length of the straight section of the racetrack	-	8.5 μm
Power Coupling coefficient Bus-Ring	0.2	0.5
Power Coupling coefficient Ring-Ring	0.0125	0.05
Gap Bus-Ring	90nm	160nm
Gap Ring-RIng	220nm	280nm
Bus Waveguide Width	300nm	450nm
Ring waveguide widht	500nm	450nm
Waveguide height	220nm	220nm

Figure 4 shows the SEM images of the fabricated MRRs realized on SOI substrates using electron beam lithography for patterning. Fabrication started with SOI substrates with a 220nm top silicon layer sitting on a 2 μm thick buried oxide. Hydrogen silsesquioxane (HSQ) has been used as negative tone resist defining waveguides, ring resonators, racetracks and other parts of the device as well as supporting structures such as markers for the alignment of further exposures. The fabrication errors for the gaps of waveguide-ring and ring-ring have been measured less than 2.5% for the racetrack resonator and 9% (82nm instead of 90nm) for the ring resonators. No degradation is expected to the performance of the MRR-assisted AOWC from these variations.

Conclusion

We presented two new AOWC schemes based on single SOA and SOI integrated photonic chips. Simulations and experiments prove the feasibility of >100Gb/s all-optical wavelength converters with low power consumption and chip real-estate efficiency.

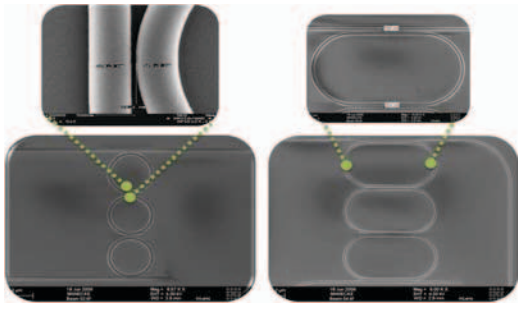

Figure 4. SEM images of 3rd order MRR and race-track resonators for single- and multi- λ AOWC

Acknowledgement

This work was supported by the European Commission through ICT-BOOM project under the 7th Framework Programme. PhoeniX BV is gratefully acknowledged for providing the ASPIC design tool

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