# The European BOOM Project: Silicon Photonics for High-Capacity Optical Packet Routers

Leontios Stampoulidis, *Member, IEEE*, Konstantinos Vyrsokinos, Karsten Voigt, Lars Zimmermann, Fausto Gomez-Agis, Harm J. S. Dorren, Zhen Sheng, *Student Member, IEEE*, Dries Van Thourhout, Ludwig Moerl, Jochen Kreissl, Behnam Sedighi, Johann-Christoph Scheytt, *Member, IEEE*, Annachiara Pagano, and Emilio Riccardi

***Abstract*—During the past years, monolithic integration in InP has been the driving force for the realization of integrated photonic routing systems. The advent of silicon as a basis for cost-effective integration and its potential blend with III–V material is now opening exciting opportunities for the development of new, high-performance switching and routing equipment. Following this rationale, BOOM—as a European research initiative—aims to develop compact, cost-effective, and power-efficient silicon photonic components to enable optical Tb/s routers for current and new generation broadband core networks. This "siliconization" of photonic routers is expected to enable ultrahigh bit rates as well as higher levels of integration and power efficiency. The BOOM "device portfolio" includes all-optical wavelength converters, ultradense wavelength-division multiplexing (UDWDM) photodetectors, and high-speed transmitters; all based on silicon waveguide substrates. Here, we present the device concepts, the fabrication of photonic building blocks and the experiments carried out as the initial steps toward the realization of the first high-capacity silicon photonic router.**

***Index Terms*—Hybrid integration, microring resonators (MRRs), optical fiber communication, optical packet switching, optical signal processing, photonic integration, semiconductor optical amplifiers, silicon-on-insulator (SOI), terabit photonic router.**

Manuscript received September 1, 2009; revised November 9, 2009; accepted November 29, 2009. Date of publication January 26, 2010; date of current version October 6, 2010. This work was supported by the European Commission through project ICT-BOOM (www.ict-boom.eu) under the 7th Framework Program (FP7), Information and Communications Technologies (ICT).

L. Stampoulidis was with the Photonics Communications Research Laboratory, National Technical University of Athens, Athens 15773, Greece. He is now with Constelex Technology Enablers, Acharnai, Athens 13671, Greece (e-mail: ls@constelex.eu).

K. Vyrsokinos is with the Photonics Communications Research Laboratory, National Technical University of Athens, Athens 15773, Greece.

K. Voigt is with the Joint Laboratory of Silicon Photonics, Technical University of Berlin, Berlin D-10587, Germany.

L. Zimmermann is with the Joint Laboratory of Silicon Photonics, Technical University of Berlin, Berlin D-10587, Germany, and also with the Joint Laboratory of Silicon Photonics, IHP Microelectronics Technology, Frankfurt (Oder) 15236, Germany.

F. Gomez-Agis and H. Dorren are with the COBRA Research Institute, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands.

Z. Sheng was with the Photonics Research Group, INTEC Department, Ghent University-IMEC, Ghent 9000, Belgium. He is now with Zhejiang University, 310058 Hangzhou, China.

D. V. Thourhout is with the Photonics Research Group, INTEC Department, Ghent University-IMEC, Ghent 9000, Belgium.

J. Kreissl and L. Moerl are with the Fraunhofer-Institut für Nachrichtentechnik, Heinrich-Hertz-Institut, Berlin 10587, Germany.

B. Sedighi and J.-C. Scheytt are with the Joint Laboratory of Silicon Photonics, IHP Microelectronics Technology, Frankfurt (Oder) 15236, Germany.

A. Pagano and E. Riccardi are with the Transport and OPB Innovation Department, Telecom Italia, Torino 10141, Italy.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSTQE.2009.2038238

## I. Introduction

POWER efficiency in telecommunication networks is a key issue for the development of the next generation telecom hardware. The energy saving checklist includes broadband core networks, which now appear to be significantly energy hungry, since electronic carrier routing systems include packet processors and routing engines that consume and dissipate large amounts of electrical power and heat, respectively [1].

The turn toward photonic technology has initiated considerable R&D investments with the development of switching systems that prove the potential of integrated optics in efficient data routing. The focus is specifically on the fabrication of a chip-scale router that will enable Tb/s switching through millimeter-scale photonic chips as well as graceful scaling to Pb/s capacities keeping down cost and footprint. To this end, monolithic InP and hybrid multielement photonic integration have been evolved in order to mark the transition from single element all-optical switches to large-scale photonic processing systems on-chip. The most recent significant R&D highlights that outline this transition include:

1) the $2\times8$ wavelength switch developed within Defense Advanced Research Projects Agency (DARPA) funded project IRIS [2];
2) the quadruple arrays of hybrid integrated semiconductor optical amplifier Mach–Zehnder interferometer (SOA-MZI) all-optical wavelength converters (AOWCs) developed within European Union (EU) funded project MUFINS [3];
3) the eight parallel SOA-MZI AOWCs integrated in InP within DARPA-funded project LASOR [4].

These achievements are now forming a new trend in functional photonic integration. From 2004 and on, the upgrade path involves doubling the throughput of photonic routing devices every two years, whereas the current state-of-the-art photonic device is offering 320 Gb/s throughput on a small chip size of $4.25 \times 14.5$ mm$^2$ [4]. These devices have enabled impressive system demonstrators involving optical packet routing with all-optical label switching [5]–[8].

In order to keep up with this emerging trend and allow for even smaller, faster, cheaper and "greener" optical routing chips, a photonic integration platform that will enable scalable, functional, and cost-effective integration is required.

Issues that are currently on the "photonic agenda" include thermal management within the photonic devices, further

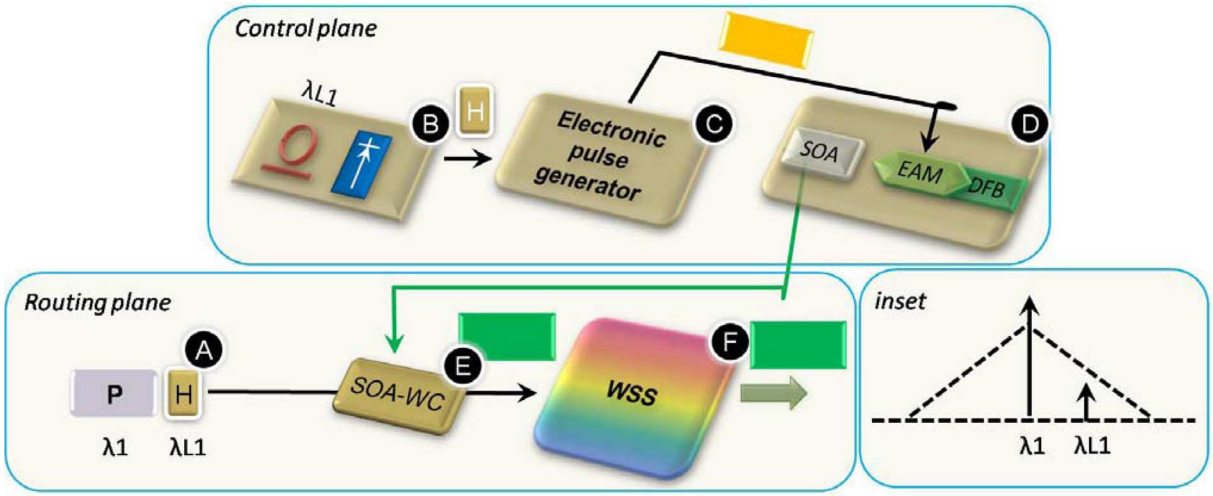



Fig. 1. BOOM photonic routing concept.

reduction of power consumption and—possibly—cost-effective fabrication with CMOS-compatible technologies.

The advent of silicon as a flexible hybrid integration platform is now providing a promising solution that can fulfill these key challenges. The blend of silicon and InP material as opposed to pure InP can combine cost efficiency and performance leading to a new generation of scalable and ultracompact integrated photonic routing building blocks. The hybrid integration using silicon offers the capability to utilize large 6-in silicon-on-insulator (SOI) wafers for realizing the integration boards and optimum utilization of the available small 2-in InP wafers [28], [29]. In terms of performance, the low-loss silicon waveguides (0.1 dB/cm) guarantee high-performance passive functionalities (the so-called optical–to-optical/O-O) such as filtering, multiplexing/demultiplexing and coupling. The O-E and E-O functionalities such as signal generation and modulation can be realized exploiting the high-frequency operation provided by InP. In fact, the effort is now to render silicon as the "host" and InP as the processing material [28].

In this rationale, the purpose of this paper is to introduce the "BOOM" silicon photonic routing concept and report the fabrication and testing of SOI and InP photonic integrated circuits that realize key functionalities of a photonic wavelength router including: ultrafast all-optical wavelength conversion, label extraction and detection, and control signal generation. Specifically, we demonstrate: 1) error-free 160 Gb/s AOWC using a single SOA and a cascaded delayed interferometer (DI) structure integrated on a 4 $\mu$m SOI substrate; 2) the fabrication of a microring resonator (MRR) SOI nanowire demultiplexer capable to filter out densely spaced (0.1 nm) in-band optical labels with an extinction of 15 dB; and 3) the integration of PIN photodetectors with 1.1 A/W responsivity and 10 pA dark current that can be cascaded after the MRR demultiplexer to efficiently detect 10 Gb/s optical labels; and 4) the fabrication of butt-coupled 10 Gb/s InP electroabsorption modulated lasers (EMLs) together with their BiCMOS SiGe drivers that can be integrated on a common SOI platform to transform electrical labels to packet-length optical control signals. All these building blocks can be employed to fabricate SOI hybrid integrated devices that can realize wavelength switching and routing of 160 Gb/s packet-mode optical signals.

## II. Boom Photonic Routing Concept

Fig. 1 illustrates a simplified sketch of the BOOM photonic routing concept. The packet format is as follows. The payload has a fixed time duration and consists of 160 Gb/s on–off keying (OOK) format Gaussian pulses. Optical labels are attached as subcarrier multiplexed signals within the broad spectrum of the payload (see inset in Fig. 1) [20], [21]. The label is a single (in the case of label swapping) nonreturn to zero (NRZ) optical pulse or multiple (in the case of label stripping) NRZ pulses with a duration equal to 1 ns, which is sufficient to trigger an optical flip-flop or an electrical pulse generator. The bandwidth of each label is 0.1 nm (or 12.5 GHz), so the label bit rate can be as high as 10 Gb/s if serial labels are employed. Assuming transform-limited pulses for the payload, the 3.4 nm 3-dB spectrum can occupy 17 labels spaced by 0.2 nm. Fig. 1 also shows the packet switching process. Packets arriving at the node front end (point A) are split into two parts. One part is injected into the label-processing unit, which starts with the label detection. Since labels are closely spaced, the detection of labels requires an UDWDM photodetector. In this case, the subsystem consists of a compact MRR demultiplexer with the transmission peaks of each MRR spaced by 0.1 nm, followed by an array of 10 GHz integrated detectors. The label (point B) triggers an electrical processing unit (e.g., FPGA), which generates an electrical signal with duration slightly longer than the packet duration (point C). This signal is then amplified with a 10 GHz modulator driver that drives an EML. The EMLs should provide pulsed optical signals with better than 100ps rise/fall times aiming to small guardbands and 50 dB ON/OFF ratio in order to obtain low crosstalk at the output of the node. The number of EMLs in the node corresponds to the number of the supported wavelength channels per input port. The EML generates an optical CW packet that powers up the AOWC and

the packet is wavelength converted (point E) and switched in a wavelength selective switch (point F). The AOWC consists of an SOA and a periodic comb-like filter for chirp filtering. The free spectral range (FSR) of the periodic filter should be equal to the channel spacing of the EMLs. Assuming that the SOA has a 3 dB ASE bandwidth of 30 nm, then the packet can be converted and routed to seven different wavelengths spaced by 4 nm.

The power consumption of the routing system will be largely determined by the electrical power consumed by the wavelength routing stage. In order to have a substantial gain over 40 Gb/s commercially available photonic systems [3], the power consumption should be lower than 12 W and the total throughput should exceed 160 Gb/s. Regarding system cascading, an approximate value of 2 dB power penalty should be achievable in order to facilitate the cascading of more than four network nodes in a typical core network.

## III. All-Optical Wavelength Converters

### A. Device Concept

Fig. 2(a) shows an artistic view of the BOOM silicon photonic AOWC. The device incorporates two monolithic integrated periodic filters and a hybrid integrated SOA. The SOA is used to induce chirp in the converted probe signal due to the refractive index modulation caused by the pulsed pump signal [10]. The first cascaded periodic filter is slightly detuned with respect to the probe wavelength and by filtering the blue (fast) chirp the acceleration of the effective recovery time of the system is achieved. The second filter is employed to restore the polarity of the optical pulses. Both periodic filters are implemented as passive MZI structures, integrated using SOI rib waveguide technology on substrates with a top silicon layer of 4 $\mu$m. The SOA can be flip-chip bonded on the same SOI board using AuSn or Sn/AgCu solder bumps.

Fig. 2(b) shows the layout of the passive SOI part of the AOWC. This involves two cascaded MZIs with differential delays of 1 and 2 ps, respectively, yielding an FSR of 8 and 4 nm, respectively. The responses at both output ports of the circuit comprising the two cascaded MZIs was simulated with VPI photonics software and the results are presented in Fig. 2(b). BAR corresponds to output T3, while CROSS port corresponds to output T4. Given the periodicity appeared on this comb-like filter structure, a high-speed optical packet injected in this AOWC can be converted on any of the CW wavelengths that coincide at a specific peak of the periodic response. Fig. 2(c)–(e) shows physical layer modeling results of the BOOM wavelength conversion scheme at 160 Gb/s. Fig. 1(c) shows the eye diagram at the output of the SOA revealing the slow recovery time of the amplifier when 160 Gb/s data are injected as pump signal. Fig. 1(d) shows the eye diagram at the output of the first detuned SOI MZI that indicates the effective recovery time of the system within the 160 Gb/s bit slot. Fig. 1(e) shows the eye diagram at the output of the second SOI MZI indicating the successful pulse polarity inversion.

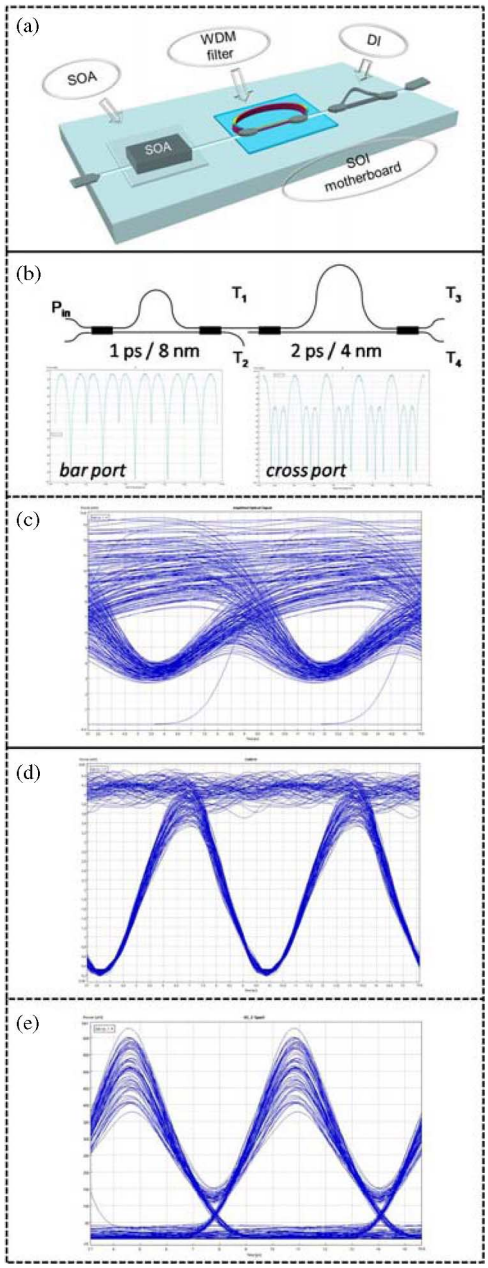



Fig. 2. (a) Schematic view of the BOOM AOWC device concept. (b) Layout of SOI MZI structure and simulated responses of bar and CROSS port. Modeling results at 160 Gb/s. (c) SOA output. (d) Output of first MZI. (e) Output of second MZI (160 Gb/s wavelength converted signal).

### B. 4 $\mu$m SOI AOWC Platform

In terms of passive functionality, the AOWC requires chirp filtering as well as polarity inversion (implemented by concatenation of two MZIs) and metallization for hybrid integration of the SOA. Waveguide optics and hybrid integration are implemented on SOI. The waveguides are rib waveguides. All optical functionality is realized by a single etch step. For rib definition, we used standard contact lithography and reactive ion etching. Additional etching and metalizations are required for hybrid integration of the SOA. We used substrates with top silicon thickness of 4 $\mu$m. The realized modes size ($\sim$4 $\mu$m) enables high coupling efficiency to lensed fibers and III–V

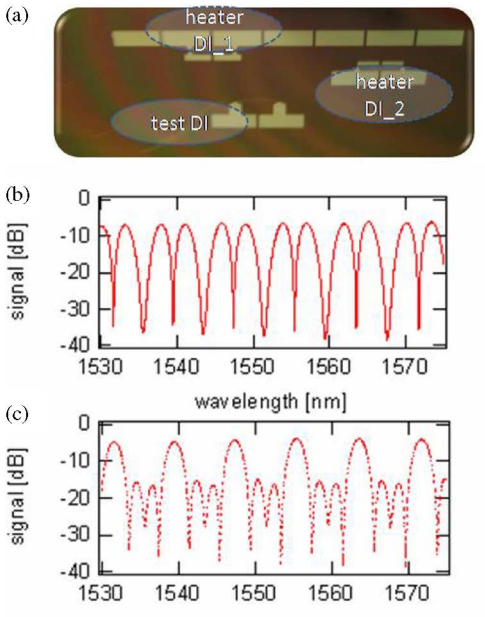



Fig. 3. (a) SOI AOWC platform with integrated heater elements. Filter characteristic of cascaded Mach–Zehnder delay interferometers with 1 and 2 ps time delay (TE-mode): solid lines correspond to (b) BAR port, (c) dashed line to CROSS port.

devices (∼0.5 dB loss per facet). Fig. 3(a) shows the fabricated SOI AOWC platform with integrated heater elements for MZI filter tuning. Results on the transfer function for BAR and CROSS port of the concatenated MZI device are illustrated in Fig. 3(b) and (c) and are in very good agreement with the simulation results of Fig. 2(b).

Extinction ratios are comparable to the results of single devices. The loss is slightly increased due to the doubling of involved interference couplers. The measured results show concatenated SOI-MZI structure delivers required performance to act as the proposed filter element following the SOA. Verification experiments with discrete SOA and SOI-DIs are presented in the next section.

Eventually, SOA and SOI-MZIs will be integrated on a single chip. Hybrid integration of DFB lasers on 4 $\mu$m SOI has already proven a promising approach for the fabrication of coarse WDM (CWDM) transmitter modules [11]. Here, we deploy a similar technique for SOAs. Devices will be soldered upside down, with butt-coupling of SOA and SOI waveguide. Vertical alignment is achieved by the buried oxide plane using etched posts. Lateral alignment is achieved by the precision flip-chip bonder. Optical coupling to the SOA will be facilitated by direct fiber attach (i.e., without a second waveguide interface). Conventional SOA fiber pigtailing techniques will be feasible. First integration tests of SOAs on SOI have been conducted. Fig. 4 shows a flip-chip-soldered SOA on an SOI motherboard. The performance of flip-chip-soldered SOAs showed little or no deterioration in comparison to nonintegrated devices. Small signal gain was 22 dB with no change in output saturation power. Coupling loss to the SOI board remained below 6 dB.

For the fabrication of the AOWCs (and also the EMLs) flip-chip mounting is preferred because performance is the central issue since we do require the minimum possible degradation of

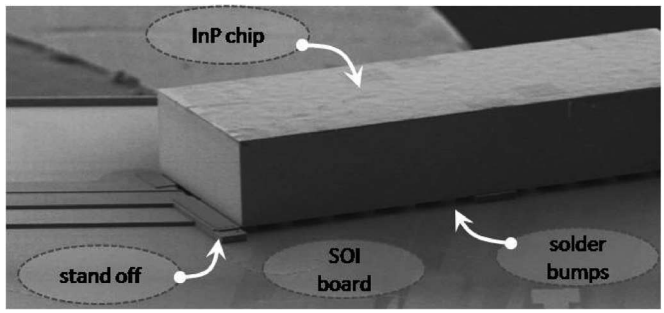



Fig. 4. Flip-chip-soldered SOA on SOI motherboard.

the data signals that transverse the optical nodes. This means that a substrate with a low-loss fiber-to-waveguide coupling as well as low-loss waveguide to active component on-chip coupling would be preferable. In this case, nanowire substrates would offer cost efficiency (mainly due to the CMOS-compatible fabrication methods) but they are still nonoptimum in terms of coupling. The coupling to the nanowire waveguides still results in high insertion losses (∼5 dB), whereas integration of high-performance prefabricated active components (such as SOAs or EMLs) is impossible due to the necessary very low alignment tolerances required, making the integration of wavelength converters and transmitters based on InP—at this stage—impossible. On the contrary, the 4 $\mu$m SOI PLC technology currently offers insertion losses <0.5 dB, low waveguide losses (∼0.1 dB/cm) and excellent mode matching between 4 $\mu$m waveguides and active InP chips, making the technology suitable for the fabrication of high-performance wavelength converters and high-speed optical transmitters.

Regarding thermal management, optical motherboards on SOI differ in two important aspects from silica-based platforms. The integration of actives (heaters, III–Vs) on SOI leads to comparatively low thermal crosstalk, since silicon is an excellent heat drain [26]. Integration density can therefore be quite high, as long as the power is dissipated effectively from the silicon (TEC or similar). Separation smaller than 300 $\mu$m is feasible for moderate cooling assumptions. On the other hand, thermal tuning will require higher power. The required power can be easily reduced by placing the heaters in close vicinity to the waveguides (without introducing additional losses). Without optimization, the power to fully tune (5.3 nm) the double MZI structure on SOI was 600 mW. Finally, efficient temperature control can be also realized using techniques based on thermally active solder bumps [27]

### *C. High-Speed, All-Optical Wavelength Conversion Using a Single SOA and the SOI MZI Chip*

The SOI photonic circuit was first characterized by coupling an amplified spontaneous emission (ASE) source coming from an erbium-doped fiber amplifier (EDFA) whose spectral range goes from 1530 to 1570 nm and measuring its spectral response. Fig. 5 shows the results of this characterization where we can observe on the normalized response an inner and an outer periodicity of 4 and 8 nm associated with the time delay introduced by each interferometer with a corresponding ratio of 7 and 22 dB,

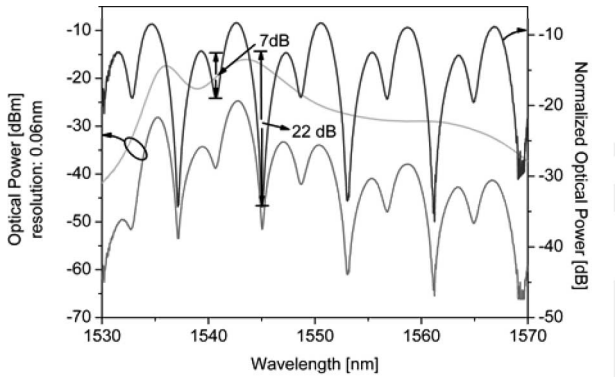



Fig. 5. Frequency response of the SOI-DI photonic circuit. (Light-gray trace) input, (gray trace) frequency response, (black trace) normalized frequency response.

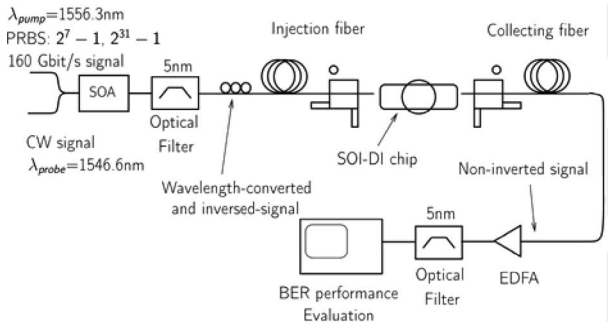



Fig. 6. Experimental setup for wavelength conversion at 160 Gb/s.

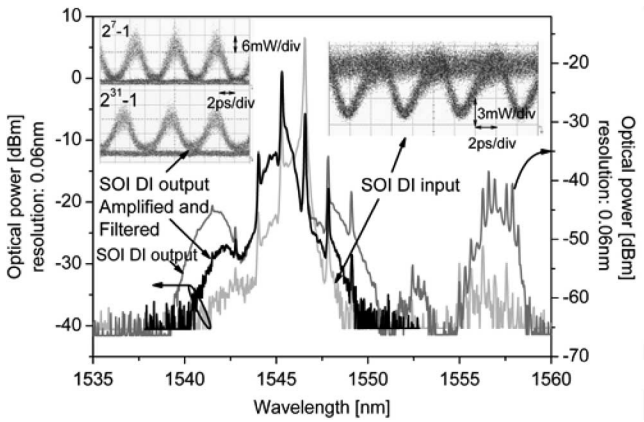



Fig. 7. Input/output spectra and eye diagrams for the SOI-DI photonic circuit. (Light-gray trace) SOI-DI input, (gray trace) SOI-DI output, (black trace) SOI-DI output amplified and filtered.

respectively. The measured response deviates slightly from the one presented in Fig. 3(b), mainly due to different temperature testing conditions of the chip as well as polarization dependency. In order to perform as a chirp filter and as a polarity inverter, it is necessary that one of the largest notch of the SOI-MZI frequency response coincide with the probe's wavelength, either by tuning the chip response (e.g., by temperature control) or by assigning the correct wavelength to the probe.

The evaluation of the SOI-based all-optical wavelength converter on ultrahigh speed optical signals is described in Fig. 6. To this effect, a 160 Gb/s bit-stream at 1556.3 nm, hereafter to be referred to as the pump, is coupled into a SOA in combination with a CW light at 1546.6 nm, hereafter to be referred to as the probe, to use wavelength conversion through XPM [10]. The employed SOA holds a 10%–90% gain recovery time of 10 ps while pumped with an injection current of 500 mA. The SOA has a saturation output power of 15 dB·m and a small-signal gain of 30 dB. The average optical powers at the SOA input were –5 and –0.9 dB·m for the pump and the probe, respectively.

At the output of the SOA, an optical bandpass filter (OBF) with a 3 dB bandwidth of 5 nm is used to select the probe and reject the pump signal. The SOA output is coupled into the SOI photonic circuit, which converts XPM into amplitude modulation and suppresses the carrier to produce a noninverted version of the wavelength converted signal. Finally, the output of the SOI photonic circuit is amplified by a low noise EDFA and filtered for bit-error-rate (BER) performance evaluation (see Fig. 6).

The produced spectra and eye diagrams using different pseudo-random binary sequence (PRBS) signals ($2^7 - 1$ and $2^{31} - 1$) at the input and output of the chip are shown in Fig. 7. The carrier of the input signal (trace in light gray) holds an extinction ratio of more than 15 dB over the harmonics at 160 GHz. At the output of the chip, the spectrum of the probe is modified (gray trace): the extinction ratio between the carrier and the spectral lines at 160 GHz varied from 15 to $-10$ dB with respect to the first spectral line on the left and from 23 to 13 dB with respect to the first spectral line on the right. This carrier suppression is translated into a noninverted version of the input signal. The output of the chip is then amplified and filtered (black trace) in order to perform BER measurements. From the eye diagrams we can verify that no patterning effect exists.

Fig. 8 shows the BER performance of the system. The circles illustrate the error-free operation of a single 40 Gb/s channel that corresponds to the case without wavelength conversion. The squares represent the 160-to-40 Gb/s without wavelength conversion used as a reference, whereas the stars represent the wavelength converter channels using the SOA-based AOWC.

All the channels achieved error-free operation (BER = 1e–9) with an average optical receiver power of –7.5 dB·m associated to an average power penalty of 5.5 dB, which is 3.5 dB higher than the target value set for optimum cascadability of the photonic routers. This penalty is due to a reduction of the SNR (OSNR) introduced by the light coupling in the SOI device and is explained as follows. The coupling losses at the input and output facets (including the insertion losses) were determined to be 11 dB. In addition, the device itself presents losses of around 3dB, which makes the total loss equal to 14 dB. Both signal and noise are affected in the same fashion by the device losses and the device mounting and alignment should not induce any degradation to the signal quality, if there was no amplifier after the chip. However, during BER measurements the signal at the output of the SOI chips had to be amplified with an EDFA with around 20–25 dB gain and ∼5–6 dB noise figure within this gain region. This implies that extra noise is added to the already noisy signal degrading the OSNR. The power penalty for error free (BER = 1e–9) operation of the all-optical wavelength

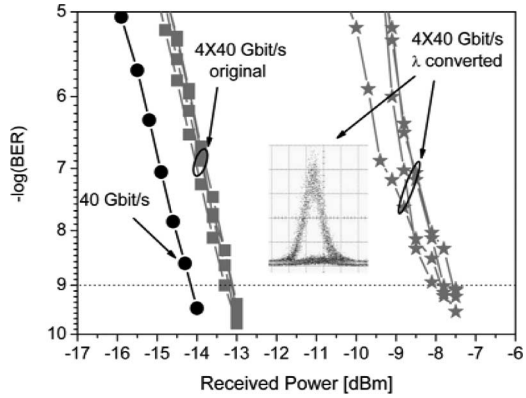



Fig. 8. BER curves of the SOA-based AOWC. (Circles) single channel without wavelength-conversion. (Squares) $4 \times 40$ Gb/s without wavelength-conversion. (Stars) $4 \times 40$ Gb/s with wavelength-conversion.

converter can be improved with the flip-chip mounting of the SOAs on the SOI platform and the SOA on-chip coupling to the MZIs. Further reduction of the power penalty can be also obtained with the employment of ultrafast SOAs [22].

In terms of electrical power consumption, the "BOOM" AOWC scheme consumes approximately 2 W, including the power for driving the SOA, the power to tune the FSR of the SOI DIs and the power consumed by the TEC. By extrapolating, a quad array AOWC with a total throughput of 640 Gb/s would require approximately 8 W, which is 1.5 times lower than the power consumed by a commercially available SOA-MZI array with a total chip throughput of 160 Gb/s.

## IV. UDWDM Photodetector

### A. Device Concept

Fig. 9(a) shows a schematic view of the UDWDM photodetector component. The device incorporates an UDWDM demultiplexer implemented with eight cascaded SOI nanowire MRRs and eight hybrid integrated evanescent photodetectors on the same chip. The device is used to filter-out the labels that are attached to an optical packet and transform them into electrical signals for subsequent processing by an electronic controller. Fig. 9(b) illustrates the microscopic image of a four-channel MRR demultiplexer fabricated on a 220 nm top-silicon layer substrate. The cross section of the waveguides is $450 \times 220\,\text{nm}^2$ and the microring radius is as low as 17 $\mu$m to obtain a large FSR per resonator. The transmission peaks of the microrings are spaced by 0.1 nm to achieve UDWDM operation, and thus, enable densely spaced in-band or out-of-band optical labels. Eventually, an array of photodetectors will be integrated on the drop ports of the UDWDM demultiplexer. In the case of the UDWDM photodetector that is responsible for the detection of labels, having no direct impact on the data signal quality the die-to-wafer bonding technique will be preferred [17]. This choice will guarantee a low fabrication cost whereas acceptable performance can be maintained by employing highly efficient photodetectors that can operate on low power injected optical signals, as presented in the next two sections.

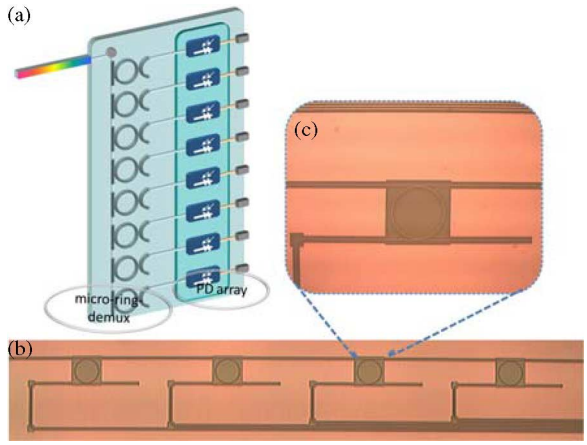



Fig. 9. (a) Schematic view of UDWDM photodetector unit, (b) microscopic image of a 4-channel SOI nanowire demultiplexer based on cascaded microring resonators, and (c) close-up on single MRR.

### B. SOI Nanowire Demultiplexer

The UDWDM demultiplexer consists of a series of cascaded MRRs based on the SOI nanowire waveguide platform [12]. The MRRs were designed to have a bending radius of 17 $\mu$m, resulting in an FSR of 5.5 nm. The latter is determined by the spacing between two adjacent data channels, which is typically 5–6 nm. Since the desired bandwidth of the resonant peak is very small in order to reduce the interchannel crosstalk, i.e., much smaller than the 0.1 nm channel spacing between the labels, the coupling strength should be very weak. However, as the coupling strength decreases, the channel drop loss increases. Fig. 10 shows how drop loss and crosstalk vary as the field transmission coefficient ($t$) increases (i.e., the coupling decreases). Two values of the propagation loss ($\alpha$) in the MRR, 3 and 10 dB/cm are considered, and the results are shown in Fig. 10(a) and (b), respectively. In both cases, the drop loss increases and the crosstalk performance improves as $t$ increases. For a given $t$, the performances are better in terms of both drop loss and crosstalk when the propagation loss is lower. Therefore, it is very important to realize a low-loss MRR, which is determined by the fabrication process.

The MRRs were fabricated using a 193 nm deep ultraviolet (DUV) lithography process [13]. Fig. 11 shows the measured spectral response of the drop port of the MRR. The FSR is about 5.34 nm (not shown here), which agrees well with the designed value (5.5 nm). The drop loss is about 12.7 dB and the 3 dB bandwidth is 0.04 nm ($Q \sim 4 \times 10^4$). This corresponds to $\alpha =$ 14 dB/cm and $t = 0.9975$. The estimated crosstalk is $\sim$15 dB when applying it for the demultiplexer with a channel spacing of 0.1 nm.

The extracted loss is much larger than the propagation loss of the straight waveguide ($\sim$3 dB/cm). As the bending radius is very large (17 $\mu$m) and a negligible bending loss can be expected, other loss sources should be responsible for this large loss. One possible reason is the coupling into the counterpropagating mode [24]. The coupling is caused by the surface-roughness-induced reflection. According to Little *et al.* [24], even a small reflection may lead to a serious contradirectional coupling when the coupling strength between the bus waveguide

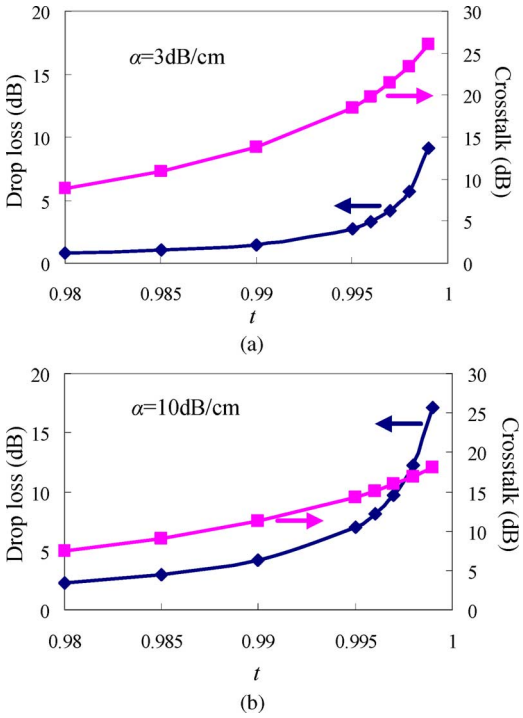



Fig. 10. Drop loss and crosstalk as a function of the field transmission coefficient ($t$).

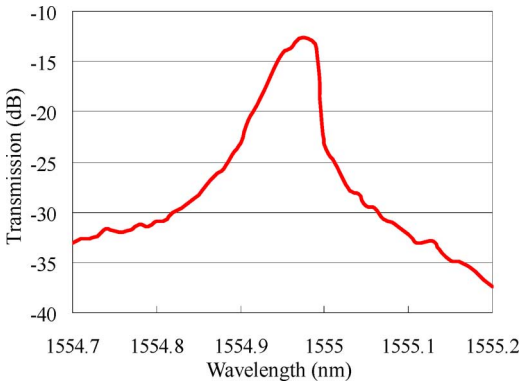



Fig. 11. Measured spectral response of the drop port of the MRR.

and the MRR is very weak, which is just our current case. This detrimental coupling may not only increase the drop loss, but also broaden (or even split) the resonant peak. In order to reduce the sidewall roughness, some postfabrication process can be used, e.g., wet chemical oxidation [25].

We also observe that the resonant wavelengths are different even for nominally identical MRRs. The difference between the resonant wavelengths can reach as high as 0.7 nm, which is seven times the channel spacing. This is caused by random process fluctuations during fabrication and is very difficult to overcome at present [14]. Therefore, in practice, it is necessary to incorporate postfabrication trimming or tuning elements. For example, the individual resonant wavelength of each MRR can be thermally tuned with microheaters [15].

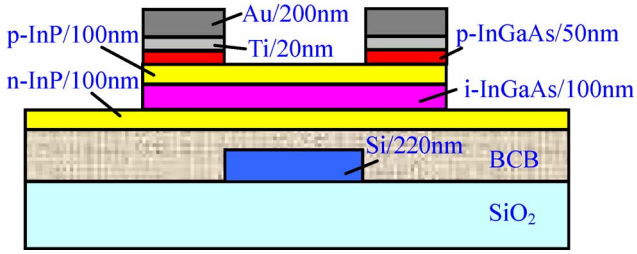



Fig. 12. Cross section of a novel configuration of a PIN photodetector evanescently coupled with an SOI waveguide, where a central opening is introduced on the p-contact layers. The thickness of each layer is also shown.

### C. SOI-Compatible Evanescent PIN Detectors

InGaAs MSM detectors integrated with silicon nanowire waveguide circuits have been previously reported [16]. These have a high efficiency (1 A/W) and relatively low dark current (1 nA). Now, we are investigating the possibility to replace the MSM detectors by PIN detectors, which might have lower dark current and require lower bias voltage. The issue with PIN detectors is that they require a thicker layer structure, and therefore, are more difficult to design under phase-matching conditions. We proposed an improved concept with sideways contacts, which can overcome this problem [17].

Fig. 12 shows the cross section of the current PIN detector evanescently coupled with an SOI waveguide, where a central opening structure is introduced on the p-contact layers. The n-type metal (not shown in the figure for clarity) is placed far away from the SOI waveguide on the n-InP lateral contact layer and, therefore, has no influence on the optical coupling. Due to the large imaginary parts of the p-metal contacts on both sides of the detector mesa, the optical mode is confined in the central part of the mesa, and the overlap of the optical field with the p-type contact layers is reduced significantly. This effectively reduces the unwanted absorption by the p-metal and p-InGaAs layers. The thickness of each III–V layer (also shown in Fig. 12) is chosen to achieve phase matching between the SOI waveguide mode and the detector mode. For the current structure, we calculated the absorbed power as a function of detector length for both the real structure and a virtual structure where we only take into account the unwanted absorption of the p-InGaAs and the p-metal layers. Fig. 13 shows the results. It is evident that the absorption by the p-type contact layers is less than 5% of the input power, while the absorption of the real structure is over 98%. This indicates that the detrimental absorption of the contact layers is effectively suppressed without sacrificing the absorption efficiency of the i-InGaAs layer.

We have also fabricated and characterized this type of PIN detectors. The measured responsivity is 1.1 A/W at the wavelength of 1550 nm (as shown in Fig. 14), which corresponds to a quantum efficiency of 88%. The dark current is around 10 pA. Since the internal electric field of the PIN junction is strong enough, no external bias voltage is needed. As the intrinsic layer is very thin (100 nm) and the detector size is quite small ($9 \times 40 \mu$m2), a high speed operation of the current PIN detectors can be expected [23].

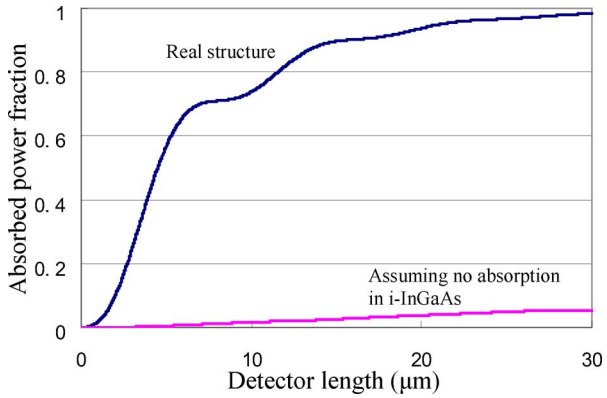



Fig. 13. Absorbed power for both the real structure and a virtual structure with no i-InGaAs absorption.

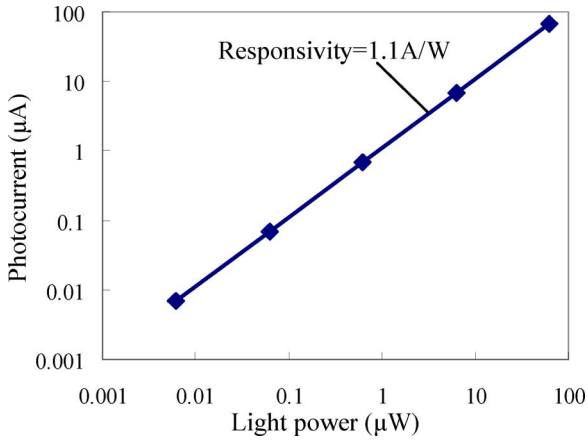



Fig. 14. Measured photoresponse (without external bias voltage) of the fabricated PIN photodetector.

## V. High-Speed Transmitters

### A. Device Concept

Fig. 15 shows a schematic view of the EML transmitter module. The device incorporates two monolithic InP EML blocks flip-chip bonded on a 4 $\mu$m top silicon SOI substrate. Cascaded on-board SOAs are incorporated as on-chip amplifiers or shutters. The SOI board incorporates also the optical waveguides, a passive multiplexer, microstrip lines, and electrical dc conductors and an SiGe BiCMOS driver to drive the modulators on-chip. The device is used to control the AOWC during the optical routing process and must exhibit fast rise and fall times. The fabrication of flip-chip-adapted EML and electronic driver is described in the next sections.

### B. Flip-Chip-Adapted EMLs

Butt coupling as monolithic integration technique was applied to form flip-chip-adapted EML devices, because it allows the utmost flexibility by individual selection of the laser's and modulator's waveguide core composition, respectively, while demanding only reasonable fabrication effort, but allowing only moderate coupling loss. Fig. 16 shows a schematic view of the investigated architecture. A DFB laser, an electroabsorption (EA) modulator and a spot-size expander are integrated in a longitudinal sequence following a common waveguide direction. The epitaxial layer stack for the modulator was selectively grown in a second growth cycle, after cutting appropriate islands out of the firstly grown layer sequence for the laser. The resulting composite core layer was then etched into a stripe and buried by InP regrowth (*BH* structure) to form the devices' waveguide. For the spot-size expander, waveguide width tapering with a passive and an active core were realized. To form the passive version the active layers of the tapered waveguide core were also etched away before regrowth of the *BH* layers, while for the active version they were kept. The latter version needs an additional p contact for pumping.

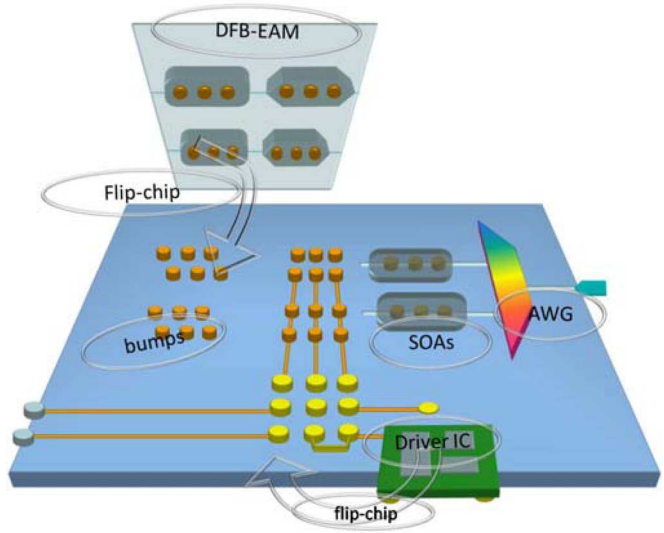



Fig. 15. Schematic view of EML transmitter unit.

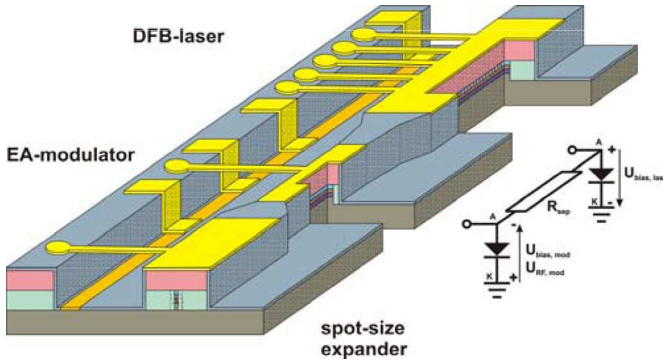



Fig. 16. Schematic depiction of the chosen architecture for BOOM EMLs with monolithically integrated spot-size expander/optical power booster.

The chosen gain curve and DFB laser gratings produce emission wavelengths between 1520 and 1580 nm, adjusted to the absorption curve of the modulator, especially in its dependence on applied bias voltage.

Fig. 17 depicts a SEM view onto the chip surface of an EML device. Clearly visible are the four functionally different sections of the waveguide stripe: DFB: DFB laser, five p-contact pads to the right; SEP: passive separation waveguide; MOD: modulator, one p-contact pad to the left; TAP: spot-size expander, passive version. The surface n-contact common for all active sections is formed by the long metallization stripe on the bottom of an etch pit parallel to the waveguide on its left side.

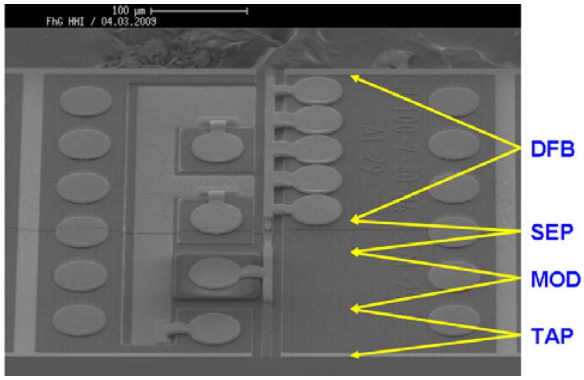



Fig. 17. SEM picture of an EML chip with passive spot-size expander.

It is connected with three contact pads on the topmost chip surface, one for the laser static bias current and two flanking the modulator's p-contact, allowing RF connection with appropriate probeheads. One row of six metal pads at the left side, one at the right, will be used for flip-chip mounting.

The passive waveguide between laser and modulator (SEP) electrically isolates these devices, biased in opposing directions (see insert in Fig. 16). Its length and cross-section (including the recess indicated in Fig. 16) defines the separation resistance, values of 100 kΩ and more were measured. The outer waveguide is kept recessed along the whole modulator section in order to minimize modulator capacity and to ensure a strong overlap of the optical mode in the waveguide with the applied electrical field, which controls the modulator's absorption.

All investigated stand-alone reference FP laser chips show a good performance with only small variations; this proves the suitability of the fabrication process. Stand-alone gain coupled DFB lasers produced a higher single mode yield, as expected. Correspondingly gain coupled EMLs are more stable against back reflections, which cannot be avoided inherently. They originate from the laser–modulator interface, where waveguides of different effective refractive index are coupled. This robustness is also found in the mode stability against changes in modulator operation parameters.

Stand-alone modulator sections with integrated passive waveguide taper, separated by cleavage, were investigated first. The assessment of the absorption behavior of stand-alone modulator sections allowed the selection of appropriate DFB laser operation wavelengths for all types of EMLs to be investigated.

The threshold currents of EMLs lie between 8 and 25 mA, their output powers at 100 mA range between 7 and 21 mW. These values depend on the respective device layout, e.g., on the position of the DFB wavelength relative to the gain curve and modulator absorption edge, on details of the EML design such as modulator waveguide geometry, active layer composition, and design of the passive waveguide sections (SEP and TAP lengths and widths). The observed threshold currents are comparable with single DFB lasers.

Results from the static performance of modulator switching are shown in Fig. 18 for an EML with a gain-coupled DFB laser. The necessary switching voltage $\Delta U_{\mathrm{EAM}}$ to achieve a static extinction ratio of ER = 10 dB depends on the EML operation values for laser bias current $I_L$ and modulator bias voltage $U_{\mathrm{EAM}}$. For lowest modulator absorption in the through-state, i.e., with $U_{\mathrm{EAM}} = 0$ V, an ER of 10 dB is achieved for $\Delta U_{\mathrm{EAM}} = 2.4$ V. If an additional modulator absorption of about 5 dB can be tolerated (at $U_{\mathrm{EAM}}$ around $-2$ V), $\Delta U_{\mathrm{EAM}} = 1.2$ V is sufficient. These measured values for the static switching voltage are in the range of what can be handled by driver ICs to be developed. As this EML device is only needed for optical processing inside the BOOM demonstrator chip and not for transmission purposes, i.e., only for switching and not for modulation, the consideration of chirp effects is not of importance in this context.

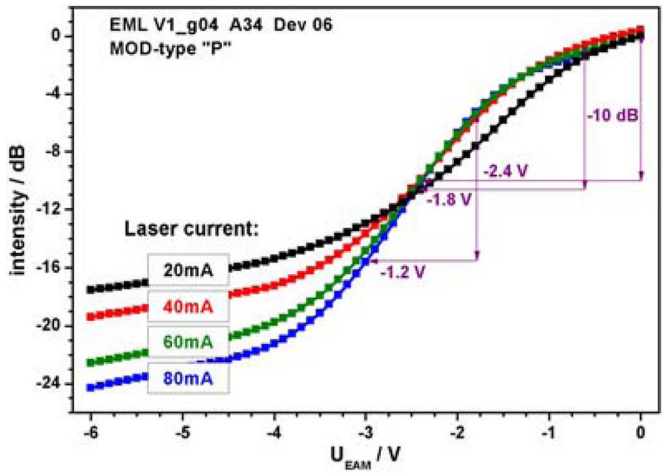


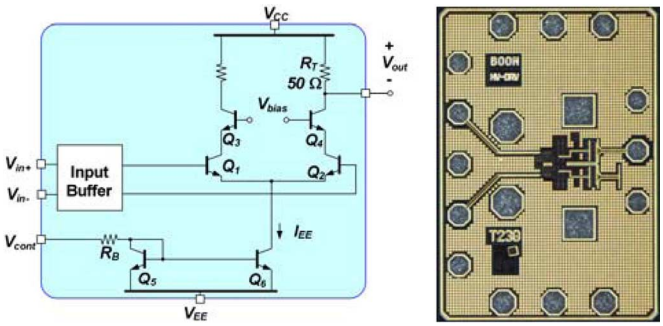

Fig. 18. Dependence of static extinction ratio on modulator bias voltage and laser bias current. Laser: gain coupled, emission wavelength: 1521 nm; modulator with selectively grown waveguide core, 100 $\mu$m long; passive spot-size expander.

Assessment of EMLs with active taper sections, working as power booster, will follow, and then the static measurements will be completed. In addition, the RF behavior of EMLs is currently under investigation.

### C. SiGe BiCMOS Drivers

The basic operation of a modulator driver chip is to supply two levels of voltage or current to the optical device corresponding to the two digital levels of electrical input signal. The modulator driver presented here has to provide 2 Vpp voltage swing for EA modulator at 10 Gbps. The block diagram of the chip is given in Fig. 19(a). It consists of a differential-in/differential-out buffer and a cascode differential pair working as current switch. Termination resistor is placed on-chip for the single-ended output. An input buffer is utilized to achieve a small input capacitance and to have a low-impedance node at the input of the differential pair, and thereby, to achieve a large bandwidth. Cascode topology is utilized since in this topology output transistor ($Q4$), which experiences a large collector–emitter voltage (higher than $\mathrm{BV_{ceo}}$ breakdown voltage) has a low base-impedance. Low base-impedance considerably improves the collector–emitter breakdown voltage in bipolar transistors [18]. Output voltage swing is controlled by changing the tail current of differential pair ($I_{\mathrm{EE}}$) using $V_{\mathrm{cont}}$ pin.

The chip is designed to have $S_{11}$ and $S_{22}$ of below –10 dB up to 8 GHz. The bandwidth of the circuit is mostly determined by




(a) (b)

Fig. 19. (a) Simplified diagram of SiGe driver chip. (b) Die photograph.

the parasitic capacitance of the EAM. For parasitic capacitance of about 0.2 pF, bandwidth will be in excess of 20 GHz, which results in rise/fall time of less than 30 ps for the output signal. The driver works with 5 V supply and consumes 0.66 mW. The driver chip was fabricated in IHP's commercial 0.25 $\mu$m SiGe BiCMOS technology, which offers transistors with a cutoff frequency ($f_T$) of 120 GHz and breakdown voltage of 2.3 V. Die photograph of the driver in shown in Fig. 19(b). Die area is 0.6 mm$^2$. The values described here indicate that the driver modulator can provide an output swing of 2.3 Vpp at 20 GHz, which is more than enough for driving the EML at 10 Gb/s with 10 dB extinction ratio.

### D. SOI AWG Multiplexer

A multiplexer (MUX) is required for the high-speed transmitters. MUX design will be based on 4 $\mu$m SOI rib waveguide technology. Previous results show that low-loss designs are possible in this technology using spot-size conversion at the transition between the waveguide and the free propagation region of the star-coupler [19].

## VI. Conclusion

In this paper, we have presented the basic device concepts, which can be realized using SOI hybrid integration, that implement key functionalities of high-capacity wavelength photonic routers. First, we have demonstrated the SOI-DI AOWC concept—a new AOWC scheme that employs a single SOA and an SOI-cascaded DI chip to perform error free 160 Gb/s all-optical wavelength conversion. In addition, we have presented the fabrication of a SOI nanowire demultiplexer consisting of cascaded MRR that can filter out densely spaced labels from high-speed optical packets. For the electrical detection of labels, we have presented the design and fabrication of $9 \times 40\ \mu\text{m}^2$ PIN detectors exhibiting 1.1 A/W responsivity and dark current as low as 10 pA. These detectors can be integrated with the MRR demultiplexer using die-to-wafer bonding techniques [17]. Finally, we have demonstrated the fabrication of InP EML blocks using the butt-coupling technique and their BiCMOS driver ICs that can be used to convert the electrical labels into optical packet-length control signals. These components can be hybridly integrated on SOI substrates and they can be combined to demonstrate wavelength switching and routing of 160 Gb/s optical packets.

## References

[1] R. S. Tucker, R. Parthiban, J. Baliga, K. Hinton, R. W. A. Ayre, and W. V. Sorin, "Evolution of WDM optical IP networks: A cost and energy perspective," *J. Lightw. Technol.*, vol. 27, no. 3, pp. 243–252, Feb. 2009.

[2] J. Gripp, "The IRIS optical packet router: A DARPA/MTO project," presented at the Int. Workshop Future Opt. Netw. (FON), Opt. Fiber Commun. Conf. (OFC 2006), Anaheim, CA.

[3] L. Stampoulidis, D. Apostolopoulos, D. Petrantonakis, P. Zakynthinos, P. Bakopoulos, O. Zouraraki, E. Kehayas, A. Poustie, G. Maxwell, and H. Avramopoulos, "Enabling Tb/s photonic routing: Development of advanced hybrid integrated photonic devices to realize high-speed, all- optical packet switching," *IEEE J. Sel. Topics Quantum Electron.*, vol. 14, no. 3, pp. 849–860, May/Jun. 2008.

[4] S. C. Nicholes, M. L. Mašanović, B. Jevremović, E. Lively, L. A. Coldren, and D. J. Blumenthal, "The world's first InP 8 $\times$ 8 monolithic tunable optical router (MOTOR) operating at 40 Gbps line rate per port," presented at the OFC/NFOEC 2009, San Diego, CA, paper PDPB1.

[5] A. Al Amin, K. Shimizu, M. Takenaka, R. Inohara, K. Nishimura, Y. Horiuchi, M. Usami, Y. Takita, Y. Kai, Y. Aoki, H. Onaka, T. Miyahara, T. Hatta, K. Motoshima, and Y. Nakano, "Label-based path switching and error-free forwarding in a prototype optical burst switching node using a fast 4 $\times$ 4 optical switch and shared wavelength conversion," in *Proc. Opt. Fiber Commun. Conf. (OFC 2006)*, Session Optical Packet Switching II (OFO), Paper OFO5.

[6] B. Xiang, Z. Zhu, H. Yang, W. Jiang, D. L. Harris, K. Ikezawa, R. Umeda, and S. J. B. Yoo, "First field trial of OLS network testbed with all-optical contention resolution of asynchronous, variable-length optical packets," in Tech. Dig. IEEE/OSA Opt. Fiber Commun. Conf., Anaheim, CA, 2007, Paper OMJ6.

[7] N. Wada, H. Furukawa, and T. Miyazaki, "Prototype 160-Gbit/s/port optical packet switch based on optical code label processing and related technologies," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 5, pp. 1551–1559, Sep./Oct. 2007.

[8] F. Ramos *et al.*, "IST-LASAGNE: Towards all-optical label swapping employing optical logic gates and optical flip-flops," *J. Lightw. Technol.*, vol. 23, no. 10, pp. 2993–3011, Oct. 2005.

[9] (2008). [Online]. Available: http://www.ict-boom.eu/

[10] Y. Liu, E. Tangdiongga, Z. Li, S. Zhang, H. de Waardt, G. D. Khoe, and H. J. S. Dorren, "Error-free all optical wavelength conversion at 160 Gb/s using a semiconductor optical amplifier and an optical bandpass filter," *J. Lightw. Technol.*, vol. 24, no. 1, pp. 230–236, Jan. 2006.

[11] T. Mitze, M. Schnarrenberger, L. Zimmermann, J. Bruns, F. Fidorra, K. Janiak, J. Kreissl, S. Fidorra, H. Heidrich, and K. Petermann, "CWDM transmitter module based on hybrid integration," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 5, pp. 983–987, Sep.–Oct. 2006.

[12] Z. Sheng, L. Liu, S. He, D. Van Thourhout, and R. Baets, "Silicon-on-insulator microring resonator for ultra dense WDM applications," presented at the 6th IEEE Int. Conf. Group IV Photon., San Francisco, CA, Sep. 9–11, 2009.

[13] W. Bogaerts, L. Liu, S. Selvaraja, P. Dumon, J. Brouckaert, D. Taillaert, D. Vermeulen, G. Roelkens, D. Van Thourhout, and R. Baets, "Silicon nanophotonic waveguides and their applications," *Proc. SPIE*, vol. 7134, pp. 71341O-1–71341O-13, 2008.

[14] S. Selvaraja, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Subnanometer linewidth uniformity in silicon nanophotonic waveguide devices using CMOS fabrication technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 1, pp. 316–324, Jan./Feb. 2010.

[15] F. Gan, T. Barwicz, M. A. Popović, M. S. Dahlem, C. W. Holzwarth, P. T. Rakich, H. I. Smith, E. P. Ippen, and F. X. Kärtner, "Maximizing the thermo-optic tuning range of silicon photonic structures," in *Proc. IEEE 2007 Photon. Switching Conf.*, San Francisco, CA, pp. 67–68.

[16] J. Brouckaert, G. Roelkens, D. Van Thourhout, and R. Baets, "Compact InAlAs-InGaAs metal-semiconductor-metal photodetectors integrated on silicon-on-insulator waveguides," *IEEE Photon. Technol. Lett.*, vol. 19, no. 19, pp. 1484–1486, Oct. 2007.

[17] Z. Sheng, L. Liu, J. Brouckaert, S. He, D. Van Thourhout, and R. Baets, "Investigation of evanescent coupling between SOI waveguides and heterogeneously-integrated III–V pin photodetectors," in *Proc. 21st IEEE Int. Conf. Indium Phosphide Rel. Mater.*, Newport Beach, CA, May 10–14, 2009, pp. 159–162.

[18] J. D. Cressler and G. Niu, *Silicon Germanium Heterojunction Bipolar Transistor*. Boston, MA: Artech House, 2003.

[19] M. Schnarrenberger, L. Zimmermann, T. Mitze, K. Voigt, J. Bruns, and K. Petermann, "Low loss star coupler concept for AWGs in rib waveguide technology," *IEEE Photon. Technol. Lett.*, vol. 18, no. 23, pp. 2469–2471, Dec. 2006.

[20] N. Calabretta, H.-D. Jung, J. Herrera Llorente, E. Tangdiongga, T. A. M. J. Koonen, and H. J. S. Dorren, "All-optical label swapping of scalable in-band address labels and 160-Gb/s data packets," *J. Lightw. Technol.*, vol. 27, no. 3, pp. 214–223, 2009.
[21] J. Herrera, E. Tangdiongga, Y. Liu, M. T. Hill, R. McDougall, A. Poustie, G. Maxwell, F. Ramos, J. Marti, H. de Waardt, G. D. Khoe, A. M. J. Koonen, and H. J. S. Dorren, "160-Gb/s all-optical packet-switching with in-band filter-based label extraction and a hybrid-integrated optical flip-flop," *IEEE Photon. Technol. Lett.*, vol. 19, no. 13, pp. 990–992, Jul. 2007.
[22] T. Hatta, T. Miyahara, T. Miyazaki, K. Takagi, K. Matsumoto, T. Aoyagi, K. Motoshima, K. Mishina, A. Maruta, and K. Kitayama, "Polarization-insensitive monolithic 40-Gbps SOA–MZI wavelength converter with narrow active waveguides," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 1, pp. 32–39, Jan./Feb. 2007.
[23] J. Bowers and C. A. Burrus, "Ultrawide-band long-wavelength p-i-n photodetectors," *J. Lightw. Technol.*, vol. 5, no. 10, pp. 1339–1350, Oct. 1987.
[24] B. E. Little, J.-P. Laine, and S. T. Chu, "Surface-roughness-induced contradirectional coupling in ring and disk resonators," *Opt. Lett.*, vol. 22, no. 1, pp. 4–6, 1997.
[25] D. K. Sparacin, S. J. Spector, and L. C. Kimerling, "Silicon waveguide sidewall smoothing by wet chemical oxidation," *J. Lightw. Technol.*, vol. 23, no. 8, pp. 2455–2461, Aug. 2005.
[26] B. Wohlfeil, L. Zimmermann, K. Petermann, J. Kreissl, and H. Gustat, "Thermal limits for integration of directly modulated lasers with driver IC on SOI," presented at the OFC, San Diego, CA, 2009, Paper JThA.
[27] P. Magill (2009, Jul.). Thermal management: A hot topic. Fibersystems Europe Magazine. [Online]. Available: http://fibresystems.org/cws/article/magazine/39834
[28] D. Liang and J. E. Bowers, "Photonic integration: Si or InP substrates?," *Electron. Lett.*, vol. 45, no. 12, pp. 578–581, Jan. 4, 2009.
[29] M. Ziari *et al.*, "Large scale integration of photonic integrated circuits on indium phosphide and high-index-contrast Si platforms," presented at the ECOC 2009, Vienna, Austria, Paper 1.7.2.

**Leontios Stampoulidis** (M'03) received the Diploma in electronic and electrical engineering from the University of Patras, Patras, Greece, in 2002, and the Ph.D. degree from the National Technical University of Athens, Athens, Greece, in 2009.

Since 2002, he has been with the Photonics Communications Research Laboratory, Athens, Greece. His current research interests include optical packet/burst switching architectures and photonic Tb/s routers based on photonic integrated components. He has authored or coauthored more than 40 papers in scientific journals and conferences.

Dr. Stampoulidis is a member of the IEEE Photonics Society [formerly known as Lasers and Electro-Optics Society (LEOS)] and a member of the Technical Chamber of Greece.

**Konstantinos Vyrsokinos** received the B.Sc. degree in physics from Aristotle University of Thessaloniki, Thessaloniki, Greece, and the Ph.D. degree from the Electrical and Computer Engineering Department, National Technical University of Athens, Athens, Greece.

Since 2002, he has been with the Photonics Communications Research Laboratory, National Technical University of Athens, where he is currently a Research Associate involved in many European (IST-LASAGNE, IST-MUFINS, IST-e-Photon/One and IST e-Photon/One+) and National research programs (PENED2003). Currently, he is participating in European BOOM project, designing silicon nanophotonic structures for all-optical wavelength conversion and add–drop functionalities. His research interests include the design and simulation of integrated components and subsystems for high-speed optical communication systems and radio over fiber subsystems as well. He has authored or coauthored more than 30 research papers in peer-reviewed journals and conferences. He is also an Adjunct Lecturer with the Informatics and Telecommunications Department, University of Western Macedonia, Kozani, Greece.

**Karsten Voigt** received the Master's degree from the Technical University of Berlin (TU-Berlin), Berlin, Germany, in 2005.

He joined TU-Berlin, where he is currently engaged in the development of interferometric photonic components based on silicon-on-insulator material systems.

**Lars Zimmermann** received the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 2003.

In 1998, he joined IMEC. In 2004, he joined the Technical University of Berlin (TU Berlin), where he worked on silicon waveguide and optical motherboard technology. Since 2006, he has been the Coordinator of the Photonic Packaging Platform ePIXpack. In 2008, he joined IHP, where he has been the Scientific Coordinator of the Joint Lab Silicon Photonics between IHP and TU Berlin. His current research interests include electronic–photonic integration and integrated optics.

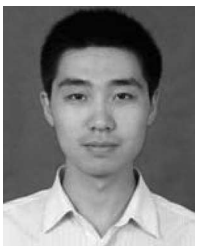
**Fausto Gomez-Agis** received the B.Sc. degree in electronics from the Instituto Tecnol$\sigma$gico de Mazatl$\alpha$n, Sinaloa, Mexico, in 1996, the M.Sc. degree in optics from CICESE Research Center, Ensenada, Mexico, in 1999, and the Ph.D. degree from the cole Nationale Sup$\iota$rieure des T$\iota\iota$communications (now TELECOM ParisTech), Paris, France, in 2008.

In 2000, he joined the last-mile access Department of TELMEX (Tel$\iota$fonos de M$\iota$xico), Jalisco, Mexico, as a Systems Engineer. From 2001 to 2004, he was with CIDEC (CONDUMEX R&D Center), Quer$\iota$taro, Mexico, where he was involved with research activities on plastic optical fiber communications such as, design, construction and evaluation of devices for fast-ethernet LAN applications. He is currently with COBRA Research Institute, Eindhoven University of Technology, Eindhoven, The Netherlands, where he is involved with research on ultrahigh-speed optical signal processing.

**Harm J. S. Dorren** received the M.Sc. degree in theoretical physics and the Ph.D. degree from Utrecht University, Utrecht, The Netherlands, in 1991and1995, respectively.

After postdoctoral positions, he joined Eindhoven University of Technology, Eindhoven, The Netherlands, in 1996, where he currently a Professor and the Scientific Director of the COBRA Research Institute. In 2002, he was also a Visiting Researcher with the National Institute of Industrial Science and Technology (AIST), Tsukuba, Japan. His current research interests include optical packet switching, digital optical signal processing, and ultrafast photonics. He has authored or coauthored more than 250 journal papers and conference proceedings.

Dr. Dorren is currently an Associate Editor for the IEEE JOURNAL OF QUANTUM ELECTRONICS.



**Zhen Sheng** (S'09) received the B.Eng. degree in 2005 from the Department of Optical Engineering, Zhejiang University, Hangzhou, China, where he is currently working toward the Ph.D. degree.

From September 2008 to September 2009, he was with the Department of Information Technology (INTEC), Ghent University, Ghent, Belgium. His current research interests include silicon-based integrated components and their heterogeneous integration with III–V materials.

**Dries Van Thourhout** received the Master's degree in applied physics and the Ph.D. degree in electrical engineering from Ghent University, Ghent, Belgium, in 1995 and 2000, respectively.

From October 2000 to September 2002, he was with Lucent Technologies, Bell Laboratories, New Providence, NJ, where he was engaged in the design, processing, and characterization of InP/InGaAsP monolithically integrated devices. In October 2002, he joined the Department of Information Technology (INTEC), Ghent University, where he is currently a member of the permanent staff of the Photonics Group and is also a Lecturer or a Colecturer for four courses within the Ghent University Master in Photonics Program (Microphotonics, Advanced Photonics Laboratory, Photonic Semiconductor Components and Technology). He is also engaged in coordinating the cleanroom activities of the research group. His research interests include the design, fabrication, and characterization of integrated photonic devices, including silicon nanophotonic devices, heterogeneous integration of InP-on-silicon, and integrated InP-based optical isolators. He is also engaged in research on the development of new fabrication processes for photonic devices, e.g., based on focused ion beam etching and die-to-wafer bonding. He has authored or coauthored more than 60 journal papers, and has presented invited papers at several major conferences.

Dr. Thourhout is a member of the IEEE Photonics Society[formerly known as IEEE Laser and Electro-Optics Society (LEOS)] and an Associate Editor for the IEEE PHOTONICS TECHNOLOGY LETTERS.

**Ludwig Moerl** received the Diploma in physics from the University of Stuttgart, Stuttgart, Germany, in 1972, and the Ph.D. degree in physics from the Technical University (TU) of Berlin, Berlin, Germany, in 1984.

During 1981–1984, he was with the Fritz-Haber-Institut/Max-Planck-Gesellschaft, investigating surface-enhanced Raman scattering from metal electrodes. In 1985, he joined the Fraunhofer-Institut für Nachrichtentech-nik, Heinrich-Hertz-Institut, Berlin, where has been engaged with the research of optoelectronic devices based on InP. His current research interests include fabrication and characterization of lasers, photodiodes, modulators, and spot-size convertors and in hybrid integration.

**Jochen Kreissl** received the Diploma in physics from the University of Leipzig, Leipzig, Germany, in 1976, and the Ph.D. degree on solid-state physics from the Humboldt University of Berlin, Berlin, Germany, in 1982.

From 1976 until 1996, he was engaged in the field of defect and impurity identification in semiconductor materials by electron paramagnetic resonance. Since 1997, he has been engaged in research and development of photonic integrated circuits at the Fraunhofer-Institut für Nachrichtentech-nik, Heinrich-Hertz-Institut, Berlin. His current research interests include technology of lasers, modulators, and SOA's based on InP.

**Behnam Sedighi** received the Ph.D. degree from Sharif University of Technology, Tehran, Iran, in 2008.

He was with KavoshCom, Iran, as a Senior Designer and with UMC, Taiwan, as a Ph.D. Intern working on high-speed analog integrated circuits and data converters. Since 2009, he has been with IHP, Frankfurt (Oder), Germany, where he is engaged in broadband ICs for optical communications.

**Johann-Christoph Scheytt** (S'96–M'01) received the diploma degree (M.Sc.) in electrical engineering and Ph.D. degrees (with highest honors) both from Ruhr University, Bochum, Germany, in 1996 and 2000, respectively.

In 2000, he cofounded advICo microelectronics GmbH, a German IC design house. For 6 years he served as CEO at advICo where he was responsible for various projects in the area of wireless and fiber-optic IC design. Since 2006, he has been with the Joint Laboratory of Silicon Photonics, IHP Microelectronics Technology, Frankfurt (Oder), where he is currently the Head of Circuit Design Department, a group of about 30 researchers working on high-frequency and broadband IC design. He has authored and coauthored more than 40 papers and holds 8 patents. His research interests include radio frequency IC and broadband IC design, phase-locked loop techniques, and design with SiGe BiCMOS technologies.

**Annachiara Pagano** was born in Torino, Italy in 1970. She received the Diploma in physics from University of Turin, Torino, in 1994.

Since 1994, she has been with the Transport and OPB Innovation Department, Telecom Italia (formerly CSELT), Torino, where she is currently engaged in optical fibre optics and dense wavelength division multiplexing metro and long distance communication systems. Her research interests include next-generation optical networks, focusing both on high capacity network design and testing, and carrier–class metro Ethernet, together with research activities on optical transmission issues in the "innovation, engineering, testing/transport and OPB group" at Telecom Italia. She has authored and coauthored more than 40 technical publications covering design and testing aspects of optical components and systems. She has also been involved in several European Projects.

**Emilio Riccardi** was born in Torino, Italy in 1966. He received the Diploma in physics from University of Turin, Torino, in 1991.

Since 1992, he has been with the Transport and OPB Innovation Department, Telecom Italia (formerly CSELT), Torino, where he is currently engaged in the nonlinear fibre propagation of digital signals. He also contributed to the development of measurement procedures for both linear and nonlinear propagation parameters, on the prototyping of fiber-based transmitters and nonlinear demultiplexers, on the design of fiber gratings and, more recently, on the analysis of dense wavelength division multiplexing (DWDM) system transmission design rules. He has also been involved in several European Projects. He is within the "Innovation, Engineering, Testing/Transport and OPB Group." His research interests include both in testing and validation of DWDM systems before their field deployment, and in scouting of optical switching, and new transmission technologies. He has coauthored more than 30 contributions to technical magazines and conferences.