The ICT-BOOM project: Photonic Routing on a Silicon-On-Insulator Hybrid Platform

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Abstract: BOOM is a photonic integration concept that aims to develop compact, cost-effective and power efficient silicon photonic components for high capacity routing functionalities. To accomplish this, flip-chip bonding and heterogeneous wafer scale fabrication techniques are employed that enable Si manufacturing with III-IV material processing. We present in this paper the second generation of BOOM devices that perform all-optical wavelength conversion, label processing and switching on SOI nano-wire boards.

I. Introduction

The huge amount of information that is being stored and exchanged for broadband applications has created real pressures in modern data centers [1]. The incorporation and interconnection of new electronic equipment for additional bandwidth and switching capability, has increased dramatically power consumption, heat dissipation and complexity. Given these limitations the penetration of photonic technology in routing industry has been unquestionable [2]. So far the main integration efforts for the development of chip-scale processing systems have been either monolithic or hybrid. With InP monolithic integration, the interconnection of the different active opto-electronic components has been feasible employing one manufacturing process but with yielding issues [3]. On the other hand with hybrid integration, the combination of both III-V and silicon-based integration can be performed on a common platform scaling down size and cost [4].

In this article we present all the devices that have been fabricated within BOOM project [5] using the hybrid approach. To blend the cost-effectiveness and integration potential of silicon with the high bandwidth and processing power of InP, we apply a flip-chip bonding technique for mounting semiconductor optical amplifiers (SOAs) and Electro-absorption Modulated Lasers (EMLs) on SOI boards as well as an heterogeneous integration for wafer scale integration of PIN detectors on SOI substrates. Furthermore, we explain the fundamental operation of each component in the final high-capacity BOOM routing platform.

II. BOOM Photonic Routing Concept

The BOOM high-capacity wavelength-routing platform incorporates hybrid 160 Gb/s wavelength converters, dual EML transmitters, UDWDM photodetectors and a 4x4 wavelength cross connect. The UDWDM photodetector is used to filter out the optical labels which are transmitted together with the data signals. Specifically, the array of photodetectors is employed to transform the optically filtered signals into electrical signals. The electrical signals are subsequently delivered to the electronic sample and hold (S&H) circuit for further electronic processing. The S&H circuit is used to implement a burst-mode, electronic latching operation by extending the duration of the electrical pulse exiting the photodetector, to match the duration of the corresponding optical data burst. The electrical burst-length signal is used to gate one of the EAMs of the EML transmitter. As such the EML transmitter performs E/O conversion by transforming the electrical pulse to an optical CW envelope signal. The optical CW signal is used to feed the integrated wavelength converter to change the wavelength of the incoming data and assist the

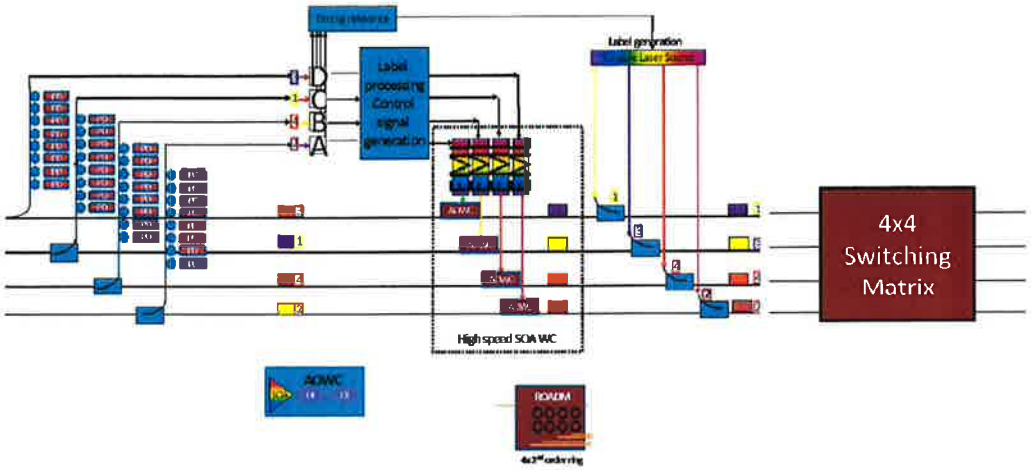

Figure 1: BOOM 4x4 optical switch detailed architecture

wavelength routing process. In the end the 4x4 wavelength cross connect is used as a switching matrix to forward packets at different output ports. Figure 1 shows all the required components for the final high capacity routing platform. Below we present the fabricated devices.

III. Flip-chip adapted SOAs

For the flip-chip adapted SOA, a buried heterostructure architecture with pn current blocking layers has been chosen. The active layer stack of the SOA yields operation in the 1550nm wavelength region: A 50nm tensile-strained ternary bulk structure embedded between 100nm quaternary material (λ_g=1.2μm) was used for active layers and a laterally tapered active waveguide was integrated on both input and output facets to serve as spot-size converter. The tensile strain value in the ternary layer was set to -0.22%. The total SOA length is 1250μm. For the horizontal alignment to the board waveguide dry etched trenches were implemented in the SOA chips as counterparts to board stand-offs.

SOA chips as depicted in Figure 2 exhibit a saturation power of 10dBm, a noise figure of 7dB, an internal single pass gain of 22dB (maximum value 25dB) and polarization sensitivity lower than 1.5dB. The ASE peak wavelength shifts from 1540nm to 1500nm for driving currents of 50mA and 150mA, respectively. The spot size converter targets at the expansion of the optical mode to result in a circle-shaped far field with an FWHM-angle of 18deg.

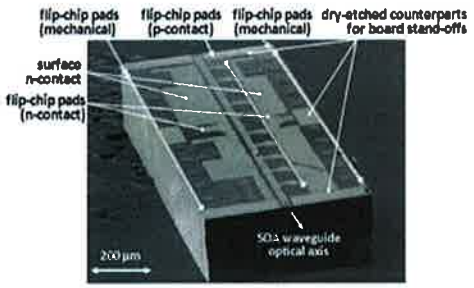

Figure 2: SEM picture of a SOA chip compatible with flip-chip mounting, after dicing.

IV. Hybrid all-optical wavelength converters

The BOOM all-optical wavelength converter consists of flip-chip adaptable SOA and two subsequent MZIs for chirp filtering and polarity inversion. The mask layout with the appropriate SOA integration zone is depicted in Figure 3. The SOA bonding technique that has been chosen is AuSn sputter technology where vertical and horizontal adjustment is performed by stand-offs and edge guides. These are fabricated on the SOI board together with suitable stand-off counterparts on the SOA chip, respectively. A pit etched into the SOI board accommodates the SOA chip so as to provide enough room for the bumps to mount. It is fabricated independently from etching the alignment features, as the necessary deep etching cannot be performed with the required precision sufficient for optical alignment, since in-situ control is not possible.

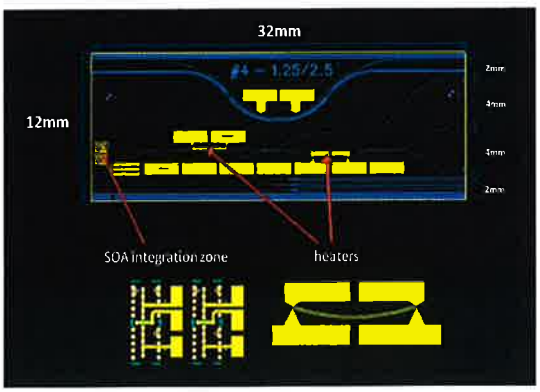

Figure 3: All-Optical Wavelength Converter Mask layout

Bump ball height after reflow is determined by the volume of the deposited Au/Sn perform and the footprint, to which the bump perform is contacting during reflow, forming a half-spherical bump ball. Together with the Au/Sn sputter thickness, an important parameter is also the relevant geometry of the processing masks laid down on the SOI board. Fabricated bump ball height of course has to be adjusted to the etch pit depth within a well defined process window, in order to assure reliable mechanical

Figure 4: SEM image demonstrating the SOA flip-chip bonded in the SOI board

bonding and electrical contact. Figure 4 demonstrates the SOA flip-chip bonded in the SOI board using the Au/Sn sputtering method and the high quality of the bumps.

V. TRIPLEX AND SOI RING STRUCTURES

Fig. 5 depicts a TriPleX™ chip that features four independent line structures, each comprising of a 2nd order micro-ring resonator (MRR) for chirp-filtering, followed by a delay interferometer (DI) for signal polarity inversion. The total footprint of the chip is 8.75mm^2 and it includes integrated heating elements that are used to spectrally adjust the MRRs and DIs. Besides its small footprint, the chip allows for the independent tuning of the spectral responses of each element in the integrated array of MMRs and DIs so that WDM-functionalities required in a routing matrix are accommodated on a single chip. Additionally the sequential MRR and DI arrayed integration on a single chip avoids pigtailing and reduces circuit losses so that no amplification is required between the MRR and the DI, resulting in a truly compact circuit. Figure 5 illustrates the mask design of the circuit.

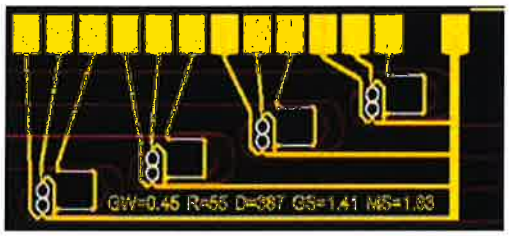

Figure 5: Mask design of the TriPleX photonic chip

The chip has been fabricated using stoichiometric silicon nitride (Si_3N_4) technology. Low-pressure chemical vapour deposition (LPCVD) processing is widely used in integrated optics because of its large refractive index (n~2.0) that enables very compact devices. By combining an additional material having a large compressive stress, such as LPCVD silicon dioxide (SiO_2), the total stress of the composite layer stack is strongly reduced. This alternating LPCVD layer stack concept can result in a rectangular channel waveguide structure with outstanding waveguiding characteristics and strong polarizing effects. This waveguide structure is formed by a cross-section of silicon nitride (Si_3N_4) filled with and encapsulated by SiO_2. The channel geometry approximates a "hollow core" system, since it consists of a low index "inner core" of SiO_2 "cladded" with the high index "outer core" of Si_3N_4. Modal characteristics depend only upon the geometry of the structure, as all composing materials are LPCVD end products with very reproducible characteristics. The whole process is CMOS-compatible, very cost-effective since only one photo-lithographical step is required, and guarantees a propagation loss of <0.1dB/cm.

The SOI micro ring resonator structures can be realized in SOI technology using electron beam lithography (EBL). A reliable fabrication process enforces an exact control about the lateral dimension of the ring resonator and the coupling distance between the resonator and the waveguides. The EBL processes used to fabricate the resonator devices are based on the use of hydrogen silsesquioxane (HSQ) as a negative tone resist material. An optimized high contrast development process with a steep resist profile and a smooth resist surface allows for a reliable pattern transfer by reactive ion etching. Thus, even challenging narrow gaps in the order of 90 nm between SOI waveguides and micro-rings can be fabricated with small tolerances (< 10%) in a reproducible manner. This enables already a 160 Gb/s operation for 3rd order racetracks without active tuning. However, MRRs of 3rd order are more sensitive to fabrication tolerances and require an additional active resonance tuning with heating elements on top of each SOI MRR. A SEM image of a 3rd order MRR is depicted in Figure 6.

Figure 6: SEM image of a 3rd order micro-ring resonator

VI. EML TRANSMITTER

Figure 7 depicts a SEM image of the BOOM EML chip that incorporates a passive spot-size expander. The electrically inactive flip-chip pads for an enhancement of adhesion are aligned in rows of six elements along the chip edges parallel to the waveguide stripe. The electrical contacts to the DFB laser and the EAM are also visible. There are five p-pads and one n-pad for the laser dc bias contacts. A large F-shaped metal area represents the surface n-contact common for all device sections. The EAM is on-chip accessible by a suitable RF probehead with two n- and one p-contact pads in GSG configuration,

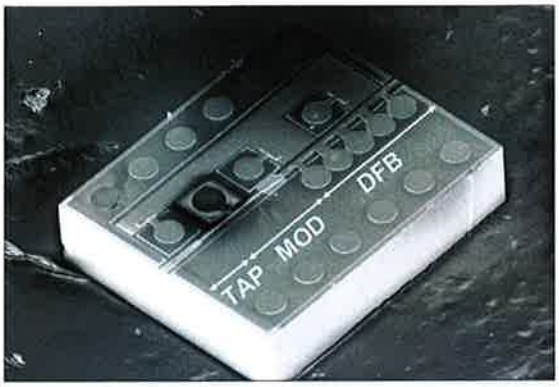

Figure 7: SEM view of a BOOM EML chip

delivering both dc bias and RF modulation signal. Two generations have already been fabricated. The first one is with pn-blocking layers and the second one with Fe-doped semi-insul (SI) InP blocking layers, both used for the waveguide cladding regrowth to achieve electrical confinement. The latter one reduces the capacitiy and allows higher bandwidth. After cleavage the EML chips are AR coated on the front facet (output waveguide with taper), while the back facet (laser waveguide) is kept as cleaved. Figure 8 illustrates a clear eye-diagram for an EML with pn-blocking at 10 Gb/s modulation driven by a PRBS 2^{31}-1 signal, fulfilling the conditions of the STM 64/OC192-standard.

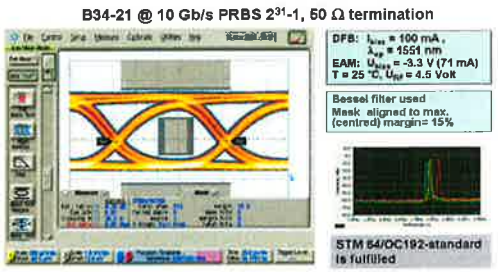

Figure 8: Experimental demonstration of EML with p-n blocking

VII. SOI Compatible Electronic Drivers

A SOI specific driver has been fabricated for EML transmitters. The driver chip has been designed for nominal 2Vpp output swing, and rise/fall time of better than 30ps. The driver has two main blocks: a) an input stage (three emitter-follower stages) acting as buffer and b) an output stage (a cascode differential pair). An on-chip spiral inductor is used to increase the bandwidth at the output node. The adjustable tail current source in the differential pair determines the output swing whereas the DC level (average output voltage) can be adjusted separately by changing a current source. The DC bias point can be adjusted in 1V range. The output voltage can change in 3V range for different settings. To avoid voltage breakdown in transistors, an adaptive biasing mechanism controls the base voltage of the output transistor such that the collector-emitter voltage always remains in the safe operation region. The designed driver was fabricated in SiGe 0.25μm BiCMOS process that provides HBT devices with a cutoff frequency (f_T) of 120GHz and breakdown voltage of V_{CEO}=2.3V. Figure 9 (a) shows the fabricated die. To check the basic functionality of the driver, on wafer measurements were performed. A PRBS generator generates the input signals for the driver and and the output pin is directly connected to a sampling oscilloscope. At target 10Gbps, the circuit works with an open eye diagram at voltage swings from 1V up to 2.4V. Figure 9 (b) shows an example of the output eye diagram. The S-parameters of the modulator were also measured with Network Analyzer and input S11 better that -20dB was observed. Power consumption of the driver is a function of output swing and DC level. Power consumption in the case similar to that of real application (EML load for driver) would be close to 0.5W.

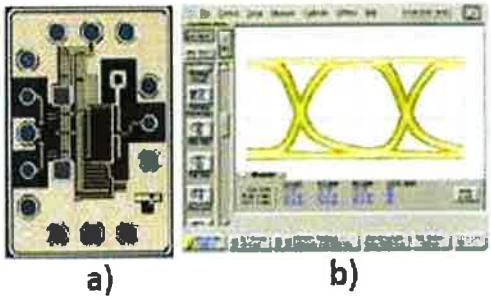

Figure 9: a) Die of SiGe Driver, b) Measured eye- diagram

VIII. UDWDM Photodetector

Figure 10 illustrates a cross-section of the fabricated PIN detectors. The size of the Si waveguide is 3μm×220nm. The III-V layer structure consists of an i-In0.53Ga0.47As layer sandwiched between a p-InP layer and an n-InP layer. All of the three layers are 100nm thick. The thicknesses of these three layers are optimized to achieve the phase matching condition for the 0th order modes as discussed above. On top of the p-InP layer, there is a 50nm-thick, highly doped p-In0.53Ga0.47As layer in order to form a good ohmic contact with the p-metal sitting above. The p-contact layers (including the p-metal and p-InGaAs layers) are only located on two sides of the SOI waveguide, in order to avoid their detrimental optical absorption of the detector mode.

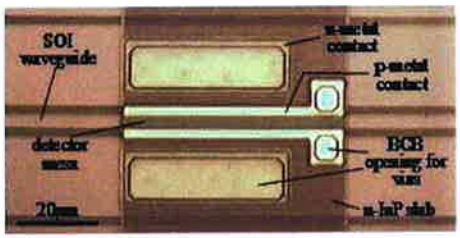

Figure 10: Top view before final metallisation

The length of the photodetectors under test was 40μm. The measured dark current under zero and 0.5V bias is around 3pA and 10pA, respectively. With higher reverse bias voltages, the dark current increases gradually but is still less than 150pA even at a reverse

bias of 10V. This value is several orders of magnitude lower than either Ge or AlGaInAs on silicon photodetectors. For the measurement of the photoresponse, TE-polarized light was coupled into the input SOI waveguides via grating couplers. The input light power varies from 6.22nW to 62.2μW in steps of 10dB. The responsivity is around 1.1A/W (corresponding to a quantum efficiency of 88%) and remains stable for a reverse bias ranging from 0V to 10V. This measured high responsivity indicates an efficient evanescent coupling between the SOI waveguide and the III-V detector layers, a negligible detrimental absorption by the p-InGaAs and p-metal layers, and a sufficient light absorption for a 40μm-long photodetector. The responsivity remains also almost constant for a power range of 40dB, indicating a good linearity and dynamic range of the photoresponse. A new generation of demultiplexers has also been designed and fabricated focused exclusively on second order ring resonators and is depicted in Figure 11. The passive devices have been fabricated using wafer scale CMOS compatible processing. The latest device under development is the integration of the novel photodetectors on top of the demultiplexer and processing of heaters on top of the rings for fine alignment.

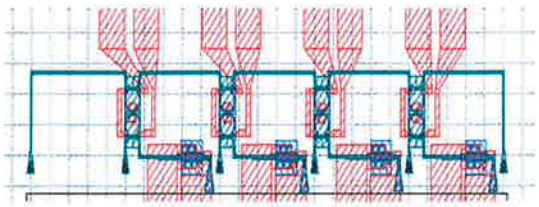

Figure 11: Mask design for demux circuits

IX. 4X4 Wavelength Cross-Connect

The final BOOM objective is to design a fully reconfigurable and ultra compact wavelength cross-connect based on two dimensional grids of micro-ring resonators. Figure 12 shows the mask design of the wavelength cross connect.

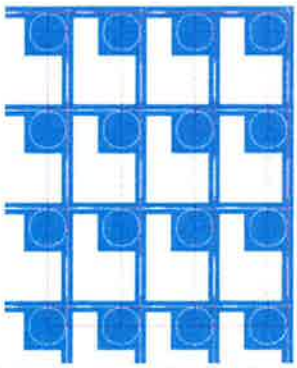

Figure 12: Core component of wavelength cross connect

One of the assets of TriPleX technology is its high fiber-to-chip coupling efficiency while in parallel, SOI technology provides strong optical confinement inside the waveguides due to the high refractive index contrast between Si and SiO_2. By combining the two technologies the best of both sides can be merged together with advanced performance with respect to insertion losses, bandwidth, and footprint. The coupling of light between an optical fiber with a mode field diameter (MFD) of 10.4 micron and a SOI waveguide with a width of 450 nm and a thickness of 220 nm experiences a loss of approximately 19 dB. By using a TripleX interposer chip that matches the MFD of the fiber on one end of the chip, and matches the MFD of the SOI chip on the other side, coupling losses can be reduced. However, a TripleX chip cannot fully bridge the gap between the MFD of the fiber and that of the proposed SOI chip. The main boundaries are formed in keeping the TripleX waveguide in the single-mode regime and by the losses to the substrate of the SOI chip that occur when this geometry is altered. Figure 13 illustrates the TriPleX structure for coupling the SOI wavelength cross-connect.

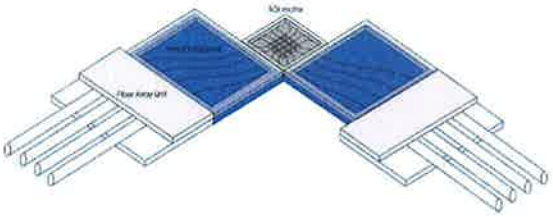

Figure 13: Scheme of a TriPleX interposer chip for adjusting the mode profile between a standard fiber and the SOI chip.

X. Conclusion

ICT-BOOM project provides a silicon photonic integration technology that enables the development of scalable, high-capacity photonic routers. A key objective is the development of a new generation of all-optical components that perform network functionalities at ultra fast line-rates up to 160Gb/s consuming less power. In this paper we have presented the second generation of devices that have been fabricated using the hybrid integration approach and we have shown how all these photonic circuits are interconnected in the final routing platform.

XI. Acknowledgment

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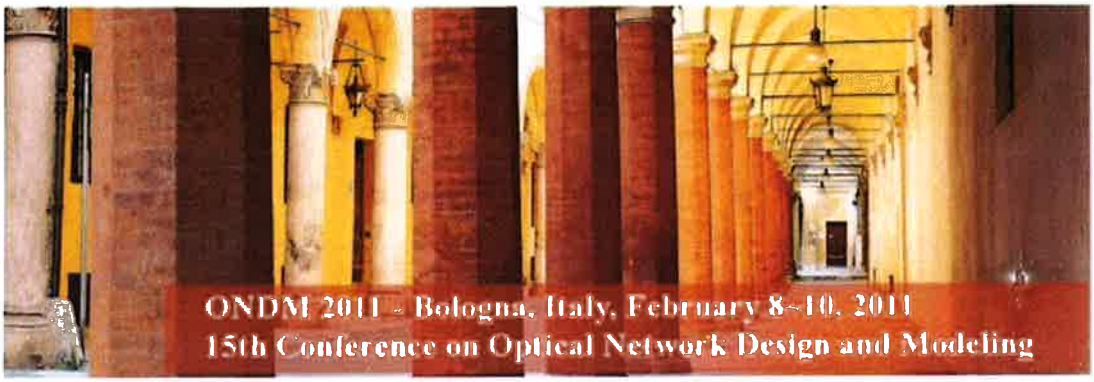

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Paolo Bolletta, Anna Del Grosso, Luca Rea, Angelo Maria Luisi, Sergio Pompei, Alessandro Valenti, Donato Del Buono

P17 *On Self-Healing for Transparent Optical Packet Switching Networks: An approach to security*
Ivan Razo-Zapata, Gerardo Castanon, Carlos Mex

P18 *Sticky 1+1 Path Protection Method by Dynamic Disjoint Path Discovery*
Shohei Kamamura, Tomonori Takeda, Takashi Miyamura, Yoshihiko Uematsu, Kohei Shiomoto

Workshop 2 - Control plane evolution in metro and core networks
Wednesday, February 09 16:00-18:20
Chair: Juan Fernández-Palacios

Workshop 2 schedule

Gala Dinner
Wednesday, February 09 20:00

Thursday, February 10 2011

Session 6 - Economic Analysis and cost/performance trade-off
Thursday, February 10 09:00-10:50
Chair: Marco Schiano

09:00 *A Customizable Two-Step Framework for General Equipment Provisioning in Optical Transport Networks (**Invited**)*
Limin Tang, Wanjun Huang, Miguel Razo, Arularasi Sivasankaran, Paolo Monti, Marco Tacca, Andrea Fumagalli

09:30 *Adapting the Transmission Reach in Mixed Line Rates WDM Transport Networks*
Kostas Christodoulopoulos, Konstantinos Manousakis, Emmanouel Varvarigos

09:50 *Optimal dimensioning of dynamic WDM networks*
Marco Tarifeño, Alejandra Beghelli, Eduardo Moreno

10:10 *Dimensioning of dynamic optical WDM networks under multi-hour traffic and soft QoS constraints*
Diego Acevedo, Alejandra Beghelli

10:30 *Traffic Re-Optimization Strategies for Dynamically Provisioned WDM Networks*
Jawwad Ahmed, Fernando Solano, Paolo Monti, Lena Wosinska

Session 7 - Optical Network Access Design and Protocols
Thursday, February 10 11:10-13:10
Chair: Brigitte Jaumard

11:10 *The ICT BOOM project: Photonic routing on a Silicon-On-Insulator hybrid platform (**Invited**)*

Christos Stamatiadis, Leontios Stampoulidis, Konstantinos Vyrsokinos, Ioannis Lazarou, Lars Zimmermann, Karsten Voigt, Ludwig Moerl, Jochen Kreissl, Behnam Sedighi, Zhen Sheng, Peter De Heyn, Dries Van Thourhout, Matthias Karl, Thorsten Wahlbrink, Jens Bolten, Arne Leinse, Rene Heideman, Fausto Gomez-Agis, H. J. S. Dorren, Annachiara Pagano, Emilio Riccardi, Hercules Avramopoulos

11:40 *Optical OFDM for ultra-high capacity long-haul transmission applications (**Invited**)*
Sander Jansen, Adriana Lobato, Susmita Adhikari, Beril Inan, Dirk van den Borne

12:10 *Wavelength Converting Optical Access Network for 10Gbit/s PON*
Bowen Cao, Darren Shea, John Mitchell

12:30 *Flexible joint scheduling DBA to promote the fair coexistence in 1G and 10G EPONs*
LLuís Gutierrez, Paola Garfias, Sebastia Sallent

12:50 *Performance Evaluation of Spectral Amplitude Codes for OCDMA PON*
Maisara Binti Othman, Jesper Jensen, Xu Zhang, Idelfonso Tafur Monroy

Session 8 - Optical Switching Performance Modeling
Thursday, February 10 14:30-16:00
Chair: Norvald Stol

14:30 *Scalability of Optical Interconnections based on the Arrayed Waveguide Grating in High Capacity Routers (**Invited**)*
Domenico Siracusa, Guido Maier, Vittorio Linzalata, Achille Pattavina

15:00 *A Comparative Blocking Analysis for Time-Driven-Switched Optical Networks*
Francesca Vismara, Francesco Musumeci, Massimo Tornatore, Achille Pattavina

15:20 *Physical Layer Performance of Optical Packet Switches: a Practical Approach*
Ivan Aldaya, Gabriel Campuzano, Joaquin Beas, Gerardo Castanon, Walter Cerroni, Carla Raffaelli, Michele Savi

15:40 *Performance model for an OBS node with a shared wavelength converter pool and an FDL buffer per link*
Muhammad Hayat, Farrukh Khan, Harmen R. van As