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Photonic Integrated Circuits on SOI for Optical Fiber Communication Applications

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Optical fiber communication networks require a large amount of optical manipulation tools for transmitting, routing and receiving optical data. Although integration of photonic circuits on high index contrast platforms such as Silicon-on-Insulator (SOI) is key to decreasing the cost, size and power consumption, it is not straightforward to achieve optical performance comparable to discrete state-of-the-art components. We will present the recent advancements in realizing high performance integrated components such as fiber-to-chip couplers and polarization rotators. These components are envisioned in optical transceivers and optical routers using wavelength demultiplexing and higher-order modulation formats.

Introduction

Optical communication applications are the main driving factor for photonic integration.
Considering the required specifications, different technological requirements divide these applications into two main categories: on-chip optical interconnects and off-chip (mainly fiber based) optical interconnects.
For on-chip optical interconnections, the integration platform of choice is critical since both the electronic and optical functionalities need to be seamlessly integrated on one single chip. Furthermore, the ultra short communication distances require small footprint optical components and high bandwidth densities. There is a wide range of research investigating different material systems and architectures for on-chip optical interconnects. A candidate platform technology is the hybrid III-V/silicon photonics framework [1] which is compatible with CMOS processing and can achieve high bandwidth densities due to compact high index contrast waveguides.
The other category are the off-chip optical interconnect applications such as optical transceivers and optical routers which are not bound to any integration platform. Here, the high integration density and tight electrical integration are not the most critical factors, but are considered, if available, to be a luxurious asset. The main difference is that an optical interface between the integrated photonic circuit and the off-chip optical medium (i.e. an optical fiber) is required. This is not straightforward and becomes increasingly more challenging if we look at the more compact integration platforms. Moreover, since the polarization of the light in an optical fiber is unknown, an integrated receiver circuit has to be able to work in a polarization independent way. In order to meet internationally specified requirements, the optical loss and polarization diversity loss (PDL) needs to be sufficiently minimized.
In this paper we will focus on the integration of Silicon-on-Insulator (SOI) optical components and circuits which are specifically developed for optical fiber

communication applications such as Fiber-To-The-Home (FTTH) transceivers, wavelength division multiplexing (WDM) routers and active optical cables.

High-Efficiency Fiber-To-Chip Grating Couplers

Subwavelength structured surfaces such as line gratings or photonic crystals are a very elegant way to tackle the interfacing problem between a SOI chip and an optical fiber. With these grating couplers one can couple out-of-plane and thus test photonic circuits on a wafer-scale without the need of any post-processing or cleaving. Furthermore because of a relaxed 1dB alignment sensitivity of 2µm, it is even possible to align several optical fibers at the same time by using fiber arrays for wafer-scale testing or packaging. Despite the fact that these grating couplers are a very good candidate for fiber interfacing for the low cost and high volume oriented silicon photonics framework, they suffer from relatively high coupling loss, making them only useful for research purposes or specific applications with a relaxed power budget. Recently however, we demonstrated grating couplers with a coupling efficiency up to -1.6dB by using a silicon overlay [2] (see Figure 1). This is the highest fiber coupling efficiency achieved for grating couplers fabricated in a CMOS pilot line.

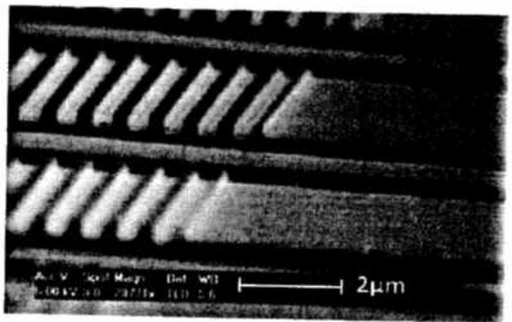

Figure 1: Bird's eye view of a silicon overlay grating fiber coupler.

High-Efficiency Broadband Polarization Rotator

In Figure 2 an artist's impression is shown of a highly directional grating coupler and a polarization rotator on SOI. The polarization rotator design is based on symmetry breaking of a single-mode waveguide with an almost square waveguide profile. A vertical taper, defined in the silicon overlay, is used as an adiabatic transition between a 450nm wide Si waveguide with a height of 220nm and an equally wide waveguide with a silicon overlay. This double patterned strip waveguide has a combined thickness of 380nm and is formed by 220nm crystalline silicon, a thin layer of silicon oxide and 160nm of polycrystalline silicon. The actual polarization rotator is formed by an asymmetric shallow etch of 70nm in a 355nm wide waveguide with silicon overlay.
Maximum conversion efficiency is only possible when a TE/TM polarized fundamental mode couples equally to both 50% TE/TM polarized fundamental modes of the asymmetrical waveguide at the symmetric-asymmetric waveguide interface. At the conversion length L_c of 8µm, both asymmetrical hybridly polarized waveguide modes will couple to the fundamental TM-mode in the output waveguide when a TE mode is launched (and vice versa when a TM mode is launched) at the asymmetric-symmetric waveguide interface and hereby obtaining polarization conversion. The short conversion

length is a consequence of the large difference in propagation constants of the two beating modes in the asymmetric waveguide and results in a large optical polarization conversion efficiency bandwidth. The efficiency is expressed in terms of polarization conversion efficiency (PCE), defined by PCE = P_{TM} = (P_{TE} +P_{TM}), where P_{TM} and P_{TE} are respectively the powers coupled into the TE/TM polarized output modes. A high polarization conversion efficiency of -0.5dB was measured over a broad wavelength range of 80nm.

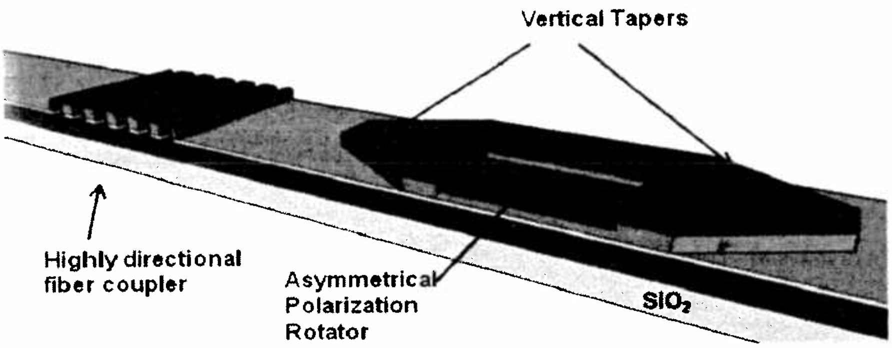

Figure 2: Artist's impression of a highly directional fiber coupler and asymmetrical polarization rotator fabricated within the same process flow. (Dimensions are not to scale).

Tunable Wavelength Router

Here, we present a compact Silicon-on-Insulator wavelength router, capable of dynamic wavelength allocation and sharing between different users, which employs a novel polarization diversity approach to minimize polarization dependence loss at the transmission wavelengths [4]. It uses thermally adjusted ring resonators to dynamically assign and share wavelengths among four users. The device simultaneously routes a data wavelength and an unmodulated carrier (for user modulated upstream data) to each user. The spectral response and schematic picture of the device is shown in Figure 3. The PDL at the transmission wavelengths was successfully reduced to well below 0.5dB using a novel polarization diversity scheme with two-dimensional grating fiber couplers and a 180° phase shifter.

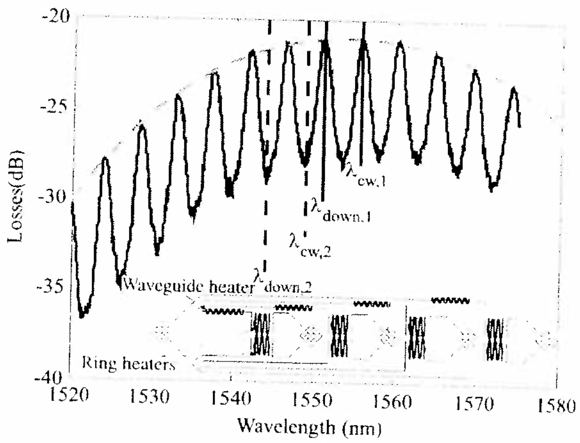

Figure 3: Measured spectral response of the wavelength router with all heaters turned OFF. The dashed envelope indicates the overall efficiency of the two 2-D grating couplers. A schematic of the device is shown in the inset.

Conclusion

Off-chip optical interconnects using Silicon-on-Insulator as an integration platform is becoming more mature and is reaching the required specifications regarding the optical link budget and polarization diversity loss (PDL). We have demonstrated high-efficiency fiber couplers using a silicon overlay to enhance the directionality of the light. Broadband and highly efficient polarization rotators are demonstrated, enabling polarization diversity circuits by means of horizontal couplers. Furthermore, we have used 2D polarization splitting grating couplers in a wavelength demultiplexing router, hereby achieving a PDL well below 0.5dB.

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References

[1] Günther Roelkens, Liu Liu, Di Liang, Richard Jones, Alexander Fang, Brian Koch, and John Bowers, "III-V/silicon photonics for on-chip and inter-chip optical interconnects," Laser & Photonics reviews, p.DOI: 10.1002/lpor.200900033, 2010.

[2] D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, and G. Roelkens, "High-efficiency silicon-on-insulator fiber-to-chip grating couplers using a silicon overlay," 6th IEEE International Conference on Group IV Photonics, 2009.

[3] D. Vermeulen, S. Selvaraja, W. Bogaerts, G. Roelkens, High-efficiency broadband CMOS-compatible polarization rotator on SOI, Group IV photonics, China, p.WC6 (2010)

[4] R. Halir, D. Vermeulen, G. Roelkens, Reducing polarization dependent loss of silicon-on-insulator fiber to chip grating couplers, IEEE Photonics Technology Letters, 22(6), p.389-391 (2010)