Photonic integrated circuits in Silicon-on-Insulator

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Silicon Photonics has gathered a substantial momentum over the past years: The combination of silicon as a good optical waveguide material with the extremely good processing technology for integrated electronics has enabled breakthroughs for integration of many photonic functions on a single chip.

Silicon is a good optical waveguide material for two reasons: it is transparent for the common telecom wavelengths of 1310nm and 1550nm. Also, it has a very high refractive index (n = 3.45). This makes it possible to create optical waveguides with submicron core dimensions that exhibit very strong confinement of light. A typical 'photonic wire' waveguide has a silicon core of 450nm width by 220nm height, surrounded by a cladding of air (n = 1.0) or silica (n = 1.45) [1]. The footprint of photonic integrated circuits is largely determined by the bend radius of the waveguides, and silicon 'photonic wires' can reduce the bend radius from millimeter-scale to micrometer-scale. This shrinks the circuit's footprint, but also enables integration of more functions onto a chip.

PHOTONIC WIRE WAVEGUIDES

The most commonly used material for photonic wire waveguide circuits is Silicon on Insulator, because it provides a high-index core layer and an optical insulation layer to the silicon substrate. The required layer thickness for the silicon and the buried oxide can vary somewhat, but for the typical wire thickness of 200-250nm (where the silicon layer supports only a single guided optical 'mode'), a buried oxide of at least 2um is required. Otherwise the light in the waveguide layer will gradually leak into the high-index silicon substrate.

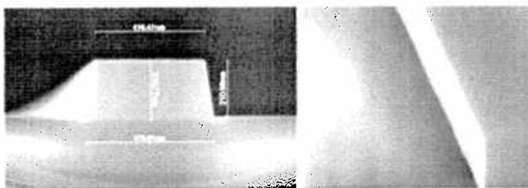

Figure 1: Photonic wire waveguide core cross section and sidewall

In *imec*, we fabricate photonic waveguide structures in 200mm SOI wafers with a 220nm silicon and 2μm buried oxide layer [2]. Circuit patterns are defined using an ASML PAS5500/1100 193nm lithography scanner and transferred into the silicon using a ICP-RIE etch with Br/Cl based chemistry. The silicon layer is etched completely, as can be seen in the SEM in Fig. 1. One of the key metrics of these waveguides is their propagation loss, which is mainly attributed to sidewall roughness and absorbing surface states. By optimizing the etch process we have reduced the propagation loss to 1.36dB/cm. The propagation losses are measured using spiral waveguides of 1-7cm length (see Fig. 2).

We can reduce the losses further if we define 'rib' waveguides which are only partially etched (70nm into the 220nm core). While such waveguides have a lower confinement (and cannot bend as tightly), they also have less sidewall surface. We have shown losses in rib waveguides as low as 0.27dB/cm, which make circuits of tens of cm feasible.

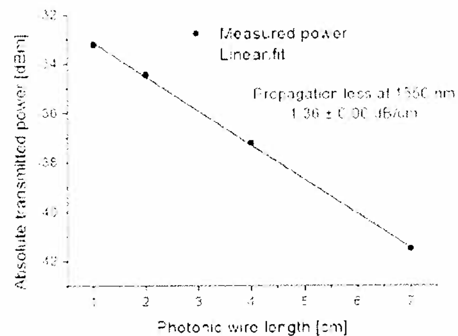

Figure 2: Photonic wire waveguide loss as measured on 4 spiral waveguides of different length

FILTERS AND TOLERANCES

One of the most common functions on a photonic integrated circuit is wavelength filtering: certain wavelengths of light are dropped into another waveguide. Such filters can be used in sensors or in optical communication networks, where signals are transported onto different carrier wavelengths.

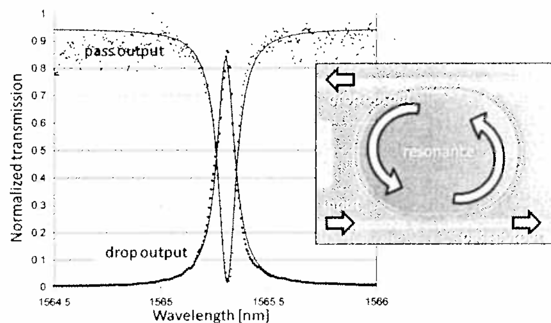

Figure 3: Ring resonator. When the wavelength fits inside the ring, the signal is dropped to the top output.

Such filters are based on (self-)interference, where light is either distributed over different delay lines, or recycled in a resonator. In both cases, control the exact optical path length is extremely important to select the correct wavelengths. The optical path length is determined not only by the actual path length, but also by the waveguide geometry: variations of 1nm on the core width or thickness can easily result in a >1nm shift in filter wavelength. Therefore, fabrication tolerances are extremely strict, of the order of 1% in both layer thickness and critical dimensions. While CD variations can be compensated on the chip by active tuning mechanisms (e.g. heaters), the required tuning power will go up dramatically with poor CD control.

In *imec*, we have optimized our process to a limit where we can control the average linewidth of a 450nm wire within 1nm within a die, within 2-3nm within a wafer and within 3-4nm between wafers [3]. While it is difficult to assess this uniformity with traditional means, optical transmission spectra of ring filters give a very accurate measurement of the *average* linewidth. This is shown in Figure 4, where we plot the transmission of a set of ring resonators on 11 dies over a wafer. We see that the spread of the peak wavelength falls within a 4nm window.

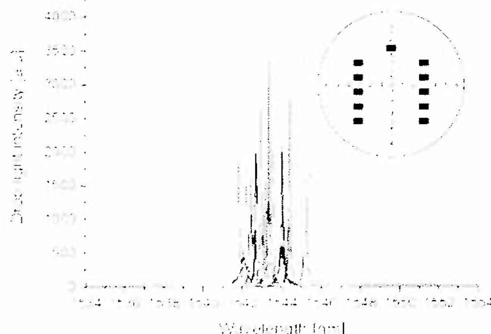

Figure 4: Uniformity of spectra of 3 identical ring resonator drop filters on 11 dies over a wafer

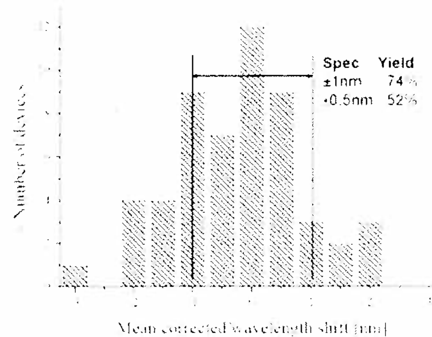

Figure 5: Yield of ring resonator drop filters for different specifications of untuned drop wavelength

DEPOSITED SILICON WAVEGUIDES

One of the drawbacks of using SOI for waveguides is the limitation of the available substrates. For more flexibility, we explored deposited silicon films. Polycrystalline silicon films have similar bulk properties as monocrystalline silicon, but the grain boundaries can cause optical scattering, as well as absorption at surface states. Therefore, we developed a PECVD process for amorphous silicon waveguides [4]. While there are no scattering grain boundaries, careful passivation of dangling bonds is required to keep the absorption loss in check. Therefore, we used in-situ Hydrogen passivation during deposition. These amorphous silicon waveguides show propagation losses which are higher than those of their crystalline counterparts: wires have losses of 3.4dB/cm, while rib waveguides have a loss of 1.4dB/cm. This indicates an additional film loss of around 1dB/cm. These deposited films give a much greater flexibility in layer thickness as well as in substrates: a-Si waveguides can easily be deposited on top of electronics, which is attractive for optical interconnect applications.

SUMMARY

We show a platform for silicon photonic circuits in silicon-on-insulator. In crystalline silicon waveguides have very low propagation losses and at the same time extremely good uniformity, which is essential for high-quality wavelength filters. Also, we can use deposited amorphous material to fabricate similar devices on top of any substrate (including CMOS) with only a small penalty in performance.

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8.03 Field Effect Resistor, A Single-Device-At-Pad Solution for Esd Protection In Deeply Scaled Soi Technology

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8.04 ESD Robustness of FDSOI Gated Diode for ESD Network Design: Thin or Thick BOX?

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8.05 High Temperature RF Behavior of SOI MOSFET Transistors for Low Power Low Voltage Applications

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SESSION 9 OPT[illegible]VICES, SENSORS, and HIGH VOLTAGE DEVICES

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9.01 Hybrid Silicon Lasers: Integration of III-V and Silicon Photonics Using Wafer Bonding

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9.02 Photonic Integrated Circuits in Silicon-on-Insulator

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9.03 Integrated Radiation Image Sensors with SOI Technology

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9.04 Disruptive Ultra-Low-Power SOI CMOS Circuits towards µW Medical Sensor Implants

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9.05 Impact of Back-Gate Biasing on Ultra-thin Silicon-On-Insulator-Based Nanoribbon Sensors

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9.06 Ultra Low Power, Harsh Environment SOI-CMOS Design of Temperature Sensor Based Threshold Detection and Wake-Up IC

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9.07 Single Trench Isolation for a 650 V SOI Technology with Low Mechanical Bow

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SESSION 10 [illegible]

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10.01 SOI-Enabled Three-Dimensional Integrated-Circuit Technology

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