Invited Paper

The BOOM project: A new Generation of Photonic Routing Subsystems using Hybrid Integration on Silicon-on-insulator Waveguide Boards

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ABSTRACT

The European BOOM project aims at the realization of high-capacity photonic routers using the silicon material as the base for functional and cost-effective integration. Here we present the design, fabrication and testing of the first BOOM-generation of hybrid integrated silicon photonic devices that implement key photonic routing functionalities. Ultra-fast all-optical wavelength converters and micro-ring resonator UDWDM label photodetectors are realized using either 4um SOI rib or SOI nanowire boards. For the realization of these devices, flip-chip compatible non-linear SOAs and evanescent PIN detectors have been designed and fabricated. These active components are integrated on the SOI boards using high precision flip-chip mounting and heterogeneous InP-to-silicon integration techniques. This type of scalable and cost-effective silicon-based component fabrication opens up the possibility for the realization of chip-scale, power efficient, Tb/s capacity photonic routers.

Keywords: Silicon-on-insulator, hybrid integration, photonic integrated circuits, silicon photonics, photonic routers, all-optical wavelength converters.

1. INTRODUCTION

Hybrid photonic integration based on low and high index contrast PLCs is becoming more and more attractive for the cost-effective fabrication of photonic integrated circuits (PICs). Silica-on-silicon and – more recently – silicon-on-insulator (SOI) have been identified as the two dominant hybrid integration platforms. Both technologies have tested their strengths with the fabrication of optical transmitters and receivers for optical transport and datacom networks. In this context silica-on-silicon integration has been employed for the demonstration of CWDM detectors [1] and QPSK transmitters [2], whereas CWDM transmitters [3, 4], coherent receivers [5, 6] and photonic interconnects [7] have been integrated on SOI substrates. Now more demanding routing applications are in the center of attention and hybrid

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Integrated optical signal processing devices have been reported including all-optical wavelength converters (AOWCs) [3], burst-mode regenerators [8], recirculating buffers [9] and optical flip-flops [10, 11]. These PICs have been used in proof-of-concept subsystem-level experiments and now the next logical step is the development of a fully functional, 1b/s capacity hybrid photonic routing system [12].

In this paper we describe how the European BOOM project is using silicon in order to provide a new generation of photonic routing sub-systems that will be employed to assemble the first 640 Gb/s silicon photonic routing platform. We present the two hybrid integration technologies developed within the project, i.e. an efficient flip-chip bonding technique for mounting high-performance semiconductor optical amplifiers (SOAs) on SOI substrates and the heterogeneous integration process for wafer-scale integration of PIN detectors on SOI nanowire boards. Finally, we demonstrate the fabrication and testing of key components such as ultra-fast AOWCs and micro-ring resonator based UDWDM photodetectors. The first steps towards the demonstration of the silicon photonic routing concept have been completed.

2. 4um SOI RIB WAVEGUIDE TECHNOLOGY

2.1 Waveguide geometry and hybrid integration process

The fabrication of high-performance hybrid PICs on silicon requires an optical board technology capable to offer low waveguide losses, high fiber-to-waveguide coupling efficiency and optimum waveguide-to-active component on-chip coupling. For optical signal processing devices, these attributes will ensure efficient photonic packaging and the minimum possible degradation of the injected optical data signals. The BOOM project relies on the 4um SOI PLC technology for the fabrication of ultra-fast all-optical wavelength converters. The technology offers insertion losses < 0.5 dB/coupling facet, low waveguide losses (~0.1 dB/cm) and excellent mode matching between 4 um waveguides and active InP chips such as SOAs. Figure 1a) shows the cross section of the waveguide geometry. Single mode rib waveguides are used for guiding the light. A typical single-mode rib waveguide features a rib height (h) of 2um, a rib width (W) of 3.2um and a silicon height (H) above the Buried Oxide (BOX) of 4um. Figure 1b) illustrates the layout of flip-chip integration on a 4um SOI PLC. The technique exploits the existence of the BOX which acts as an alignment plane in the y-direction. The alignment along the x-axis is controlled by alignment masks. The SOI board is divided in three planes. The top silicon layer which contains the waveguide components and standoffs, the BOX and a third plane realized by deep etching through the BOX into the silicon substrate which contains the solder bumps for the mechanical and electrical connection of the active component.

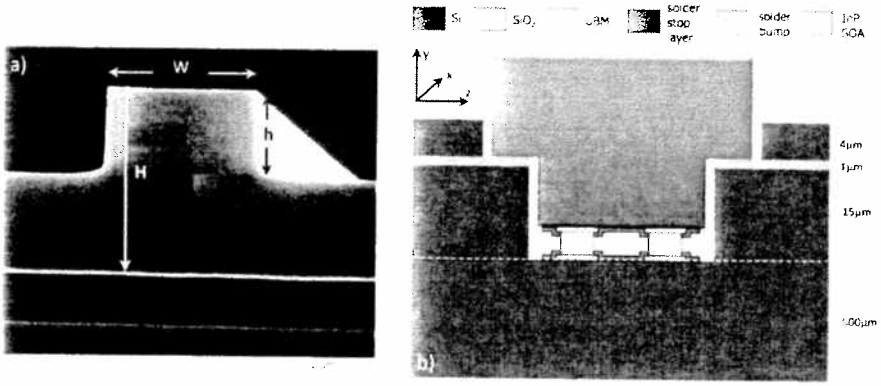

Figure 1. a) 4um SOI rib waveguide cross-section, b) layout of flip-chip integration on SOI.

2.2 SOI-delayed interferometer 160 Gb/s all-optical wavelength converter

The BOOM ultra-fast AOWC concept is based on the chirp filtering technique [13]. The scheme requires a single SOA, an optical filter and a delayed interferometer (DI). We propose a new integrated implementation of the scheme by realizing both the filter and the DI as cascaded SOI Mach-Zehnder periodic structures. Figure 2a) shows the layout. The SOA is used for the non-linear processes: it induces chirp in the converted probe signal due to the refractive index modulation caused by the pulsed pump signal. The first SOI-MZI filter is slightly detuned with respect to the probe

wavelength and by filtering the blue (fast) chirp the acceleration of the effective recovery time of the system is achieved. The second SOI-MZI filter is employed to restore the polarity of the optical pulses. The differential delays of the MZIs are 1.25 and 2.5 ps respectively yielding a free spectral range (FSR) of 6.4 and 3.2 nm respectively. Given the periodicity appeared on this comb-like filter structure, a high-speed optical packet injected in this AOWC can be converted on any of the CW wavelengths that coincide at a specific peak of the periodic response. Figure 2b) (left) shows the device blueprint. This includes the two cascaded MZIs and a test MZI structure (upper part of the layout) used as a reference. For optimum performance, integrated heater elements are included on-chip for tuning each of the MZIs separately. Figure 2b) (right) shows the SOA integration area with the probe pads being 200x300 um^2 in size. Figure 2c) (left) shows the fabricated SOI chip. All optical functionality is realized by a single etch step. The rib definition is performed using standard contact lithography and reactive ion etching. Multi Mode Interference (MMI) couplers are used for the input and output coupling stages at the two MZIs. Additional etching and metallizations are implemented for hybrid integration of the SOA. The realized mode size (~ 4μm) enables high coupling efficiency to lensed fibers and III-V devices (~ 0.5 dB loss per facet). The total size of the chip (including the test structure) is 12x32 mm^2. Figure 2c) (right) shows a close up of the integrated heater surrounding the bend waveguide of the first MZI.

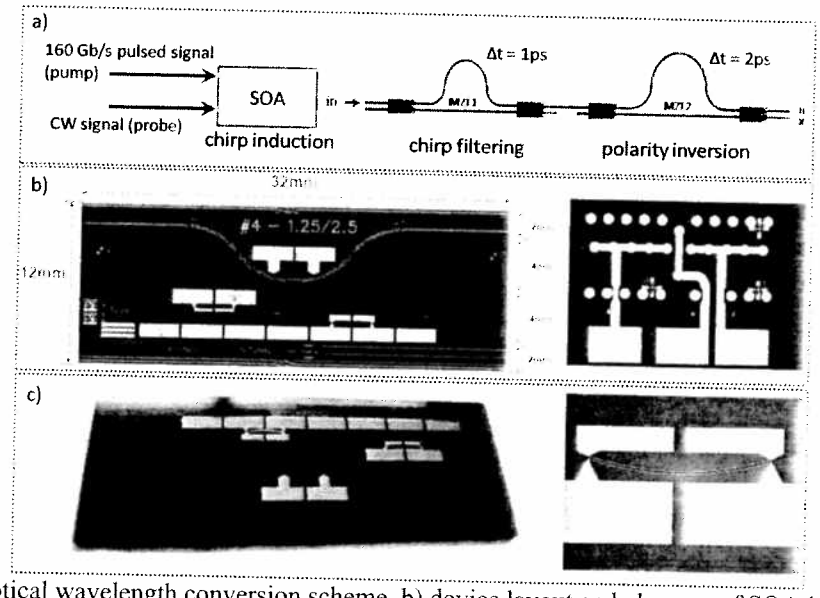

Figure 2. a) All-optical wavelength conversion scheme, b) device layout and close up of SOA integration area, c) fabricated SOI-DI chip and close-up of integrated heater element.

The SOI chip has been tested in combination with a fiber-pigtailed 40 Gb/s commercial SOA in a 160 Gb/s wavelength conversion experiment. A data stream of 160 Gb/s RZ data at 1556.3 nm is injected into the SOA together with a CW light at 1546.6 nm. The Cross-Phase Modulation (XPM) effect results to a wavelength converted inverted signal at the output of the SOA (figure 3a). This signal passes through the SOI chip where chirp filtering and pulse polarity inversion takes place. Figures 3b) and 3c) show the inverted 160 Gb/s wavelength converted stream and a 40 Gb/s demultiplexed channel respectively. The results indicate successful wavelength conversion with effective system recovery within the 160 Gb/s bitslot. In terms of electrical power consumption, the SOI-DI AOWC scheme consumes approximately 2 W, including the power for driving the SOA, the power to tune the FSR of the two MZIs and the power consumed by the TEC. This is less than half the power consumed by a 40 Gb/s commercial all-optical SOA-MZI wavelength converter.

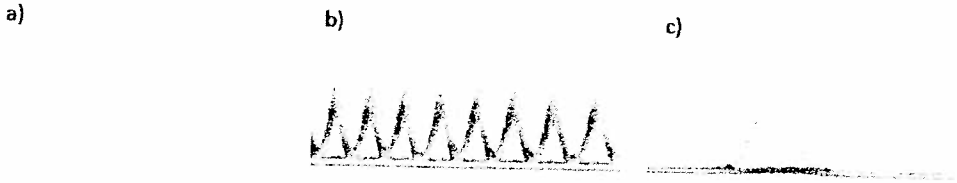

Figure 3. Eye diagrams at a) SOA output, b) SOI chip output and c) 160-to-40 Gb/s demultiplexer

2.3 SOA-on-SOI hybrid integration

In order to have the first fully operational silicon photonic wavelength converter on a single chip, the hybrid integration of the SOAs on the silicon board is required. The work is in progress and here we present the first SOA bonding results. SOA chips suitable for flip-chip mounting were fabricated (figure 4a) as well as SOI motherboards that contain bumps, vertical alignment stands, contact lines for SOA driving and waveguides (figure 4b). The SOA flip-chip bonding processes were carried out using a high precision flip chip bonder (FC150). Figure 4c) and d) shows the SEM inspection of the bonded SOA chips. The inspection reveals alignment precision down to the micron level on all three axes and the absence of any tilt from the assembly. These results indicate that the SOAs can be successfully integrated hybridly on the SOI AOWC boards and the final run for generating the fully integrated devices are underway.

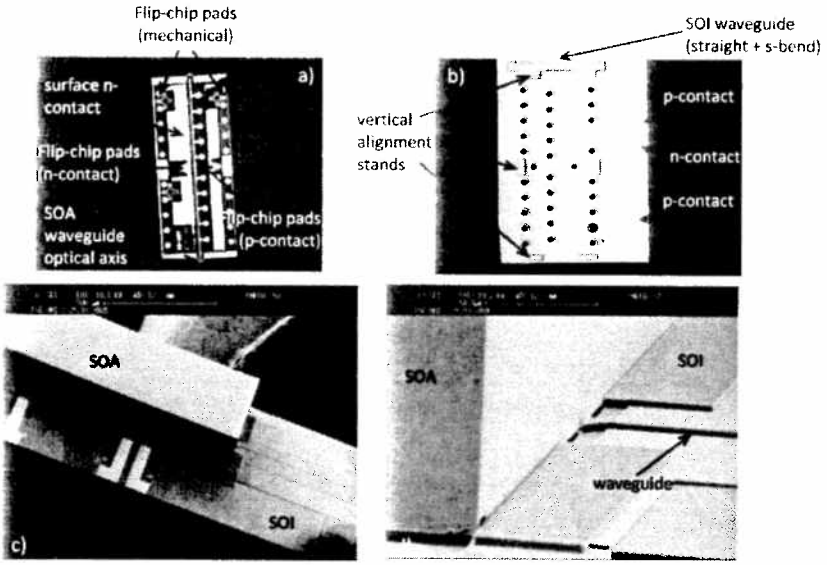

Figure 4. a) Flip-chip compatible SOA, b) SOI motherboard with AuSn bumps for hybrid integration, c), d) SOA mounted on SOI waveguide substrate.

3. SOI NANOWIRE TECHNOLOGY

3.1 SOI nanophotonics and heterogeneous InP-to-silicon integration

SOI nanowires represent a technology platform that enables CMOS compatible fabrication of nano-photonic circuits. Nanowires are implemented as strip waveguides with typical cross-section of 450×220 nm^2. The small waveguide dimensions combined with the high index contrast SOI material enables very sharp bends and consequently the fabrication of ultra-compact add-drop filters in the form of micro-ring resonators [14]. The BOOM project relies on the cascading of high-order micro-ring resonators in order to realize filtering of dense wavelength division multiplexed optical labels. For the electrical detection of labels, BOOM employs the heterogeneous integration technique for integrating PIN detector arrays on the micro-ring resonator demultiplexer chip. Figure 5 illustrates the basic fabrication steps to be followed for the fabrication of the UDWDM photodetector. The process involves the bonding of unprocessed III-V dies on the SOI substrate and the removal of the III-V substrate through mechanical and chemical processing. Subsequently the photodetectors are fabricated through wafer-scale processing and are lithographically aligned to the underlying SOI waveguides.

3.2 UDWDM label photodetector on SOI

The BOOM packet labeling technique is based on the concept of in-band optical labels [15]. This technique involves the insertion of low rate optical labels that are modulated on a sub-carrier wavelength within the broad spectrum (~5nm) of the 160 Gb/s packet signal. In order to have a large amount of label patterns available and support a large number of ports in the optical router, the labels should be placed as densely as possible into the packet spectrum. This requires an UDWDM detection unit inside the router, to isolate and detect each one of the attached labels. The target here is to

achieve a label channel spacing of 12.5 GHz, which means that up to 50 optical labels can be inserted in the 5 nm data spectrum. In the BOOM router the UDWDM demultiplexer is realized with Si/SiO_2 cladding based ring resonators due to the strong confinement of the light into the waveguide that enables the implementation of filters with very high Q factors. The micro-ring resonators were designed to have a bending radius of 17 μm, resulting in a FSR of 5.5 nm. The latter is determined by the channel spacing of WDM-multiplexed 160 Gb/s channels which is typically 5~6 nm. Since the desired bandwidth of the resonant peak is very small in order to reduce the inter-channel crosstalk, i.e., much smaller than the 0.1 nm-channel spacing between the labels, the coupling strength should be very weak. Figure 6a) shows a 4-channel micro-ring resonator demultiplexer fabricated on a SOI wafer, using the 193nm DUV based process [14].

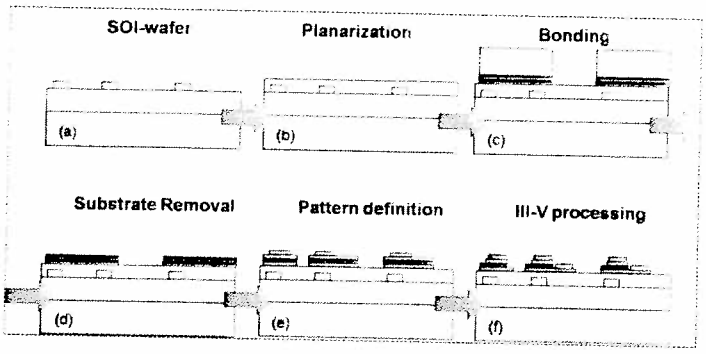

Figure 5. Heterogeneous InP-to-silicon fabrication process

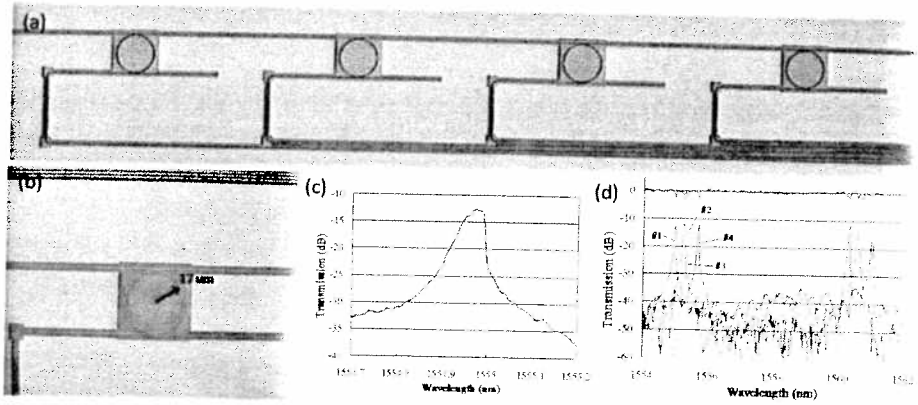

Figure 6. a) Microscopic image of a 4-channel SOI nanowire demultiplexer based on cascaded micro-ring resonators, b) close-up on single micro-ring resonator, c) measured spectral response of the drop port of a single micro-ring resonator, d) measured spectral response of the 4-channel UDWDM demultiplexer.

Figure 6c) and d) show the measurement results. The bandwidth of the drop port of a single micro-ring resonator is equal to 0.04 nm, resulting a Q factor of 40000. In addition, the FSR is about 5.34 nm which agrees well with the target specifications. The drop loss is about 12.7 dB. This corresponds to a propagation loss (α) of 14 dB/cm and a field transmission coefficient (t) of 0.9975. The estimated crosstalk is ~15 dB when applying it for the demultiplexer with a channel spacing of 0.1 nm. However it is evident that the transmission peaks of the micro-ring resonators exhibit a small misalignment due to fabrication errors. In order to compensate these fabrication errors and obtain precise channel spacing, an UDWDM demultiplexer with integrated micro-heaters for the independent tuning of the micro-ring resonators was developed. Figure 7a) shows a ring resonator with integrated microheater (100nm Ti). Thermal tuning results from this device are depicted in Figure 7b). The maximum wavelength shift of 0.8 nm, which can be achieved consuming ~18 mW, is adequate for fine tuning the spectral response of the component.

Figure 8 a) shows the cross-section view of the "Viking" detector, a new type of PIN photodetector designed for hybrid integration on the SOI nanowire demultiplexer platform. The III-V layer structure consists of an i-$In_{0.53}Ga_{0.47}As$ layer sandwiched between a p-InP layer and an n-InP layer. All of the three layers are 100 nm thick. The thicknesses of these three layers are optimized to achieve the phase matching condition for the 0th order modes as discussed above. On top of the p-InP layer, there is a 50 nm-thick, highly doped p-$In_{0.53}Ga_{0.47}As$ layer in order to form a good ohmic contact with

p-metal sitting above. The whole p-contact layers (including the p-metal and p-InGaAs layers) are only located on sides of the SOI waveguide, in order to avoid their detrimental optical absorption of the detector mode.

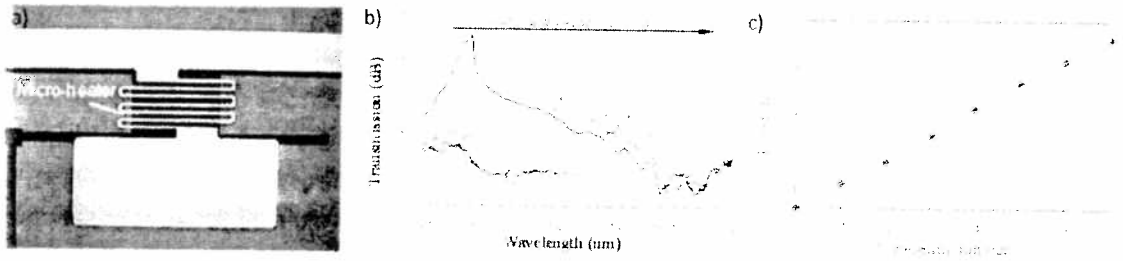

Figure 7. a) Fabricated ring resonator with integrated microheater, b) spectrum shifting vs. microheater's power, c) wavelength shift vs. microheater's power.

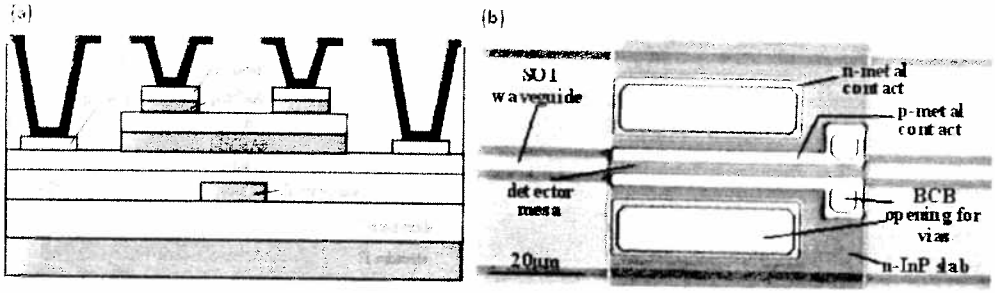

Figure 8: a) Cross-section view of fabricated detector and b) top view before final metallization

The fabrication started with the DVS-BCB die-to-wafer bonding. After bonding the III-V die onto the patterned SOI substrate, the InP substrate was removed through a combination of mechanical grinding and chemical etching. Then a pair of InGaAs/InP sacrificial layers was removed by chemical wet etching, exposing the p-InGaAs contact layer. A Ti/Au p-metal contact was deposited afterwards. This metal pattern was lithographically aligned to the underlying SOI waveguide. Subsequently, the p-InGaAs layer was etched through by using this p-metal contact layer as the etching mask. Then the detector mesa was defined by etching through the p-InP and i-InGaAs layers. The remaining n-InP layer was removed where it was not needed, e.g., on top of the access SOI waveguides and fiber grating couplers. The AuGe/Ni n-metal contact was then fabricated. A ~600 nm-thick BCB dielectric layer was spin-coated on top of the whole device, and vias were opened (with an O_2 and SF_6 plasma etching process) down to the p- and n-metal contacts. Finally, another Ti/Au layer was prepared as the metal plugs as well as the probe pads. All the etching of the III-V materials were done with wet chemistry, in order to minimize the damage to the sidewalls. Figure 8b) shows the top view of a fabricated device before the final metallization for plugs and pads.

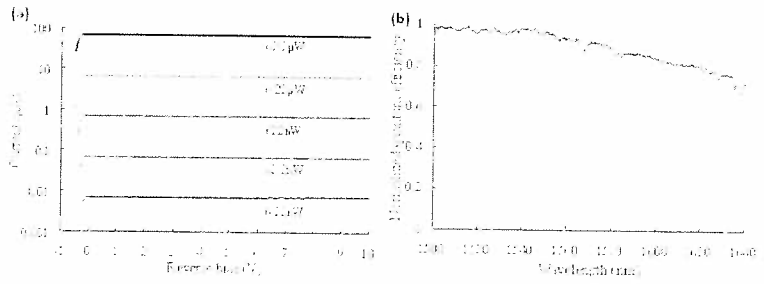

Figure 9: a) Detector response as function of reverse bias and b) wavelength dependence normalised to value at 1500nm

The performance of the fabricated detectors is summarized in Figure 9. The length of the photodetectors under test was 40μm. The measured dark current under zero and 0.5 V bias is around 3 pA and 10 pA, respectively. With higher reverse bias voltages, the dark current increases gradually but is still less than 150 pA even at a reverse bias of 10 V. This is of several orders of magnitude lower than either the Ge photodetectors [16,17] or the AlGaInAs photodetector [18] on silicon demonstrated previously. We attribute this low dark current level to the mild and noninvasive wet etching of the

i-InGaAs layer and the timely passivation of the etched sidewalls. For the measurement of the photo-response, TE-polarized light was coupled into the input SOI waveguides with the help of grating couplers. Figure 9a) shows the I-V curves under illumination at a wavelength of 1550nm. The input light power varies from 6.22 nW to 62.2 μW in steps of 10 dB. The responsivity is around 1.1 A/W (corresponding to a quantum efficiency of 88%) and remains stable for a reverse bias ranging from 0 V to 10 V. Therefore, the proposed photodetector can work well even without an external bias. This measured high responsivity indicates an efficient evanescent coupling between the SOI waveguide and the III-V detector layers, a negligible detrimental absorption by the p-InGaAs and p-metal layers, and a sufficient light absorption for a 40 μm-long photodetector. The responsivity remains almost constant for a power range of 40 dB, indicating a good linearity and dynamic range of the photoresponse. The low dark current of the present photodetector enables a reliable detection of the light power in the order of nW. Compared to previously demonstrated InAlAs–InGaAs metal-semiconductor-metal (MSM) photodetectors integrated on SOI waveguides [19], the proposed InGaAs PIN photodetectors have a lower dark current due to the larger potential barrier formed by the PIN junction than that of the Schottky junction. The required bias voltage is also lower. Figure 9b) shows the normalized quantum efficiency (QE) as a function of wavelength. Due to the large absorption coefficient of InGaAs and the efficient evanescent coupling for a wide range of wavelengths, the QE maintains over 90% of the peak efficiency up to 1580nm, and remains about 70% at the wavelength of 1640 nm. Therefore, the photodetector can work for the whole S, C and L communication band. Further improvement of the responsivity for longer wavelengths can be achieved by using a thinner BCB bonding layer or a longer device length.

4. CONCLUSION

In this paper we have presented new PICs, which can be realized using SOI hybrid integration, implementing key functionalities of high-capacity wavelength photonic routers. We have presented the SOI-DI AOWC concept – a new AOWC scheme that employs a single SOA and a SOI cascaded DI chip to perform error free 160 Gb/s all-optical wavelength conversion. In addition, we have presented the fabrication of a SOI nanowire demultiplexer consisting of cascaded micro-ring resonators that can filter out densely spaced labels from high-speed optical packets. For the electrical detection of labels we have presented the design and fabrication of PIN detectors exhibiting 1.1 A/W responsivity and dark current as low as 10 pA. These detectors are integrated on the nanowire platform using die-to-wafer bonding technique. These components can be employed to assemble a high-capacity photonic routing platform and open the possibility for a new generation of cost-effective broadband photonic systems integrated in silicon.

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