Subnanometer Linewidth Uniformity in Silicon Nanophotonic Waveguide Devices Using CMOS Fabrication Technology

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***Abstract*—We report subnanometer linewidth uniformity in silicon nanophotonics devices fabricated using high-volume CMOS fabrication tools. We use wavelength-selective devices such as ring resonators, Mach–Zehnder interferometers, and arrayed waveguide gratings to assess the device nonuniformity within and between chips. The devices were fabricated using 193 or 248 nm optical lithography and dry etching in silicon-on-insulator wafer technology. Using 193 nm optical lithography, we have achieved a linewidth uniformity of 2 nm (after lithography) and 2.6 nm (after dry etch) over 200 mm wafer. Furthermore, with the developed fabrication process, using wavelength-selective devices, we have demonstrated a linewidth control better than 0.6 nm within chip and better than 2 nm chip-to-chip. The necessity for high-resolution optical lithography is demonstrated by comparing device nonuniformity between the 248 and 193 nm optical lithography processes.**

***Index Terms*—Arrayed waveguide grating (AWG), optical lithography, photonic wire, ring resonator, silicon-on-insulator (SOI), silicon photonics, uniformity.**

I. Introduction

HIGH-INDEX contrast material technology, and especially silicon-on-insulator (SOI), is an attractive platform for making a compact and high-density photonic integrated circuit. Recently, tremendous progress has been made in reducing propagation loss and the loss of microbends [1]–[3]. Taking advantage of this development, a wide range of discrete components and integrated systems has been recently demonstrated [4], [5]. With the major focus of the silicon photonics research community on developing systems for next generation of electronics and communication systems, the actual mass manufacturability and reproducibility of these devices are seldom addressed. As silicon photonics is maturing, this issue should, however, be addressed urgently.

One of the major issues in using a high-index contrast platform such as SOI for photonic devices is its sensitivity to dimensional variations. Deviations in the width or the height of the devices will cause a proportional shift in the spectral response of these devices. These variations affect not only stand-alone devices such as rings, where they result in a shift of the resonance frequency, but also discrete parts of larger devices such as the delay arms in an arrayed waveguide grating (AWG), where they typically result in reduced crosstalk performance. By taking advantage of the thermooptic effect in silicon, thermal tuning can be employed to compensate for nonuniformity, but the power required for tuning is proportional to the as-fabricated device nonuniformity [6]. To reduce power consumption for tuning, high device uniformity is an absolute necessity.

Even though most of the silicon photonic devices are made fabricated with e-beam lithography, there is some literature addressing reproducibility issues. Barwicz *et al.* [7] demonstrated matching of two rings in a second-order ring filter with high accuracy (26 pm) using e-beam lithography. The reliability of a high-resolution e-beam resist on the device response was recently presented in [8]. Xia *et al.* [9] used e-beam lithography to fabricate optical buffers using multiple notch ring resonators, thus showing a nonuniformity of 0.46 nm. Though these papers directly or indirectly address the issue of uniformity, there are no studies yet addressing the issue in a holistic way.

In this paper, we present highly uniform silicon photonic devices fabricated using 193 nm optical lithography and dry etching in a 200 mm CMOS fabrication facility. We use an ASML PAS5500/1100 step-and-scan system for lithography and a Lam Research Versys chamber for dry etching. The desired mask pattern is replicated over a 200 mm wafer using step-and-scan lithography technique that results in nominally identical dies or chips. We have developed a fabrication process with high uniformity and tested the process on wavelength-selective devices. Using this process, we have achieved subnanometer device uniformity. Within a chip, we have achieved a nonuniformity of <0.6 nm and we demonstrated a chip-to-chip nonuniformity of <2 nm.

Reproducibility of devices within a chip, chip-to-chip, and wafer-to-wafer depends on various factors, but fabrication imperfection is one of the main causes of variation. Though the device design can be adapted to accommodate fabrication tolerances (design for manufacturability) in order to make fabrication-tolerant devices, the fabrication process limitations should be studied first.

This paper is organized as follows. In Section II, we briefly illustrate the effect of dimensional nonuniformity on integrated optical devices. A detailed introduction on different types of nonuniformity and the respective sources are presented in

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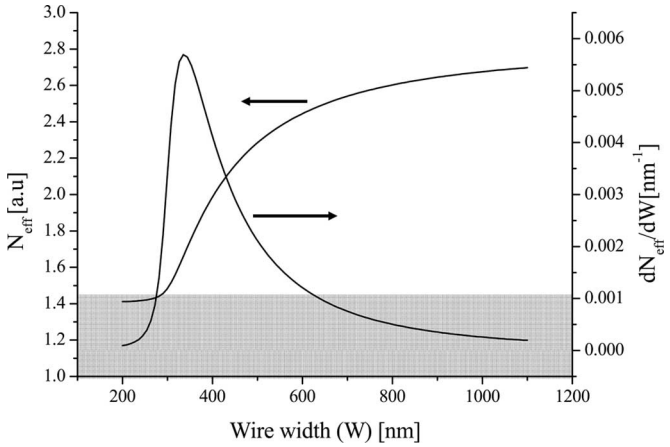

Fig. 1. Sensitivity of effective index of the TE_0 mode to photonic wire width at 1550 nm. The height of the wire is 220 nm. The gray region depicts the cutoff region.

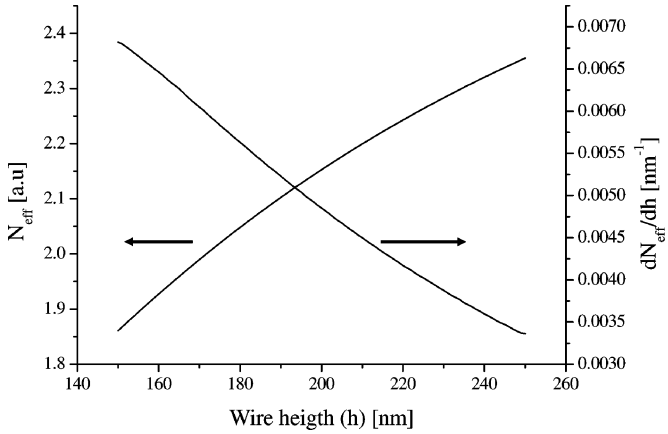

Fig. 2. Sensitivity of effective index of the TE_0 mode to photonic wire height at 1550 nm. The width of the wire is 500 nm.

Section III. In Section IV, we present the nonuniformity of the fabrication process (193 nm optical lithography and dry etch). The details about the wavelength-selective test structures and their nonuniformity are presented in Sections V and VI. In Section VII, we propose a lithography-centric adaptive process control to reduce chip-to-chip nonuniformities induced by the fabrication process over a 200-mm wafer.

II. High-Refractive-Index Platform

The high refractive index of the SOI waveguide platform can be exploited for making waveguides with very high modal confinement and micrometer scale bends allowing to shrink the size of integrated circuits by several orders of magnitude. However, at the same time, it results in a very high sensitivity to fabrication tolerances, thus making it difficult to achieve good uniformity within a device from device-to-device and from chip-to-chip.

The spectral response of any photonic-wire-based optical device depends on the effective index (N_{eff}) of the photonic wire, which is, for a given waveguide structure, fully determined by its width and height. Therefore, any change in the latter two parameters will change the effective index of the photonic wires, and as a consequence, the spectral response of the device will shift accordingly.

Using a film mode matching method, the change in the effective index as a function of the dimensions was calculated for a waveguide with nominal dimensions of 500 nm (width) $\times$ 220 nm (height). Figs. 1 and 2 show the change in N_{eff} as a function of width and height, respectively. Also, the sensitivities dN/dW and dN/dh are shown. From dN/dW, we can clearly see that around a width of 400 nm, N_{eff} is very sensitive, while at larger waveguide widths, the sensitivity is reduced. This is a consequence of the high confinement (fill factor) of the optical mode at a width of 400 nm. At the nominal waveguide dimensions, N_{eff} changes by 0.013/nm and 0.05/nm for a change in the waveguide width and height [10] corresponding to a $\approx$1 nm/nm (width) and $\approx$2 nm/nm (thickness) shift in the resonance wavelength of the devices. However, to accurately determine the resulting resonance wavelength shift for a device, the width and height changes in any device should be integrated over the length of the device. Hence, it is important to note that for uniformity, the average width and height of the devices should be matched, rather than the absolute local width and height of the devices.

III. Classification and Sources of Nonuniformity

The variations in spectral response between devices may originate from two types of sources: environmental and physical factors. Environmental factors such as temperature of the chip, input power, etc., affect the devices during operation. Physical factors during manufacturing result in structural variations that are essentially permanent. The distribution of the variation could be randomly or systematically distributed over time and space. An important goal in controlling such variation is to isolate the systematic, repeatable, or deterministic contributions to the variations.

The permanent structural nonuniformity in devices is obviously influenced by the fabrication process employed in making them. The variation in the process manifests itself across time and space. Temporal process variation is often related to drift in consumables, changes in the incoming wafers, or process conditions over time. For example, the ageing of photoresist often changes the viscosity and contrast, thereby directly affecting the printed dimensions. Temporal variation is of critical concern in a mass manufacturing environment and results in nonuniformity from wafer to wafer and batch to batch. Besides temporal variation, spatial variation over the wafer also plays an important role in nonuniformity during the fabrication process.

At the wafer level, we can separate sources of physical or structural variation into two categories: intradie and interdie(or within wafer) nonuniformity. The magnitude and distribution of variations within a die can be different from those between dies (die-to-die). Fig. 3 illustrates these variations at different levels.

Fabrication of photonic devices goes through two type of processing steps: 1) wafer-level processes such as deposition, chemical mechanical polishing (CMP), baking, and etching and (b) die-level processes such as optical lithography.

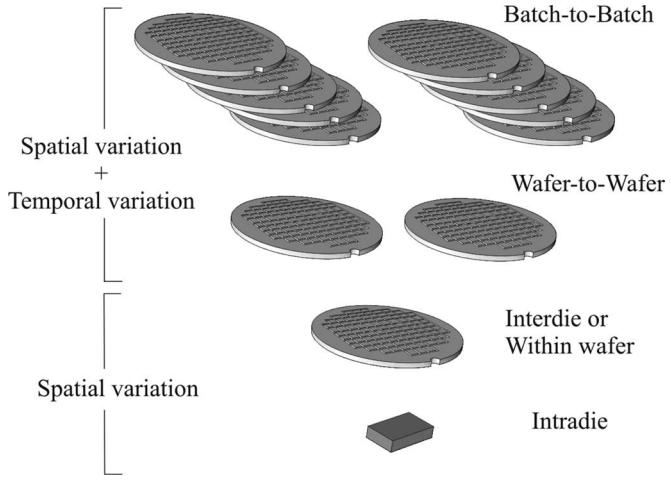

Fig. 3. Spatial and temporal variations.

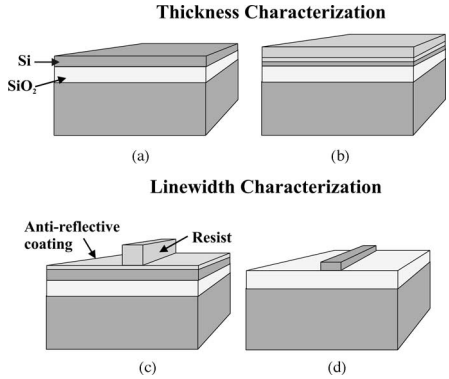

Fig. 4. Thickness and linewidth characterization at different stages of the fabrication process. (a) Si thickness measurement. (b) Photoresist and BARC thickness measurement. (c) Resist linewidth measurement. (d) Si linewidth measurement.

Nonuniformity in wafer-level processes can result in a shift of the average linewidth from die to die. Die-level processes, and in particular optical lithography, can introduce additional nonuniformity. The uniformity in scanning a die depends, among others, on the mask quality, pattern density in the mask, resist thickness, bottom antireflection layer thickness (BARC), and projection optics in the tool.

A. Intradie Nonuniformity

Intradie nonuniformity is the deviation occurring spatially within a die. Contrary to interdie variation, which affects all the structures on a die equally, intradie nonuniformity affects individual structures on the same die, thus resulting in mismatch between identical devices on a die (or even within a single device). Intradie nonuniformity can manifest itself in different length scales. With a die size of $8 \times 12\ \text{mm}^2$, the variation in the lithography process can affect linewidth in micrometer-length scale, while the Si thickness variation affects the device in millimeter-length scale.

Unlike the wafer-level processes, it is easy to extract the systematic variation in a given die. Even though it is obvious to observe such systematic variation, it is often difficult to clearly understand the source of such variation. Therefore, any attempt to control the variations should start with complete information about the mask (resolution, layout, pattern density, etc.).

B. Interdie Nonuniformity

Nonuniformity between dies, which are fabricated on the same wafer or on different wafers, is referred to as interdie nonuniformity. Interdie nonuniformity is generally caused by the fabrication tool and process design. Interdie nonuniformity often has a specific signature on the wafer. A CMP process, for example, creates a radially varying thickness from the center to the edge of the wafer. Fig. 7 is a typical example of nonuniformity generated by a plasma process. Since each die is a replica of every other, in most cases, the fingerprint of variation within one die can be seen in all other dies. But since the dies are spatially distributed over the wafer, the interdie uniformity will be affected by Si thickness variations over the wafer and plasma nonuniformity during the dry etch process. Knowledge of interdie variation is essential to clearly identify different sources of nonuniformity, and it is relatively easy to extract the sources of interdie nonuniformity compared to intradie nonuniformity.

IV. Fabrication

The photonic circuits were fabricated in a 200 mm monocrystalline SOI wafer using 193-nm optical lithography and a plasma etch process. The wafer is first coated with a BARC layer and positive photoresist in a clean track. Then, the wafer is exposed with the desired mask in a step and scan optical lithography tool using 193 nm ArK laser. The exposed areas are developed and the pattern from the photoresist is transferred into Si through an inductively coupled plasma-reactive ion etching (ICP-RIE) dry etch process. A detailed explanation about the fabrication process used in our experiment can be found elsewhere [11]. Before fabricating the devices, the lithography and etching processes were characterized for their uniformity using top-down scanning electron microscope (SEM) inspection on a photonic wire with nominal width of 450 nm as the test vehicle. The linewidth of the photonic wires was measured using top-down critical dimension SEM (CD-SEM), and the thickness of different layers over the wafer was measured using spectroscopic ellipsometry. Fig. 4 and Table I summarize the different metrology steps and respective measured quantity during the processing. They are described in more detail in the remainder of this section.

1) Measure the thickness of the incoming silicon layer using spectroscopic ellipsometry [Fig. 4(a)].
2) Apply photoresist and bottom antireflection layer (BARC).
3) Measure the thickness of the photoresist and BARC [Fig. 4(b)].
4) Expose the wafer with desired mask in the scanner.
5) Measure the linewidth of the resist line after development [Fig. 4(c)].
6) Etch 220 nm of Si using the dry etching process.
7) Strip the remaining resist and do wet clean.
8) Measure the linewidth of Si wires [Fig. 4(d)].

TABLE I
SUMMARY OF LAYER THICKNESS METROLOGY AFTER 10 mm Edge Exclusion

	Thickness[nm]		
	Si	BARC	Resist
Wafer mean (nm)	219.1	76.8	333.7
Wafer stand. dev. (nm)	2	0.09	0.7
Wafer range (nm)	7.1	0.5	3.4
Wafer stand. dev. (%)	0.9	0.1	0.2
Wafer range(%)	3.2	0.7	1

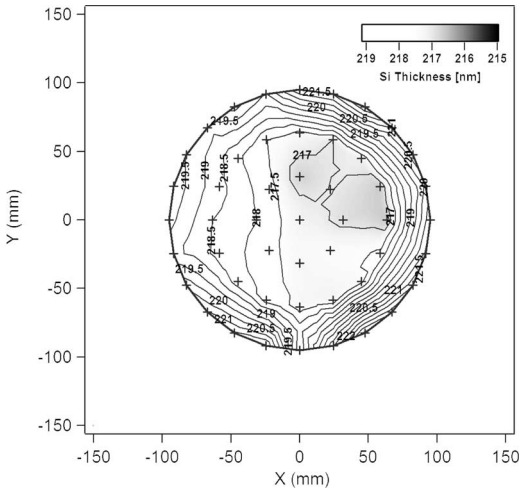

Fig. 5. Silicon layer thickness map over a 200 mm SOI wafer.

A. Thickness Characterization

Before optical lithography, the thickness of the top Si layer in the SOI wafer is measured using spectroscopic ellipsometry. The results for the 200 mm SOI wafer is shown in the uniformity map of Fig. 5 and the first column of Table I. The radial thickness profile ("bull's-eye"') is typical for a CMP process such as the one used in the SOI wafer fabrication process [12]. We observe a thickness variation of 3 nm radially from the center to the edge of the wafer. Also, within a shorter distance scale of 10 mm, the thickness varies by 1 nm, which will cause observable nonuniformity within a die.

The thicknesses of the BARC and photoresist used in the photolithography process influence both absolute linewidth and linewidth uniformity. The thicknesses of these layers were also measured using ellipsometry. To simplify the complexity of the model used for ellipsometry parameter extraction, the uniformities of the BARC and photoresist layers were characterized by coating them on a bare silicon wafer. Table I summarizes the thickness characterization of all layers. The thicknesses of the BARC and photoresist are controlled down to subnanometer nonuniformity, which is crucial in achieving a reproducible lithography process.

B. Linewidth Characterization

The linewidth of the photonic wire after lithography and after dry etch was measured using CD-SEM inspection. The CD-SEM used in our experiment has an accuracy of 2 nm, which is below our uniformity specification of ± 4.5 nm, so we could achieve reliable measurements. To characterize the linewidth uniformity over a wafer, the measurement location within the die is kept constant from die to die. The linewidth measurement was automated, which reduces the measurement errors. Figs. 6 and 7 show the linewidth uniformity over a 200 mm wafer. We achieved a linewidth uniformity of 0.45% after the lithography process and 0.76% after the etch process, respectively (standard deviation over the wafer). Table II summarizes the measurement statistics. The average linewidth of the photonic wire increases by 19 nm after dry etch, due to the sloped sidewalls of the photonic wires. This increase in linewidth can be compensated for by adapting the exposure dose such that, following lithography, the linewidth is reduced by 19 nm. This will not affect the uniformity.

The linewidth measured in the resist pattern (Fig. 6) does not show any systematic variation over the wafer, which implies that

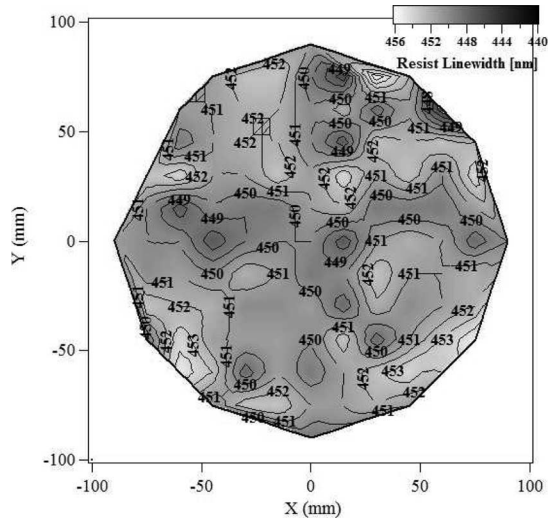

Fig. 6. Photoresist linewidth uniformity after optical lithography.

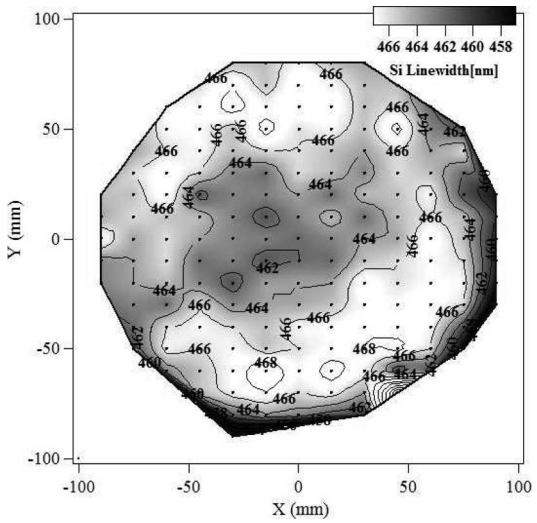

Fig. 7. Silicon wire linewidth uniformity after dry etch.

TABLE II
LINEWIDTH STATISTICS AFTER OPTICAL LITHOGRAPHY AND DRY ETCH
TARGET LINEWIDTH = 450 nm

	Linewidth	
	After Lithography	After Etch
Wafer mean (nm)	450.9	469.8
Wafer stand. dev. (nm)	2.01	2.59
Wafer range (nm)	5.5	7.5
Wafer stand. dev. (%)	0.45	0.76
Wafer range(%)	1.22	1.61

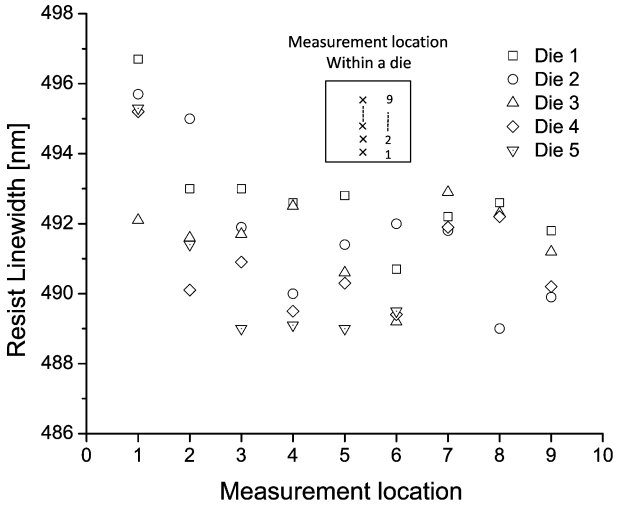

Fig. 8. Photoresist linewidth uniformity within a die after optical lithography.

there is no observable systematic variation from die to die (or within wafer) coming from optical lithography. The uniformity of the resist and BARC thickness over the wafer definitely help in reaching this uniformity. After the dry etch process (Fig. 7), we see a donut-shaped variation, typical for a plasma process, and this is caused by a variation of reactive species in the plasma. The finally resulting linewidth variation over the wafer of 0.76% meets our specification of $<1\%$.

Since we are using a step-and-scan-based lithography process, local variations in the lens system, mask error, or scanning system will result in a reproducible variation within a die. These variations can be deduced from measuring photonic wires at multiple locations within each die and comparing these to similar measurements from neighboring dies. Fig. 8 depicts within-die linewidth variation between five dies, following the lithography process. We can clearly see that for all dies, the linewidth of the photonic wires at the bottom of the die (numbered 1–3) is, on average, larger than that for the other wires. This variation can be attributed to a systematic error, e.g., in the mask, which is replicated in every die. We also observed a good correlation between this linewidth variation and the device response (see Section VI).

The nonuniformity within a die caused by the dry etch process strongly depends on the loading (structure density) of the structures. Presence of large open spaces or abrupt changes in the device density can cause large nonuniformity in the linewidth [13].

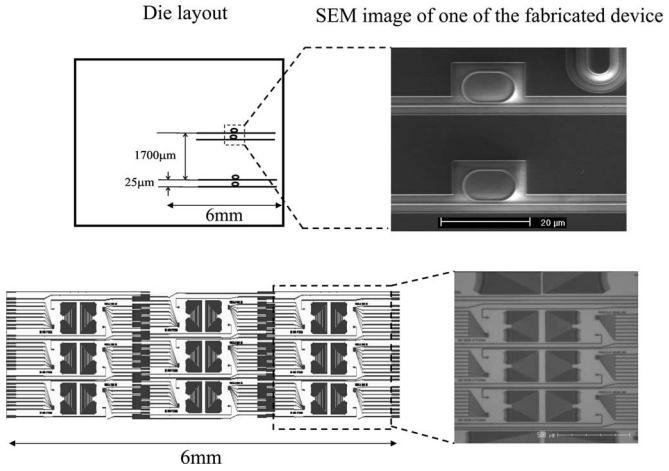

Fig. 9. Placement of test devices within a die.

As all die are replicas, after dry etch, the lithographic finger print will be preserved, but with a shift in the mean linewidth. This shift in the mean linewidth is due to plasma nonuniformity during the dry etch process.

Although the top-down CD-SEM linewidth measurement of photonic wires over a 200 mm wafer gives a good indication of uniformity, the photonic wire device uniformity does not depend only on the absolute linewidth of the device. Also, for devices that use directional couplers (e.g., ring resonators, splitters), the gap width uniformity between the waveguides does not depend on the absolute gap width. In either case, the uniformity of the device depends on the average linewidth/trench width variation along the length of the device. With the CMOS characterization tools and algorithms available, it is not possible to accurately measure the average linewidth over a distance of few tens of micrometers, and therefore, optical characterization is the only way to characterize actual device uniformity. This is described in the following section.

V. UNIFORMITY TEST DEVICES

To characterize the process uniformity, we designed a number of suitable test devices. Almost all silicon photonic devices are sensitive to dimensional variation; hence, we have a wide variety of components to choose from. We selected three types of wavelength-selective devices in our experiments; all-pass racetrack ring resonators (RTRs), 1X1 Mach–Zehnder interferometers (MZIs), and eight-channel AWGs. These are all interferometric devices, and variations in the spectral response directly reflect any variation in the dimensions (width and height).

The devices were arranged so that both short- and long-distance nonuniformities could be studied. RTRs and MZIs were placed in pairs of two on two locations of the die (Fig. 9, top). The distance between two devices in a pair was 25 μm and was representative for short-range uniformity. The distance between the two pairs was 1700 μm, which is suitable for long-range uniformity assessment. The RTRs were designed with a ring radius of 4 μm, a coupling length of 4 μm, and a coupling gap of 180 nm. The 1X1 MZIs had a delay length of 50 μm in one of the arms and used two Y junctions for splitting and combining the light.

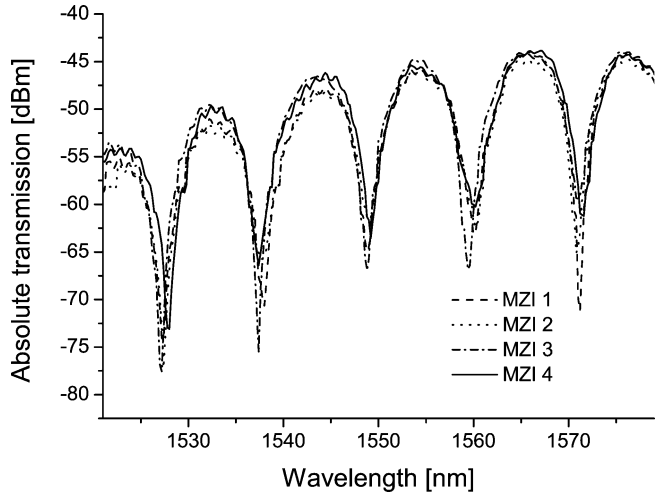

Fig. 10. Intradie uniformity of four identically designed MZIs fabricated using 193 nm optical lithography.

The AWGs were arranged in an array of rows and columns, with each AWG having a closest neighbor at 250 μm, while the farthest distance between two arrays was 4500 μm. In total, 18 devices cover an area of 0.7×6 mm^2 in each die. The eight-channel AWGs were designed to have a channel spacing of 400 GHz. They have a footprint of 200×35 μm^2 each. The relatively large footprint of the array of AWGs enables us to study the effects of long-length scale variation within a die.

VI. Device Measurement Results and Discussion

To analyze intradie (within) and die-to-die uniformity, we measured the spectral response of the fabricated devices. They were characterized by coupling in TE-polarized light from a broadband light source and measuring the output from the devices through a spectrum analyzer with a resolution of 0.12 nm. Some of the devices were characterized using a tunable laser with a resolution of 20 pm. The measurement spectrum was limited to the 1550 nm telecommunication wavelength range (1520–1600 nm). Shifts of the resonant peaks due to nonlinear and thermal effects in the resonators were avoided by using low input power [14] and a temperature-controlled measurement stage. Grating fiber couplers [15] were used for in and out coupling of light.

A. Intradie Device Nonuniformity

In general, within a die, the devices can be placed from a few tens of nanometers (coupled devices) to a few hundreds of micrometers away from each other.

Fig. 10 shows the spectral response of four MZIs within a die, organized as shown in Fig. 10. Table III summarizes the results for the intradie uniformity, measured from 13 different dies. For MZI devices that are located close together (25 μm), we measured an average variation of 0.2 nm for the resonance wavelength and a minimum variation of 20 pm (Fig. 11). Distantly spaced devices show a variation of 0.6 nm. For RTRs, we measured a variation of 0.15 and 0.55 nm, respectively.

Compared to RTRs and MZIs, AWGs are larger in size (few tens of micrometers), which makes them more vulnerable to

TABLE III
Within-Die/Chip Device Uniformity

Distance between device	Mean standard deviation of $\lambda_{res}[nm]$		
	ring resonator	MZI	AWG
25μm	0.15	0.2	-
275μm	-	-	0.54
770μm	-	-	0.52
1700μm	0.55	0.6	-

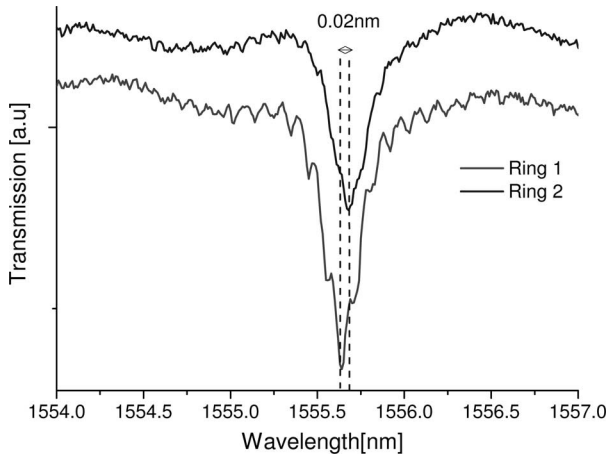

Fig. 11. Spectral response of two RTRs spaced 25 μm apart.

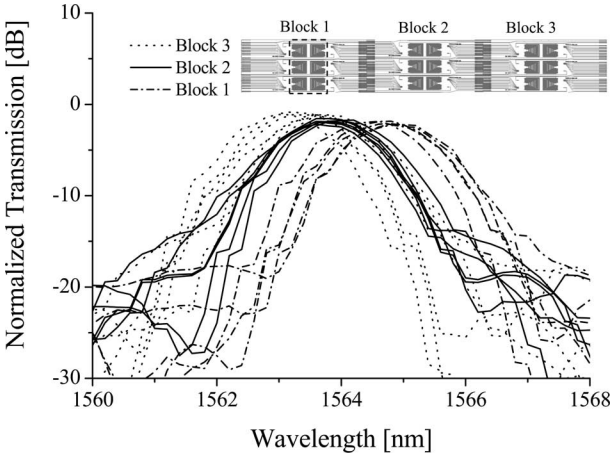

Fig. 12. Transmission of one of the eight channels of 17 AWGs on the same die fabricated using 193 nm optical lithography.

different sources of variations. Within a die, we have measured an average nonuniformity of 0.57 nm. From the spectral measurement of 17 AWGs (Fig. 12), we observe a strong correlation between the peak wavelength shift and the position of the devices. A possible origin for this rather systematic variation could be the shift in the silicon layer thickness. The AWGs were spread over a length of 6 mm in the die, and as shown before, the silicon layer thickness can vary by 0.5 nm over this distance. A mask error could be another possible cause.

It is clear from our measurements that within a die, device nonuniformity increases with an increase in distance between them. A good correlation of the linewidth measurements (Fig. 8)

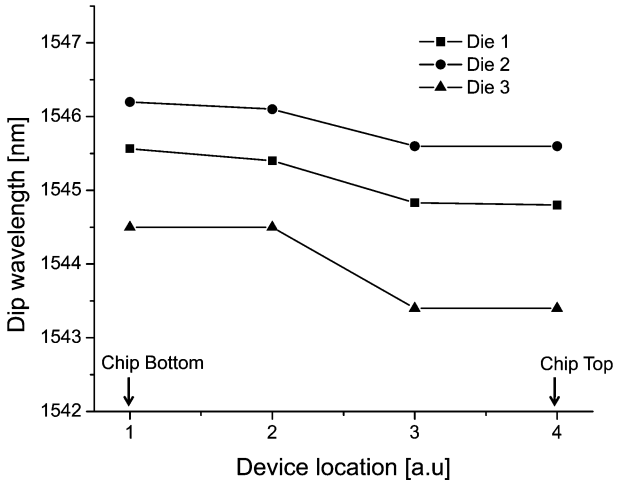

Fig. 13. Die-to-die resonance wavelength trend between three dies.

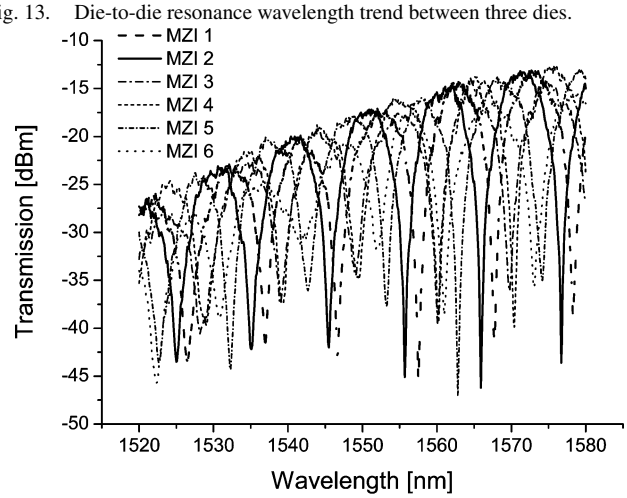

Fig. 14. Within-die uniformity of MZI fabricated using 248 nm optical lithography.

and the spectral shift measurement (Fig. 13) clearly indicates that mask fabrication and/or local mask density is the main source of nonuniformity.

To estimate the influence of the fabrication process, we fabricated devices using the same mask but using a 248 nm optical lithography process and a previously developed dry etch process [16]. The results are shown in Fig. 14. Though we have used an identical mask, the variation is substantially higher for the 248 nm lithography process compared to the results obtained with the 193 nm lithography process described before. We found an average wavelength shift of 0.7 and 7.3 nm for the short- and long-distance scales, respectively. Reducing the illumination wavelength of the optical lithography system from 248 to 193 nm thus considerably enhances the process uniformity.

B. Interdie Device Nonuniformity

As defined before, interdie or die-to-die uniformity is the device uniformity between nominally identical chips within a wafer. As already discussed in Section III, interdie uniformity is influenced by process design and wafer nonuniformity. We characterized interdie nonuniformity by measuring 36 MZIs from 13 different dies and 53 AWGs from 3 dies. From these measurements, we have found a nonuniformity of <2 nm for MZIs and AWGs (Table IV). Fig. 15 depicts the spectral response of 12 MZIs from three dies. The results extracted from Fig. 15 are summarized in Fig. 13.

TABLE IV
DIE-TO-DIE DEVICE UNIFORMITY

Distance between device	Mean standard deviation of $\lambda_{res}[nm]$		
	ring resonator	MZI	AWG
10,000μm	1.3	1.08	0.4
20,000μm	1.8	1.73	–

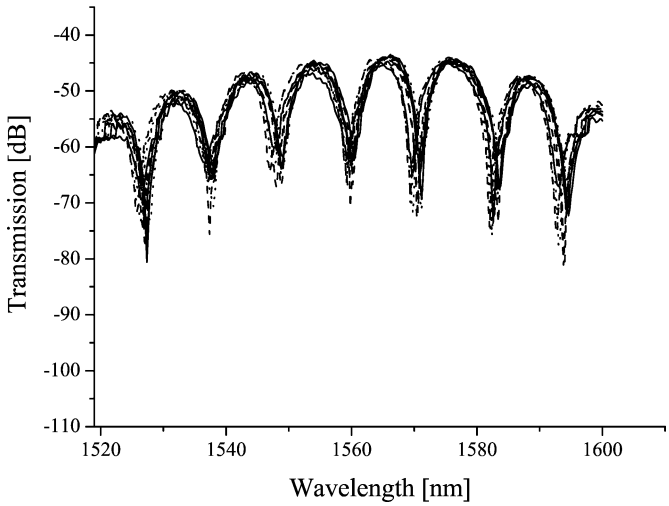

Fig. 15. Transmission spectrum of 12 MZIs from three normally identical dies from a wafer.

The die-to-die resonance shift of the MZI and AWG is shown in Figs. 13 and 16, respectively. It can be clearly seen that all dies show a fingerprint variation, but with a shift in the mean peak wavelength, which is in agreement with our initial argument in Section III. This shift in the wavelength as a function of device location is mainly caused by variation in mask.

We observe a standard deviation of 0.4 nm in the die-to-die AWG mean peak wavelength, which can be attributed either to plasma or Si thickness variation. Because both show a radial varying pattern over the wafer, it is difficult to differentiate between both effects. Hence, special fabrication procedures, such as rotation and shifting of the wafer, would be required to discriminate between the influence of silicon layer thickness variation and plasma variation over the wafer.

VII. PROPOSAL FOR UNIFORMITY IMPROVEMENT

Though we managed to control the nonuniformity and reduce it below a nanometer, such results are only sustainable by using an adaptive process flow. During the fabrication process, each process step is a potential source of nonuniformity; hence, controlling each step is vital. In any CMOS production line, each fabrication tool and the process have to be monitored. For photonics device fabrication, the tolerances are tighter ($<1\%$) than

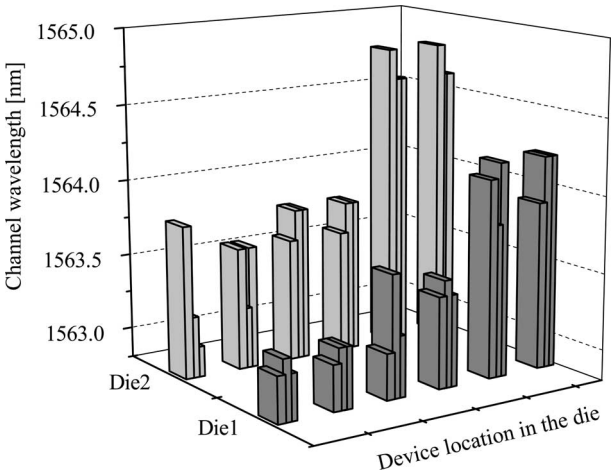

Fig. 16. Die-to-die uniformity of AWGs within a wafer.

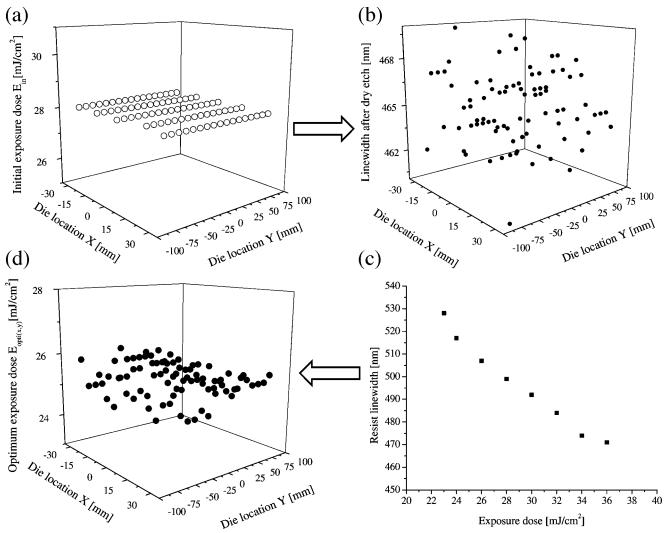

Fig. 17. Exposure dose compensation for dry etch nonuniformity.

CMOS (<5%–10%), and therefore, the monitoring process has to adapted to these more stringent device specifications.

Fig. 17 illustrates a simple uniformity control through exposure dose optimization during the optical lithography process. Fig. 17(b) shows the die-to-die linewidth variation after dry etch when fabricated with a uniform exposure dose, as shown in Fig. 17(a). The etch nonuniformity can be controlled by tuning the exposure dose of each die. Using the dose-to-target data [Fig. 17(c)], the exposure dose can be adjusted to compensate the dry etch nonuniformity with a dose map $E_{\mathrm{opti}(x,y)}$, as shown in Fig. 17(d).

The adaptive process control presented can be further extended to compensate for Si thickness nonuniformity over a 200 mm SOI wafer. Fig. 18 shows the proposed fabrication flow. Since the lithography process is a die-per-die process, it can be adapted "on the fly." The dashed line in Fig. 18 shows the flow of process monitor data, which can be bused during device fabrication to tune the process for maximal uniformity. The first step in the fabrication process should be mapping the Si thickness and its variation over the incoming wafers. From

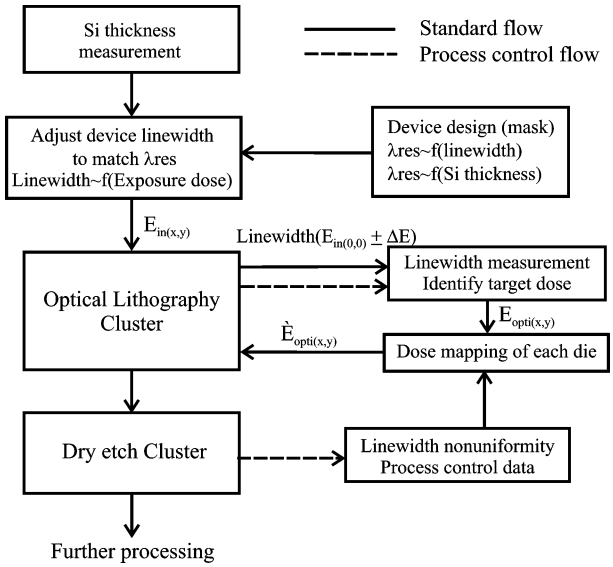

Fig. 18. Proposed process flow model to improve device uniformity in a production environment.

the obtained data and based on input from the designer, the linewidth optimized to match the required device response can be determined for each location on the wafer. From these data and the linewidth dose-to-target graph [Fig. 17(c)], we can then determine the initial exposure dose ($E_{\mathrm{in}(x,y)}$). The latter can then be exported to the lithography process while keeping all other settings (defocus, numerical aperture, etc...) unchanged.

First, a send-ahead wafer is exposed with an exposure dose matrix and ($E_{\mathrm{in}(x,y)}$) is tuned to the optimum dose ($E_{\mathrm{opti}(x,y)}$) if needed. As described earlier, the dry etch nonuniformity can be controlled by further tuning the optimized exposure dose for each die ($\grave{E}_{\mathrm{opti}(x,y)}$).

VIII. Conclusion

In this paper, we demonstrated that by using 193 nm optical lithography and an optimized dry etching process, it is possible to achieve a linewidth nonuniformity of $<1\%$ over a 200 mm wafer. Wavelength-selective devices showed a nonuniformity in the spectral response of <0.6 nm within a chip and <2 nm between chips. Though discriminating the sources of nonuniformity in the subnanometer range is difficult, from our experiments, we conclude that the intrachip nonuniformity is mainly caused by mask errors while the interchip nonuniformity is mainly caused by the etch plasma and wafer thickness variations. By comparing 248 and 193 nm optical lithography, we showed that the shorter illumination wavelength is absolutely necessary for achieving the $<1\%$ nonuniformity required for practical applications. In the future, using extreme ultraviolet (13 nm) optical lithography may improve the uniformity further.

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