Hybrid III-V/Silicon laser based on DVS-BCB bonding

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Recent years have witnessed an increasing research interest in hybrid lasers based on evanescent coupling between III-V materials and silicon waveguides. Recently reported state-of-the-art devices utilize molecular die-to-wafer bonding of III-V epitaxial layers to silicon waveguides, which imposes strict requirements on the cleanliness and quality of the bonded surfaces. In this paper, we propose a hybrid III-V/silicon laser based on adhesive DVS-BCB bonding providing less strict surface quality requirements and a fabrication procedure suitable for large-scale production. The general layout of the device and its simulated properties are presented and discussed.

Introduction

Silicon photonics has recently emerged as a state-of-the-art technology for implementing passive and some of the active functions in integrated photonic circuits. Transparency of silicon at the communication wavelengths of 1.3 μm and 1.5 μm offers great potential for applications in the next-generation integrated devices for high-speed communications. However, due to the indirect bandgap of silicon, fabrication of the light sources on this platform is a serious challenge. One way to address this problem is the heterogeneous integration of light sources fabricated in III-V semiconductor materials with the SOI waveguide platform. It combines the light emission from III-V materials with low-cost and high-yield of CMOS fabrication processes used for the SOI waveguide structures.

Researchers have recently demonstrated several devices based on evanescent coupling between III-V laser cavity and SOI waveguide optical modes. The first evanescent hybrid III-V/Silicon, Fabry-Perot laser (emitting at 1.55 μm), was reported in 2006 [1], followed by another FP laser (λ =1.31 μm) in 2007 [2] and DBR [3] and DFB lasers [4], in 2008. These devices were based on molecular, O_2 plasma-assisted, wafer bonding procedure, which is based on van der Waals forces and thus requires ultimately clean, smooth and contamination-free bonding surfaces. Surface roughness, contamination or presence of small particles will result in large unbonded areas between two surfaces and ultimately reduce the process yield. Therefore, this technique may not be robust enough for industrial scale fabrication where such strict requirements are difficult to meet.

To address this problem, we propose an alternative approach based on the adhesive die-to-wafer bonding technique, using a commercially available DVS-BCB polymer (cyclotene®^{TM}). In this paper, we present the general layout of the hybrid III-V/Silicon evanescent laser based on the DVS-BCB bonding technique and its critical parameters. The results of optical and thermal simulations are also presented and discussed.

Evanescent Hybrid Laser Design

The general layout of the hybrid III-V/silicon evanescent laser is given in Figure 1a). The underlying rib waveguide is made on a standard SOI platform, with 1 μm thick buried oxide layer. Silicon rib waveguide thickness is H = 500 nm, the rib etch depth is R = 220 nm, the silicon waveguide width is W = 1.2 μm, and the trench width is T = 3.4

μm. The epitaxial III-V structure is bonded on top of the SOI waveguide, using a spin-coated DVS-BCB adhesive layer. It comprises the n-type InP spacer layer and the mesa structure on top of it. The mesa is made of the multiple quantum well (MQW) region (8 InGaAlAs-based QWs and 9 barriers, emitting at λ = 1.3 μm), carrier blocking (CB) layer, a separated confinement heterostructure (SCH) layer, a p-type InP top cladding layer and an ohmic contact.

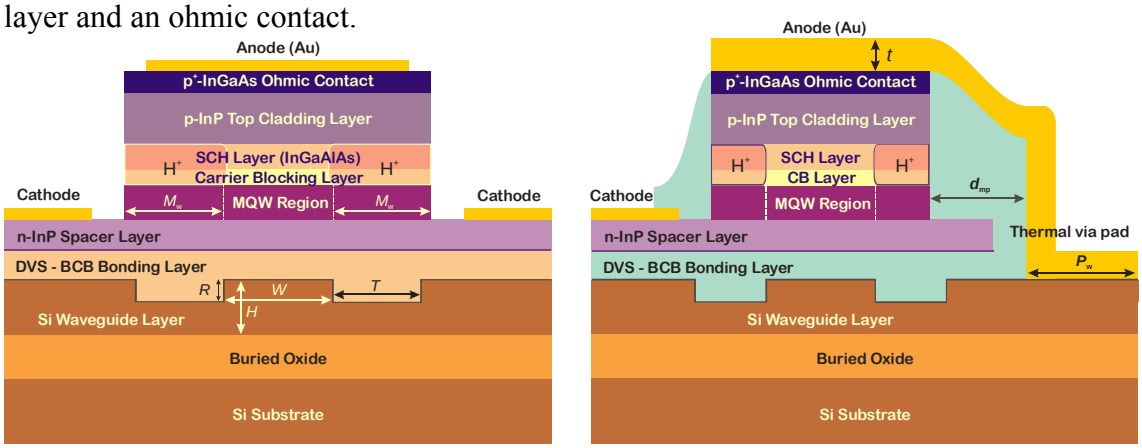

Figure 1. a) Evanescent III-V/silicon hybrid laser cross-section (device without thermal via); b) Cross-section of the hybrid III-V/silicon laser with a thermal via.

To achieve an effective evanescent coupling between the modes supported by the III-V region and the underlying SOI waveguide, the distance between the III-V active layers and the SOI waveguide must be sufficiently small. The goal is to design a device having its fundamental hybrid mode predominantly confined within Si waveguide, with only a fraction of its power within MQW active region. Thus, no additional coupling (using a taper, for example) is necessary, as the bulk of the optical power leaving the laser is already confined within the Si waveguide. Confinement factor for the fundamental mode within Si waveguide (Γ_{Si}) of around 70% is considered sufficiently high for this purpose, while the confinement factor within MQW active regions (Γ_{MQW}) should be at least 3%.

Due to fabrication tolerances, the thickness of the BCB layer may vary, which in turn changes the distance between the Si waveguide and MQW active region and eventually affects the layout of the lasing hybrid mode. The primary goal in designing a hybrid laser is to find the optimal thicknesses of n-type spacer layer and SCH layer, so that the variations in BCB thickness have the minimum impact on the fundamental mode layout.

Optical and Thermal Properties of the Device

Optical properties of the device were studied using FIMMWAVE, a fully vectorial mode finder software. Fundamental (TE) modes and the corresponding confinement factors (Γ_{Si} and Γ_{MQW}) were calculated for various thicknesses of BCB, SCH and spacer layers. The results of these simulations, given as plots of confinement factors versus BCB layer thickness, are presented in Figure 2 and Figure 3. We can conclude that, within the range of BCB thickness variations (20 nm – 120 nm), values for Γ_{Si} and Γ_{MQW}, in general, strongly depend on both the SCH and spacer layer thicknesses, but there are some optimal values that provide relatively stable confinement factor values and consequently, stable fundamental mode profiles. These values are 210 nm and 230

nm, for SCH layer and spacer layer thicknesses, respectively. Calculated values for Γ_{Si} and Γ_{MQW} are around 73% and between 3% and 3.5%, respectively. Parameter that can also be changed is the width of III-V mesa – more specifically, the width of mesa wing section (M_w), (see Figure 1a)). In all the simulations, we used value M_w = 3 μm, meaning that the mesa width was 7.2 μm (double M_w value + Si waveguide width). Increasing the mesa width above this value had very small impact on the fundamental mode profile.

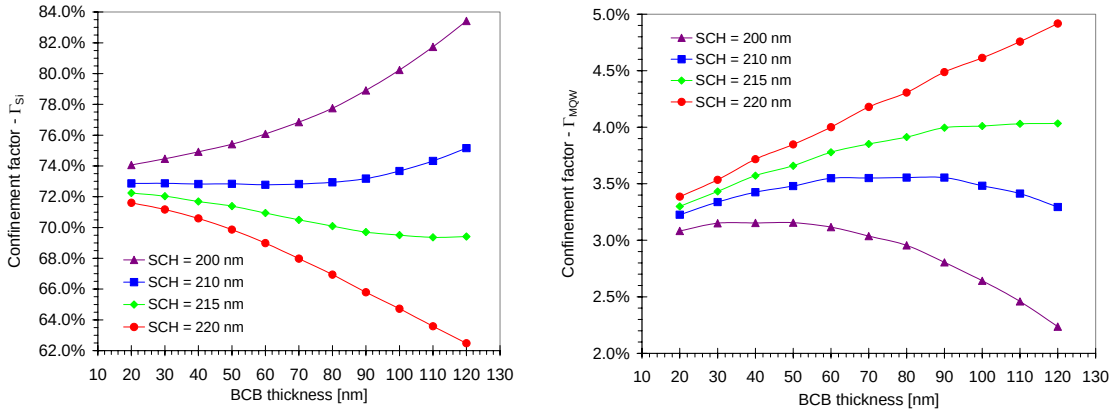

Figure 2. Fundamental mode confinement factors dependence on SCH layer and BCB layer thicknesses for a device with 230 nm thick spacer layer (Γ_{Si} – left plot, Γ_{MQW} – right plot).

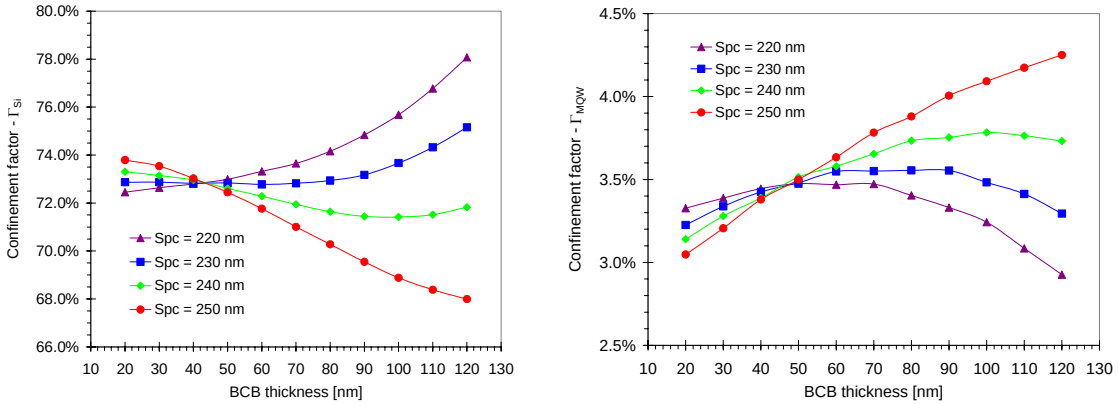

Figure 3. Fundamental mode confinement factors dependence on spacer layer and BCB layer thicknesses for a device with 210 nm thick SCH layer (Γ_{Si} – left plot, Γ_{MQW} – right plot).

Regarding the thermal properties, the goal is to design a device with the lowest possible thermal resistivity. Problem arises from the fact that BCB has a very low thermal conductivity (0.3 W/m·K) which hinders the heat flow from the III-V region down to SOI structure Thus, it is essential to design a device that will remove the excessive heat in an efficient way and better cope with high injection current and/or high ambient temperature. Thermal properties of the device were studied using COMSOL Multiphysics® software. The heat source, with a constant heat flux of 10 kW/cm^2, was confined within the central part of the MQW active region (as the proton implantation in lateral mesa regions will confine current flow to this area). Initially, we studied devices with the cross-section as presented in Figure 1a), with 200 nm thick gold contact on top of the mesa, but with various mesa wing widths. Results of these simulations, presented in Figure 4, show that increasing M_w significantly reduces thermal resistivity R_{th} of the device. However, larger M_w values lead to an increased

electrical resistance and the corresponding heat dissipation in the spacer layer. Additional thermal simulations should include this more realistic model of heat generation in order to provide the optimum mesa width value.

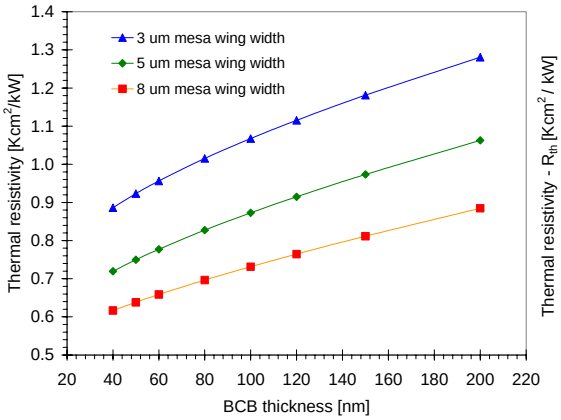

Figure 4. Thermal resistivity R_{th} for devices with various mesa widths (no thermal via).

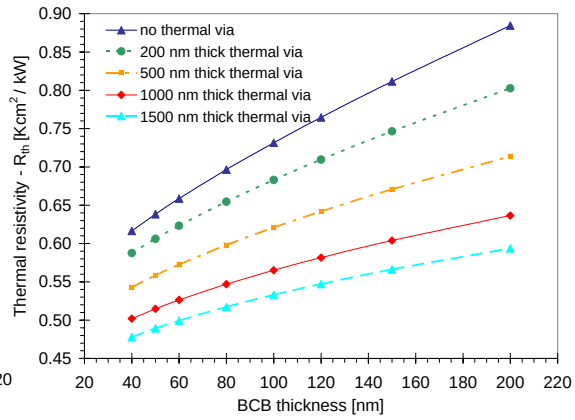

Figure 5. Thermal resistivity R_{th} for devices with various thermal via thicknesses.

In order to achieve even smaller values for R_{th}, adding a metallic thermal via, as given in Figure 1b), is proposed. The idea is to use good thermal conductivity of the gold (320 W/m·K) to remove heat from the mesa and direct it to the Si layer, which also has high thermal conductivity (130 W/m·K). In our simulations, we used a thermal via with 10 μm wide pad (P_w) and 10 μm mesa-to-pad distance (d_{mp}). Simulation results, presented in Figure 5, show that increasing the thermal via thickness (t) decreases the thermal resistivity and for t = 1.5 μm, R_{th} can be reduced by 20% to 30% (more for thicker BCB layers). This is a significant improvement and we believe that adding a thermal via is the best option for enhancing thermal properties of the device. Additional simulations revealed that increasing thermal via pad width or reducing mesa-to-pad distance, only marginally reduces R_{th}. Therefore, the thickness of the gold layer is the most important parameter of the via and simulation results suggest that it should be at least 1.5 μm.

Conclusions

In this paper we propose a hybrid III-V/Silicon evanescent laser, based on InGaAlAs multiple quantum wells, emitting at λ = 1.3 μm. Simulations presented us with the optimal values for n-InP spacer layer and SCH layer thicknesses, that provide fairly constant confinement factors for a broad range of the BCB layer thicknesses. Thermal simulations reveal that increasing the mesa width (to some extent) and adding a thermal via significantly improves device's thermal properties. In our future work, we plan to fabricate devices according to this design and characterize them.

References

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