Silicon nanophotonics: towards VLSI photonic integrated circuits

G. Roelkens, W. Bogaerts, D. Taillaert, P. Dumon, L. Liu, S. Selvaraja, J. Brouckaert, J. Van Campenhout, K. De Vos, P. Debackere, D. Van Thourhout, R. Baets
Ghent University/IMEC – Photonics Research Group, Sint-Pietersnieuwstraat 41, B-9000 Ghent, Belgium
www.photonics.intec.ugent.be
e-mail: Gunther.Roelkens@intec.ugent.be

Abstract

Silicon photonics is emerging as a disruptive technology for passive integrated optical functions and for active optical functions like (electronically controlled) light modulation and switching. In this presentation we will review the work carried out in the Photonics Research Group in the field of silicon photonics. This includes the fabrication of photonic integrated circuits using CMOS deep UV lithography, examples of integrated silicon components for wavelength selective optical functions for use in optical communication and optical sensing, and examples of coupling structures for interfacing the nanophotonic integrated circuits with an optical fiber.

1. Introduction

Fabrication techniques with the aim of integrating a set of optical functions on a single optical chip have advanced to the stage of being technically feasible, a discipline which is referred to as *integrated photonics*. This is comparable to what has been happening in electronics over the last decades, where the number of transistors on state-of-the-art processors doubles approximately every two years. The research in the field of integrated photonics is driven by the advantages seen in integrating electronic functions on electronic integrated circuits, which are ubiquitously used today. Analogous to electronic integrated circuits, integrating photonic functions on a single chip allows realizing cheaper and more compact optical systems with lower power consumption.

In recent years, the use of silicon as a material platform for integrating optical functions has emerged. This material platform offers the potential of realizing cheap optical functions due to the fact that standard CMOS fabrication tools and processes can be used to fabricate the optical circuits, as if they were electronic integrated circuits. The same economy of scale which renders electronic integrated circuits economically viable today, therefore applies to the cost reduction of the photonic integrated circuits. Moreover, the optical functions can be made ultra-compact, due to the very high refractive index contrast that can be achieved in the Silicon-on-Insulator (SOI) material system, a material platform which is nowadays used for the fabrication of high-end electronic integrated circuits. In this material system, the optical mode is guided in a dielectric waveguide consisting of a Silicon waveguide core with a typical cross-section of $0.1\mu m^2$ ($n_{Si}=3.45$), surrounded by a low refractive index SiO_2 or air cladding layer (n=1). This huge refractive index contrast allows making wavelength scale integrated optical functions. This scaling of the size of the optical circuit further leverages the cost reduction, as more photonic integrated circuits can be obtained from a single 200mm/300mm SOI wafer.

From this discussion it is clear that *Silicon photonics* is emerging as a disruptive technology for passive integrated optical functions and for active optical functions like (electronically controlled) light modulation and switching. In this presentation we will review the work carried out in the Photonics Research Group in the field of silicon photonics. This includes the fabrication of photonic integrated circuits using CMOS deep UV lithography, examples of integrated silicon components for wavelength selective optical functions for use in optical communication and optical sensing, and examples of coupling structures for interfacing the nanophotonic integrated circuits with an optical fiber.

2. Silicon-on-insulator waveguides

A silicon-on-insulator (SOI) layer stack consists of a silicon waveguide layer on top of a buried SiO_2 layer, fabricated on a silicon substrate. Two types of silicon-on-insulator waveguides are used. Large core rib SOI waveguides consist of a silicon waveguide layer, which is multiple material wavelengths thick. Lateral confinement is obtained by defining a rib waveguide geometry. By carefully adjusting the etch depth and the width of the waveguide, single-mode operation can be achieved. This requires shallow etching of the waveguides, reducing the lateral refractive index

contrast. While the increase of the minimal waveguide radius due to this low refractive index contrast can be countered by the use of total internal reflection mirrors, the minimum pitch of the waveguides has to remain large enough to avoid crosstalk between adjacent waveguides. The general understanding is that this waveguide system allows to fabricate optical circuits with low polarization dependence, low propagation loss and allow fiber insertion loss at the expense of compactness.

In SOI photonic wire technology, a silicon waveguide layer thickness on the order of half a material wavelength is used and the lateral confinement is achieved by completely etching through the silicon waveguide layer. In this way, a large omni-directional index contrast is achieved (n_{Si} = 3.45, n_{SiO2}=1.45), which allows high density integration of optical functions. Due to the high lateral refractive index contrast, waveguide widths smaller than 500nm are necessary to obtain single-mode operation. The compactness of this waveguide structure makes it however more sensitive to scattering loss at rough waveguide boundaries and it inherently behaves different for transverse electric and magnetic polarization. Due to the large discrepancy in mode size between photonic wire waveguides and optical fibers, fiber coupling structures have to be designed that accommodate this difference.

Both types of SOI waveguides are shown in figure 1, together with the design criteria for single mode operation. In the Photonics Research Group we focus on the SOI photonic wire technology, as it allows creating ultra-compact photonic functions, paving the way towards VLSI photonic integrated circuits. We will show in the remainder of the paper that by using state-of-the-art CMOS fabrication technology, SOI photonic wires can be fabricated with a loss on the order of 2-3dB/cm. This allows the fabrication of high performance integrated optical functions like ring resonators, arrayed waveguide gratings and planar concave gratings. The issue of polarization dependent behavior and the interfacing with a standard single mode fiber can be tackled by a single integrated optical function consisting of a two-dimensional periodic grating structure, as will be shown further on.

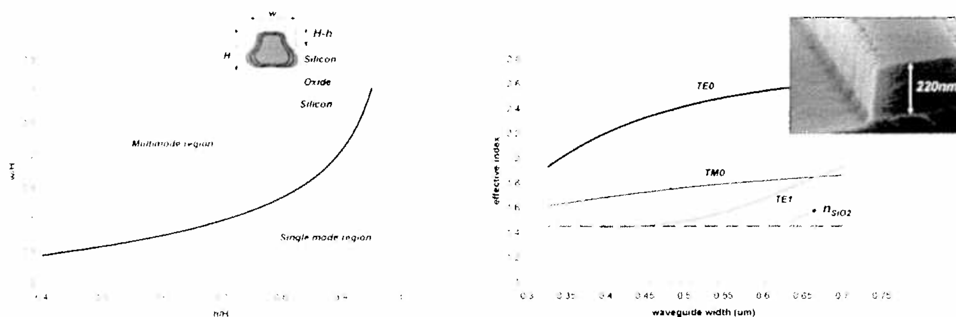

Figure 1: large core SOI rib waveguide structures (left, multiple material wavelengths thick Silicon waveguide layer) versus SOI photonic wire technology (right, half material wavelength Silicon strip waveguide): waveguide cross-section and single mode design criteria.

3. Silicon-on-Insulator waveguide fabrication technology

Silicon-on-Insulator waveguide structures are defined on a 200mm wafer in a CMOS pilot line. The SOI wafer consists of a 220nm Silicon waveguide layer on top of a 2μm buried SiO2 layer (fabricated on a silicon wafer) to optically isolate the Silicon waveguide mode from the Silicon substrate. Photoresist is coated on the wafer, and then pre-baked. On top of the photoresist, an anti-reflective coating is spun to eliminate reflections at the interface between the air and the photoresist during the lithography. These reflections would induce standing waves in the photoresist, and therefore lead to inhomogeneous illumination. After photoresist coating, the wafer is sent to the stepper, which illuminates the photoresist with the pattern on the mask. As a 200mm wafer can contain many dies, the pattern is repeated across the wafer. While stepping over the wafer surface, the exposure conditions (focus and exposure dose) can be varied, which makes it possible to do detailed process characterization. After lithography, the resist goes through a post-exposure bake, and is then developed. The developed photoresist is then used directly as a mask for etching. The process flow is depicted in figure 2. A scanning electron microscopy image of a fabricated photonic wire can be seen in the inset of figure 1b. For the silicon etch, a low-pressure/high-density Cl_2/O_2/He/HBr plasma chemistry is used. Losses down to 2-3dB/cm (λ=1.55μm, TE polarization) were obtained on 500nm wide photonic wires, fabricated using the process described above. These loss values are sufficiently low to fabricate high quality optical functions in silicon-on-insulator.

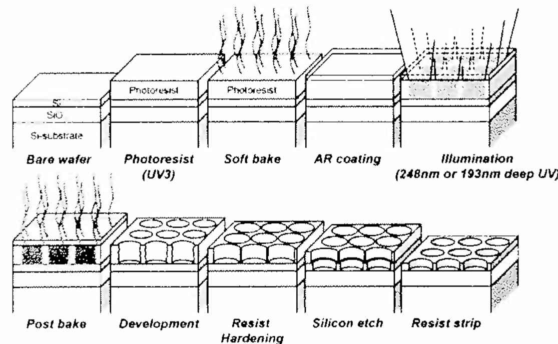

Figure 2: SOI waveguide fabrication process on a 200mm SOI wafer using standard CMOS technology

4. Integrated optical functions based on SOI photonic wire technology

Wavelength selective optical functions are key components for optical networks, where information is encoded on a set of optical carriers with a different wavelength (wavelength division multiplexing). In the nodes of the network, the different carriers need to be multiplexed or demultiplexed, wavelength channels need to be dropped or added, etc. The silicon-on-insulator material system (and especially the SOI photonic wire technology) is very well suited to realize this kind of optical functions. Three examples of integrated wavelength selective functions will be presented at the conference: SOI ring resonators, capable of adding and dropping wavelength channels on an area of about 100μm^2, arrayed waveguide gratings and planar concave gratings, capable of multiplexing and demultiplexing a set of optical carriers with a constant central wavelength difference. A scanning electron microscopy image of all three components is shown in figure 3. Arrayed waveguide grating and planar concave gratings channel spacing depend on the design (and the area that the device occupies scales inversely proportional to this wavelength separation), which will be discussed at the conference. Ring resonators with a quality factor of 10000-20000 and a free spectral range on the order of 20-30nm are obtained. Besides for wavelength selection, these devices can also be used for optical sensing of strain, biomolecules attaching to the waveguide wall, temperature,... as the resonance wavelength of the device is sensitive to these environment variables.

Figure 3: SEM images of SOI integrated optical functions for wavelength selection and (de)multiplexing: ring resonator (left), planar concave grating (middle) and arrayed waveguide multiplexer (right)

5. Interfacing nanophotonic integrated circuits with an optical fiber

A hurdle that has to be overcome when implementing an optical function on the SOI material platform, is the interfacing with the outside world, i.e. the optical fiber. This interfacing with SOI photonic wire circuits was thought to be difficult and inefficient due to the large mismatch between the cross-sectional dimensions of the core of an optical fiber (typically 60μm^2) and the cross-sectional dimension of an integrated SOI waveguide (typically 0.1 μm^2). In the Photonics Research Group we demonstrated that using a diffractive grating structure on top of the SOI waveguide a highly efficient interface between an optical fiber and the integrated optical circuit can be obtained with efficiencies as high as 80%, in spite of the large mismatch in size between the SOI waveguide and the core of the optical fiber. An additional advantage of this approach is that the optical fiber is positioned vertically on top of the SOI waveguide circuit. This approach allows for testing the photonic integrated circuits on a wafer-scale (to select the known-good

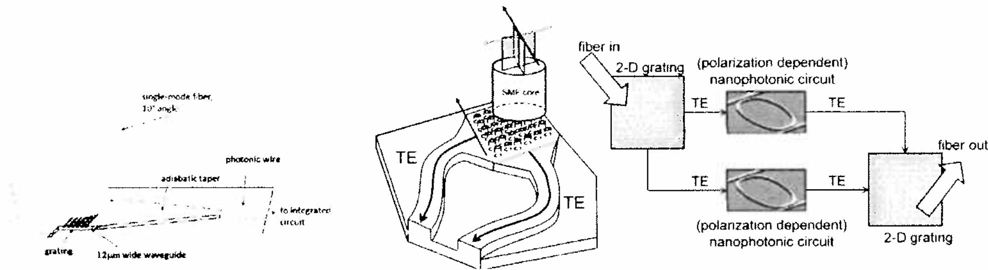

Figure 4: The use of one-dimensional (left) and two-dimensional diffraction gratings (right) for interfacing with an optical fiber

dies), as no longer a cleaved waveguide facet is needed. This approach could even allow for wafer-level packaging of the optical circuits, which can have an important influence on the cost reduction, as packaging of a photonic integrated circuit typically accounts for 50% of the total component cost. This type of one-dimensional diffraction grating is shown in figure 4(left).

Based on this development, we extended the concept of using a diffraction grating to interface with an optical fiber to also tackle the problem of the large polarization dependence of integrated SOI photonic wire optical circuits. This problem can be solved by using a polarization diversity configuration, in combination with a two-dimensional diffraction grating to interface with an optical fiber. This two-dimensional diffraction grating spatially separates the orthogonal polarizations propagating in the optical fiber, into two (nearly) orthogonal waveguides, where the light propagates as a TE polarized mode. By using a polarization diversity approach, where two identical circuits are connected to the respective waveguides and an additional two-dimensional grating is used for combining both polarizations, polarization independent operation can be obtained. The principle is graphically illustrated in figure 4(right).

6. III-V/Silicon photonics

The integration of light emitters and photodetectors operating at telecommunication wavelengths onto the Silicon-on-Insulator material platform is hampered by the indirect band gap of Silicon. As this is a rather fundamental issue, these optical functions still require the use of III-V semiconductor materials. Therefore, a technology is required to integrate these III-V semiconductors on the SOI waveguide platform, while maintaining the advantages of the CMOS manufacturing process, namely the low-cost, high yield and the economy of scale. In the Photonics Research Group we developed a technology to integrate a direct band gap III-V layer (an InP/InGaAsP heterostructure operating at telecommunication wavelengths) on top of the silicon-on-insulator waveguide substrate. This is achieved by bonding III-V dies onto the SOI waveguide circuit using a polymer bonding layer (DVS-BCB). After pick-and-placing the individual III-V dies onto the SOI, the original InP growth substrate is removed, leaving only a thin epitaxial InP/InGaAsP film attached to the SOI waveguide circuit. After this bonding process, the opto-electronic components (laser diode and photodetectors) are fabricated, again on a wafer scale and lithographically aligned to the underlying SOI waveguide circuit. Integrated photodetectors, integrated Fabry-Perot lasers and integrated microdisk lasers were fabricated and optically coupled to the underlying SOI waveguide circuit.. An III-V epitaxial layer structure bonded onto an SOI waveguide structure is shown in figure 5, together with a top view of a bonded Fabry-Perot laser diode.

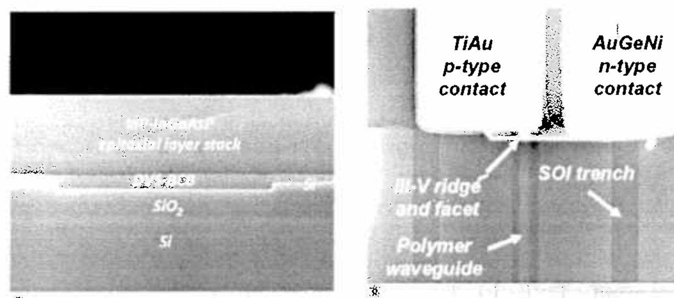

Figure 5: InP/InGaAsP film bonded onto an SOI waveguide circuit and top view of a bonded Fabry-Perot laser

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