Heterogeneous Integration of III-V Active Devices on a Silicon-on-Insulator Photonic Platform

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***Abstract*— We present the heterogeneous integration of III-V active opto-electronic devices on top of a silicon-on-insulator photonic integrated circuit. This is achieved by adhesive die-to-wafer bonding of an unprocessed InP/InGaAsP epitaxial layer structure, after which laser diodes and photodetectors were fabricated in the bonded layer and optically coupled to the underlying silicon-on-insulator waveguide circuit.**

I. INTRODUCTION

Silicon-on-insulator (SOI) provides a platform for high density integrated optics due to the high refractive index contrast between silicon core and SiO_2 cladding ($\Delta n \cong 2$). These integrated circuits can be fabricated in a reliable way by using standard CMOS technology, enabling mass-fabrication and cost reduction due to the economy of scale [1]. Even the monolithic integration of electronic and photonic integrated circuits can be envisioned. While interesting for passive optical functions (waveguiding, optical filters, power splitting,…) and active optical functions like modulation and switching, the indirect band gap of silicon hampers efficient light emission and amplification. As silicon is transparent at telecommunication wavelengths, also photodetection requires alternative solutions. While there are significant efforts to achieve light emission and amplification from silicon, either by modifying the silicon on a nano-scale [2] or by exploiting its nonlinear optical properties [3], the devices presented so far either rely on or can not compete with III-V semiconductor based light emitting devices available today. On the photodetection side, a lot of effort is put in developing SiGe or pure Ge based photodetectors [4]. However, InGaAs has an unchallenged position in low dark current, high speed and high sensitivity integrated near-infrared photodetectors. Combining these observations leads to the conclusion that heterogeneously integrating III-V material on top of a silicon-on-insulator photonic integrated circuit can combine best of both worlds. As an additional advantage of using the silicon-on-insulator material system was the ability to use CMOS mass-fabrication technology, the integration of III-V devices on top of the SOI waveguide circuit should not compromise mass-fabrication. Therefore, in this paper, the transfer of III-V epitaxial layers to the SOI wafer by means of a die-to-wafer bonding process is proposed, which has the advantage that, after bonding of the unstructured epitaxial layers, the III-V opto-electronic components can be fabricated, lithographically aligned to the underlying SOI circuits using CMOS technology. The proposed integration process is presented in figure 1.

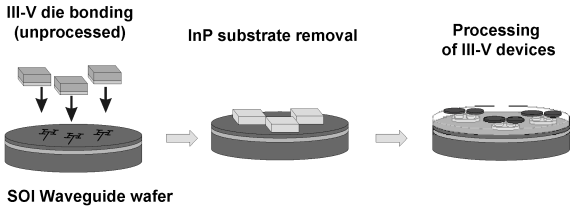

Fig. 1. Processing scheme for heterogeneously integrating III-V opto-electronic devices on top of SOI waveguide circuits

Several bonding approaches can be envisioned for the heterogeneous integration process. While molecular bonding is a well established technology for the fabrication of silicon-on-insulator wafers, the requirements of wafer surface quality to achieve molecular bonding are often hard to meet for epitaxially grown III-V wafer surfaces. Therefore, in this paper we will present an adhesive die-to-wafer bonding process using DVS-BCB, for which the requirements on surface quality are far less strict [5].

II. DVS-BCB ADHESIVE DIE-TO-WAFER BONDING

Several adhesives can be envisioned for the heterogeneous integration process. An important factor in the choice of adhesive is the temperature stability of

the material. We selected DVS-BCB, a thermosetting polymer with a glass transition temperature up to 400C for the integration process. Besides the high temperatures it can sustain, it has excellent planarization properties (in order to planarize the SOI waveguide topography), it has a low curing temperature (250C) which limits the thermal stress in the bonded stack, it is transparent for near-infrared wavelengths, it doesn't outgas upon curing and is resistant to a wide range of chemicals. The DVS-BCB adhesive die-to-wafer bonding process consists of a sequence of processing steps as shown in figure 2.

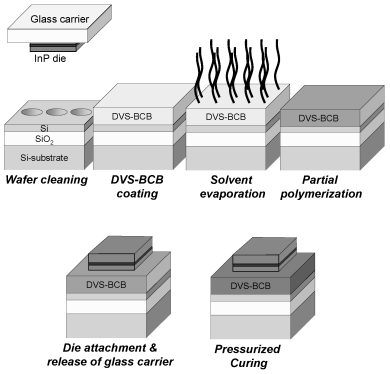

Fig. 2. Sequence of processing steps for adhesive DVS-BCB die-to-wafer bonding

The cleaning of both the III-V die surface (which is temporarily attached to a glass carrier for ease of handling) and the SOI wafer surface was optimized in order to remove pinned particles from the bonding interface, which would otherwise result in large unbonded areas, and to avoid organic contamination of the surfaces, which reduces the adhesion of the DVS-BCB. On the SOI wafer surface, a Standard Clean 1 solution ($1NH_3$:$4H_2O_2$:$20H_2O$ at 70C) was used to lift off particles and to render the surface hydrophilic. On the III-V side, the removal of a sacrificial InP/InGaAs layer pair using 3HCl:H_2O and $1H_2SO_4$:$3H_2O_2$:$1H_2O$ respectively, resulted in particle and contamination free surfaces. The DVS-BCB layer is spin-coated afterwards onto the SOI waveguide circuit. For the devices that will be presented in Section III, a bonding layer thickness (defined as the spacing between the bottom of the III-V layer and the top of the SOI waveguide layer) in the order of 200-300nm is required. As no commercially available DVS-BCB solution exists to obtain these thin layers, a custom solution was formulated by diluting the commercial CYCLOTENE 3022-35 with mesitylene (2DVS-BCB:3Mes). A double spin coating procedure was used resulting in an aggregate bonding layer thickness of 300nm and a degree of planarization of over 95% over a 220nm high waveguide topography. After spincoating the DVS-BCB layer, the mesitylene solvent is evaporated by a short baking step at 150C, after which the DVS-BCB is transformed from a liquid to a sol-gel rubber by baking for 2 minutes at 250C in a nitrogen ambient. After rendering the III-V surface hydrophilic by immersion into a HF solution, the III-V die and the SOI waveguide circuit are attached and cured at 250C for 1 hour under a uniform pressure of 300kPa in order to intimately contact both surfaces. After curing, the InP growth substrate is removed using a combination of mechanical grinding and wet chemical etching using 3HCl:H_2O until an InGaAs etch stop layer is reached.

III. Integrated III-V devices coupled to SOI

After transfer of the InP/InGaAsP epitaxial layer structures, both laser diodes and photodetectors were integrated on and coupled to the underlying SOI waveguide circuit. 500μm long Fabry-Perot type laser diodes were fabricated and an adiabatic inverted taper coupling scheme based on a polymer waveguide overlay was used to collect the light exiting the laser facet into the SOI waveguide. Only pulsed operation was obtained due to the large thermal resistance of the DVS-BCB bonding layer. 1mW optical power (at a wavelength of 1.55μm) was coupled into the SOI waveguide circuit [6]. In order to circumvent the problem of the low thermal conductivity of the DVS-BCB, an integrated heat sink structure was designed and fabricated, as shown in figure 3. This heat sink structure, consisting of a plated top gold contact that is contacted through the DVS-BCB bonding layer in order to obtain a thermal via, allowed continuous wave operation of the bonded devices at room temperature [7]. By reverse biasing this laser diode structure, photodetection operation could be obtained. A

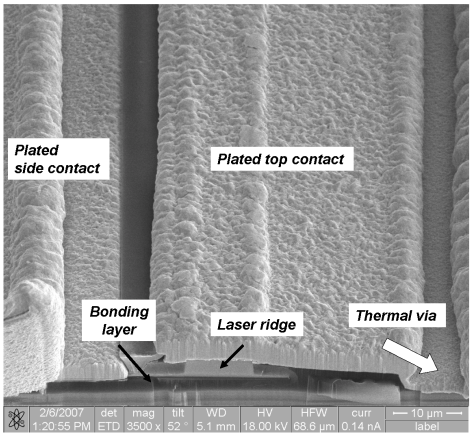

Fig. 3. SEM image of a DVS-BCB bonded Fabry-Perot laser diode with an integrated heat sink structure

responsivity of 0.23A/W for a 50µm long device was measured at a wavelength of 1.55µm. While this type of photodetector is interesting in the cases where the photonic integrated circuit requires both laser diodes and photodetectors, the processing is relatively complex. Therefore, a new type of III-V photodetector integrated on top of the SOI waveguide circuit was designed and fabricated, showing easier processing and higher responsivity. The fabricated photodetector structure is shown in figure 4 and is a waveguide-coupled metal-semiconductor-metal photodetector, consisting of an InGaAs absorption layer and two TiAu Schottky-contacts.

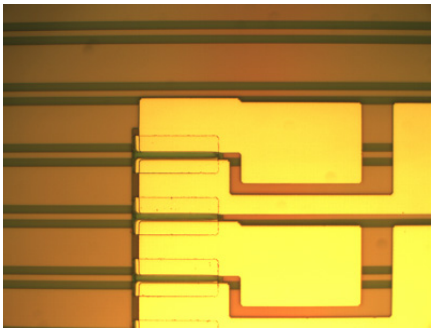

Fig. 4. Microscope image of a metal-semiconductor-metal InGaAs photodetector coupled to an underlying SOI waveguide circuit

In order reduce the Schottky-contact leakage current, an InAlAs Schottky barrier enhancement layer (SBEL) was added on top of the InGaAs absorption layer. Optical coupling between the SOI waveguide layer and the III-V photodetector is achieved by a vertical directional coupler mechanism. The processing sequence consists of a die-to-wafer bonding step as outlined in section II until an InGaAs etch stop layer is reached. This etch stop layer on top of an InP sacrificial layer is removed by a selective wet etch using H_2SO_4:H_2O_2:H_20 and finally, the InP sacrificial layer on top of the 40nm InAlAs barrier enhancement layer is removed using 1HCl:1H_3PO_4:2CH_3COOH. The detector mesa is etched down to the DVS-BCB bonding layer by means of non-selective wet etching using 1H_3PO_4:1H_2O_2:20H_2O. In a next step, a DVS-BCB insulation layer is spun and a contact window is opened above the detectors. Native oxide from the exposed InAlAs layer is removed by a 20s dip in 1NH_4OH:10H_2O and finally, the coplanar Schottky contacts are defined. The 3µm spacing between the coplanar Schottky contacts equals the SOI waveguide width. The dark current of the device was 3.0nA at a bias voltage of 5V (for a device length of 25µm), while the detector responsivity is 1.0A/W at 1.55µm and a bias voltage of 5V [8]. These measurement results are in good comparison with previous reported simulation results. The dark current of this device is at least 100 times lower as compared with previous reported results of III-V-on-SOI detectors [9] and Ge-on-SiN detectors [4].

IV. Towards Compact Laser Sources

While the previous presented integrated laser diodes provided high optical power to the SOI waveguide circuit, its device footprint is relatively large. In some applications like intra-chip optical interconnect or digital photonic applications, preferably small footprint laser diodes are required, at the expense of lower output power. While recently demonstrated using molecular die-to-wafer bonding, the concept of integrating a microdisk laser structure on top of and evanescently coupled to the SOI waveguide circuit can be achieved using DVS-BCB bonding as well [10]. The issue of device heating can be tackled in the same way as discussed in section III.

V. Acknowledgements

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VI. References

[1] W. Bogaerts et al., "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology", *Journ. of Lightwave Technology*, Vol. 23(1), pp. 401 – 412, 2005.

[2] L. Pavesi, Will silicon be the photonic material of the third millenium?, *Journ. of Physics-Condensed Matter*, Vol. 15(26): pp. R1169-R1196, 2003.

[3] H.S. Rong et al., Monolithic integrated Raman silicon laser. *Optics Express,* Vol. 14(15): pp. 6705-6712, 2006.

[4] D. Ahn et al., High performance, waveguide integrated Ge photodetectors, *Optics. Express*, vol. 15, pp. 3916-3921, 2007.

[5] G. Roelkens et al., Adhesive bonding of InP/InGaAsP dies to processed silicon-on-insulator wafers using DVS-bis-benzocyclobutene, *Journal of the Electrochemical Society*, vol. 153, pp. G1015-G1019, 2006.

[6] G. Roelkens et al., Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a silicon-on-insulator waveguide circuit, *Optics Express* **14**(18): p. 8154-8159, 2006.

[7] G. Roelkens et al., Continuous-wave lasing from DVS-BCB heterogeneously integrated laser diodes, *IPNRA 2007.*

[8] J. Brouckaert et al., Compact InAlAs/InGaAs metal-semiconductor-metal photodetectors coupled with SOI waveguides, submitted for publication in Photonics Technology Letters

[9] G. Roelkens et al., Integration of InP/InGaAsP photodetectors onto silicon-on-insulator waveguide circuits, *Optics Express* 13, p. 12, 2005.

[10] J. Van Campenhout et al., Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit, accepted for publication in Optics Express