Workshop on Silicon Photonics
Mainz, November 10 2006

Silicon-on-Insulator based Nanophotonics
Why, How, What for?

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Photonics Research Group

Overview

- Introduction to SOI nanophotonics
- Why?
- What for?
- How?
- Conclusions

The key bottleneck of photonic integration

(By far too) many degrees of freedom

- many different materials
- many different component types
- many different wavelength ranges

Hence:

- no generic integration technology for many different applications
- no high volume technology platforms
- too high cost

Hence:

Integration is not an industrial reality (yet)

The way out - a roadmap

1. Use mainstream Silicon(-based) technology
   - wherever possible, CMOS fab compatible
   - otherwise, use dedicated Silicon fab
2. Add other materials where needed
   - for specialty functions
   - if the added value motivates it
3. By using
   - wherever possible : wafer-scale front-end and back-end technology
   - otherwise, die-scale technology
4. Build a photonic IC industry on this basis

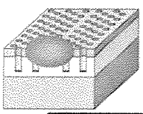
SOI nanophotonic waveguides

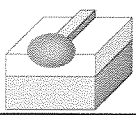
Nanophotonics

- High index contrast: photonic crystals, photonic wires
- Strong confinement: small waveguide cores, sharp bends

Silicon-on-insulator

- Transparent at telecom wavelengths (1550, 1300nm)
- High refractive index contrast 3.45 (Silicon) to 1.0 (air)





Both cases:
• feature size : 50-500 nm
• required accuracy of features: 1-10 nm
NANO-PHOTONIC waveguides

SOI-nanophotonic wires

Group	Date	h [nm]	w [nm]	loss [dB/cm]	BOX [um]	top clad	Fab.
IMEC	Apr. '04	220	500	2.4	1	no	DUV
IBM	Apr. '04	220	445	3.6	2	no	EBeam
Cornell	Aug. '03	270	470	5.0	3	no	EBeam
NTT	Feb. '05	300 200	300 400	7.8 2.8	3	yes	EBeam
Yokohama	Dec. '02	320	400	105.0	1	no	EBeam
MIT	Dec. '01	200	500	32.0	1	yes	G-line
LETI / LPM	Apr. '05	300 200	300 500	15.0 5.0	1	yes	DUV
Columbia	Oct. 03	260	600	110.0	1	yes	EBeam
NEC	Oct. '04	300	300	19.0	1	yes	EBeam

And many others ...

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Why?

imec

Why?

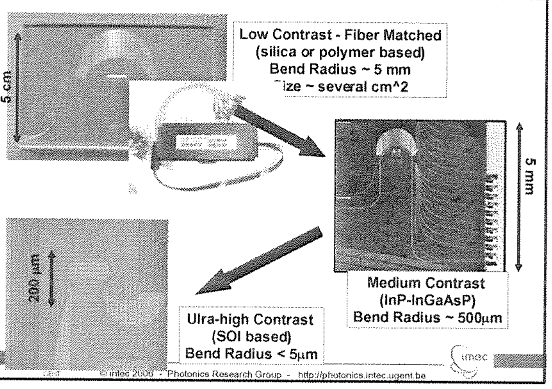
3 sets of good reasons:

- Functionality + performance
- Technology
- Cost

Or why not?

- The polarisation problem
- The extreme accuracy problem
- The source problem

Increasing Index Contrast



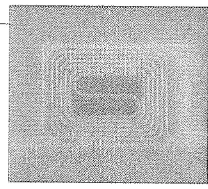
Bend losses

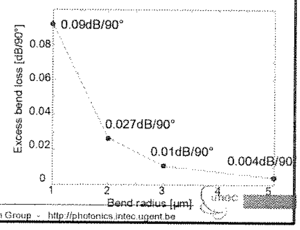
Increase for narrower waveguides:

- Weaker confinement: bend radiation
- More sensitive to roughness

Increase for smaller bend radii

e.g. wire width = 540nm





Technology

Need:

- smallest feature size : 50-500 nm
- required accuracy of features: 1-10 nm
- required aspect ratios: mostly < 1:1

This matches amazingly well with the capabilities of advanced CMOS

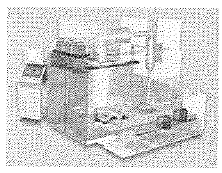
Fabrication with deep UV Litho

248nm excimer laser Lithography

- ASML PAS 5500/750 Step-and-scan
- Automated in-line processing (spin-coating, pre- and post-bake, development)
- 4X reticles
- Standard process

193nm excimer laser Lithography

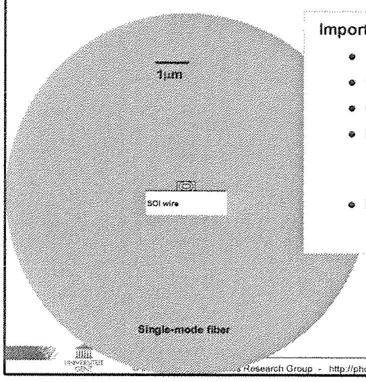
- ASML PAS 5500/1100 Step-and-scan
- 4X reticles



Low cost

- Wafer-scale fabrication on large wafers with high yield
- Wafer-scale testing
- Low cost packaging

Coupling into SOI nanophotonics

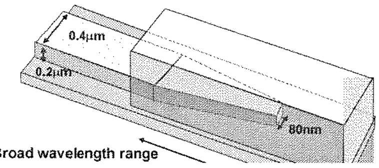


Important:

- Low loss
- Large bandwidth
- Coupling tolerance
- Fabrication
  - Limited extra processing
  - Tolerant to fabrication
- Polarization

Coupling to fiber – Inverse taper

Inverse taper



- Broad wavelength range

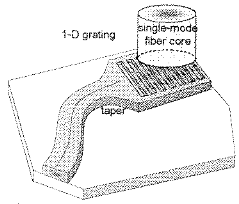
polished

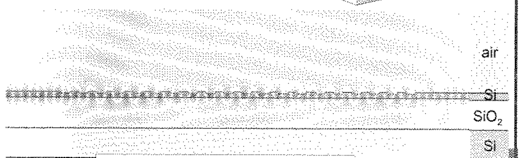
Group	h [nm]	w [nm]	L [um]	tip width [nm]	Cladding Material	Cladding Size	Loss
IBM	220	445	150.0	75.0	Polymer	2x2	< 1dB
Cornell	270	470	40.0	100.0	SiO2	2x00	< 4dB
NTT	300	300	200.0	60.0	Polymer/Si 3N4	3x3	0.8

Vertical Fibre Coupler

1-D grating

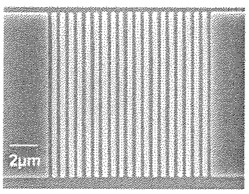
- Butt-coupled
- Period ~ 600 nm
- 20 periods
- Etch depth = 45 nm
- Simple design: 31% coupling
- Bandwidth: ~ 50nm

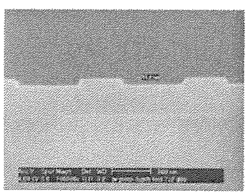




Taillaert et al, JQE 38(7), p. 949 (2002)

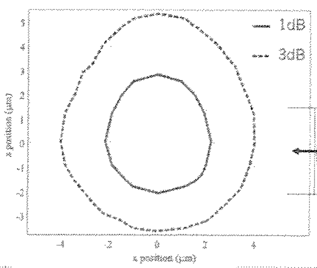
Vertical fibre coupler

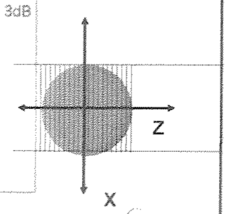




Alignment tolerances

- good alignment tolerances
- measurement of P/P_{max} versus fiber position





Taillaert et al, JQE 38(7), p. 949 (2002)

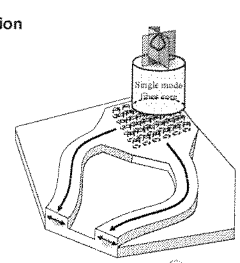
The polarisation problem

High index contrast makes polarisation independence (almost) impossible.

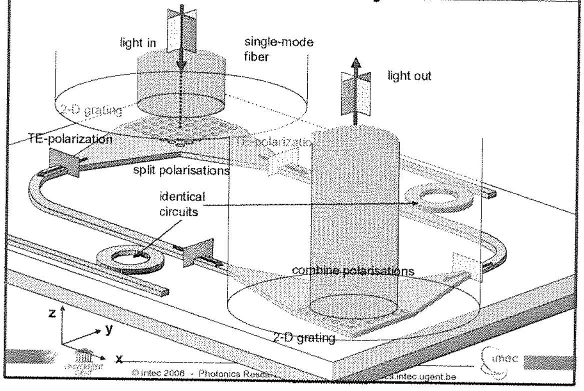
2D grating fiber coupler – polarisation splitter

Fiber to waveguide interface for polarisation independent photonic integrated circuit

- 2D grating
- couples each fiber polarisation in its own waveguide
- in the waveguides the polarisation is the same (TE)
- Allows for polarisation diversity approach



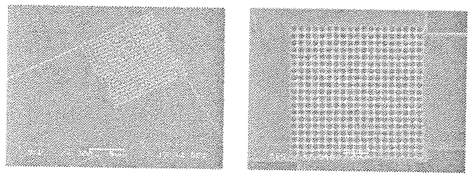
Polarisation Diversity Circuit



Experimental results

Fabrication

- SOI: 220nm Si / 1000nm SiO_2
- Etch depth: 90nm
- Square lattice of holes: 580nm period



The extreme accuracy problem

High index contrast components:

- interference based filters,

$$\frac{\partial \lambda}{\lambda} \approx \frac{\partial d}{d}$$ with d the waveguide width (≈λ)

- cavity resonance wavelength

$$\frac{\partial \lambda}{\lambda} \approx \frac{\partial d}{d}$$ with d the cavity length (a few λ)

- photonic crystal

$$\frac{\partial \lambda}{\lambda} \approx \frac{\partial d}{d}$$ with d the hole diameter (≈λ)

if tolerable wavelength error : 1 nm
⇓
tolerable length scale error : (of the order of) 1 nm

The source problem

How to integrate sources:

- that are compact
- that are efficient
- that have high modulation bandwidth
- by means of wafer-scale processes

??????????????????????????????????????

Approaches: gain from

- optical pumping
  - Raman gain
  - Four wave mixing gain
  - Nanocrystals
- electrical pumping
  - nanocrystals?
  - Impurity doped Silicon?
  - bonded III-V layers : most successful approach to date

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What for?

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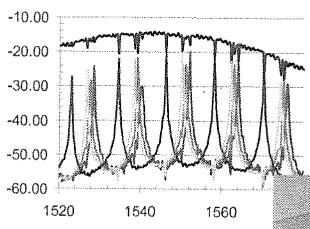
Applications

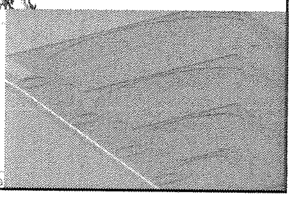
- Transceivers
- WDM components
- Intra-chip optical interconnect
- Sensors
- Digital photonics
- ...

Optical Ring Resonators



Ring resonator demux

- 4 rings in series
- Linearly increasing radius
- λ_0 does not increase linearly as expected !!
- Fabrication problem: mask discretisation

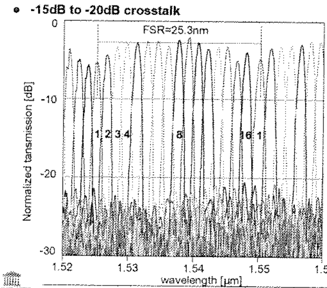


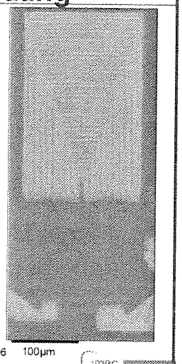
Arrayed Waveguide Grating

16-channel AWG, 200GHz

200µm x 500µm area

- -3dB insertion loss
- -15dB to -20dB crosstalk

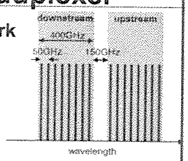


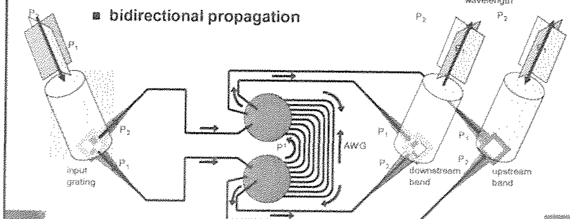


Polarization diversity duplexer

Duplexer for WDM-PON access network

- Polarization diversity approach
- 2-D fiber couplers: polarization splitting
- AWG:
  - 2 x 400GHz bands
  - bidirectional propagation

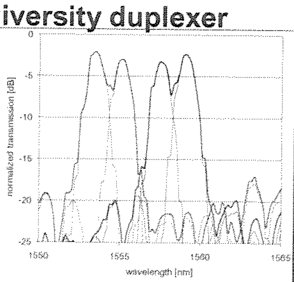


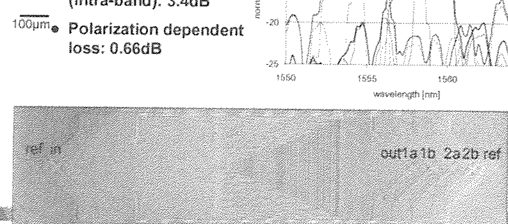


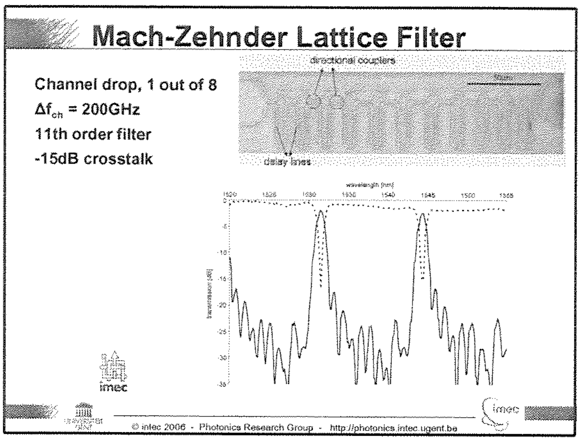
Polarization diversity duplexer

Results:

- Crosstalk: -15dB
- Insertion loss: -2.2 to -5.6dB
- Nonuniformity (intra-band): 3.4dB
- Polarization dependent loss: 0.66dB






Mach-Zehnder Lattice Filter
Channel drop, 1 out of 8
Δf_ch = 200GHz
11th order filter
-15dB crosstalk
directional couplers
delay lines
imec
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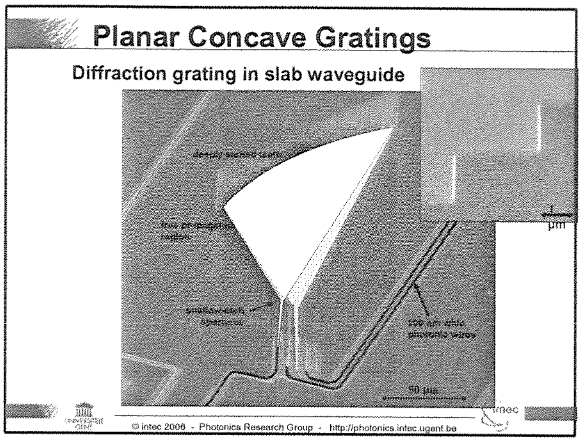
Planar Concave Gratings
Diffraction grating in slab waveguide
50 µm
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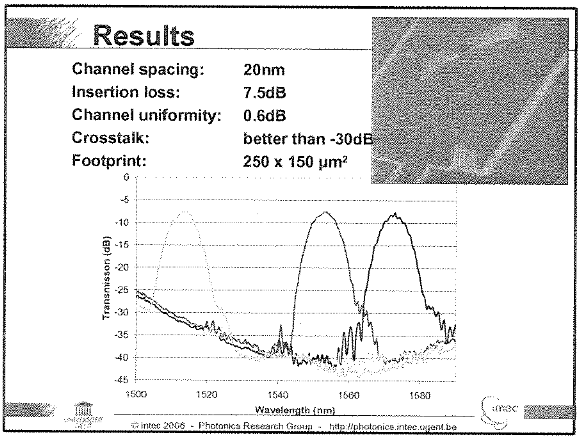
Results
Channel spacing: 20nm
Insertion loss: 7.5dB
Channel uniformity: 0.6dB
Crosstalk: better than -30dB
Footprint: 250 x 150 µm²
Transmission (dB)
Wavelength (nm)
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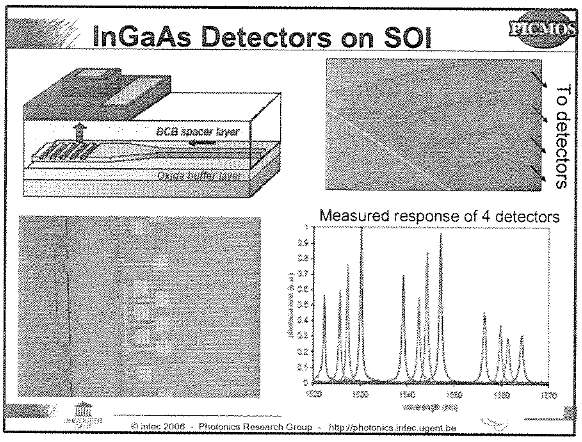
InGaAs Detectors on SOI
PICMOS
BCB spacer layer
Oxide buffer layer
To detectors
Measured response of 4 detectors
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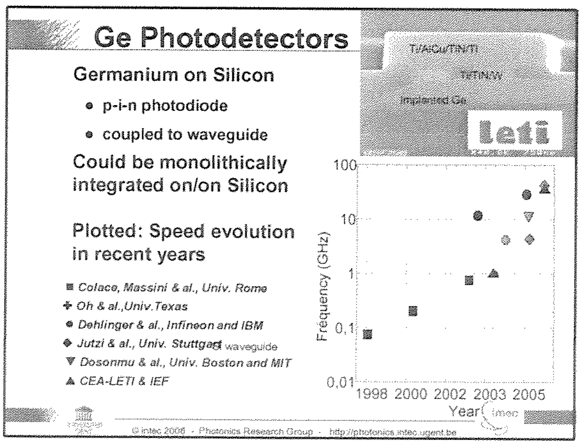
Ge Photodetectors
Germanium on Silicon
p-i-n photodiode
coupled to waveguide
Could be monolithically integrated on/on Silicon
Plotted: Speed evolution in recent years
Colace, Massini & al., Univ. Rome
Oh & al.,Univ.Texas
Dehlinger & al., Infineon and IBM
Jutzi & al., Univ. Stuttgart waveguide
Dosonmu & al., Univ. Boston and MIT
CEA-LETI & IEF
Ti/AlCu/TiN/Ti
Ti/TiN/W
Implanted Ge
leti
Frequency (GHz)
Year
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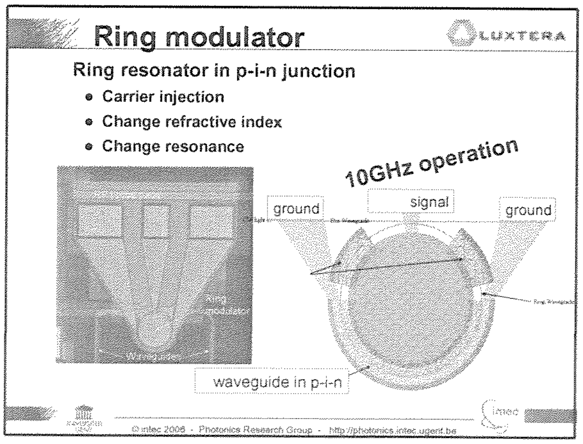
Ring modulator
LUXTERA
Ring resonator in p-i-n junction
Carrier injection
Change refractive index
Change resonance
10GHz operation
ground
signal
ground
waveguide in p-i-n
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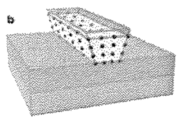
Strained Silicon

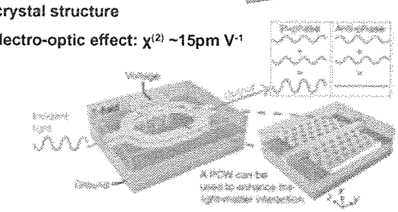
Silicon:

- centrosymmetric crystal structure
- no electro-optic effect

Apply Si_3N_4 strain layer

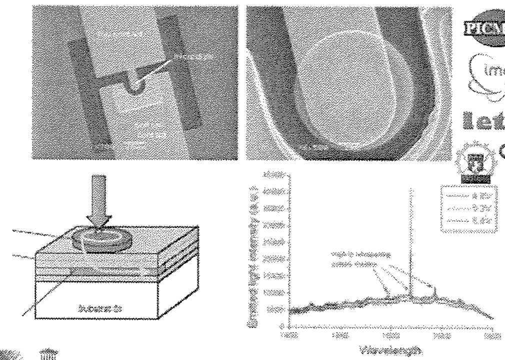
- Deform crystal structure
- Induce electro-optic effect: $\chi^{(2)}$ ~15pm V^{-1}





Jacobson et al., nature 04706 (May 2006)

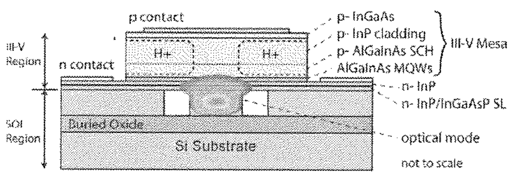
Electrically pumped InP μdisk laser



"Hybrid Silicon Laser"

AlGaInAs membrane bonded on SOI wafer

- length ~800μm
- Cavity defined only by silicon waveguide (no critical alignment)

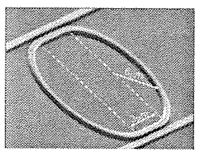


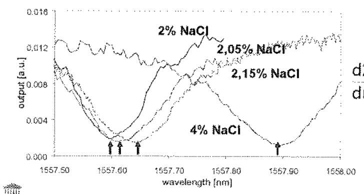
Fang et al. OpEx 14(20), p. 9203 (2006)

SOI microring sensor

Measure salt concentration

- Fluid overcladding
- Refr. index ~ Salt concentration
- Response of ring ~ refr. index
- Q = 20000 → minimum Δn ~ 5.10^{-5}





$\frac{d\lambda}{dn}$ = 86,6nm/RIU

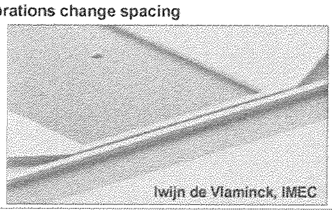
SOI NEMS Vibration Sensor

SOI directional coupler

- 2 waveguides close together: light leaks
- coupling efficiency ~ waveguide spacing

Freely Suspended directional coupler

- Oxide removal
- Vibrations change spacing



Iwijn de Vlaminck, IMEC

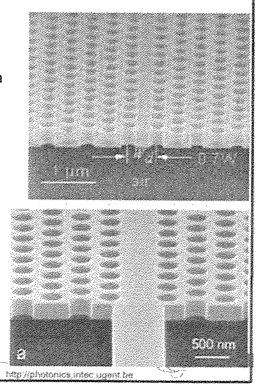
Photonic Crystals

NTT

- E-beam lithography
- Low propagation losses: 6dB/cm
- Low-loss interface to fiber

IBM

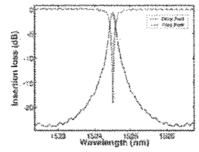
- In-house CMOS processes
- e-beam lithography is the only out-of-the-line step
- Photonic crystals: low propagation losses
- Slow light in Photonic crystals (Nature, 3/11)

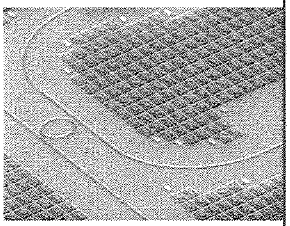


Integration with CMOS

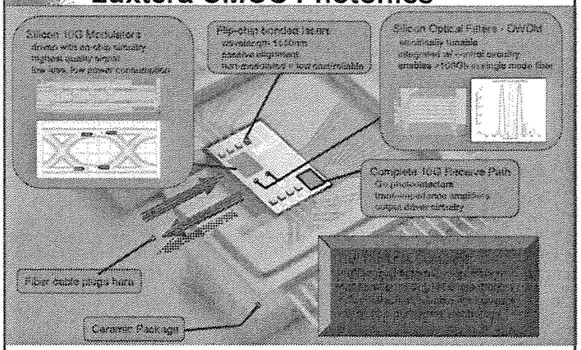
Luxtera

- Fabless Silicon Photonics (Fabrication by Freescale)
- Integration of CMOS and photonic circuits: Waveguides are defined together with transistor gates
- Low-loss rib waveguide
- Grating fiber couplers





Luxtera CMOS Photonics



LUXTERA

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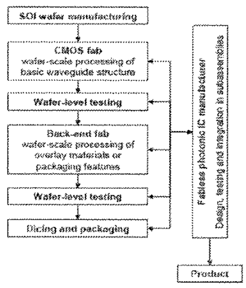
How?

Cost of ownership

Cost of ownership of advanced CMOS technology is too high for:

- most research entities in Silicon photonics
- most photonic component companies

Hence the need for a fabless model



THE challenge of Silicon photonics

CMOS

- large, mature technology base
- strong, focused innovative drive
- large organisations, big budgets

Challenge: overcome this mismatch with a critical mass

Silicon Photonics

- Recent rapid progress
- (still) relatively small actors
- limited budgets

Successful industrial deployment requires extensive interaction between CMOS and photonics community

Silicon Photonics Platform

Network of Excellence ePIXnet develops platforms for photonic integration:

- Silicon photonics platform
- InP photonics platform
- Nanostructuring platform
- Packaging platform
- High speed measurement platform
- Modelling platform

www.epixnet.org

Si Photonics platform

Long-term objective:

- to enable a route towards commercial deployment of silicon photonics.

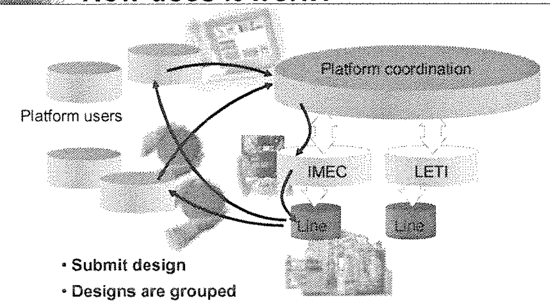
Methodology:

- *Facility Access Programme (foundry service) for Research and Prototyping*:
  - Making mature fabrication processes on high-end industrial CMOS tools available to many research groups or projects
  - Sharing masks and processing: dramatic cost reduction
- *Roadmap for Silicon Photonics Technologies:*
  - Identifying the challenges and evolutionary solutions in this field
- *Commercial Manufacturing Routes:*
  - Gradual involvement of commercial foundries
- *Promotion and lobbying*
  - For the field of Silicon photonics in the interest of Europe's position in this field.

Platform structure

- Steering group: strategic decisions
- Coordinator : daily operation
- Core fabrication partners
  - IMEC (Gent-Leuven)
  - CEA-LETI (Grenoble)
  - Other in the future?
- Members
  - Anybody interested in and committed to the mission
- Users
  - Those who use the foundry service

How does it work?



- Submit design
- Designs are grouped
- Designs are fabricated
- Wafers are distributed

What does the platform offer?

Passive SOI waveguide circuits:

- Users supply layout (subject to some design rules)
- Standard SOI wafers
- Patterning (DUV litho) and etching

Process modules:

- set of standard processing steps (strict design rules)
- designs (mask) supplied by platform
- examples:
  - grating fiber couplers (IMEC)
  - Future: Ge photodetectors (LETI)

Custom processing steps:

- users supply own design and requirements
- few boundary conditions on designs
- examples:
  - SiGe and Ge epitaxy
  - amorphous Silicon deposition (+ patterning)

Summary

SOI Photonics

- Nanophotonic high index contrast waveguides open up a new paradigm in photonic integration
- The use of the mature silicon CMOS technology base provides an enormous opportunity
- But the cost of ownership of CMOS technology is a barrier

Silicon Photonics Platform

- Support transition to industrial deployment of Silicon photonics
- By building a fabless industry model
- By organizing a foundry service for Research & Prototyping
- Affordable by cost sharing

PROGRAM

8.30 **Registration**

9.00 **Welcoming and Opening**

Prof. Dr. Manfred Helm, Forschungszentrum Rossendorf, Dresden, Germany

9.10 **Silicon-on-insulator based nanophotonics: why, how and what for?**

- The merits of high index contrast waveguiding structures
- The merits of Silicon-based approaches
- Challenges in SOI nanophotonics
- Applications of SOI nanophotonics

Prof. Dr. Ir. Roel Baets, Dries Van Thourhout, Wim Bogaerts, University of Ghent – INTEC, Belgium

9.40 **Silicon-on-insulator based planar lightwave technology**

- Optical board technology
- Hybrid integration
- C-WDM transceiver
- Silicon based optical components

Prof. Dr. Klaus Petermann, Technical University of Berlin, Germany

10.10 **Low loss amorphous silicon-on-insulator waveguides and components**

- a-Si film deposition
- Absorption of film waveguides
- Properties of multi and single mode waveguides
- Splitters and couplers

Prof. Dr.-Ing. Jörg Müller, Technical University of Hamburg-Harburg, Germany

10.40 **Coffee Break**

11.00 **Photonic integrated circuits based on silicon waveguides**

- Traditional and multistep patterning
- Bends, mirrors, tapers, couplers and switches
- 3x3 switch matrix and 8-channel AWG
- Fiber and laser coupling

Dr. Timo Aalto, VTT Technical Research Centre of Finland, Espoo, Finland

11.30 **Monolithic silicon photoreceivers**

- Photodetectors in Standard Silicon Technologies
- Photodetectors in Modified Silicon Technologies
- Bipolar, CMOS, and BiCMOS Photodiode ICs (PDICs)
- New Circuit Concepts for PDICs

Prof. Dr. Horst Zimmermann, Technical University of Vienna, Austria

12.00 **Silicon-based photodetectors for high-speed integrated optical receivers**

- Ge/Si photodetectors – results and challenges
- Speed limitations of integrated detectors
- Quantum well and quantum dot structures
- Resonant cavity enhancement

Prof. Dr. Erich Kasper, University of Stuttgart, Germany

12.30 **Lunch Break**

13.20 **The present status on the way towards a silicon laser**

- limitations and potentialities of silicon
- silicon nanocrystals for lasins
- impurity doped silicon for lasing
- hybrid approaches to a silicon laser

Prof. Dr. L. Pavesi, University of Trento, Italy

13.50 **Silicon MOS light emitters by rare earth doping**

- Why MOS light emitters
- Advantages of rare earth doping
- Optimisation features
- Application purposes: Towards bioapplications

Dr. W. Skorupa, Forschungszentrum Rossendorf, Dresden, Gemany

14.20 **Fabrication aspects on the combination of photonics and electronics**

- Challenge for adding photonics on a CMOS circuit

Dr. J. M. Fedeli, CEA-LETI, Grenoble, France

14.50 **Coffee Break**

15.10 **Silicon based photonic crystals**

- Photonic crystal physics
- Ridge-waveguide vs. photonic crystal waveguides
- Dispersion properties, coupling issues and losses of photonic crystal waveguides
- Application of photonic crystal waveguides such as DC, modulators etc.

Prof. Dr. Ralf Wehrspohn, University of Paderborn, Germany

15.40 **Optical interconnects**

- Evolution and macrotrends of interconnects
- Current bottlenecks: Speed, Power, Integrity
- Fundamental, Material, Device, Circuit and Systems limits of interconnects
- Appealing features of optical interconnects

Dr. Z. Gaburro, University of Trento, Italy

16.10 **Integrated optical systems for lab-on-a-chip applications**

- Advantages of integrated optics in lab-on-a-chip systems
- Integration of planar waveguides and microfluidic channels
- Glass waveguides vs. polymer waveguides
- Applications

Dr. Klaus B. Mogensen, Technical University of Denmark

16.40 **Closing and the option to visit Sensitec-Naomi wafer fab** optence

Kompetenznetz
Optische Technologien
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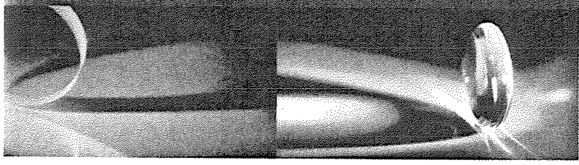

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