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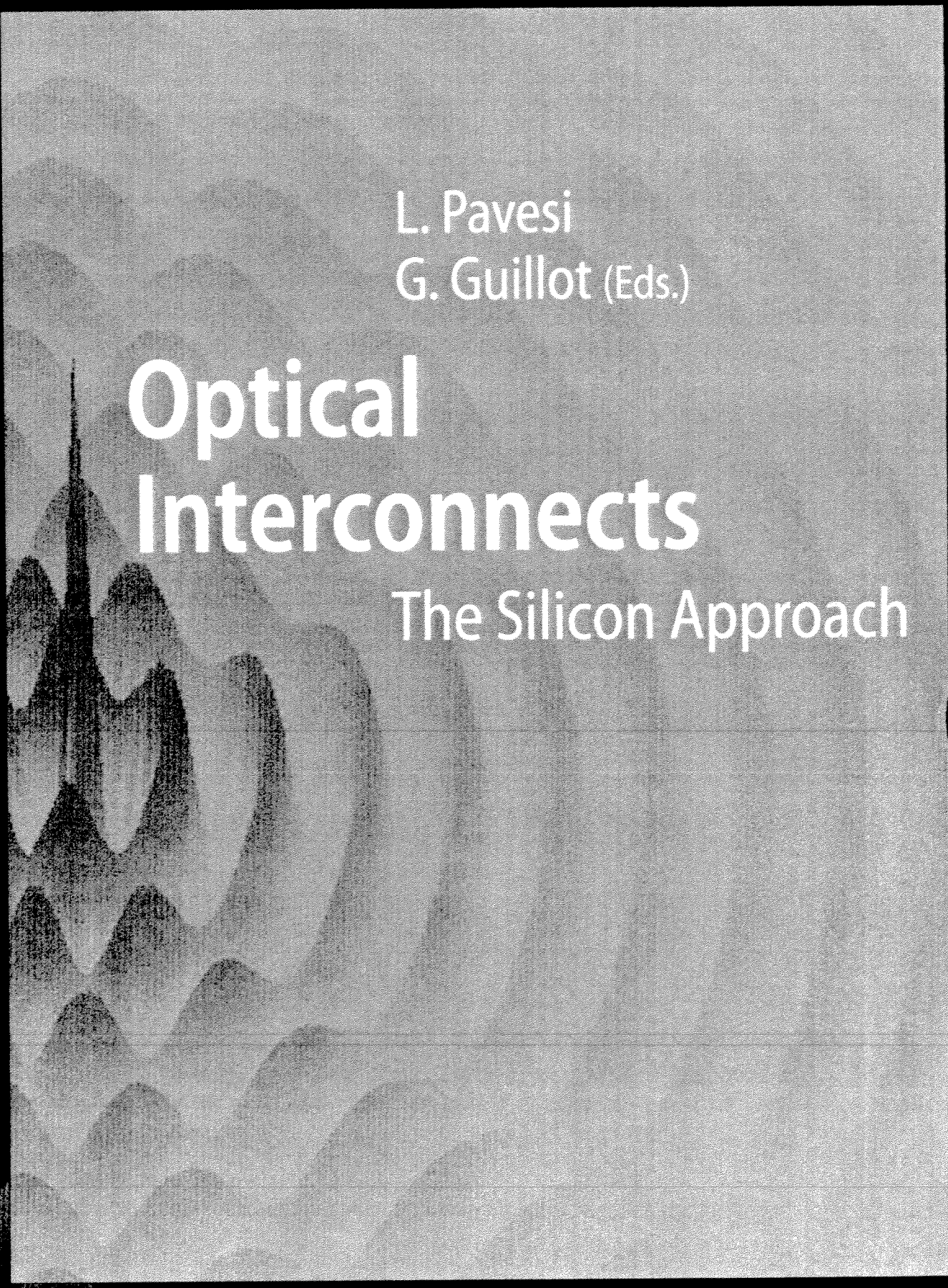

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Optical Interconnects

The Silicon Approach

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L. Pavesi
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Submicron Silicon Strip Waveguides

D. Van Thourhout, W. Bogaerts, and P. Dumon

Summary. Submicron silicon strip waveguides have recently attracted a lot of attention and are currently studied by several research groups. The use of submicron silicon strip waveguides allows realizing extremely compact photonic circuits, using standard CMOS-processing methods. Therefore, they are a promising candidate for fabricating future photonic ICs using a cost-effective and high-yield process. We review the state-of-the-art of submicron silicon strip waveguides, starting from its basic properties including the single mode condition, scattering losses, bend losses, and polarization behavior. Subsequently we review the fabrication methods employed for realizing these circuits and discuss the compatibility with advanced CMOS-fabrication methods. Then basic waveguide structures such as splitters and fiber couplers are studied. Finally some examples of more complex devices, including cascaded Mach-Zehnder interferometers and arrayed waveguide gratings are shown.

8.1 Introduction

While state-of-the-art electronic circuits have unit dimensions between a few tens of nanometers to a few micrometers for their basic functional blocks, the dimensions of photonic devices are typically much larger, varying from a few micrometer (e.g., for the core of a single mode fiber) to several centimeter (e.g., for arrayed waveguide grating routers). This huge size difference makes it not interesting in most cases to integrate electronics and photonics on a single substrate. To make optoelectronic integration more attractive there is a need for considerably more compact passive optical interconnect structures (waveguides, bends, splitters, combiners, etc.), more compact wavelength selective devices (high Q-resonators, highly dispersive elements), and more compact nonlinear functions. Realizing this requires the use of ultra-high optical index contrast waveguides. In the past, so-called super-high-Δ planar lightwave circuits (PLC) have been presented, with a 1.5% index contrast between the silica cladding and the germanium-doped waveguide core [1]. However, the minimum acceptable bending radius in this material system is still 2 mm and therefore, incompatible with tight optoelectronic integration. III–V

based waveguides allow a bending radius from 500 μm to a few tens of μm and very compact devices have been presented for so-called "deeply etched" waveguides, which were defined by etching completely through the high-index guiding layer and therefore show a very high lateral index contrast. However, when using a very small bending radius, light leaks out of the bend through the substrate because of the low vertical index contrast. To avoid this, also the vertical-index contrast has to be increased. Such a high-index contrast has been demonstrated in InP-based membrane type devices, GaAs/AlO_x based devices, and SOI-based devices, all of which consist of a thin high refractive index semiconductor core layer between low index cladding layers (dielectric or air) and allow for the realization of ultracompact waveguide elements.

An additional problem of photonic devices, however, is the fact that they, for several reasons, often suffer from a low yield compared to their electronic counterparts [2], which makes optoelectronic integration not very appealing. Therefore, it is important to adopt, as much as possible, fabrication methods and tools used in the silicon-based electronics industry. From this point of view, SOI-based devices show the most potential for integration with electronic devices and therefore form one of the most promising solutions for dense on-chip optical interconnects. These waveguides are typically fabricated starting from an SOI wafer, consisting of a silicon substrate, an SiO_2 box layer (thickness t_{box}), and a silicon guiding layer (thickness h). The waveguides are formed in this guiding layer. In some cases a SiO_2 cladding layer is deposited following the etch process. Figure 8.1 shows the basic waveguide structure. The most relevant parameters are the waveguide width w and the height h. Due to the extremely high-index contrast, these will typically be limited to a few hundreds of nanometer for single mode waveguides.

Table 8.1 gives a review of publications discussing submicron silicon strip waveguides, showing a strongly enhanced activity in this domain during the last few years. Two main categories of waveguide structures can be distinguished. Some groups are aiming to reach polarization independence by choosing the waveguide width equal to its height [14, 19, 23, 26]. Most groups, however, opt for an asymmetric guide with a core height varying between 200

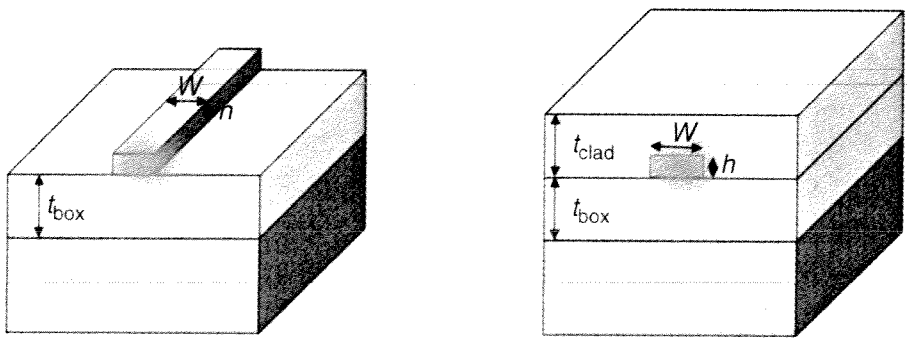

Fig. 8.1. Basic Silicon strip waveguide structure with air top cladding (*left*) and silica top cladding (*right*)

Table 8.1. Publication overview submicron SOI wires

aff.	date	h (nm)	w (nm)	loss (db cm^{-1})	box (um)	top clad	fab.	ref.
IMEC	Apr 2004	220	500	2.4	1	no	DUV	[3–7]
IBM	Apr 2004	220	445	3.6	2	no	EBeam	[8,9]
Cornell	Aug 2003	270	470	5.0	3	no	EBeam	[10,11]
NTT	Feb 2005	300	300	7.8	3	yes	EBeam	[12–14]
		200	400	2.8				
Yokohama	Dec 2002	320	400	105.0	1	no	EBeam	[15–19]
MIT	Dec 2001	200	500	32.0	1	yes	G-line	[20,21]
		50	200	0.8			+oxidation	
LETI / LPM	Apr 2005	300	300	15.0	1	yes	DUV	[22,23]
		200	500	5.0				
Columbia	Oct 2003	260	600	110.0	1	yes	EBeam	[24,25]
NEC	Oct 2004	300	300	19	1	yes	EBeam	[26]

and 340 nm and a width varying from 400 to 600 nm. The latter is in most cases determined by the single mode condition (see later). Reported losses for single mode waveguides vary from +100 dB cm^{-1} to less than 3 dB cm^{-1}. In [20] a 0.8 dB cm^{-1} loss was reported. However, the dimensions of this waveguide were too small to strongly confine the light and this wire can no longer be considered as a high contrast waveguide.

In Sect. 8.2 we will investigate the basic properties of submicron silicon strip waveguides. Unless otherwise noted all calculations were performed using $h = 220$ nm and $w = 500$ nm at a wavelength of 1550 nm and for TE-polarization. A full-vectorial mode-solver based on the film-matching method was used.

8.2 Basic Properties

8.2.1 Refractive Index, Group Index, Single Mode Condition

The refractive indices of the silicon core layer and the SiO_2 cladding at a wavelength of 1550 nm are, respectively, given by 3.45 and 1.46. Figure 8.2 shows the effective index for the lowest order TE-like and TM-like modes for a waveguide with a 220 nm high core as function of the waveguide width, respectively, without and with a SiO_2 overcladding. For the air cladded waveguide we see an anticrossing between the dispersion curves for the first-order TE-like mode and the zeroth-order TM-like mode at $w = 680$ nm and at this point the modes have a hybrid character. For a width $w = 600$ nm the first-order TE-like mode is cutoff and for smaller widths the waveguides are single mode. Adding a SiO_2 top-cladding slightly decreases the refractive index contrast. The single mode width is decreased to 480 nm.

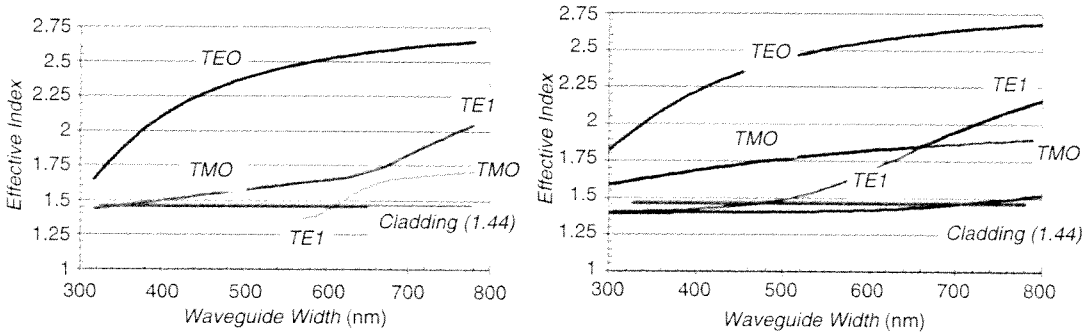

Fig. 8.2. Effective index of zeroth- and first-order mode for a waveguide with a 220 nm high core as a function of the waveguide width, respectively, without (*left*) and with (*right*) an SiO_2 overcladding

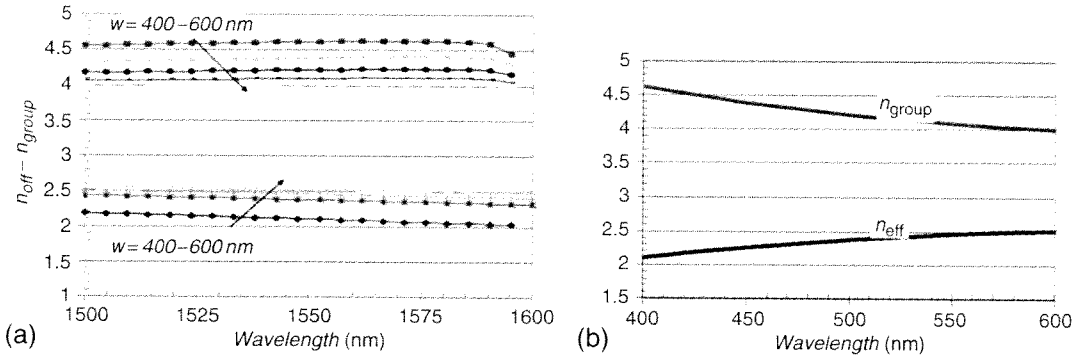

Fig. 8.3. Effective index and group index as a function of wavelength (**a**) and as a function of waveguide width (**b**)

The wavelength dependence of the silicon refractive index can be found in [27]. Since we are operating relatively far away from the bandedge the material dispersion is limited and negligible compared to the waveguide dispersion. Figure 8.3a shows the effective index and the group index ($n_g = n_{eff} - \lambda dn_{eff}/d\lambda$) as a function of wavelength. Because of the high waveguide dispersion, the group index is considerably higher than the effective index, which may be relevant when determining the latency of an optical link. Also important filter characteristics, such as the free spectral range of ring resonators and arrayed waveguide gratings (AWGs) are determined by the group index. Figure 8.3b gives the variation of the group index as a function of the waveguide width and shows an increase in the group index for smaller waveguides.

8.2.2 Losses

Published losses for single mode waveguides vary from a few db cm^{-1} to several hundreds of db cm^{-1} (see Table 8.1). The most relevant loss factors are fundamental material absorption (e.g., due to free carrier absorption),

substrate leakage (see Sect. 8.2.3), and scattering at interface roughness. The first two factors can be reduced to negligible values by, respectively, choosing sufficiently high resistivity wafers and a sufficiently high box layer thickness (see later). Reducing scattering losses requires careful process optimization to reduce sidewall roughness. Several authors have developed models to evaluate the influence of roughness on the propagation loss. Most authors agree that the scattering loss increases with index contrast and field strength but sources disagree on the exact relationship. Using the simple model proposed by Tien [28], the propagation loss is calculated as

$$\alpha_s \propto \frac{\sigma^2 E_s^2}{\int E^2 \mathrm{d}x} \Delta n^2. \tag{8.1}$$

With σ the interface roughness, E_s the electric field at the interface, and Δn the refractive index contrast. More advanced models also include the coherence length L_c of the roughness [29]. In [30] the loss due to scattering was calculated for square silicon wire waveguides as a function of their dimensions and for several values of roughness amplitude and correlation length. The calculated losses agree well with the values reported in literature. An example is given in Fig. 8.4. Due to the increasing intensity of the light at the sidewall interface, the losses are increasing considerably with decreasing waveguide width. However, at a certain critical width (~260 nm in Fig. 8.4), the light is no longer strongly confined in the waveguide core and the optical mode width starts increasing again, leading to a reduced loss. However, the reduced confinement also will result in an increased minimal acceptable bend radius and increased substrate leakage losses (see later).

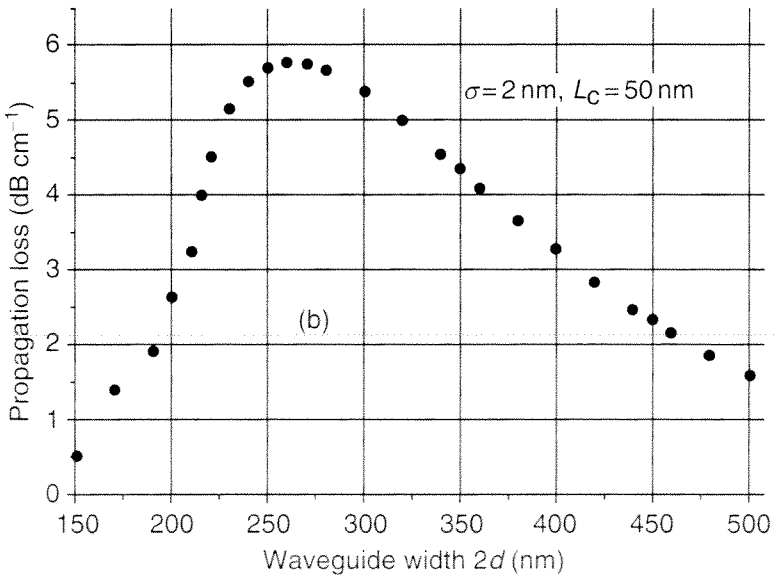

Fig. 8.4. Calculated propagation losses versus waveguide width for $\sigma = 2\,\mathrm{nm}$, $L_c = 5\,\mathrm{nm}$ (from [30])

In literature, values varying from $\sigma = 11\,\text{nm}$, $L_c = 70\,\text{nm}$ [19] to $\sigma = 2\,\text{nm}$, $L_c = 50\,\text{nm}$ [9] have been reported for the roughness standard deviation and coherence length, resulting in a corresponding reduction in losses from over $100\,\text{db}\,\text{cm}^{-1}$ to below $4\,\text{db}\,\text{cm}^{-1}$ for single mode waveguides. Figure 8.5 shows the measured waveguide loss as function of waveguide width for waveguides fabricated in our facilities (crosses, [3]), demonstrating the expected increase in loss for smaller width waveguides. The data point indicated by the black square is taken from [9], the data point indicated by the black diamond is taken from [14].

Figure 8.6 shows the loss for a waveguide with height $h = 220\,\text{nm}$, width $w = 450\,\text{nm}$ and a box layer thickness of $2\,\mu\text{m}$, as function of the wavelength (taken from [9]). The minimal loss is observed around 1450–1500 nm. For higher and lower wavelength values, the loss increases considerably. According to the authors of [9], for higher wavelengths this may be explained by the increase in mode field diameter and the corresponding increase in interaction with the sidewall roughness and substrate leakage. For smaller wavelengths, the roughness amplitude increases relatively with respect to the wavelength, also leading to higher losses. Similar results were presented in [23]. In [14], the response over a similar wavelength range was almost completely flat, however. Figure 8.6 also shows the strong polarization dependence of the loss. Based on a dipole scattering mode, Bogaerts [6] found that for typical etching induced sidewall roughness consisting of vertical striations TM-polarized light is scattered much more efficiently than TM-polarized light and therefore the TM-losses should be higher. At 1550 nm, this was also experimentally observed [4, 9]. However, Vlasov [9] noted that, due to

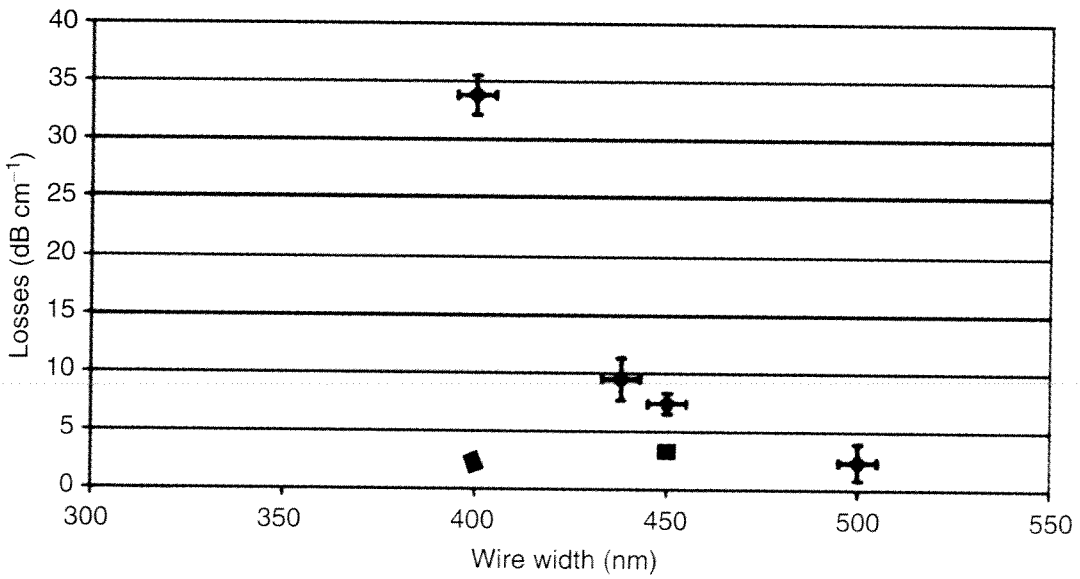

Fig. 8.5. Measured waveguide loss as function of width as reported by Bogaerts [6]. The square and the diamond denotes the loss reported by, respectively, Vlasov [9] and Tsuchizawa [14]

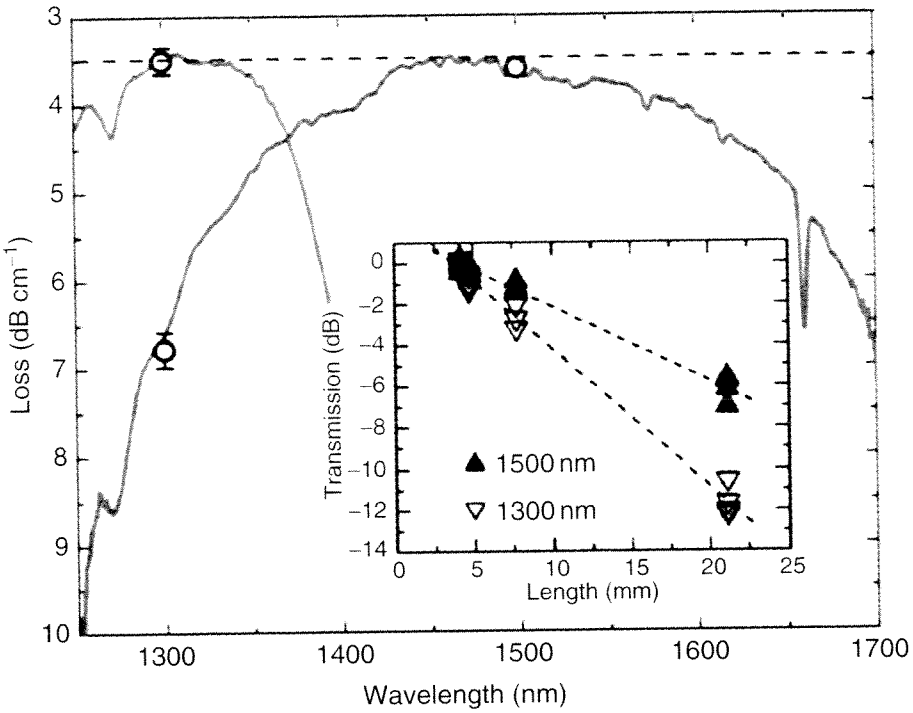

Fig. 8.6. Waveguide loss as function of wavelength (from [9])

the boundary condition imposed on discontinuity in the electric field the TE-polarized mode has a higher field strength at the sidewall and therefore should have a higher loss.

As explained earlier, process optimization has led to a propagation loss reduction from over 100 db cm^{-1} to ~2 db cm^{-1} for single mode silicon strip waveguides. Despite this spectacular improvement, such losses are still much higher than those reported for silica-based waveguides [1], where, depending on the refractive index contrast, losses from 0.01 db cm^{-1} (minimum bend radius 25 mm) to 0.07 db cm^{-1} (minimum bend radius 2 mm) are reported. However, while the dimensions of typical PLC-based devices such as AWGs are in the order of centimeters, dimensions of silicon wire based devices have dimensions below 100 µm (see next sections), leading to total propagation losses per device that are comparable for both optical waveguide platforms.

8.2.3 Box Layer Thickness

Another important parameter is the thickness t_{box} of the SiO_2 box layer. As can be seen in Table 8.1, values between 1 and 3 µm are typically employed. Making t_{box} thicker is technologically more challenging but smaller values may cause leakage to the substrate. Figure 8.7 shows the calculated substrate leakage as a function of the oxide buffer thickness for different waveguide

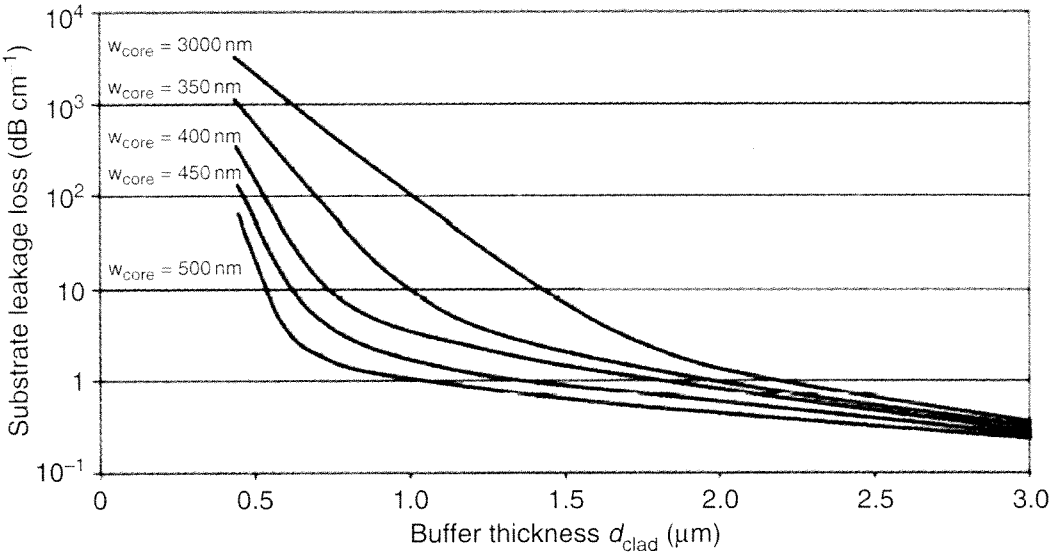

Fig. 8.7. Calculated substrate leakage (from [6])

widths [6]. For reducing the substrate leakage loss of single mode waveguides below 1 db cm^{-1}, a buffer thickness of at least 1 μm has to be chosen. Also note that the substrate leakage loss increases rapidly with decreasing waveguide width. For TM-polarization, the loss is higher because the field is less confined in the waveguide core.

8.2.4 Polarization

Figure 8.2 shows that waveguides with a rectangular cross-section exhibit very different modal properties for TE- and TM-polarized light. As mentioned in Sect. 8.2.3, also the loss is very polarization sensitive (e.g. see Fig. 8.6). To overcome this problem, several authors have proposed using waveguides with a square cross-section (typically 300 nm × 300 nm) [14, 19, 23, 26], which results in equal properties for TE-like and TM-like modes. Since the sidewall roughness is typically present at the vertical interfaces, the polarization dependent loss will remain important, however. An additional problem to be resolved is the polarization crosstalk in bends with a small radius (<5 μm). This issue was discussed in detail in [19]. Using FDTD-simulations the maximum polarization crosstalk induced in a 1 μm radius bend was calculated to be −25 dB, which is acceptable for practical implementations. The actual measured polarization crosstalk was much larger, however, up to −10 dB. The authors explained this by a ∼5° tilt of the sidewall of the fabricated waveguide. Also the scattering loss in the bend may play a role. For on-chip optical interconnect, the polarization issue is less important. For other applications polarization diversity approaches can be used [41] (see the section "Grating Couplers").

8.2.5 Temperature Dependence

Since the temperature over a CMOS chip may vary considerably, the influence of operating temperature on the waveguide properties has to be investigated, in particular when optical filters and resonators are used. The change of the refractive index of silicon is around $1.79 \times 10^{-4}\,\mathrm{K}^{-1}$ at 1550 nm [32]. The refractive index change of SiO_2 depends on the fabrication method but is an order of magnitude smaller than that of silicon. From these values the refractive index change of the propagation index and the related shift in filter peak wavelength value can easily be calculated. For most classical filter structures such as Mach-Zehnder interferometers (MZI), ring resonators, and phased-arrays the wavelength shift depends in the same way on the change in refractive index and is given by $\mathrm{d}\lambda/\lambda = \mathrm{d}n_\mathrm{g}/n_\mathrm{g}$. Based on the values given above, we calculated a wavelength shift of $140\,\mathrm{pm\,K}^{-1}$. Measured temperature dependence of the peak wavelength for ring resonators and cascaded MZI-structures shows a good linearity but a reduced shift of $80\,\mathrm{pm\,K}^{-1}$ and $89\,\mathrm{pm\,K}^{-1}$, respectively (Fig. 8.8). We believe the discrepancy between calculations and measured results may be caused by stress in the SOI-structure.

The strong temperature dependence may be a problem for stabilizing wavelength dependent structures but can also be used for making compact switches [25]. This is discussed later in this chapter.

8.2.6 Bend Radius

Obviously, one of the most attractive features offered by silicon wire waveguides is the possibility for realizing an extremely short bending radius. Both theoretical (FDTD) and experimental results have been reported by several authors. The lowest experimental losses were reported by Vlasov [9],

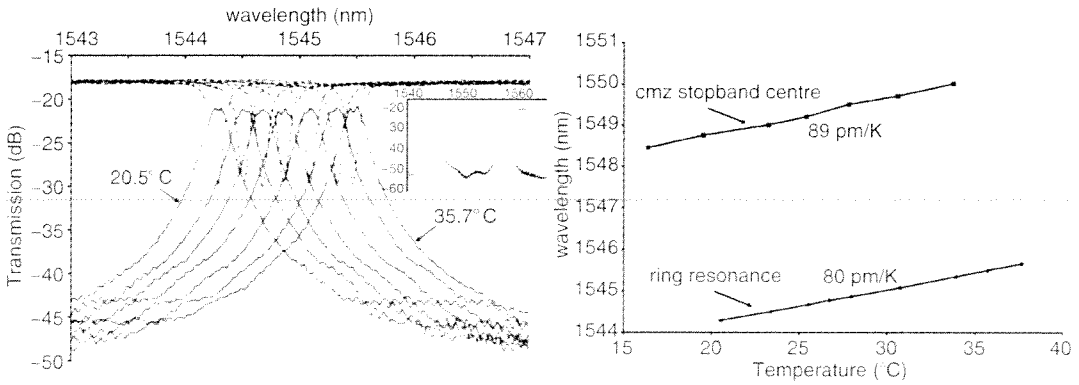

Fig. 8.8. Laser-to-detector transmission spectra to pass and drop ports of a racetrack resonator with 5 µm radius while temperature was increased from 20.5 to 35.7°C (*left*). Measured temperature dependence of passband wavelength for ring resonator filter and cascaded MZI (*right*)

who reports losses of 0.086, 0.013, and 0 dB for a 90° turn with bend radius of, respectively, 1, 2, and 5 μm (uncertainty +/− 0.005 dB per turn) for waveguides with a rectangular cross-section, using TE-polarized light at a wavelength of 1500 nm. For TM-polarization, the losses at a wavelength of 1500 nm increase. In [14], 0.15 and 0.6 dB per turn were measured for waveguides with, respectively, a rectangular and a square cross-section and a 2 μm bend radius. Also in this case the loss for 5 μm bends is negligible. Similar results were found in [23]. FDTD-simulations in [19] show very good agreement with the experimental results of [9]. The authors of [19] also investigated the influence of the bend pattern on the polarization crosstalk and the losses and mention an increased crosstalk for S-shaped bends compared to U-shaped bends.

Several authors [24, 33, 34] have proposed and/or demonstrated corner-mirror and resonator-based bend structures with the goal of further decreasing the bend loss and size. However, in view of the excellent results reported earlier for standard bend structures and the increased sensitivity to wavelength, polarization, and side wall angle for the resonant structures, it is very unlikely that they will have any practical use.

8.2.7 Waveguide Pitch

To increase the total data density, the minimum waveguide pitch is an important parameter. The minimum waveguide pitch is defined here as the minimum center-to-center spacing that is allowed without causing crosstalk between the channels and is dependent on the distance over which the channels are running alongside each other and the acceptable crosstalk level.[1] Figure 8.9 shows the minimum allowable center-to-center spacing as function of waveguide height and width (for $-20\,\mathrm{db\,cm^{-1}}$ crosstalk level). For wider waveguides the minimum pitch obviously increases. Since for smaller widths the mode gets less confined in the core, however, also for decreasing width the minimum pitch increases and as a consequence there is an optimum for the waveguide width. Due to the higher confinement, waveguides with an increased core layer height h allow for a smaller pitch.

The minimum acceptable waveguide pitch also imposes an upper boundary for the data density per square centimeter. Further increasing the data density would require further increasing the refractive index contrast. In principle this can be done by decreasing the cladding refractive index (using air-cladding or low-k dielectrics) or increasing the core refractive index. At this moment, none of these seems viable, however. Alternatively, new waveguide types such as plasmon waveguides [35] may be considered. In principle, such waveguides can confine the electromagnetic radiation in a smaller volume. However, they intrinsically show extremely high propagation losses. Note that photonic crystal

[1] The acceptable crosstalk level will depend on the application and the difference in power levels between different channels

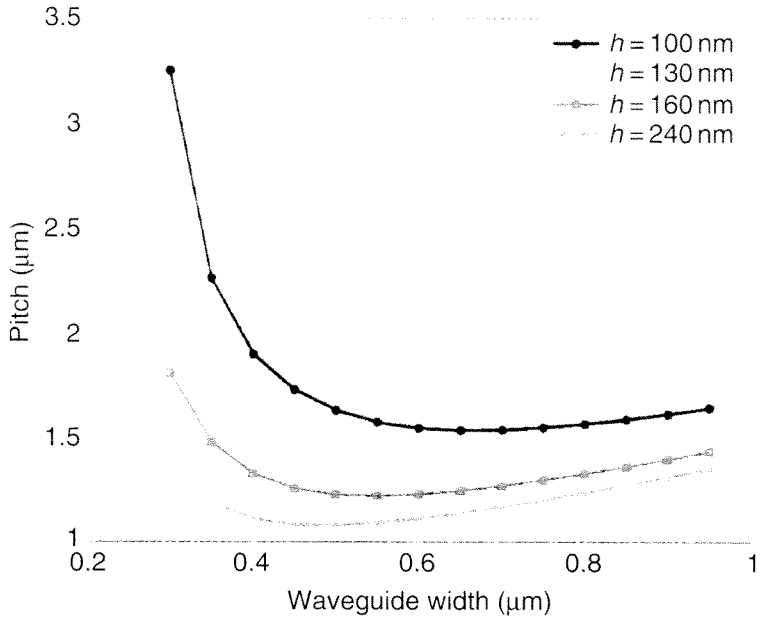

Fig. 8.9. Minimum allowable center-to-center spacing for a maximum crosstalk of $20\,\mathrm{db\,cm^{-1}}$

waveguides cannot bring a solution here since, although the optical mode itself may be more confined, they typically require several rows of holes to reach this effect.

8.3 Fabrication

8.3.1 Introduction

Table 8.2 gives a review of the fabrication methods used by several groups. Most research groups are using Ebeam lithography for defining the silicon stripe waveguides. Ebeam lithography allows for very high accuracy and is an excellent research tool. For obtaining low loss waveguides and avoiding roughness in the resist pattern, a stringent optimization of the writing process (spot size, overlap) and the resist process is required [12, 14, 16].

For large scale applications, however, such as on-chip optical interconnect, a mask-based lithography approach has to be developed. In [4] and [23] deep UV lithography is used (248 nm illumination wavelength). In [20] a G-line stepper (436 nm illumination wavelength) is used, which is in principle sufficient for defining 500 nm lines but will not be useful when finer features such as small gaps in directional couplers or star couplers have to be defined. Also mixed approaches combining mask based lithography for the wider lines and Ebeam lithography for the finer features have been demonstrated [22]. Sect. 8.3.2 will describe in detail the DUV-based fabrication process.

For transferring the resist pattern in the silicon core layer, different etching processes have been employed. In most cases a SiO_2-mask or a metal hard

Table 8.2. Fabrication approaches

aff.	loss ($db\,cm^{-1}$)	box (um)	top clad	fab.	mask	etch method
IMEC	2.4	1	no	DUV	Resist	Cl_2/He/Hbr/O_2 (ICP)
IBM	3.6	2	no	EBeam	SiO_2	CF_4/CHF3/Ar (oxide) + HBr (silicon)
Cornell	5.0	3	no	EBeam		ICP
NTT	6.0	3	no	EBeam	SiO_2	SF_6/CF_4 etch. ECR-etch
Yokohama	105.0	1	no	EBeam	metal	ICP (CF_4 + Xe)
MIT	32.0 0.8		yes	G-line	SiO_2 oxidation	RIE (SF_6)
LETI	15.0 5.0	1	yes	DUV mixed	SiO_2	HBr etching
Columbia	110.0	1	yes	EBeam	Aluminium	RIE (CF_4:Ar)
Ebeam	19.0	1	yes	EBeam	SiO_2	ICP

mask is used. In [4] a resist mask is used, however. For etching the silicon an ICP-based or ECR-based etching procedure is preferred for making smooth sidewalls with little damage. In Sect. 8.3.2, the DUV process developed at IMEC is described in more detail.

8.3.2 CMOS-Compatible Deep-UV Lithography Based Fabrication Process

Introduction

Using CMOS-technology for nanophotonic circuits brings the potential of low cost, volume manufacturing, and solving the yield problems suffered now by photonic devices. Therefore, we investigated the possibilities and limitations of using deep UV lithography and CMOS etching processes for fabricating nanophotonic devices.

The process flow is very similar to that of conventional projection lithography. We used commercial SOI wafers from SOITEC fabricated using the UNIBOND process [37]. The SOI wafers have a 220 nm top silicon layer and a 1 µm silica box layer. In a first step the wafer is coated with photoresist and an antireflective coating which is used to avoid standing wave patterns in the photoresist. Subsequently, a 248 or 193 nm stepper is used for illumination of the resist. The pattern is typically repeated several times over the wafer and different exposure conditions can be used for the different dies allowing to make a detailed process characterization. In a next step, the resist pattern is postbaked and developed. An additional plasma treatment is used for resist hardening before etching. The photoresist is used directly as an etch mask for the silicon etch. If needed thermal oxidation or oxide deposition processes can be added to the process flow.

Deep UV Lithography

For our experiments an ASML PAS5500/750 stepper with 248 nm illumination wavelength connected to an automated track for preprocessing and postprocessing was used. The resolution of optical projection lithography is mainly determined by the illumination wavelength and the numerical aperture (NA) of the projection system and the smallest feature that can be imaged is proportional to λ/NA. Decreasing the illumination wavelength or increasing the NA therefore enhances the resolution. The drawback of increasing the resolution by increasing the NA invariably leads to a decrease in depth of focus (DOF) for the optical system which makes the fabrication much more sensitive to variations in wafer topography. For characterizing the process, both hole and line patterns were printed with different exposure doses. Lines are defined by etching two 1–3 µm wide tracks spaced by the required width (i.e., the actual line width). The results can be seen in Fig. 8.10. The hole diameters increase with increasing exposure dose, while the line width of a photonic wire decreases. For a given feature size on the mask, a wide range of printed feature sizes can be obtained. The range of exposure energies where the structure is still within specification is called the exposure latitude. One of the difficulties of the lithographic process is to print different types of structures such as isolated lines, narrow gaps, photonic crystal structures, and gratings with the same accuracy. As can be seen from Fig. 8.10, even for isolated lines, the dose-to-target (required exposure dose for reaching the designed feature size) may differ considerably depending on the designed line width. In order to print all features correctly, a bias may have to be applied in the design phase and therefore a thorough optimization of the whole process in advance is needed.

Also optical proximity effects have to be corrected. If features with dimensions close to the illumination wavelength are defined, diffraction may cause the images of neighboring structures to overlap, resulting in either destructive or constructive interference and as a consequence the features size of (semi)isolated structures may differ from that of structures in a dense array. Figure 8.11 shows two examples of optical proximity effects. In the left picture, the width of a line is influenced by a line printed next to it and even

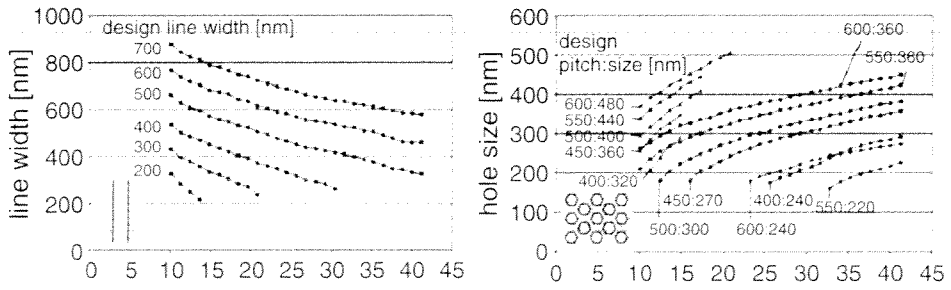

Fig. 8.10. Size of lines (*left*) and holes (*right*) as function of exposure dose ($\mathrm{mJ\,cm^{-2}}$)

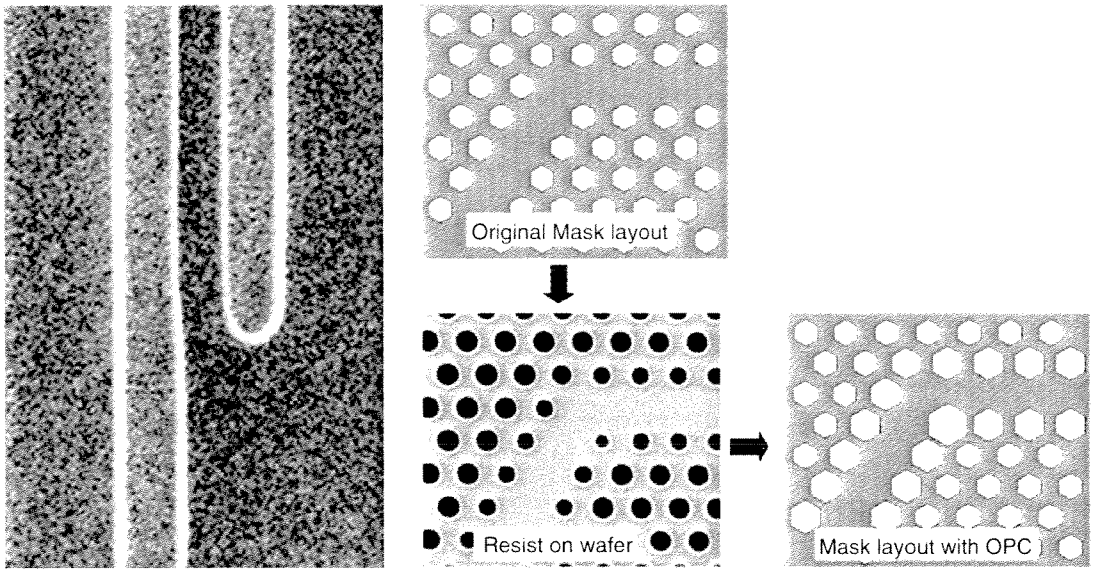

Fig. 8.11. Optical proximity effects for lines (*left*) and photonic crystals (*right*). Optical proximity corrections (OPC) on the mask can compensate for this (the corrections in the figure above are exaggerated)

the waveguide center is displaced. The right picture shows how the diameter of holes in a photonic crystal lattice is different in the bulk of the lattice and at the waveguide borders and corners. By adding a correction in the mask, OPE-effects can be compensated for. Note that, due to electron scattering, proximity effects also form a problem for Ebeam lithography. However, since the effect is coherent for mask based lithography it is more difficult to simulate.

Etching

The structures are etched on a LAM A6 platform. For the silicon etch a $Cl_2/O_2/He/HBr$ chemistry was used. The original process, including the resist thickness, was optimized for also etching the underlying silica cladding layer using a CF_4/O_2 chemistry. This, however, resulted in a very high roughness (Fig. 8.12, left), which can be overcome partly by oxidation (see section "Oxidation"). For photonic wires the deep etch is not needed, however, and the oxide etch can be omitted. To overcome a considerable bias between lithography and etch, a resist hardening plasma treatment is introduced in this case. This results in a considerable roughness reduction with a residual sidewall roughness in the order of 5 nm or less (Fig. 8.12, right) and low propagation losses (Fig. 8.5).

Oxidation

Several authors have found that a high temperature oxidation step following the waveguide etching can smoothen the sidewalls of the photonic wires [4,14, 20,21]. This was studied in detail in [20,21], where the waveguide losses before and after oxidation were determined and the oxidation kinetics were studied.

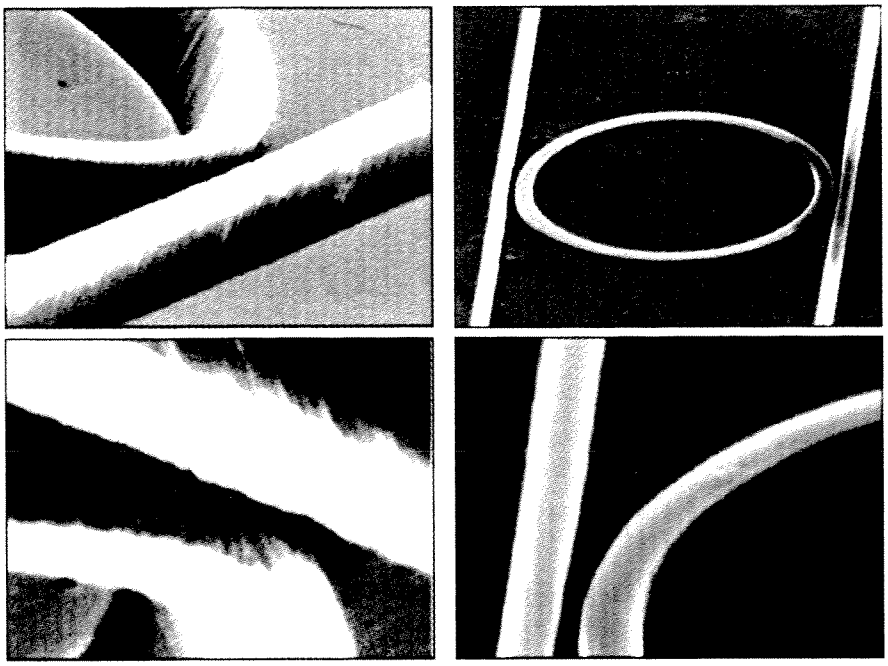

Fig. 8.12. Deeply etched structures showing high roughness and high loss ($\sim$300 db cm^{-1}) (*left*) and shallowly etched strip waveguides with reduced losses (2.4 db cm^{-1})(*right*)

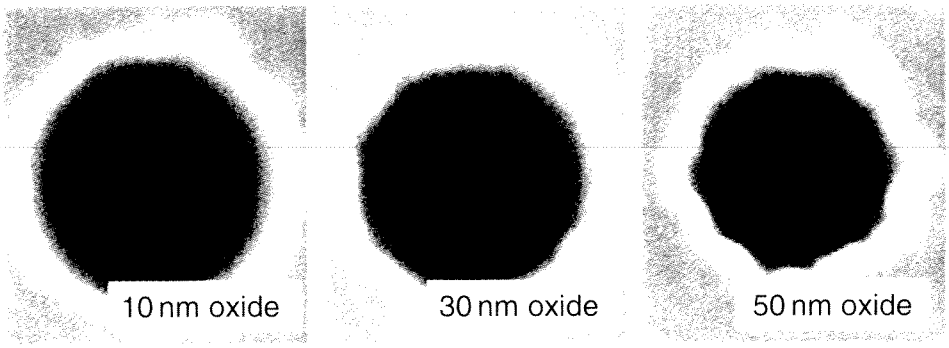

Fig. 8.13. Sidewall smoothing due to oxidation

Oxidation led to a reduction of the sidewall rms roughness from 10 to 2 nm. However, as explained above the resulting waveguide had a core thickness of only 50 nm and can no longer strongly confine the light.

Figure 8.13 shows the effect of oxidation on the sidewall roughness of a small hole. Although there is an apparent increase of the roughness at the SiO_2/air interface one may assume that the roughness which is actually relevant, namely at the Si/SiO_2 interface, is smoother due to the diffuse nature of the oxidation process.

A drawback of the oxidation process is the high temperature required (>1,000°C), which makes the process incompatible with back-end processing. While the oxidation can indeed reduce the losses, most of the low propagation loss results [3, 9, 14] were obtained without oxidation.

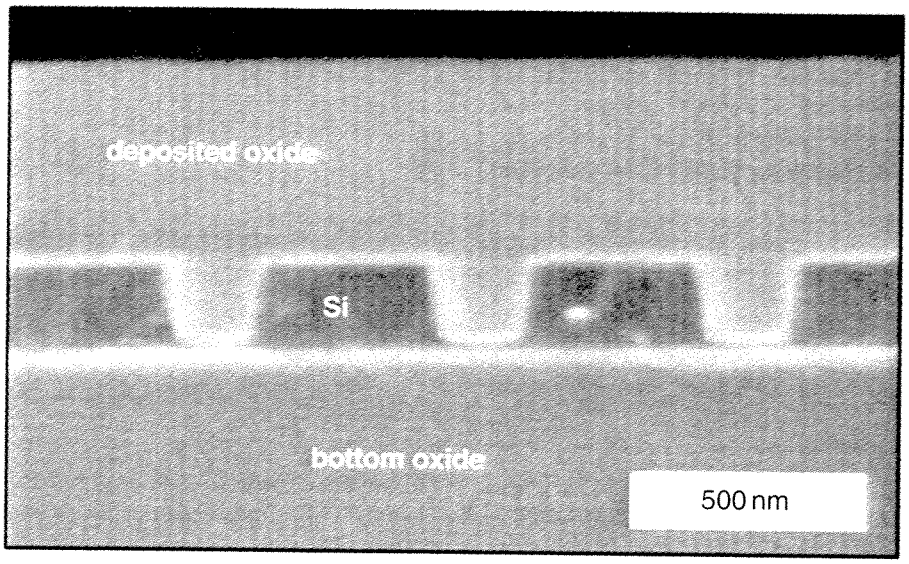

Fig. 8.14. Cross-section of photonic crystal holes with 500 nm pitch after oxide deposition

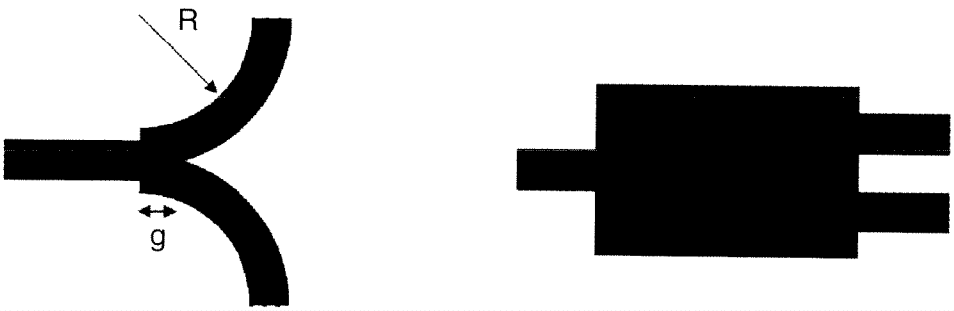

Fig. 8.15. Compact branch type coupler (**a**) and MMI-type coupler (**b**)

Oxide Deposition for Top Cladding

Due to the reduced index contrast, a silica top cladding should, for a given width, lead to a further decrease of the propagation loss. However, as can be seen from Fig. 8.2, adding a top cladding also requires considerably smaller waveguides if the single mode condition has to be fulfilled. Table 8.1 shows that several authors have indeed used a top cladding layer. Figure 8.14 shows an example of a photonic crystal structure covered with a 500 nm oxide layer deposited using a TEOS CVD process (following a 5 nm oxidation). Note that no artifacts such as voids are visible and that the deposition process creates a smooth planar top cladding.

8.3.3 CMOS-Compatibility

While deep UV-lithography is capable of printing features with the dimensions of photonic wires and photonic crystals there are some important differences

between nanophotonic components and typical CMOS-structures and some issues to be taken into account when designing photonic components. These include sidewall roughness and depth of focus, as mentioned earlier. Some other potential problems are described later.

CMOS Components are Layered

In a typical process flow for the fabrication of high-end electronic devices the components are layered. Each layer contains only critical structures of a certain type (transistor gates, contact holes, interconnect wires, etc.) and a given dimension. Therefore, the process can be optimized for each layer individually. In planar nanophotonics, small alignment tolerances require that all structures are fabricated in the same lithographic step. As explained earlier, the optimal process conditions may differ strongly for different structures, however, and this requires difficult precompensation on the mask level.

Note that with typical steppers an alignment accuracy better than 100 nm between different layers can be obtained. However, for the ultracompact waveguide structures considered here this is still not sufficient and would lead to considerable transition losses. A possible solution would be to incorporate optimized transition sections, which are wider or exhibit a lower transversal index contrast and, therefore, are more tolerant to discontinuities.

Type of Structures

Also the type of structures may differ considerably between CMOS and photonics. A typical example includes super dense photonic crystal lattices. The best equivalent in CMOS is a 1:1 dense array of contact holes, in which case the hole diameter is equal to the spacing in between. In triangular photonic crystal lattices, the spacing between the holes can be reduced to virtual nothing, however.

Required Accuracy

As described in [6.38], the properties of high-contrast nanophotonic devices are extremely sensitive to deviations in the fabrication process. For wavelength dependent circuits (filters, demultiplexers, etc.) the spectral transmission shifts as a result of the waveguide thickness. In most type of circuits, the relative wavelength shift is equal to the relative change in effective index. This leads to the equation:

$$\frac{\partial \lambda}{\lambda} = -\frac{\partial k_z}{k_z} = \frac{k_x^2}{k_z^2}\frac{\partial k_x}{k_x} = -\frac{k_x^2}{k_z^2}\frac{\partial d}{d} \tag{8.2}$$

with k_z the propagation coefficient, k_x the k-vector perpendicular to the waveguide axis and d the waveguide width. Since for high contrast waveguides $k_z \approx k_x$ this means the structural dimensions need to have the same accuracy as the accuracy required for the wavelength dependent transfer of the

device. In the same way, one can show that, for interference type filters such as Fabry-Pérot cavities

$$\frac{\partial\lambda}{\lambda} = \frac{\partial L}{L} \tag{8.3}$$

with L the cavity length. Again, if L is of the order of the wavelength, as needed for ultracompact resonators with large FSR and only a few modes, the tolerable thickness inaccuracy is of the same order as the tolerable resonance wavelength inaccuracy.

A lot of more advanced filter structures such as AWGs and Cascaded MZI-structures (see later) are based on multipath interference and are very sensitive to phase-errors accumulated along the way. We believe this is the main reason for the relatively high crosstalk level reported thus far for this kind of devices [7, 14, 16]. This issue is also related to another problem, namely the mask pixelization. The DUV-mask is written with a finite resolution. This may lead to coherence in the induced sidewall roughness, which enhances problems due to roughness-induced phase errors. Another problem is the limited control over the exact dimensions of structures, as e.g., has been noticed by several authors when defining ring resonator based multichannel add-drop multiplexers (e.g., see Fig. 8.25)

8.4 Devices

8.4.1 Couplers–Splitters

Except for simple point-to-point interconnections, most circuits will require splitters or couplers. This is for example the case in clock distribution networks, where the input signal has to be evenly divided toward a very large number of detectors, but also in every filter function, such as ring resonators, where couplers always form one of the basic building blocks.

Couplers and splitters have to fulfill several requirements:

1. Negligible insertion loss
2. Precise splitting and/or coupling ratio
   - For 3 dB-splitters (e.g., used in clock distribution networks or Mach-Zehnder interferometer based switches ...) an equal distribution ratio is extremely important.
   - Some types of wavelength selective filters (e.g., ring resonators, cascaded Mach-Zehnder interferometers, ladder type filters) require very accurate control over the coupling ratio, which can vary from less than 1% to 50%.
3. Wavelength independent operation
4. Tolerance to fabrication deviations

Directional coupler type devices consisting of two identical waveguides brought close together are best suited for realizing *variable coupling ratios*. They need narrow gaps between both waveguides (in some cases down to a few

tens of nanometers, mostly in the order of 200–300 nm, however) and, therefore, may be sensitive to optical proximity effects (e.g., see Fig. 8.11). They are also not trivial to simulate because of the high index contrast. However, they are conceptually simple and relatively broadband. Optical directional couplers for square cross-section silicon wires, including their polarization dependent and wavelength dependent behavior were studied in detail in [26,39]. MMI-type devices with variable coupling ratio have been demonstrated in other material systems but to our knowledge not yet employing submicron SOI-wires.

Different designs for compact 3 dB-couplers splitting the power evenly over two output waveguides were studied in detail in [18], both using simulations (2D and 3D FDTD) and experimentally. The simple branch consisting of two offset bends as sketched in Fig. 8.15a turned out to have the lowest insertion loss and to be the most manufacturable. FDTD simulations (3D) predict a 0.2 dB excess loss for such a structure. Experimentally, an excess loss of 0.3 dB was demonstrated. By optimizing the length g and the bend radius R, the structure can be made very tolerant to process variations. The optimized structure was used in [17] to construct a 3-level H-tree. A 2–5 dB fluctuation was measured over the 16 ports.

In [23], MMI-type couplers (Fig. 8.15b) were experimentally demonstrated and a 1-to-8 distribution tree was demonstrated. The experimental imbalance remains smaller than 0.5 dB over a 400 nm spectral range. The size of the 1×2 MMI was $2 \times 5.4\,\mu\text{m}^2$.

8.4.2 Crossings

One of the advantages of optical interconnects often mentioned is the possibility to make crosstalk free crossings, which would simplify the interconnect problem considerably. For free space interconnects this assumption holds but for guided wave solutions part of the light of the main channel will leak into the intersecting channel and this will become worse with increasing optical confinement (or in other words, increasing numerical aperture). Since SOI-wires confine the optical mode to a very small cross-section we can expect a large crosstalk and reflections at intersections. This problem has been investigated by Fukazawa [40] using 3D-FDTD-simulations and experimentally. For a simple cross-section (Fig. 8.16a) the insertion loss and crosstalk were estimated (3D-FDTD) to be 1.4 and −9.2 dB, respectively, which is totally unacceptable for practical applications. Expanding the mode as in Fig. 8.16b makes the angular spectrum smaller and leads to an improved performance (<0.1 dB loss and <−30 dB crosstalk). This structure was also fabricated and performance comparable with the simulations was demonstrated (<0.1 dB loss and <−25 dB crosstalk). However, in practice also the intersecting waveguide should be tapered as in Fig. 8.16c, again leading to higher losses (0.4 dB). In [34] a resonant coupler with <0.2 dB insertion loss was presented. However, the simulations were limited to 2D FDTD and the transmission band of the resonant coupler was limited to a few nanometer.

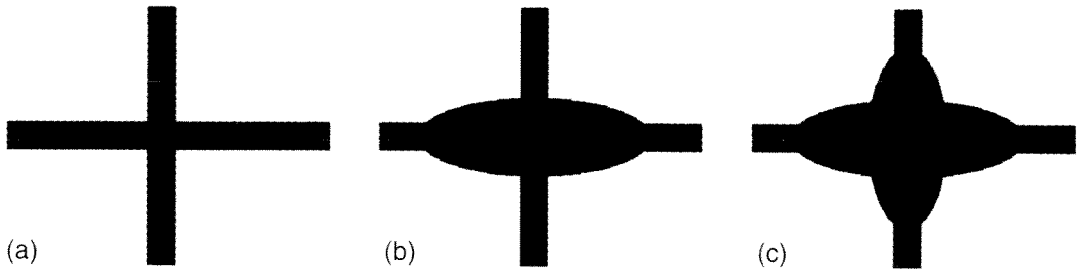

Fig. 8.16. (**a**) Standard crossing. (**b**) Crossing with single parabolic taper. (**c**) Crossing with double parabolic taper

An additional drawback of the resonant crossing and the parabolic crossing are the additional floor space required, which may be a problem in ultradense interconnect circuits. At this moment no satisfactory solution is available for realizing crossings and an interconnect layout requiring no crossings should be used, potentially using multiple wiring levels combined with vertical optical vias.

8.4.3 Fiber-Chip Couplers

Introduction

For on-chip optical interconnect, coupling between the photonic wires and an optical fiber is not necessary. For all other applications, however, the coupling of light between the fiber and the chip is one of the most essential parts of the device and determines a huge fraction of the cost of the packaged device. In some material systems, such as polymer or silica-on-silicon, the size of the basic optical waveguide mode is identical to that of the optical fiber and the coupling is straightforward. Losses below 0.1/dB per connection point have been demonstrated [1]. In a lot of cases, however, there is a large mismatch between the optical mode on and off the chip resulting in large coupling losses if no mode adapters are used. This is the case, for example, for InP-laser diodes and a fortiori, for the submicron silicon wire waveguides discussed here. In general two approaches can be followed. In the first one, the field is adapted outside of the chip, e.g., using small ball lenses or a lensed fiber. Such an approach has the advantage of not requiring additional processing for making the on-chip mode adapters but leads to high packaging costs because of the additional components required (if ball lenses are used) and because of the very high alignment accuracy required. In the second approach, the mode adapter is integrated on the chip and the alignment accuracy is relaxed, which also results in lower packaging cost. The processing becomes more complex, however, and the tradeoff between processing cost and packaging cost will determine what solution is to be preferred.

Because of the extremely large mismatch, external mode adaptation is almost impossible for silicon wires and a solution with on-chip mode adapters has to be used. A good solution has to fulfill several requirements:

- Except for a few specific cases, in general *broadband operation* is required for the fiber-chip coupler (several tens of nanometers). This requirement excludes the use of long gratings and directional coupler based devices that may have a good efficiency but work only for a narrow bandwidth range.
- *Low loss.* The loss per connection should be reduced to values comparable with current high-contrast PLC solutions, i.e., at least below 1 dB/connection and preferably below 0.5 dB/connection.
- *Low reflection.* AR-coatings can be applied but approaches avoiding this clearly have an advantage.
- Large alignment tolerance.
- *Correct fabrication tolerance.* If the coupling structure (or parts thereof) is defined in the same step as the wires themselves, very high alignment accuracy can be reached and narrow lines can be defined. Parts of the structure defined in a postprocessing step have to be more tolerant to deviations and typically will have larger minimum dimensions.
- "CMOS-compatible"-fabrication, both in terms of materials and in terms of processing (e.g., taking into account available DOF). The etching of very deep silicon structures has to be avoided.
- Size.
- Limited extra processing steps.

Different solutions have been proposed in literature and the chapter on couplers in this book describes different possible solutions. Below we are discussing two options, which were developed specifically having SOI-wires in mind and which according to us show the most promise taking into account the above requirements.

Inverse Tapers

The inverse taper approach shown in Fig. 8.17 has been demonstrated by several groups (see Table 8.3). Over a length of a few tens to a few hundreds

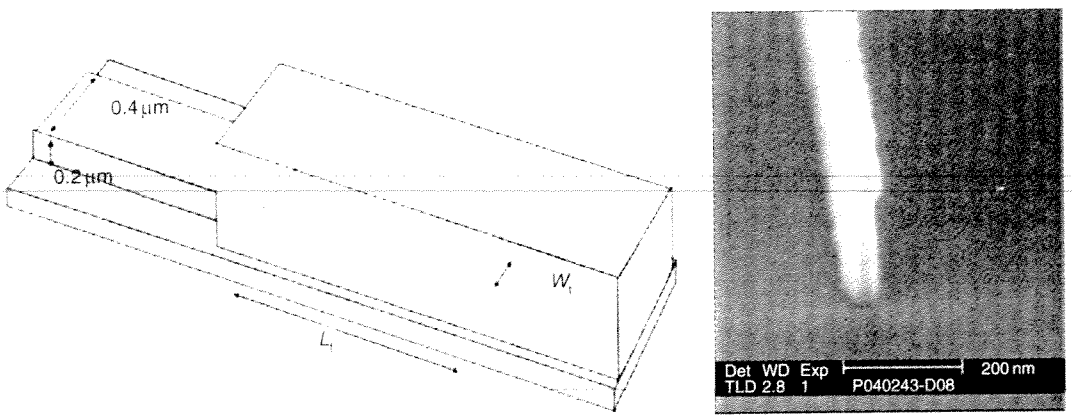

Fig. 8.17. Inverse taper based fiber-chip coupler (*left*) and tapers defined by DUV (*right*)

Table 8.3. Inverse taper review table

Aff.	h (nm)	w (nm)	L_t (um)	W_t (nm)	cladding material	cladding Size (μm^2)	loss per connection	ref.
IBM	220	445	150.0	75.0	Polymer	2×2	<0.5 dB	[9]
Cornell	270	470	40.0	100.0	SiO_2	2×00	<4 dB	[10]
NTT	200	400	300.0	80.0	Polymer	3×3	0.8 dB	[14]
					SiON	3×3	0.5 dB	

of micrometers the silicon waveguide is narrowed down and the optical field is pushed upward to a low-index overlay. In most cases this overlay is patterned to form a single mode waveguide, which is then used to bring the optical mode to the edge of the chip. In [10] the overlay was not patterned and the chip had to be diced directly at the end of the silicon taper. In most cases the chip is coupled to a high NA single mode fiber with a mode diameter smaller than standard single mode fiber. Using this approach low-loss broadband operation was demonstrated (<0.5 dB per connection over range 1250–1750 nm in [9, 14]). The loss is mainly determined by the taper tip width W_t and its length L_t and a compromise between acceptable loss and size has to be found.

Both polymer-based approaches [9, 14] and inorganic-based approaches [10, 14] have been demonstrated. The latter may be more reliable and can withstand high optical input powers such as those required for nonlinear optical devices, while polymers are potentially cheaper and are easier to deposit. An additional advantage of the inverse taper approach is the inherent low facet reflection.

All of the demonstrated devices until now used Ebeam lithography for defining the narrow taper tips. We recently demonstrated the fabrication of such tapers using a combination of 248 nm DUV lithography and trimming, demonstrating that these couplers are also compatible with standard CMOS processing techniques (Fig. 8.17).

Grating Couplers

The idea of using a grating for coupling light to an optical waveguide has been around for a very long time. In most cases, however, a long, weak grating is used, leading to a narrow bandwidth. Moreover, such a solution may require an additional lens because the gaussian beam exiting the grating is not adapted to the fiber mode.

We proposed an alternative approach using a short but strong grating as shown schematically in Fig. 8.18. The mode exiting this grating has the same dimensions as the single mode fiber and therefore direct butt coupling between the fiber and the chip is possible. This method has several advantages:

- *Large bandwidth.* Since a strong grating is used, the bandwidth can be several tens of nanometers.

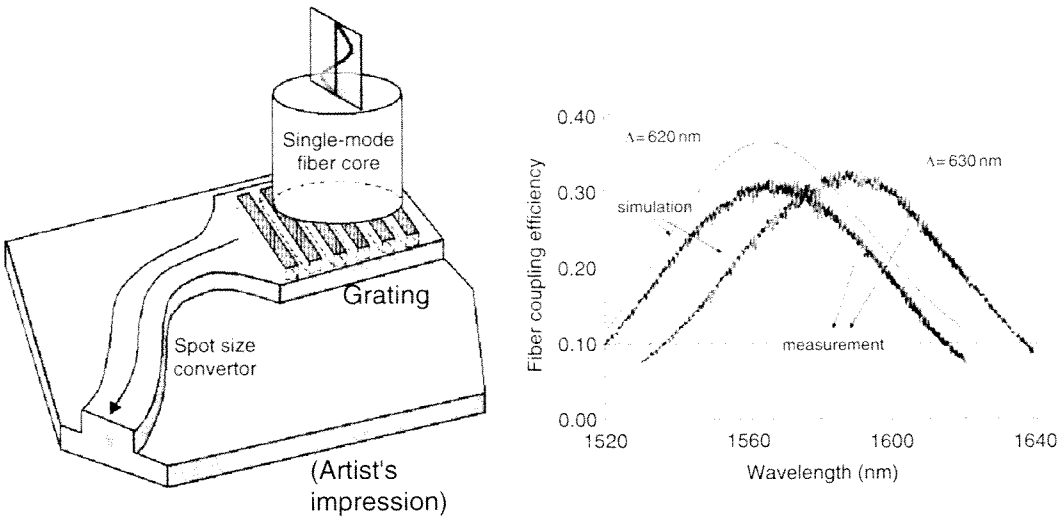

Fig. 8.18. Grating-based fiber chip coupler, only the core of the fiber is shown (*left*). Theoretical and experimental results for fabricated structure (*right*)

- Small size.
- Low reflections.
- No need for facet polishing or cleaving.
- *Wafer scale testability.* Since the devices can be accessed from the top, testing during the fabrication cycle is possible.

We designed and optimized a grating for coupling between an SOI waveguide, with a 220 nm thin Si core layer, and a single-mode optical fiber [41]. In a first stage, we have optimized the parameters of a uniform grating. For a uniform grating, the maximum coupling efficiency that can be achieved is approximately 55% and the 1-dB bandwidth for that structure is 43 nm. The parameters that were optimized are the etch depth, grating period and duty cycle, and the thickness of the buried oxide layer of the SOI. Also an index matching layer is used between the grating and the fiber. The fiber is placed not exactly vertical, but at a small angle (8°) with respect to the vertical direction, to avoid back-reflection into the fiber or waveguide. However, for the actual fabricated structure, the thickness of the BOX-layer was not optimized, leading to a reduction of the expected maximum coupling efficiency. Theoretical and experimental results for the fabricated grating are shown in Fig. 8.18. As can be seen from this picture a maximum coupling efficiency of 33% was measured. The 1 dB-bandwidth was 40 nm. For obtaining the theoretical results a 1D calculation was used. If also the lateral dimension is taken into account the discrepancy between theoretical and experimental results reduces to a few percent.

The efficiency of a uniform grating is limited by two factors. First, a uniform grating creates an approximately exponentially decaying output field along the propagation direction. The fiber-mode has a Gaussian profile. As a result, there is a mode mismatch between the two and this limits the

theoretical coupling efficiency. Second, the grating does not only couple light from the waveguide upward toward the fiber, but also downward toward the substrate. The light coupled to the substrate is lost and limits the efficiency. To avoid this, a mirror (dielectric DBR or metal mirror) can be added under the grating. If the position of the mirror is correctly chosen, all the light can be coupled upward and no light is lost to the substrate.

We have optimized such a grating using a genetic algorithm. Both the width of the grating teeth and the spacing between the grating teeth is optimized. More details on the design and optimization of this structure can be found in [42]. The resulting structure is shown in Fig. 8.19, together with a field plot and the calculated transmission. The coupling efficiency is 95% and the 1-dB bandwidth is 43 nm. When regular SOI is used instead of SOI with a bottom reflector, the coupling efficiency is 63%. The regular SOI wafers are commercially available products, the fabrication of wafers with a bottom reflector requires additional processing steps. The cited values are for TE-polarization.

The 1D grating only couples TE-polarized into the circuits and TM-polarized light is lost. If a 2D grating is used, however, both polarizations couple toward different directions perpendicular with respect to each other. Therefore, the 2D grating coupler can be used as a polarization splitter [31] and for implementing a polarization diversity scheme as presented in Fig. 8.20. As discussed earlier, such a scheme could provide a solution for the extremely polarization dependent behavior of the submicron silicon wire circuits.

For making a compact transition between the grating coupler having a lateral width of 10 μm and the 500 nm wide single mode wire, compact interference type filters were designed [43] using a genetic algorithm and fabricated. A typical structure and the measured performance is shown in Fig. 8.21.

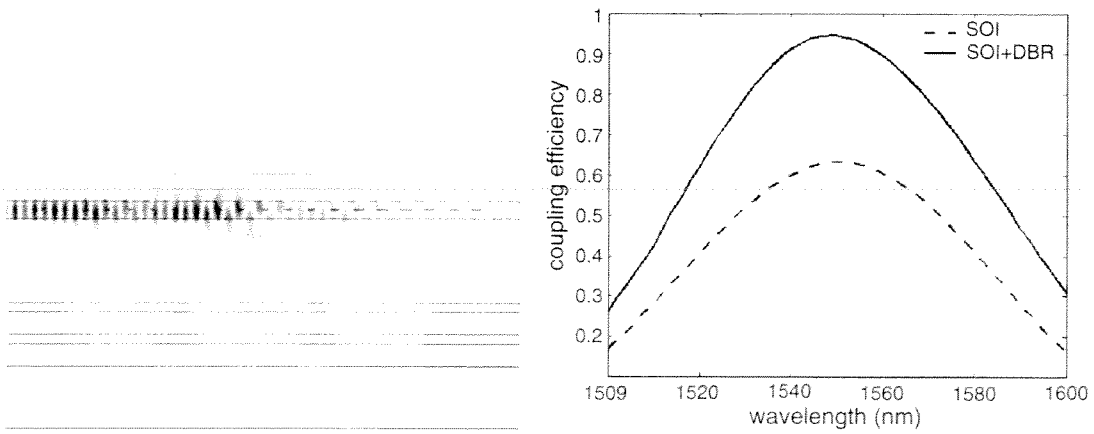

Fig. 8.19. Optimized grating structure with nonuniform grating and bottom reflector. Field plot (*left*) and calculated transmittance (*right*)

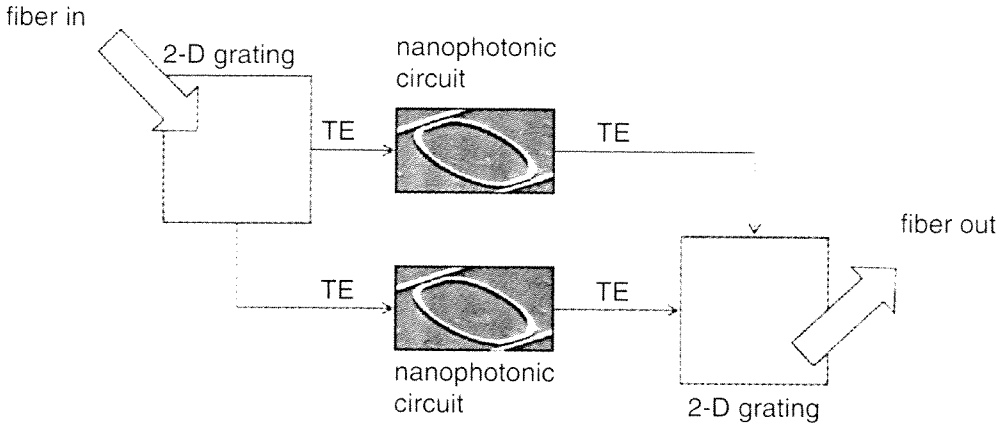

Fig. 8.20. Polarization diversity scheme using 2D-grating coupler

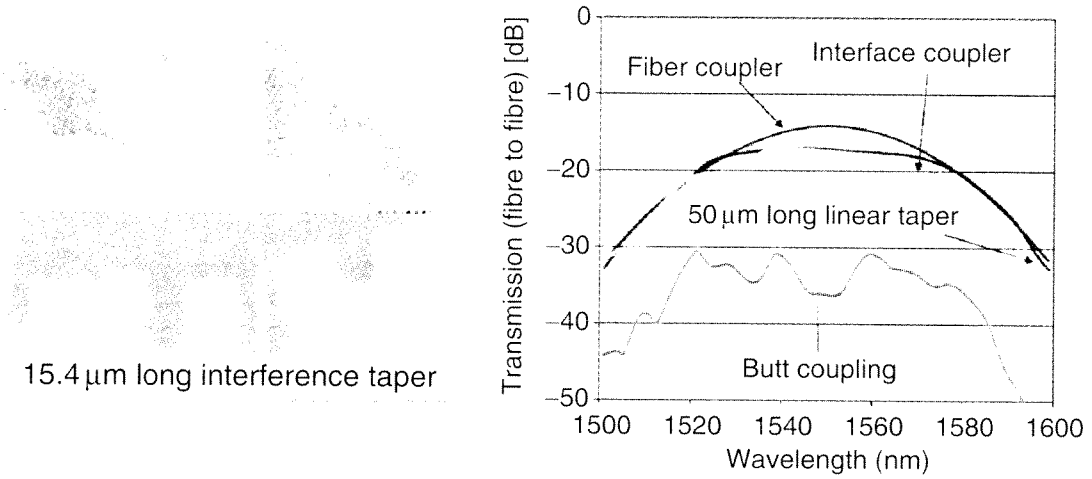

Fig. 8.21. Compact interference taper. Structure and field plot (*left*) and measured transmission (*right*)

8.4.4 Ring Resonators

Compact microring resonators can be a building block for densely integrated wavelength selective filters. Since SOI-based photonic wires enable the fabrication of bend waveguides with very short bend radius they are suited very well for fabricating ring resonators with a large free spectral range (FSR), which is important for the fabrication of useful add-drop filters. A large finesse and high extinction ratios are of utter importance too. For increasing the roll-off and for obtaining a flat-top transmission, higher-order filters can be fabricated by connecting several ring resonators in series [44]. Reliable fabrication of such devices is challenging, however, and ring resonators also form a very good test for the quality and reproducibility of the technology.

SOI-based ring resonators have been presented by several authors [11, 14, 36, 45]. We fabricated a series of devices using DUV-lithography. The most challenging part of the fabrication process is defining the narrow gap between

the bus and ring waveguides in the coupler region in a reliable manner, since it is influenced strongly by optical proximity effects (e.g., see Fig. 8.11, left). The resonators have radii up to 8 μm and are laterally coupled to two waveguides for channel dropping purposes. We studied different coupling alternatives in order to achieve low crosstalk and high finesse while maintaining a large free spectral range.

The first devices fabricated are circular ring resonators coupled to two straight waveguides. The gap between ring and straight waveguide is limited to about 200 nm due to technological limitations. This makes coupling between the ring and waveguides difficult and smaller than 1%. With a 5 μm radius ring, a FSR of 17 nm is obtained but drop efficiency is very low due to the low coupling. Also, Fig. 8.22, left shows that resonances are often split. This is due to coupling to the counter-propagating mode induced by the surface roughness. As explained in [46] this effect only appears if the coupling coefficient is sufficiently low. We applied a BCB top cladding in order to enhance the coupling. This polymer has a higher refractive index (1.5) than the original air cladding, which increases the coupling coefficient slightly. The measurements in Fig. 8.22, right clearly show the resulting increase of the coupling and the absence or large reduction in the splitting of the resonances. Reduced waveguide dispersion also leads to a net increase of the FSR to 18.5 nm.

Due to low coupling and high FSR the finesse of this kind of device is high, up to 120. However, for WDM purposes coupling should be increased. Therefore, we looked at other ring resonator configurations to enhance coupling between cavity and waveguides.

One option is to include a straight coupling section, leading to a racetrack resonator (e.g., see Fig. 8.23, left). We fabricated racetracks with radii of the bend section between 1 and 6 μm. With 1 μm radius, a Q of around 2,100 is obtained but the drop efficiency is low. For larger radii, the ring losses decrease quickly. With a 2 μm radius, drop efficiency is already much larger and Q factors in the range 5,000–9,000 are obtained. We also fabricated racetracks with 5 μm radius and larger coupling section. The larger coupling leads to a high

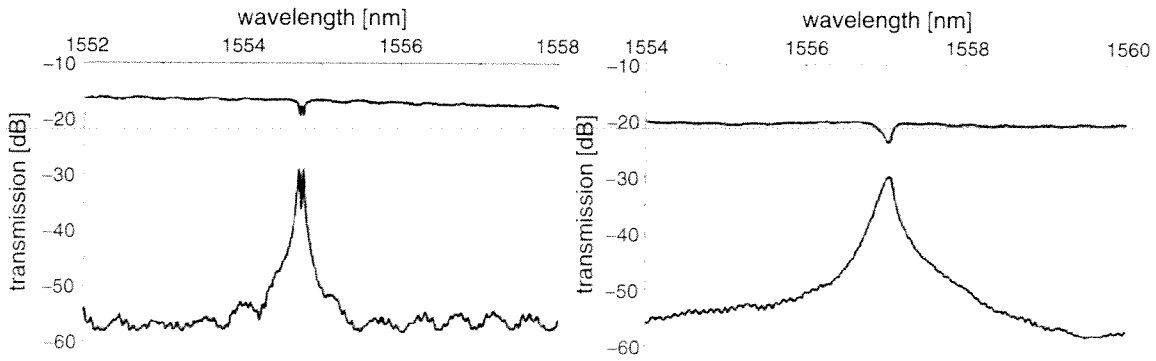

Fig. 8.22. Detail of transmission spectra of a ring resonator with 5 μm radius (*left*). Same ring with a BCB top cladding, resonance in the same wavelength range (*right*)

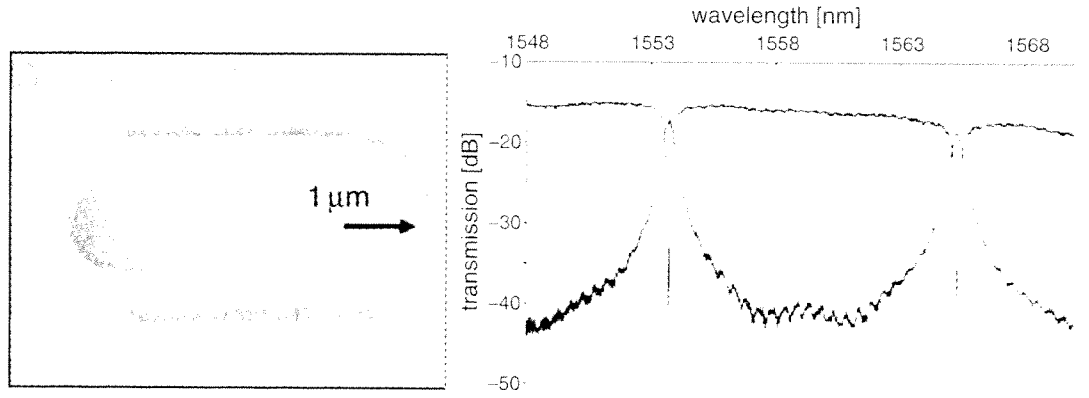

Fig. 8.23. Racetrack resonator with 1 µm radius (*left*). Transmission spectra of racetrack resonator with 5 µm radius (*right*)

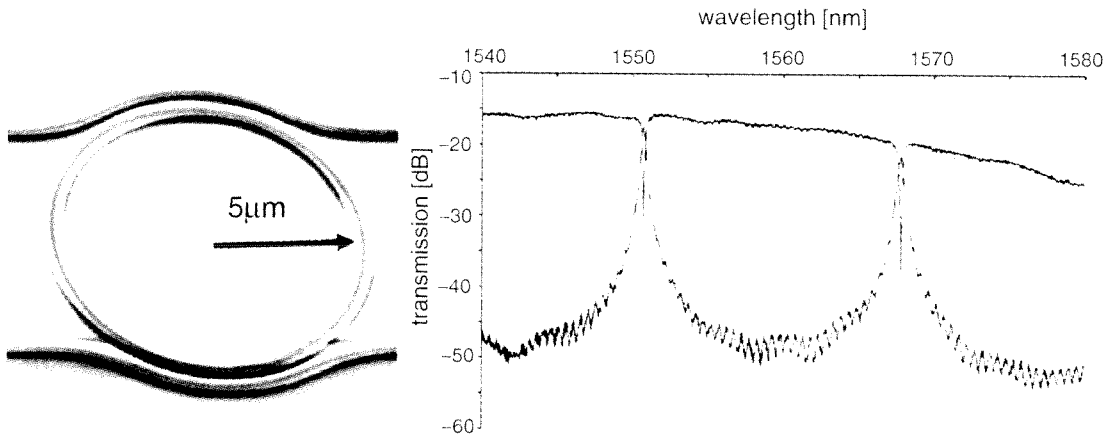

Fig. 8.24. SEM picture (*left*) and transmission spectra (*right*) of a bend-coupled ring resonator with 5 µm radius

add-drop extinction ratio of −20 dB and 50–70% drop efficiency at Q factors still larger than 3,000 (Fig. 8.23).

While racetrack resonators can clearly enhance coupling, their FSR is limited. Another option is coupling to bend waveguides (Fig. 8.24). By carefully choosing the widths of cavity and bus waveguides, a good phase matching can be obtained and coupling can be high without lowering the FSR as in the case of the racetrack resonator. We fabricated bend-coupled resonators with 5 and 8 µm radius. The amount of coupling is varied by varying the angle over which both waveguides are coupled. Coupling is large enough to obtain a relatively high extinction ratio (−10 to −15 dB) and high drop efficiency, although these first devices are still far from optimized.

We fabricated a four channel add-drop filter with racetrack resonators with different radius. By varying the radius, the resonance wavelength is changed and each cavity is tuned to another set of dropped wavelengths. One must keep in mind that with this approach the FSR also varies. Figure 8.25 shows

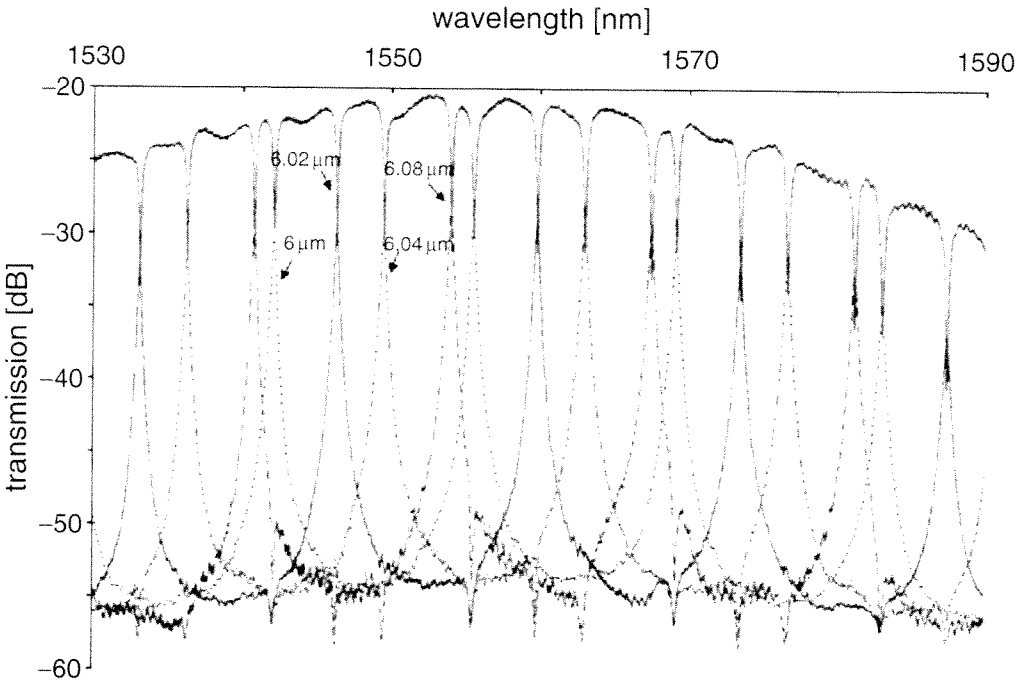

Fig. 8.25. Overlaid transmission spectra of a 1-by-4 demux with four racetracks with varying radius (indicated)

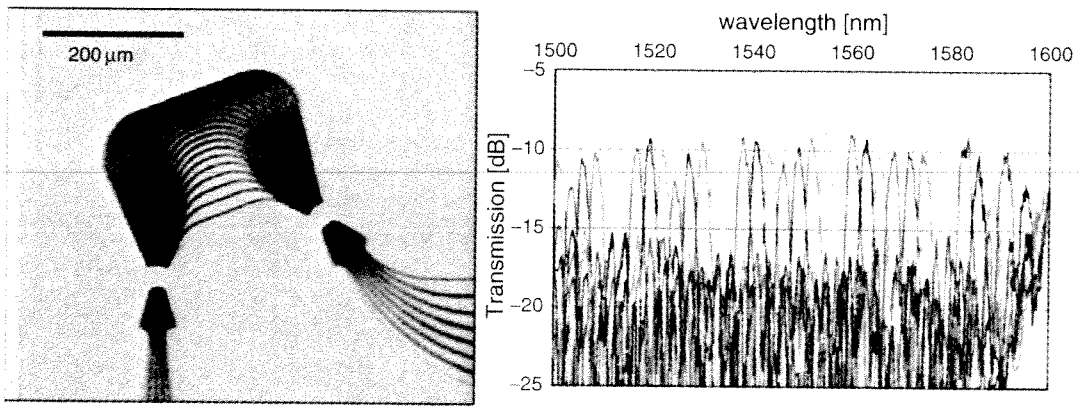

Fig. 8.26. SEM-picture of SOI-based eight-channel AWG and measured transfer curves

the overlaid transmission spectra for four resonators with 6, 6.02, 6.04, and 6.08 µm. A BCB top cladding was applied. We see that a large part of the FSR can be reached by changing the radius over only 80 nm. However, better control over the exact resonance wavelengths is needed.

8.4.5 Arrayed Waveguide Grating Devices

Silica-on-silicon AWGs are currently the most popular integrated device for multiplexing and demultiplexing multiple wavelength channels. We have designed and fabricated an 8-channel AWG (Fig. 8.26). This device has a

footprint of $380\,\mu m \times 290\,\mu m$ or about $0.1\,mm^2$. The transfer from the input port to the 8 output waveguides is also plotted in Fig. 8.26. The small ripple is caused by residual reflections in the grating couplers. The channel spacing is 3 nm, with a free spectral range of 24 nm. The on-chip insertion loss was approximately 8 dB. We believe this loss is mainly caused by reflections in the star coupler and can be reduced by adapting the transition zone between the grating arms and the star coupler. The main problem, however, is the high crosstalk level, limited to values around −7 dB, which is clearly not sufficient for practical applications. Also in [16] an AWG fabricated using SOI-wires was presented. The authors optimized the devices for compactness and demonstrated a $110 \times 93\,\mu m^2$ device with a 6 nm channel spacing and a 90 nm FSR. However, also in this case, the crosstalk was limited to a few dB.

The high crosstalk may be caused by several reasons such as reflections or overspill in the star coupler [47]. We believe the crosstalk is mainly caused by phase errors in the grating arms, however. Due to the high refractive index contrast even the very small roughness can lead to random phase fluctuations over the array arms and lead to the observed crosstalk level.

8.4.6 Cascaded Mach-Zehnder Interferometers

SOI-wire based Cascaded Mach-Zehnder interferometers have been demonstrated by several authors [14, 24, 48]. As shown in Fig. 8.27, such filters consist of a series of Mach-Zehnder interferometers with constant path-length difference but with varying coupling ratio optimized to obtain the desired wavelength dependent transmittance. The measured transmission for the fabricated device is shown in Fig. 8.27b. A crosstalk slightly better than −10 dB was measured, limited by a nonoptimized choice of the coupling ratios and by phase errors in the interferometers. In [14], a similar device having a −12 dB crosstalk level and a 80 nm spectral range was demonstrated. By cascading three devices in series, the crosstalk could be increased to −30 dB. Also multiple wavelength add-drops where demonstrated.

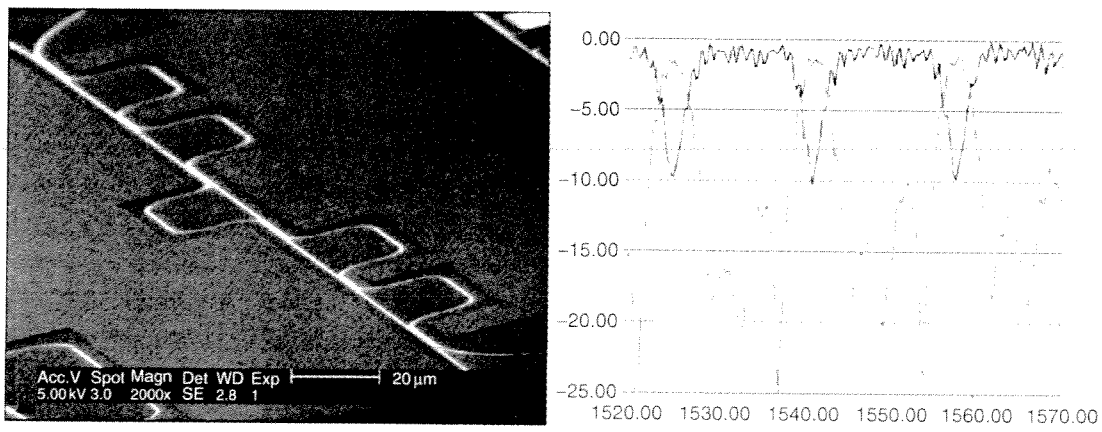

Fig. 8.27. Cascaded Mach-Zehnder interferometer. Fabricated device (*left*) and measured performance (*right*)

8.4.7 Active Devices

The demonstration of active devices using submicron silicon wires has been limited till now and mainly modulator type devices have been demonstrated. As discussed extensively in a separate chapter in this book, the two main mechanisms for modulating the refractive index of silicon are carrier injection and thermo-optic tuning.

In [25], a compact thermo-optically tuned switch based on a Mach-Zehnder interferometer was demonstrated. The Cr–Au heaters were deposited on a 1 μm SiO_2-buffer layer. The total switching power required was 50 mW, the total length of the device was ~1.5 mm. A <3.5 μs rise time was demonstrated. We demonstrated thermo-optic tuning of ring resonators and cascaded Mach-Zehnder interferometers (Fig. 8.9) [50].

In [11] FP-type modulator using deeply etching DBR-mirrors was demonstrated. Also all-optical switching in a ring resonator was demonstrated in [11]. Recently, also gain through Raman pumping has been demonstrated [49].

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References

1. Miya et al., IEEE Select Top. Quantum Electron. 2000, p. 38
2. L. Pavesi and D.J. Lockwood, "Silicon Photonics", Springer Berlin Heidelberg, New York, 2004
3. P. Dumon et al., "Low-loss photonic wires and ring resonators fabricated with deep UV lithography". IEEE Photon. Technol. Lett. Vol. 16 (5), 2004 pp. 1328–1330
4. W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology", J. Lightwave Technol., Vol. 23 (1), 2005, pp. 401–412
5. P. Dumon et al., "Micro-ring resonators in silicon-on-insulator", ECIO '05, Grenoble, April 2005
6. Wim Bogaerts, "Nanophotonic waveguides and photonic crystals in silicon-on-insulator", PhD Thesis, Ghent University, April 2004
7. P. Dumon, W. Bogaerts, D. Van Thourhout, D. Taillaert, V. Wiaux, S. Beckx, J. Wouters, and R. Bockstaele, Wavelength-selective components in SOI photonic wires fabricated with deep UV lithography, Group IV Photonics, Hong Kong, p. WB5 2004
8. S.J. McNab, "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides", Opt. Express Vol. 11 (22), November 2003, pp. 2927–2939

9. Y.A. Vlasov, "Losses in single-mode silicon-on-insulator strip waveguides and bends", Opt. Express Vol. 12 (8), April 2004, pp. 1622–1631
10. V.R. Almeida et al., "Nanotaper for compact mode conversion", Opt. Lett. Vol. 28, August 2003, pp. 1302–1304
11. M. Lipson, "Controlling light on a microelectronics' chip: solving the coupling, modulation and switching challenges", Group IV Photonics '04, Hong Kong, WB1
12. T. Tsuchizawa et al., "Fabrication and evaluation of submicron-square Si wire waveguides with spot size converters", Leos Annual Meeting 2002, Glasgow, paper TuU$_2$
13. T. Shoji et al., "Low loss mode size converter from 0.3 um square Si wire waveguides to singlemode fibres", Electron. Lett. Vol. 38 (25), December 2002, 1669–1670
14. T. Tsuchizawa et al., "Microphotonics devices based on silicon microfabrication technology", IEEE J. Select. Top. Quantum. Electron. Vol. 11 (1) 2005, pp. 232–240
15. A. Sakai et al., "Propagation characteristics of ultrahigh-δ optical waveguide on silicon-on-insulator substrate", Jpn J. Appl. Phys. Vol. 40, April 2001, pp. L383–L385
16. T. Fukazawa et al., "Very compact arrayed-waveguide grating demultiplexer using Si photonic wire waveguides", Jpn J. Appl. Phys. Vol. 43, 2004, pp. L673–L675
17. T. Fukazawa et al., "H-Tree-type optical clock signal distribution circuit using a Si photonic wire waveguide", Jpn J. Appl. Phys. Vol. 41, December 2002, pp. L1461–L1463
18. A. Sakai et al., "Low loss ultra-small branches in a silicon photonic wire waveguide", IECE Trans. Electron. Vol. E85-C (4), April 2002, pp. 1033–1038
19. A. Sakai et al., "Estimation of polarization crosstalk at a micro-bend in Si-photonic wire waveguide", IEEE J. Lightwave Technol. Vol. 22 (2), February 2004, pp. 520–525
20. K.K. Lee et al., "Fabrication of ultralow-loss Si/SiO$_2$ waveguides by roughness reduction", Opt. Lett., Vol. 26, December 2001, pp. 1888–1890
21. D.K. Sparacin et al., "Oxidation kinetics of waveguie roughness minimization in silicon microphotonics", IPR '03, paper ITuC4-1
22. R. Orobtchouk, "Optical interconnects on SOI: a front end approach", Proceedings of the IEEE 2002 International Interconnect Technology Conference, 2002, San Fransisco
23. R. Orobtchouk, "Compact building blocks for optical link on SOI technology", ECIO 05, Grenoble, April 2005
24. R.U. Ahmad, F. Pizzuto, G.S. Camarda, R.L. Espinola, H. Rao, and R.M. Osgood, Jr., "Ultracompact corner-mirrors and t-branches in silicon-on-insulator" IEEE Photon. Technol. Lett., Vol. 14 (1), January 2002, pp. 65–67
25. R.L. Espinola, M.-C. Tsai, James T. Yardley, and R.M. Osgood, Jr., "Fast and low-power thermooptic switch on thin silicon-on-insulator", IEEE Photon. Technol. Lett. Vol. 15 (10), October 2003, pp. 1366–1368
26. H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Optical directional coupler based on Si-wire waveguides", Group IV Photonics '04, Hong Kong, FA3
27. Refractive index silicon
28. P.K. Tien, "Light waves in thin films and integrated optics", Appl. Opt. Vol. 10, 1971 p. 2395

29. F.P. Payne and J.P.R. Lacey, "A theoretical analysis of scattering loss from planar optical waveguides," Opt. Quantum Electron. Vol. 26, 1994, 977
30. F. Grillot et al., "Size influence on the propagation loss induced by sidewall roughness in ultrasmall SOI waveguides", IEEE Photon. Technol. Lett. Vol. 16 (7), July 2004, pp. 1661-1663, Doerr pol diversity
31. D. Taillaert et al., "A compact two-dimensional grating coupler used as a polarization splitter", IEEE Photon. Technol. Lett. Vol. 15 (9), 2003, pp. 1249–1251
32. J. McCaulley et al., "Temperature dependence of the near-infrared refractive index of silicon, gallium arsenide and indium phosphide", Phys. Rev. B, Vol. 49 (11), 1994. pp. 7408–7417
33. Mode-coupling analysis of multipole symmetric resonant add/drop filters, "Khan, M.J.; Manolatou, C.; Shanhui Fan; Villeneuve, P.R.; Haus, H.A.; Joannopoulos, J.D.; Quantum Electronics, IEEE Journal of, Vol. 35, Issue: 10, October 1999, pp. 1451–1460
34. Manolatou et al., "High-density integrated optics", IEEE J. Lightwave Technol. Vol. 17, September 1999, pp. 1682–1692
35. W.L. Barnes et al., "Surface plasmon subwavelength optics", Nature, Vol. 424, August 2003, pp. 824–830
36. P. Dumon et al., "Temperature behaviour of silicon-on-insulator photonic wires", to be published
37. "SOITEC's UNIBOND(r) process," Microelectron. J. Vol. 27 (4/5), 1996, p. R36
38. R. Baets, W. Bogaerts, D. Taillaert, P. Dumon, P. Bienstman, D. Van Thourhout, J. Van Campenhout, V. Wiaux, J. Wouters, and S. Beckx, Low loss nanophotonic waveguides and ring resonators in silicon-on-insulator, Proceedings of the International School of Quantum Electronics , 39th course "Microresonators as building blocks for VLSI photonics", 709, Italy. 2003, pp. 308–327
39. H. Yamada, T. Chu, S. Ishida, et al., "Optical directional coupler based on Si-wire waveguides", IEEE Photon. Technol. Lett. Vol. 17 (3), March 2005, pp. 585–587
40. Fukazawa et al., "Low loss intersection of Si photonic wire waveguides", Jpn. J. Appl. Phys. Vol. 43 (2), 2004, pp. 646–647
41. D. Taillaert et al., "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers", IEEE J. Quantum Electron. Vol. 38 (7), 2002, pp. 949–955
42. D. Taillaert et al., "Compact efficient broadband grating coupler for silicon-on-insulator waveguides", Opt. Lett. Vol. 29 (23), December 2004, pp. 2749–2751
43. B. Luyssaert, P. Vandersteegen, D. Taillaert, P. Dumon, W. Bogaerts, P. Bienstman, D. Van Thourhout, V. Wiaux, S. Beckx, and R. Baets, "A compact horizontal spot-size converter realized in silicon-on-insulator", IEEE Photon. Technol. Lett. Vol. 17 (1), 2005, pp. 73–75
44. B.E. Little, "A VLSI photonic platform", OFC '03
45. B.E. Little et al., "Ultra-compact Si-SiO2 microring resonator optical channel dropping filters", IEEE PTL, Vol. 10, 1998, pp. 549–550
46. B.E. Little et al., "Surface-roughness-induced contradirectional coupling in ring and disk resonators", Opt. Lett. Vol. 22 (1), 1997, pp. 4–6
47. C. Van Dam, PhD Thesis, TUDELFT '99
48. K. Yamada et al., "Silicon-wire-based ultrasmall lattice filters with wide free spectral ranges", Opti. Lett. Vol. 28, September 2003, pp. 1663–1664

49. R.L. Espinola, J.I. Dadap, R.M. Osgood, Jr., S.J. McNab, and Y.A. Vlasov, "Raman amplification in ultrasmall silicon-on-insulator wire waveguides", Opt. Express, Vol. 12 (16), August 2004, pp. 3713–3718
50. I. Christiaens, D. Van Thourhout, and R. Baets, "Low power thermo-optic tuning of vertically coupled microring resonators", IEE Electron. Lett., Vol. 40 (9), 2004, pp. 560–561