Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a Silicon-on-Insulator waveguide circuit

G. Roelkens, D. Van Thourhout, and R. Baets

Photonics Research Group, Department of Information Technology, Ghent University, B-9000 Ghent, Belgium
Gunther.Roelkens@intec.Ugent.be

R. Nötzel, and M. Smit

Technical University Eindhoven, OED group, Den Dolech 2, 5600 MB Eindhoven, The Netherlands

Abstract: Laser emission from an InP/InGaAsP thin film epitaxial layer bonded to a Silicon-on-Insulator waveguide circuit was observed. Adhesive bonding using divinyl-tetramethyldisiloxane-benzocyclobutene (DVS-BCB) was used to integrate the InP/InGaAsP epitaxial layers onto the waveguide circuit. Light is coupled from the laser diode into an underlying waveguide using an adiabatic inverted taper approach. 0.9mW optical power was coupled into the SOI waveguide using a 500μm long laser. Besides for use as a laser diode, the same type of devices can be used as a photodetector. 50μm long devices obtained a responsivity of 0.23A/W.

OCIS codes: (130.0130) Integrated Optics; (220.4610) Optical fabrication

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1. Introduction

Silicon-on-Insulator (SOI) is gaining importance for the fabrication of ultra-compact photonic integrated circuits, due to the high refractive index contrast between Silicon core (n=3.45) and SiO_2 cladding (n=1.45). Moreover, standard CMOS technology for the fabrication of the devices can be used increasing the yield, reproducibility and economy of scale of the fabricated devices [1]. Low loss nanophotonic waveguides are obtained and very compact optical functions (ring resonators, arrayed waveguide gratings,…) have been realized [2], [3]. As Silicon has an indirect bandgap, electrically pumped laser diodes have not yet been achieved, despite significant work in the field of Silicon photonics [4], [5]. The integration of direct bandgap III-V semiconductor layers (and more in particular InP/InGaAsP epitaxial layer structures for laser emission at 1.55μm) on top of the SOI waveguide circuits is therefore the most straightforward way to achieve electrically pumped laser emission and coupling to an SOI waveguide. Moreover, as Silicon is transparent for wavelengths above 1.1μm, it cannot be used for light detection at telecommunication wavelengths. To overcome this problem, the epitaxial growth of Germanium on top of the Silicon waveguide core is being investigated [6]. However, we will show here that using the same type of InP/InGaAsP layer structure and the same processing steps, one can also fabricate III-V photodetectors for telecommunication wavelengths integrated on top of SOI waveguide circuits.

2. Integration of InP/InGaAsP layers on top of Silicon-on-Insulator

There are different approaches to integrate III-V layers on a Silicon-on-Insulator substrate. Hetero-epitaxial growth results in large threading and misfit dislocation densities due to the large mismatch in lattice constants of the two material systems. The occurrence of these large dislocations densities in the active region can be overcome for example by epitaxial lateral overgrowth [7], by using the strain field induced by quantum dots to prevent the dislocation from reaching the optically active region [8] or by using buffer layers [9]. Although significant progress is being made in the field, the epitaxial layer quality is still lower compared to layers grown on a lattice matched substrate. To circumvent the problem of epitaxial layer quality, wafer bonding techniques can be used to integrate high quality InP/InGaAsP layer structures on a Silicon substrate. In [10] a low temperature O_2 plasma-assisted direct wafer bonding process was used to bond AlGaInAs quantum well heterostructures onto a processed Silicon-on-Insulator waveguide substrate. Laser diodes were fabricated by cleaving the devices and were optically pumped. Here, we present the use of an adhesive bonding process using divinyl-tetramethyldisiloxane-benzocyclobutene (DVS-BCB) [11] to create, to our knowledge, the first electrically injected thin film InP/InGaAsP laser diode integrated on and coupled to a Silicon-on-Insulator waveguide circuit.

3. DVS-BCB adhesive bonding

DVS-BCB was used to bond an InP/InGaAsP epitaxial layer structure grown on an InP substrate, epitaxial layers down onto a processed SOI substrate. The SOI substrate consists of a 220nm thick Silicon waveguide core layer on a 1μm SiO_2 buffer layer. The SOI waveguides are formed by etching through the Silicon waveguide layer, leaving a topology of 220nm height on the SOI surface. After cleaning the SOI wafer using $3H_2SO_4$:$1H_2O_2$ and $1NH_3$:$4H_2O_2$:$20H_2O$ to remove the hydrocarbon contamination and particles that are pinned to the surface respectively, two layers of DVS-BCB were spin coated on the surface to achieve an aggregate bonding layer thickness of 300nm. This double coating process was used to obtain a degree of planarization of the spin coating process above 90 percent. After spin coating, the DVS-BCB is partially cured for 2min at 250C to transform the liquid DVS-BCB into a sol/gel rubber. This is done in a nitrogen environment to prevent the oxidation of the DVS-BCB. Subsequently, InP/InGaAsP dies are bonded to the SOI substrate in a vacuum environment to prevent the inclusion of air at the bonding interface. The wafer stack is cured at 250C for 1 hour in a nitrogen environment to completely polymerize the DVS-BCB. A pressure of 300kPa is applied during curing to obtain an intimate contact between both wafer

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surfaces. After bonding, the original InP substrate is removed using a combination of mechanical grinding and wet etching using 3HCl:H_2O, until an InGaAs etch stop layer is reached. This leaves the InP/InGaAsP epitaxial layer stack attached to the SOI waveguide circuit as is shown in figure 1.

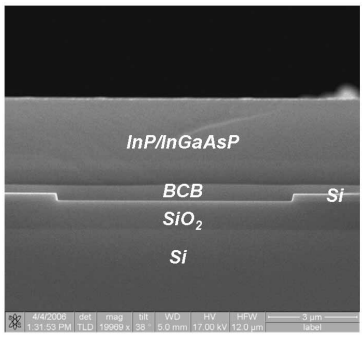

Fig.1. Cross section of the bonding interface after InP substrate removal.

4. Coupling between SOI and InP/InGaAsP

In order to efficiently couple light between the InP/InGaAsP active layer and the SOI waveguide circuit, a coupling scheme based on an inverted adiabatic taper was used as shown in Fig. 2. The inverted taper adiabatically transforms the SOI waveguide mode to the fundamental mode of a polymer waveguide, which lies on top of the inverted taper and is butt coupled to the InP/InGaAsP active layer. The design parameters of the inverted taper structure are shown in Fig. 3. The polymer waveguide consists of a polyimide waveguide core (n=1.67) surrounded by a DVS-BCB (n=1.54) cladding layer, which is not drawn for clarity. This type of coupling structure has been shown to result in a high efficiency and large optical bandwidth coupling [12].

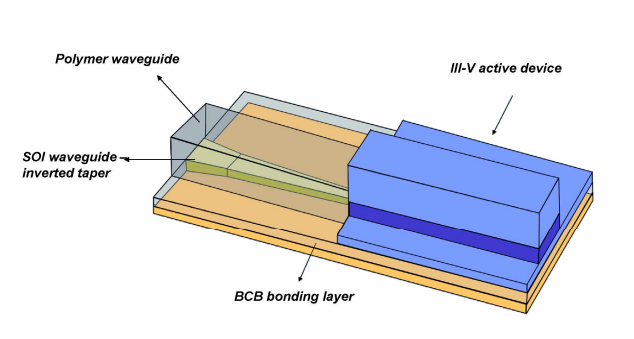

Fig. 2. Coupling scheme to couple light from an SOI waveguide to the InP/InGaAsP waveguide layer.

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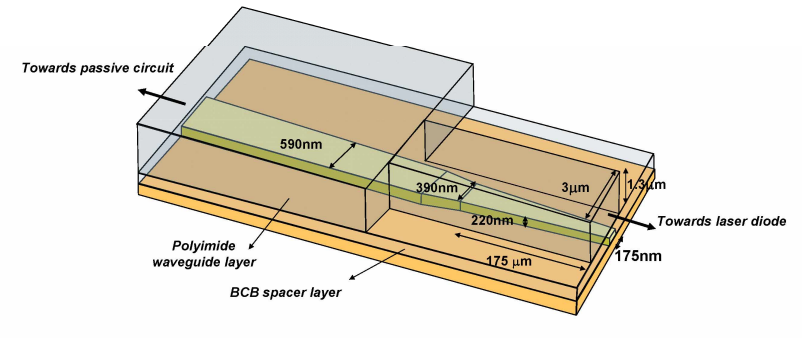

Fig. 3. Design parameters for the adiabatic inverted taper structure.

The InP/InGaAsP layer stack consists of a 600nm n-type InP undercladding, six InGaAsP quantum wells with a bandgap wavelength of 1550nm in between two separate confinement layers of 150nm (bandgap wavelength 1.25µm) and a 2µm p-type InP and 150nm p++ InGaAs contact layer.

The polyimide waveguide core height was designed for an optimal coupling between the fundamental III-V waveguide mode and the polymer waveguide mode. The coupling efficiency is plotted in figure 4. Calculations were based on a 3 dimensional fully vectorial eigenmode expansion method. A coupling loss of 1.4dB is obtained at an optimum polyimide waveguide height of 1.3µm. About 0.6dB is due to the reflection at the polymer/III-V interface.

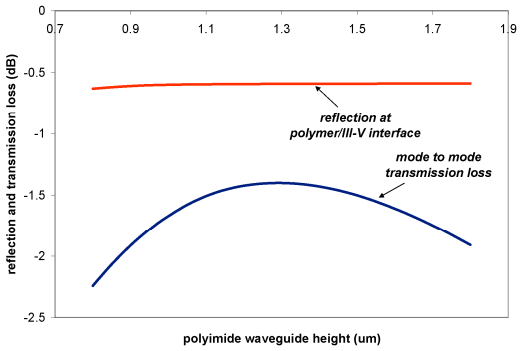

Fig. 4. Butt coupling efficiency at the polymer/III-V interface as a function of polyimide waveguide core height.

5. Fabrication of devices

Silicon-on-Insulator waveguides were defined using 248nm deep UV lithography and etched through the Silicon waveguide layer using a low pressure/high density Cl_2/O_2/He/Hbr plasma. The fabrication sequence of the active devices is outlined in figure 5. After transfer of the epitaxial layers to the Silicon-on-Insulator waveguide substrate using the bonding process described in section 3, the laser cavity facets are defined by dry etching using a CH_4:H_2/O_2 plasma (a). A 100nm Ti hard mask is used for the 3.2µm deep etch. After facet etching a polyimide layer was spin coated over the surface (b) and after curing at 300C for 1 hour it was again removed on top of the InP/InGaAsP material (c). This defines the polymer waveguide layer for the inverse taper structure. In a next step the laser diode/photodetector waveguide was defined together with the polymer waveguide structure using a CH_4:H_2/O_2 plasma, such that there is no misalignment at the polymer/III-V interface (d). The laser ridges were 3µm wide. III-V waveguides are etched through the active layer to be able to access the n-type

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contact layer. The polyimide waveguide layer was completely etched through. A DVS-BCB isolation layer is spin coated (which also serves as a cladding layer for the polyimide waveguide) (e) and openings are made to define the p-type TiAu contact and the n-type AuGeNi contact, which where subjected to a rapid thermal annealing at 400C (f). All alignment was done lithographically to the underlying SOI features. A top view of a fabricated structure is shown in figure 6, showing the InP/InGaAsP component butt coupled to the polymer waveguide. The SOI inverted taper structure is not visible as it is buried underneath the polymer waveguide.

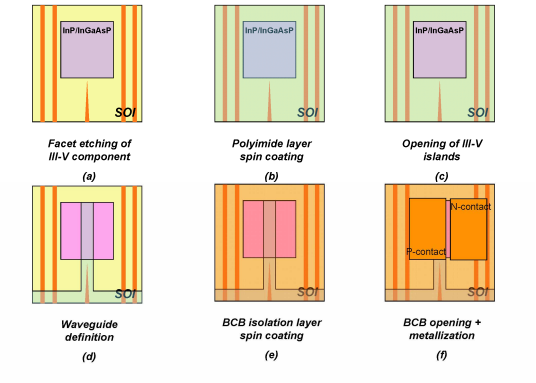

Fig. 5. Fabrication sequence of electrically injected thin film laser diodes and thin film photodetectors.

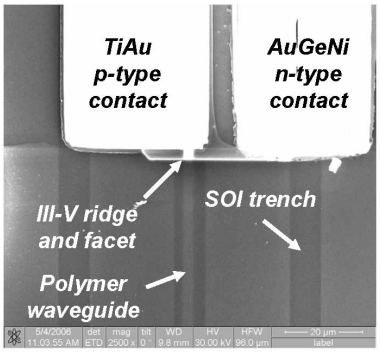

Fig. 6. Top view of a fabricated device.

6. Characterization

Laser emission from bonded devices was observed in pulsed operation as is shown in Fig. 7. The light was collected from the SOI waveguide using a lensed fiber. A 10μs long square wave current pulse with a 1 percent duty cycle was applied to drive the laser. The theoretical coupling efficiency between the lensed fiber and SOI waveguide was assumed. Threshold current density is relatively high (10.4kA/cm^2 for a 500 μm long device). This high threshold current density is related to the quality of the etched facets and can be reduced by optimizing the etching process. No continuous wave operation was obtained due to the high thermal resistance of the bonded device. This is due to the low thermal conductivity of the DVS-BCB bonding layer ($k_{DVS\text{-}BCB}$=0.3W/mK) and SiO_2 buffer layer (k_{oxide}=1.2W/mK). This problem can be circumvented however by integrating a heat sink structure on the laser diode structure as we showed in Ref. [13].

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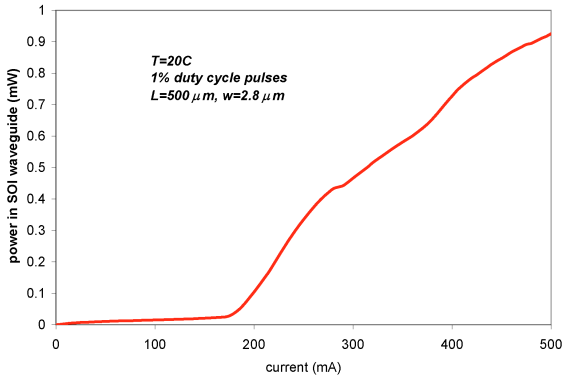

Fig. 7. Detected power versus injected current for a 500 μm long laser cavity.

The responsivity of photodetectors with identical layout as the laser diodes, only shorter device lengths, was measured by injecting light into the SOI waveguide using a lensed fiber. The theoretical coupling efficiency from lensed fiber to SOI waveguide was used to estimate the optical power traveling in the waveguide, therefore resulting in a lower boundary for the responsivity of the photodetector. A responsivity of 0.23A/W was obtained at a wavelength of 1555nm. The current versus voltage curves with and without illumination are shown in figure 8 (device length of 50μm) for an estimated 95μW waveguide power. The dark current of the device is about 50nA at 2V reverse bias. The non-ideal behavior of the IV curve for the illuminated device in forward bias and around zero bias is related to a residual n-type doping of the absorbing layer of about $2x10^{16}cm^{-3}$. At sufficiently high reverse bias these free carriers are also swept away, resulting in the expected behavior of an illuminated photodetector.

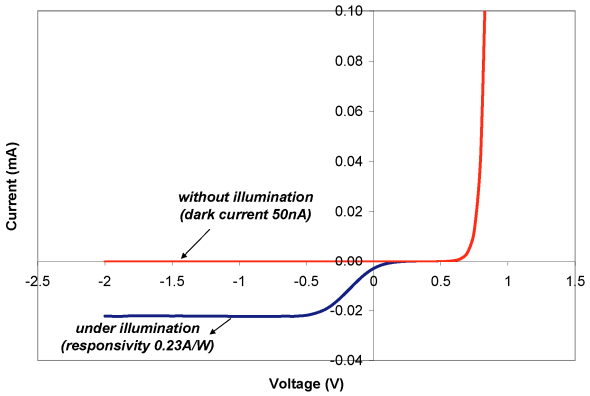

Fig. 8. Voltage versus current characteristics for a 50μm long photodetector with and without illumination.

7. Conclusion

For the first time electrically injected thin film laser diodes and thin film photodetectors were integrated on and coupled to a Silicon-on-Insulator waveguide circuit. This type of integration paves the way to more complex optical functionalities based on the advantages of passive Silicon-on-Insulator waveguide circuits and active III-V devices.

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