Compact wavelength router based on a Silicon-on-insulator arrayed waveguide grating pigtailed to a fiber array

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Abstract: We demonstrate a compact, fiber-pigtailed, 4-by-4 wavelength router in Silicon-on-insulator photonic wires, fabricated using CMOS processing methods. The core is an AWG with a 250GHz channel spacing and 1THz free spectral range, on a 425×155 μm^2 footprint. The insertion loss of the AWG was reduced to 3.5dB by applying a two-step processing technique. The crosstalk is -12dB. The device was pigtailed using vertical fiber couplers and an eight-fiber array connector.

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1. Introduction

Submicron Silicon-on-insulator (SOI) photonic wire technology promises a boost in the integration scale of photonic integrated circuits. This is realized by exploiting a high lateral and vertical index contrast. With bend radii down to just a few μm having very low excess loss and compact splitters and other functions, the size of many devices, especially wavelength filters, can be scaled down considerably. Combining this Silicon approach with CMOS technology has advantages for telecom applications but also enables the technology to be used in other application areas.

However, currently no actually fiber pigtailed devices with acceptable performance have been reported. Recently, broadband low-loss connection to fiber has been demonstrated [1], however using reduced core single mode fiber. Moreover, while promising wavelength filtering functionality is being shown [2, 3, 4], device insertion losses and crosstalk are still problems for actual application. These issues are harder to solve with high index contrast technology and must be tackled if one wishes to integrate many functions on one chip.

Here we show an ultra-compact SOI wavelength router pigtailed to a commercially available standard single mode fiber array connector using vertical fiber coupling [5]. The die size of the component is smaller than the connector surface, enabling a very elegant and mechanically tolerant packaging approach. The same connector and coupling principle can be used for waferscale testing of the devices. The device was fabricated using waferscale CMOS-based processes, including 248nm deep UV lithography [6]. The wavelength router is a 4-by-4 arrayed waveguide grating (AWG) [7] with a footprint smaller than $0.07mm^2$. The insertion loss of the device is reduced compared to [8] by using a double etch technique in order to lower index contrast in the star couplers of the AWG.

2. Waveguides and fabrication

Structures were created in 200mm SOI wafers with a Silicon layer thickness of 220nm and a 1μm burried oxide. A deep UV lithography stepper with a 248nm illumination wavelength defines patterns in resist. The patterns are transferred into the Silicon layer by a dry etching process. A 220nm deep etch step renders photonic wires and broader (access) waveguides. A preceding lithography and 70nm deep etch step can be used to overlay the deeply etched structures with more shallow structures (Fig. 1). In this work, we used the shallow etch step for simultaneously obtaining the grating fiber couplers and a shallow etch region around the star couplers of the AWG devices (see section 3). The alignment tolerance of the stepper is good enough to avoid additional insertion loss in the tapers between deep and shallow etched waveguides. After etching, de structures are covered with a 750nm thick silica top cladding. The thickness of this oxide cladding was chosen to maximize the grating coupler efficiency (see section 4).

A detailed overview of the processing steps can be found in [6]. The processes are basically CMOS processes, characterized and adapted for the fabrication of photonic circuits, which enforce quite different boundary conditions on the fabrication processes.

Earlier, we measured propagation losses of 2.4dB/cm for 500nm wide wires with an air top cladding and TE polarisation [6]. The device uses a bend radius of 3μm, yielding excess bend losses of the order of 0.01dB [9]. The TM mode has different guiding properties. While it is very hard, if possible, to make a single circuit polarisation-independent, this problem can be resolved using a polarisation diversity scheme [10].
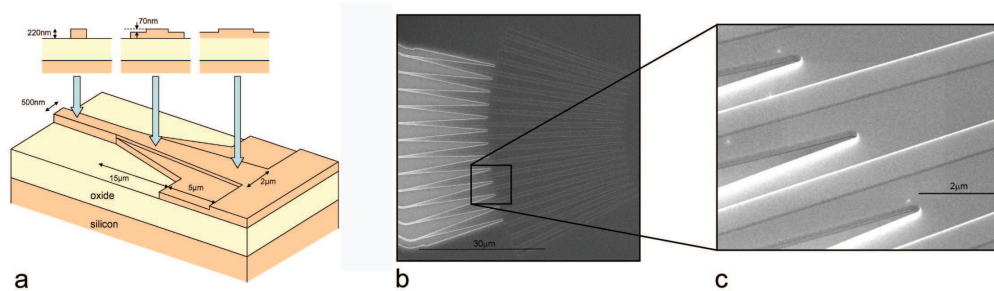
Fig. 1. Star coupler (a) Schematic of the deep to shallow transition (b) SEM picture (c) Detailed SEM picture of the two-level structures

3. Arrayed waveguide grating

The footprint of the actual AWG is 425µm × 155µm (0.066mm^2), using waveguide bends with 3µm radius. Its design parameters are listed in Fig. 2. The device size is limited by the delay length needed in order to obtain the 1THz free spectral range (71.36µm) and the number of waveguides used (10).

In order to reduce the insertion loss of the AWG devices, we applied a double-etch technique. The principle is similar to [11]. All waveguide apertures to the slab region of the star couplers are etched first 70nm deep, yielding a little lower index contrast waveguides better matched to the slab region than the wire waveguides. These waveguides are adiabatically tapered towards the slab region in order to obtain a high star coupler transmission. Then, in a second step the deep wire waveguides are created, using a double lateral taper approach to connect wires and shallow apertures. This is clarified in Fig. 1. Although a lower index contrast is used in the coupler region, the effect on the total AWG size is limited in this case.

As the waveguide propagation constant changes considerably with waveguide width, calculations show that random phase errors in the arrayed waveguides due to stochastic nm-scale width variations (roughness and larger-scale variations) can introduce a high level of crosstalk. Additional phase errors may result from mask digitization. These phase error problems were not tackled yet here. Better fabrication processes and a design that is more tolerant to small width variations, possibly combined with tuning, will be needed in order to achieve a lower crosstalk level. Also, the tapered shallow waveguides are coupled due to the lower index contrast and the small spacing between the apertures (± 200nm). Coupling between the arrayed waveguides at the star couplers lowers insertion loss. However, in these designs, not only the apertures of the arrayed waveguides, but also the input and output waveguides of the AWG were coupled. The abberations introduced by this coupling can enhance the star coupler transmission, but the phase deviations arising from this should be corrected for [7]. This was not done in these designs, which can be expected to result in avoidable higher crosstalk.

4. Fiber pigtailing and chip design

In order to couple light from and to fiber, we use broadband shallow grating couplers. Light is coupled to standard single mode (9µm core) fibers. The fibers are mounted under an 8° angle and the gratings couple light into broad waveguides [5]. These waveguides are then tapered down to narrow wires using an adiabatic linear tapers. The etching depth of the gratings is 70nm again. With a 750nm thick oxide top cladding and an index matching material between fiber and grating, the theoretical maximum coupling efficiency is 46%, with a 1dB bandwidth of 46nm, giving sufficient power budget for many applications and characterization.
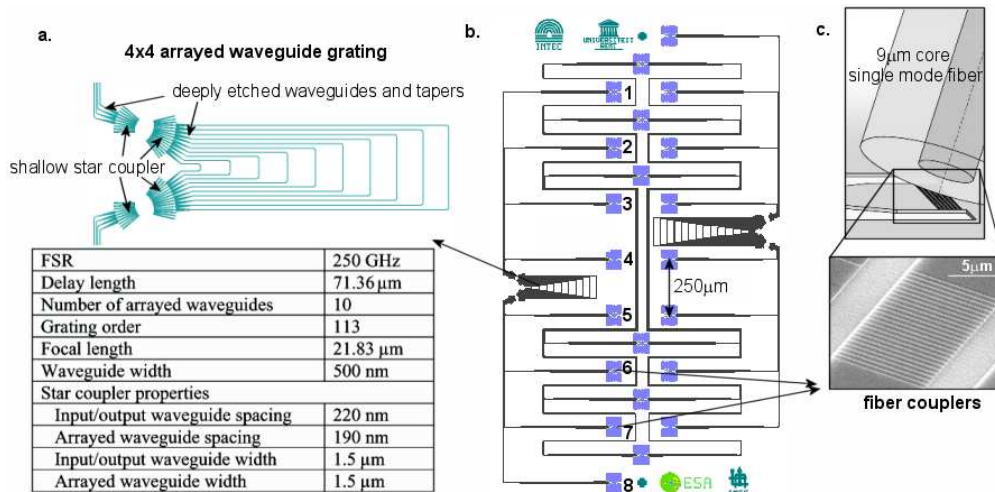
a.

4x4 arrayed waveguide grating

deeply etched waveguides and tapers

shallow star coupler

FSR	250 GHz
Delay length	71.36 μm
Number of arrayed waveguides	10
Grating order	113
Focal length	21.83 μm
Waveguide width	500 nm
Star coupler properties	
Input/output waveguide spacing	220 nm
Arrayed waveguide spacing	190 nm
Input/output waveguide width	1.5 μm
Arrayed waveguide width	1.5 μm

b.

250μm

c.

9μm core/single mode fiber

5μm

fiber couplers

Fig. 2. (a) AWG and its designed parameters. (b) chip layout of the AWG with access waveguides and fiber couplers (numbered 1 to 8). (c) fiber coupler setup principle and SEM picture of the grating coupler.

The advantages of this approach are the relaxed alignment tolerances and the possibility of waferscale testing. A higher coupling efficiency can be obtained by using a non-uniform grating and a bottom reflector, theoretically yielding less than 1dB loss over a 35nm bandwidth [12]. The grating couplers work for TE polarisation, with a measured TE/TM extinction ratio of about 20dB. However, the polarisation dependency of the complete integrated circuit can be resolved by extending the fibre coupler idea to two dimensions [10].

The 4×4 AWG devices were designed with all input and output port fiber couplers in a 1-by-8 array with a spacing of 250μm. The die is 2mm^2 in size and contains two separate AWG devices, access waveguides, fiber couplers and alignment features. Six additional fiber couplers, connected two by two by simple waveguides, are used for aligment. The chip layout is show in Fig. 2, also illustrating the fiber coupler principle.

The 250μm fiber coupler spacing allows us to use a commercially available eight single-mode fiber array connector to align to all ports simulteaneously. This connector consists is a Si V-groove assembly with a pyrex cover and fiber facets under a 8° angle. First the connector is aligned (with in-plane translation and optimization of two rotational axes) to the six aligment fiber couplers. At this stage, a transmission measurement can be done on each of the connected fiber pairs. Then, the connector is translated to the AWG inputs and outputs and transmission measurements can be taken again. The connector is slightly tilted under 1° with respect to the chip in order to let the connector safely rest on the sample after alignment. After alignment, the connector is glued to the chip using UV cureable glue with low shrinkage. The great alignment tolerance of the fiber couplers, combined with on-chip alignment features facilitate alignment and surviving the gluing. The fiber coupling is illustrated in Fig. 3. As the actual die size is smaller than the connector surface, the chip could be cleaved to just that area and the final component will be barely larger than the connector. Also mechanically, this configuration is very attractive.
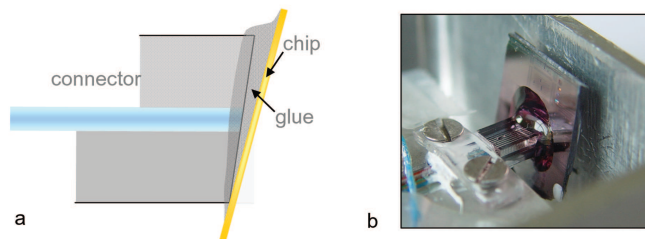
Fig. 3. Pigtailed chip. (a) Schematic (b) Picture. here the chip was cleaved larger than necessary. The actual die size is smaller than the connector surface.
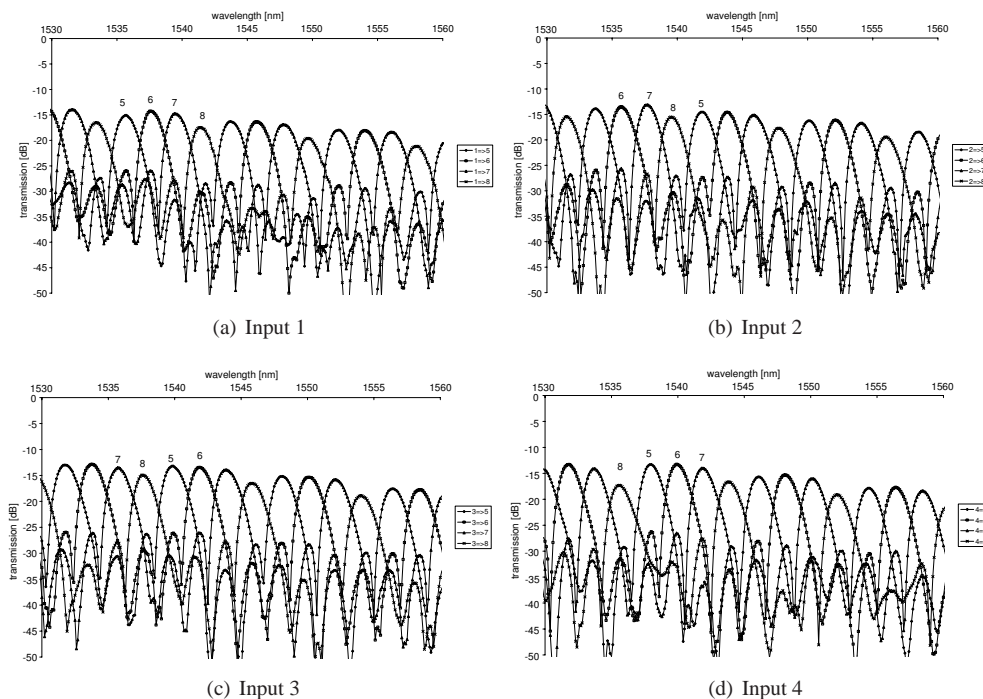

(a) Input 1

(b) Input 2

(c) Input 3

(d) Input 4

Fig. 4. Overlayed normalized fiber-to-fiber transmission spectra of a 250GHz channel spacing AWG. Spectra from the each input to all outputs are shown

5. Performance of the pigtailed device

Structures were characterized in transmission using the ASE of an EDFA as a broadband light source and a spectrum analyzer. The polarisation was filtered and optimized for maximum transmission. The obtained transmission spectra were normalized on the direct transmission from light source to spectrum analyzer, and thus give the total fiber-to-fiber loss including connector, fiber coupler and access waveguide loss and the insertion loss of the AWG.

Figure 4 shows the transmission spectra of the AWG with a 2nm (250GHz) designed channel spacing and 8nm (1THz) designed free spectral range (FSR). Transmission of each input port to all 4 output ports is shown. The channel spacing is 250GHz, but the 1.025THz FSR slightly deviates from the designed value, making the AWG not perfectly circular. The total (fiber-to-fiber) insertion loss of the device is 12.5dB for the best channels.

In this device, the fiber-to-fiber insertion loss for the outer input and output ports (1,4,5,8) is intrinsically higher than that for the inner ports (2,3,6,7). However, the transmission spectra and the low waveguide propagation loss suggest the fiber-to-fiber insertion loss non-uniformity is dominated by a residual in-plane rotational misalignment of the connector to the chip, making the outer input and output ports experience higher loss. The shortest alignment waveguide on the sample is 2.4mm long. On a nominally identical sample, the fiber-to-fiber transmission through this waveguide (and the to fiber couplers) was -13dB before gluing the connector to the chip. With about 0.5dB of waveguide losses, the maximal fiber coupler transmission efficiency is then about 24% (with the air gap). The actual AWG insertion losses for the inner and outer input waveguide to all output waveguides can be calculated from transmission measurements on the AWG (taken again before gluing). One has to compare with the transmission of the alignment waveguides. However, the uncertainty on this comparison is quite high due to the possible difference in alignment. By comparing with the shortest alignment waveguide, and compensating for the difference in aligment and access waveguide lengths, we can calculate the upper limit for the the actual AWG insertion loss of the best channel to be 3.5dB.(It is possibly better but difficult to measure). This is significantly better than the 8dB of an AWG device previously reported on [8]. After addition of the (index matching) glue, the fiber coupler efficiency is expected to be higher. However, during the gluing alignment can get slightly disturbed. Still, with the best fiber-to-fiber insertion loss of 12.5dB and an upper limit of the AWG device insertion losses of 3.5dB, this gives an upper limit of the fiber coupler efficiency of 35% with the glue. As mentioned in Section 4, the coupling efficiency can be enhanced by a more advanced coupler design.

The sidelobe level of the measured transmission spectra (crosstalk) is still -12dB in the case of this pigtailed component, which clearly leaves room for future improvement. As mentioned in Section 3, we think this crosstalk level is mainly due to (stochastic) phase errors in the arrayed waveguides.

6. Conclusion

We fabricated a compact 4-by-4 arrayed waveguide grating wavelength router with a 250GHz channel spacing in submicron Silicon-on-insulator technology. The device is vertically coupled to an eight-fiber array connector glued to the chip. By applying a double etch technique, the insertion loss of the AWG device has been reduced to maximally -3.5dB for the best input to output path. The best fiber-to-fiber insertion loss is 12.5dB. Crosstalk is still -12dB, however it is possible to further reduce this. Fabrication of the SOI devices was done using CMOS processing methods including 248nm deep UV lithography.