TOLERANCE CONTROL FOR PHOTONIC CRYSTAL STRUCTURES FABRICATED WITH DEEP UV LITHOGRAPHY

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Abstract *We describe the need for good tolerance control in planar photonic crystals. Although resolutions of 200nm are possible, an accuracy of 10nm is difficult. We discuss techniques to improve this accuracy for deep UV lithography.*

Introduction

Nanophotonic structures, like photonic crystals, have wavelength-scale dimensions. For telecom wavelengths, the smallest features thus have a size of about 200nm. While these are large compared to state-of-the-art CMOS structures, the required accuracy for nanophotonics is of the order of 10nm. However, most fabrication processes, including high-resolution lithography, can introduce deviations, either reproducible or random, to the design, that are too large for any commercial application. While deep UV lithography has the required resolution of 200nm, tolerance control down to 10nm is difficult without special precautions or additional processing. This applies to feature size as well as to roughness due to processing. With the standard process, our photonic crystal waveguides are limited to losses of 20dB/mm.
In this paper, we discuss some causes of deviations in nanophotonic structures deep UV lithography, and some techniques to improve the tolerance control.

Fabrication Process

While most of the effects described here apply to any fabrication process, we used deep UV lithography at 248nm on Silicon-on-insulator as our standard process [1]. The features are defined with a stepper on an 8" SOI wafer (220nm top Silicon with 1μm of oxide), and the illumination conditions can be varied for each die to do detailed process characterisation. The wafers then go through a silicon etch and an oxide etch, about 800nm into the oxide. Figure 1 shows some examples of these structures. Note that there is still significant roughness on the sidewalls.

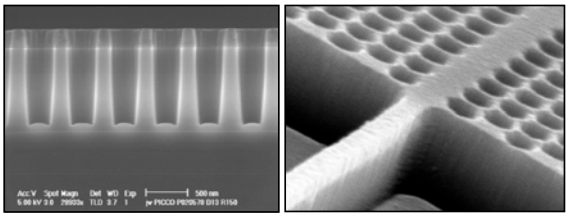

Figure 1:SOI photonic crystals fabricated with deep UV lithography. Pitch/diameter = 500nm/300nm.

Process window

Reproducibility is very important for commercial application. This requires a process that doesn't vary much over time, and with a window of process parameters large enough to allow for acceptable deviations. In CMOS devices, different types of structures are defined in separate steps, so the process is optimised for each structure individually. In nanophotonics, alignment between waveguides is often so critical that all structures should be defined together. In photonic crystal circuits, ridge waveguides should be printed together with photonic crystal holes. Figure 1 compares photonic crystal holes with waveguide lines as a function of lithography exposure dose. With increasing dose, the lines shrink and the holes grow. Therefore, to print both together on target, a bias has to be applied to one or the other on the mask.

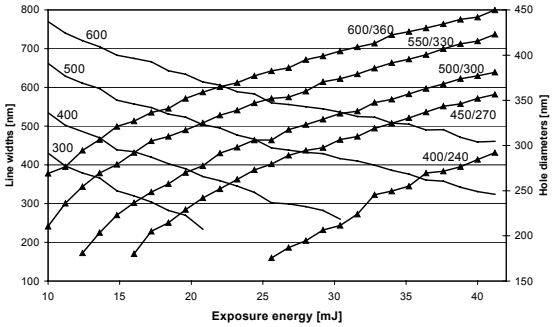

Figure 1: Hole diameters and line widths as a function of lithography exposure dose. Markers: hexagonal lattices of holes, marked with design pitch and diameter. Lines: Lines marked with design line width.

Generally, the lithography process window is defined by the allowed variation in focus and exposure dose. For larger process windows, one can increase the resolution by changing either the illumination wavelength or the numerical aperture, or use better resists. Figure 2 shows the best elliptical process window a triangular lattice of 300nm holes with 500nm pitch and for 200nm holes with 400nm pitch for the following processes.

	λ	NA	Resist
A	248nm	0.63	UV3
B	248nm	0.70	UV3
C	248nm	0.70	TIS248
D	193nm	0.63	TIS193

Contours indicate the largest elliptical area where the hole diameter deviates less than 5% from the design value. It is clear that the process window can easily be enlarged, even without using 193nm lithography.

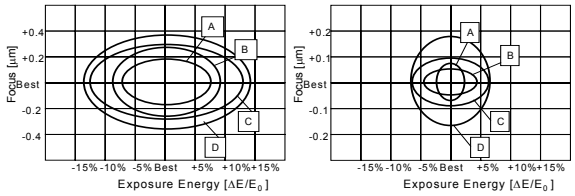

Figure 2: Process windows for photonic crystal holes with the different processes listed in the table above. Pitch/diameter [nm]: 500/300(left), 400/200 (right).

Optical proximity effects

Photonic crystals consist of densely packed lattices of submicron holes. During lithography, neighbouring holes will influence each other during lithography. These proximity effects also occur in e-beam lithography, but in optical lithography the effect is coherent, so it can be either positive or negative [1]. While the lithography can be targeted to print the bulk holes correctly, near the borders of the lattice (or near intentional defects like waveguides) the holes will print either larger or smaller than in the bulk. As the functionality of photonic crystal structures is often determined by the precise geometry of the defects, optical proximity effects have significant consequences. Figure 3 shows band diagrams of a W1 photonic crystal waveguide (one missing row) of 300nm holes with 500nm pitch. For larger border holes we see a significant change, with the mini-stop-band (MSB) wavelength dropping as much as 50nm for a 20nm increase in border hole diameter. Without corrections optical proximity effects can amount to 40nm with standard 248nm lithography.

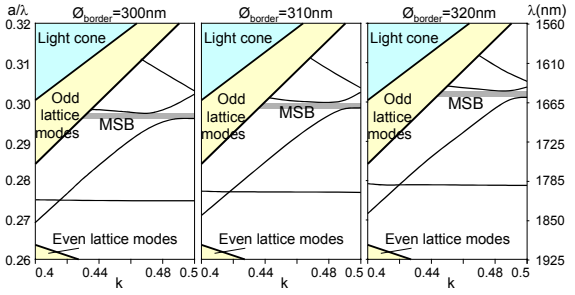

Figure 3: Band diagrams of W1 photonic crystal waveguide with modified border holes. The bulk lattice has a pitch of 500nm and a hole size of 300nm.

Optical proximity effects decrease with higher resolutions. Where a correction is still necessary, it should be applied directly on the mask at the design stage. However, these optical proximity corrections are hard to model. Therefore, we have designed a large number of test structures to empirically determine the necessary corrections for a variety of photonic crystal structures. These corrections have then been applied to the next mask.

Roughness

High-contrast photonics often require deep etching. However, most dry-etch technologies cause a significant amount of sidewall roughness. In nanophotonic structures, this can cause serious scattering [2]. Our experimental results show that for structures without treatment for sidewall roughness, losses for both photonic crystal waveguides and single-mode photonic wires are limited to 20dB/mm.

There are several methods to reduce this sidewall roughness. In many cases, this roughness is caused by irregularities at the boundaries of the resist patterns. Smoothening the resist patterns with a plasma treatment can significantly reduce the roughness, as shown by Lam Research.

An alternative in the SOI material system is a partial thermal reoxidation of the silicon top layer [3]. Because this is a diffuse process, reoxidation smoothens the silicon sidewalls. Because the thus grown oxide is more voluminous than the original silicon, the holes will be reduced in size. However, this technique only applies to the silicon top layer, and the oxidation has no effect on the silica cladding.

Conclusion

Current fabrication technology for nanophotonic structures requires extremely accurate process characterisation and control. While several lithography techniques attain the resolution of 200nm required for photonic crystals, the 10nm accuracy on the feature size is very difficult to achieve.

We compared process parameters for deep UV lithography and determined the process window for different of photonic crystal structures. We also studied the optical proximity effects in photonic crystal waveguides and determined the required corrections.

Because dry etching causes significant sidewall roughness, we studied a number of ways for smoothening the sidewalls and reduce scattering.

Acknowledgements

Part of this research was supported by the European Union in under the IST-PICCO project.

Part of this research was carried out in the framework of the Belgian IAP project PHOTONnetwork.

Wim Bogaerts thanks the Flemish Institute for the industrial advancement of scientific and technological Research (IWT) for a specialisation grant.

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