Fabrication of Photonic Crystals in Silicon-on-Insulator Using 248-nm Deep UV Lithography

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***Abstract*—We demonstrate wavelength-scale photonic nanostructures, including photonic crystals, fabricated in silicon-on-insulator using deep ultraviolet (UV) lithography. We discuss the mass-manufacturing capabilities of deep UV lithography compared to e-beam lithography. This is illustrated with experimental results. Finally, we present some of the issues that arise when trying to use established complementary metal–oxide–semiconductor processes for the fabrication of photonic integrated circuits.**

***Index Terms*—Integrated optics, lithography, nanotechnology.**

I. Introduction

In THE last decade, optical communication has been one of the driving forces behind the rapid expansion of the Internet, providing the huge bandwidths needed for the explosively increasing data traffic. However, when compared to the ultralarge-scale integration of complementary metal–oxide–semiconductor (CMOS) circuits, the optical components used for routing and switching in fiber-optical links are large and primitive looking, and the larger part of the functionality is still performed in the electrical domain, requiring many electrooptical conversions.

In recent years, more and more functions are being implemented optically and combined into photonic integrated circuits (PICs). Still, current PICs combine only a limited number of functions on a single chip, as large areas are required just to guide the light from one functional element to another through waveguides. In particular, waveguide bends prove a crucial limitation, as the bend radius needs to be adequately large to prevent radiation losses.

Therefore, to increase the level of integration in PICs, it is not only necessary to scale down the individual functional elements, but also reduce the area required for waveguiding. This requires narrow waveguides that can have tight bends with little loss.

One possible solution to implement these efficient waveguides, and possibly other functions, is the use of photonic crystals (PhCs). PhCs are wavelength-scale periodic structures with a strong refractive index contrast. Another candidate is the photonic wire (PW), a narrow ridge waveguide, typically a few hundred nanometers in width, with high refractive index contrast.

Because of the large refractive index contrast needed for photonic crystals and photonic wires, semiconductor is the preferred material for ultracompact PICs. For active devices, one needs a material system that can emit light at the required wavelengths, implying the use of III-V semiconductors. For passive applications, it is also possible to use silicon, particularly in the form of silicon-on-insulator (SOI). SOI consists of a thin silicon film separated from the silicon substrate by an oxide layer. Because of the large refractive index difference between Si and SiO_2, this material can act as a highly confined optical waveguide.

Both PhCs and PWs have features well below 1 μm in size, and need to be fabricated with a precision of tens of nanometers. For research purposes, the most used pattern definition technique is e-beam lithography. However, this technique is not suitable for mass manufacturing, as it is a serial and, therefore, slow process. Classical photolithography, used for the fabrication of the current generation of PICs, lacks the resolution to fabricate these submicrometer structures.

Deep ultraviolet (UV) lithography is the continuation of optical lithography into the deep UV wavelengths range. With illumination wavelengths of 248 nm or less, this technique offers both the resolution and the speed required for the mass manufacturing of PICs with submicrometer features.

In this paper, we will discuss experiments to fabricate SOI components for ultracompact PICs, and in particular photonic crystals, using deep UV lithography with an illumination wavelength of 248 nm. First, an overview of photonic crystals and their use in optical waveguides is given in Section II. Section III discusses the SOI material system for optical applications. Current lithography techniques for the fabrication of PICs are compared to deep UV lithography in Section IV. In Section V, we give an overview of the experiments, and the issues that arose are described in Section VI, as well as the proposed solutions to address them.

II. Photonic Crystals

A. Photonic Crystals

Photonic crystals are one-dimensional (1-D), two-dimensional (2-D), or three-dimensional (3-D) periodic structures with a high refractive index contrast within a unit cell. From the moment of their conception [1], these structures promised to

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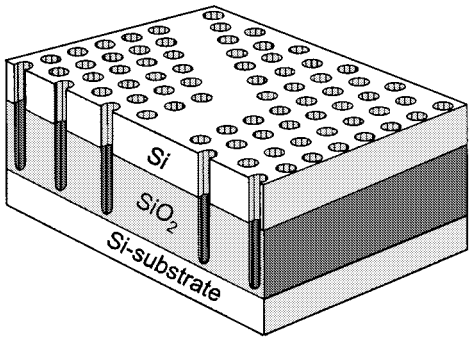

Fig. 1. Schematic drawing of a photonic crystal slab waveguide in silicon-on-insulator. The light is confined in the top silicon layer by total internal reflection, while horizontally it is confined by the photonic crystal holes.

scale down the size of optical components significantly. Their high refractive index contrast with wavelength-scale periodic modulation gives these structures strong diffractive properties, including photonic band gaps (PBGs). These are wavelength ranges in which the light is forbidden to propagate through the PhC. Because of the PBG, light will be bound to defects introduced in the crystal, like waveguides (line defects) or high-Q cavities (point defects) [2]. When completely embedded in a photonic crystal, these structures can be completely lossless, allowing for short bends without radiation loss. In addition, photonic crystals can be very dispersive, being able to act as wavelength selective element [3].

An important condition for the emergence of a photonic bandgap is a sufficiently high refractive index contrast within a unit cell, typically 2–1. This sets a limit to the possible material systems for photonic crystals. For infrared and optical applications, the most promising material system is semiconductor. Not only does it have a high refractive index n (typically $n > 3$), but it is also a suitable material for microfabrication.

B. Photonic Crystal Slabs

Photonic crystals can be made periodic in one, two, or three dimensions. 3-D photonic crystals control light in all directions, but because of their volumetric nature are hard to make for optical wavelengths. Alternatively, we can use a combination of a 2-D PhC with slab waveguide [4]–[6]. A schematic drawing of a waveguide in a 2-D photonic crystal slab made of a triangular lattice of air holes in semiconductor is given in Fig. 1. In these photonic crystal slab waveguides, light is controlled in plane by the photonic crystal made of holes or rods in high index material. Vertically, the light is confined in the high index layer of the slab by total internal reflection. Even though the confinement is not perfect, these structures have the advantage that they can be fabricated with existing high-definition lithography and dry etching techniques, as is discussed further.

Photonic crystal geometry is heavily dependent on the used polarization. For TE-like polarization (dominant electric field in the plane of the slab waveguide), the best photonic crystals consist of triangular lattice of air holes in high index materials. These holes should be superdense, i.e., the hole should be large compared to the interhole spacing. For TM-like polarization, one should use square lattices of high-index pillars in air [2]. In this paper, we will only discuss photonic crystals for TE-like polarization.

C. Out-of-Plane Scattering

Unlike 3-D photonic crystals, 2-D photonic crystal slabs do not confine light perfectly. In the slab material, light is confined by the vertical index contrast, but this confinement is lost where the material has been removed, like in the air holes of Fig. 1. This lack of confinement can cause out-of-plane scattering of the light, resulting in unwanted loss of light in photonic crystal waveguides, cavities, or lattices.

The out-of-plane scattering losses are very much dependent on the choice of vertical layer structure. Simulations show that in layer stacks with a low vertical index contrast, like InP or GaAs–AlGaAs-based heterostructures, light will always couple to the radiation modes in the substrate, but this coupling is weak and results in only low or modest out-of-plane scattering losses [7]–[9]. This will be so for periodic structures, like photonic crystal waveguides, but also where the periodicity is broken, like bends or cavities.

For high vertical index contrasts, like in silicon-on-insulator (SOI), GaAs–AlO_x or semiconductor membranes, light can be kept absolutely confined in periodic structures. It is therefore possible to make PhC-based waveguide that supports a fully guided Bloch mode and, therefore, is completely lossless [6]. However, when the periodicity is broken, losses can be higher than for low-index-contrast layers [8], [9].

Because of out-of-plane scattering losses, the choice of material system very much determines the possible applications. A high vertical index contrast is useful for large structures in which the periodicity is seldom broken, like long, straight waveguides. For waveguides with many bends and other components, a low vertical refractive index contrast might be preferable.

III. Silicon-on-Insulator for Integrated Optics

A. SOI as a Slab Waveguide

SOI was first introduced for CMOS applications to reduce the parasitary capacitance to the silicon substrate. However, it soon proved equally suitable for the purpose of guided-wave optics. SOI consists of a thin silicon layer separated from the silicon substrate by a layer of SiO_2.

Because of the high index contrast between Si $(n = 3.45)$ and SiO_2 $(n = 1.45)$, the top layer can act as an optical waveguide. Moreover, the vertical index contrast is high enough to support a guided Bloch mode in a photonic crystal waveguides.

The use of SOI as an optical waveguide is not a recent development. However, current PICs implemented in SOI use waveguides with large cores, with top Si layers of up to 10 μm thick [11]. For our experiments, we used a top layer with a thickness of only 205 nm.

B. Fabrication of SOI Wafers

SOI wafers are typically fabricated using wafer bonding. For our experiments, we ordered wafers from SOITEC fabricated with the UNIBOND process. First a wafer is oxidized to create the buried oxide layer. Then hydrogen ions are implanted at a well-controlled depth, creating a Smart Cut. This wafer is then

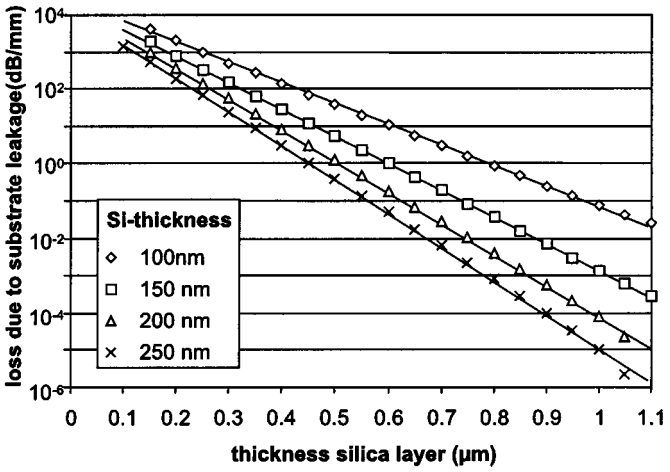

Fig. 2. Semi-log graph of the substrate loss in db/mm as a function of silica layer thickness for four different values of silicon layer thickness.

bonded to a clean Si wafer. Then the substrate of the first wafer is separated along the implanted Smart Cut, and then annealed and polished. For a more detailed description of the UNIBOND process, see [10] and [12].

For the first experiments, we used standard UNIBOND wafers with a buried oxide of 400 nm and a top silicon layer of 205 nm.

C. Substrate Losses

With its high-index contrast, SOI is a good candidate material system for photonic crystal components. However, as the substrate is made out of the same high-index material as the optically guiding layer, part of the light will leak away through the cladding layer into the substrate. This loss sets an upper limit to the performance of any component in the material system. Therefore, it is important that the thickness of both the top Si layer as the buried oxide is chosen well, to keep leakage low while still keeping a single mode waveguide.

1) Calculation Method: We simulated the substrate loss of a TE mode in an SOI slab waveguide at a wavelength of 1.55 μm using the mode expansion tool CAMFR [13]. Refractive indexes were obtained from [14]. To simulate the loss to the open substrate, perfectly matched layer (PML) absorbing boundary conditions were used.

2) Substrate Loss: Calculations show that losses due to substrate leakage decrease exponentially with increasing thickness of the oxide layer. Fig. 2 shows this loss expressed in dB/mm.

Also, the thickness of the top silicon layer has its effect on the substrate leakage. With increasing layer thickness light is better confined into the layer, resulting in a smaller tail in the substrate and a smaller leakage. The slab waveguide remains single mode for a silicon thickness up to 268 nm.

3) Conclusion: To keep leakage of light to the substrate negligible, an SOI layer stack with a thick buried oxide is required. The wafers used for the fabrication experiments discussed in this paper have only 400 nm of buried oxide. According to our calculations, this would give us a minimum loss of 6 dB/mm. For future experiments, a thicker oxide layer will be used.

D. Material Choice

Our choice for SOI as a base material was motivated by several factors. As already mentioned, SOI is a good material for optical waveguides. Moreover, with its high refractive index contrasts, it is possible to make photonic crystal waveguides that sustain guided Bloch modes. Another important factor is that SOI is available in 200-mm wafers, compatible with the IMEC processing facilities.

For these first experiments, we used off-the-shelf wafers from SOITEC, with a 400-nm buried oxide and 205 nm of top silicon. Because of the large substrate leakage of this layer structure, custom-made SOI wafers with a thicker oxide will be used for the final components.

IV. Lithography for Photonic Crystals

A. E-Beam Lithography

Because of their submicrometer features and the need to control the feature size within tens of nanometers, conventional optical lithography is not suitable for pattern definition of these structures. Because of the need for high resolution, e-beam lithography is the most-used technique for research purposes and prototyping. This process, in which structures are written directly into photoresist with a focused electron beam, is capable of defining extremely small features. However, because everything is written in a serial way, the process is very slow and, therefore, not suitable for large volumes.

B. Deep UV Lithography

For mass fabrication, a parallel process is needed that can print all patterns simultaneously. Optical lithography has always been the workhorse for this purpose, but it is limited by optical diffraction. Features reduced down to the size of the illumination wavelength become fuzzy or do not print at all. Therefore, the next generation of optical lithography employs excimer lasers with wavelengths in the deep UV, starting at 248 and 193 nm with research being conducted at 157 nm. At these wavelengths, it is possible to fabricate certain isolated structures with dimensions below 100 nm [15].

For periodic structures, like photonic crystals, optical lithography imposes a limit on the periodicity. The period of the smallest periodic structure that will still print is defined by the illumination wavelength divided by the numerical aperture (NA) of the lens system used [16]. With NAs of 0.6 or larger now common in high-end deep UV steppers, the smallest usable period for 248-nm lithography is therefore about 400 nm.

Because of the prohibitive acquisition and maintenance costs, deep UV lithography is rarely used for scientific purposes, but it is already widely adopted for commercial CMOS fabrication.

C. CMOS Structures Versus Photonic Crystals

Even though the use of deep UV lithography for the fabrication of electronic integrated circuits (ICs) is already widespread, the techniques optimized for CMOS cannot be ported to other fields in a straightforward way.

Structures used for photonic ICs are often different than those used for their electrical counterpart. This is also true for

photonic crystals. While the spacing between contact holes for CMOS circuits is never smaller than the hole itself, the holes in photonic crystal slabs are packed very close together.

Another difference is that for photonic ICs, it is sometimes necessary to fabricate very different structures in a single processing step. An example could be a ridge waveguide, consisting of a single line, coupling into a photonic crystal waveguide, consisting of a superdense array of small holes. For optimal alignment between these two waveguides, both should be printed together. However, the very different nature of both structures requires different exposure conditions for the lithography process.

V. Fabrication Experiments

The fabrication was done at IMEC in Leuven, Belgium. Even though there is a large difference between CMOS structures and photonic crystals, the first lithography and etching experiments were performed using CMOS process evaluation masks with large arrays of densely packed contact holes in a square lattice. For further experiments on photonic crystals, a dedicated mask was designed.

A. Fabrication Process

1) Lithography: The deep UV lithography facilities we used at IMEC for these experiments consist of an ASML PAS 5500/300 deep UV stepper with an illumination wavelength of 248 nm and a 4× reduction factor from the mask to the wafer. The stepper uses 200-mm wafers and is attached to an automated wafer-processing track that handles resist coating, baking, and development.

The fabrication process is illustrated in Fig. 3. First, a 200-mm SOI wafer is coated with resist. For this purpose, we experimented with different thickness of Shipley UV3 resist. Before illumination, the resist is prebaked and a NFC antireflective coating is spun on top. Then the wafer is illuminated in the stepper. Before it is developed, the resist goes through a post-exposure bake. After development, the wafer is ready for etching.

2) Etching: The etching of the SOI wafer is done using a double etch recipe, in different chambers. There is no exposure to air when changing between the two etch chambers. The top silicon layer is etched using an ICP low pressure/high density etch system with a chemistry based on Cl_2–HBr–He–O_2. For the buried oxide, we used a dual frequency, medium pressure/medium density etch system with a CF_4–CHF_3 chemistry.

For the first experiments, the etching was evaluated on a-SOI wafers. These are wafers with a similar layer structure as the commercial SOI wafers we used, but the top silicon layer is replaced by a layer of amorphous silicon. These wafers can be fabricated in-house from ordinary silicon wafers. Although the a-SOI layer structure is different from crystalline SOI from the viewpoint of optical components, it has comparable etch properties at a substantially lower cost per wafer.

B. Dense Square Lattices

The first lithography tests were carried out using a CMOS process evaluation mask with dense contact holes. The mask consists of square lattices of holes of various size and pitch, with spaces equal to the hole's diameter or larger. To make superdense lattices similar to photonic crystals, we overexposed these structures to print the holes larger, but with the same pitch.

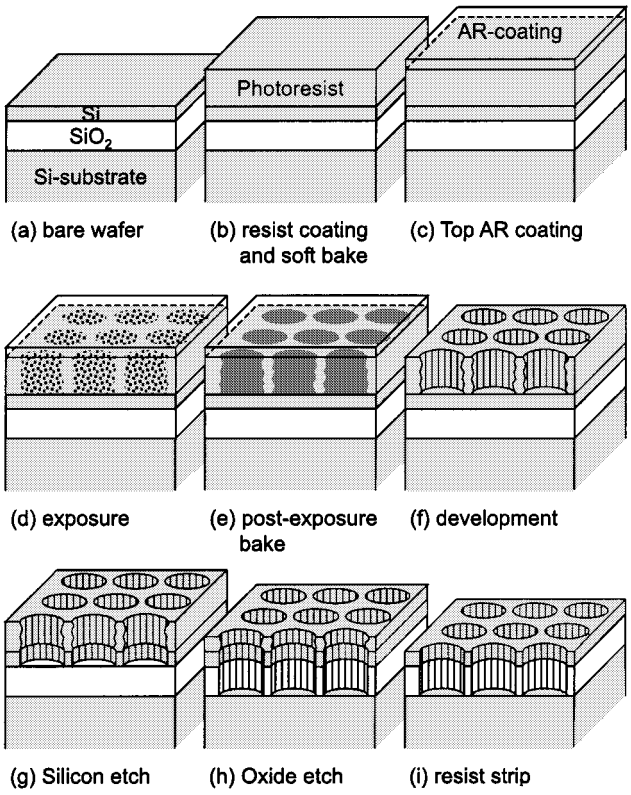

Fig. 3. Fabrication process with deep UV lithography in SOI.

We manufactured lattices with pitches from 400 to 600 nm, and using overexposure reached radius/pitch ratios of 0.25–0.35. For each target we had an adequate budget in both focus and exposure dose.

Etch tests on a-SOI wafers show holes with straight sidewalls in both the a-Si layer and the oxide layer, with no discernible discontinuities between the different layers. Sidewalls have little deviation from the vertical and show very little roughness. We also performed the same test on a standard SOI wafer. This showed similar quality of sidewall smoothness. Fig. 4 shows a top-down and a cross section of 300-nm holes with a pitch of 500 nm.

Even though these structures are not really photonic crystal, we can conclude that is possible to fabricate superdense, photonic crystal-like structures with deep UV lithography.

C. Superdense Triangular Lattices

For further evaluations, a dedicated mask with photonic crystal structures was designed. This mask contains triangular lattices with various pitch and hole size, both for inspection in top-down view as cross section. It also contains some photonic crystal designs described in literature, where necessary adapted to the SOI layer structure [17], [18].

Lithography tests on these structures show well-defined resist patterns for the holes. Even as the holes on the reticle are defined as hexagons in a triangular lattice, they are rounded

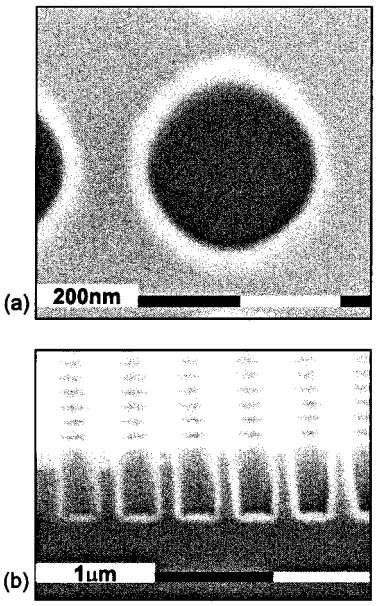

Fig. 4. Top–down view and cross section of etched holes in SOI. Pitch is 500 nm, hole size is 350 nm.

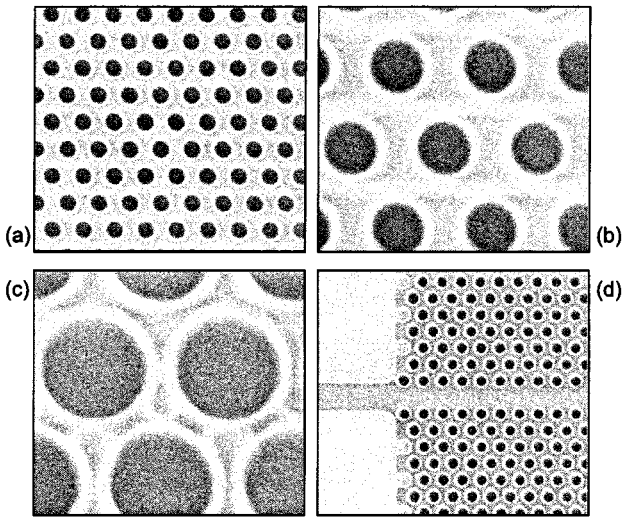

Fig. 5. Resist patterns of superdense holes in a triangular lattice. (a), (b) Pitch = 500 nm, hole diameter = 300 nm. (c) Pitch = 500 nm, Hole Diameter = 430 nm, resist channeling between holes. (d) Photonic crystal waveguide, Pitch = 460 nm, Hole diameter = 280 nm.

by the lithography process. For the various pitches hole diameters, the holes are very uniform throughout the lattice. Fig. 5(a) and (b) shows the resist patterns of a triangular lattice with 500-nm pitch and 300-nm holes. Fig. 5(d) shows a photonic crystal waveguide with 460-nm pitch and 280-nm holes together with a narrow incoupling waveguide. Only for the extremely dense $(\mathrm{radius/pitch} > 0.4)$ holes the resist between the holes is broken down. This is mainly due to the strong effect of sidelobes from the hole's image in the resist. An example is given in Fig. 5(c).

VI. Lithography Issues

Although these first experiments are promising for the fabrication of photonic ICs with deep UV lithography, there are some issues that need to be addressed. A common problem in dense structures is proximity effects: the shape and size of a structure is changed with the presence or absence of a neighboring structure. Secondly, the various structures on photonic ICs each require different lithography conditions to print on target.

A. Optical Proximity Effects

1) Principle: Photonic crystals are superdense periodic structures with feature sizes close to the illumination wavelength. This causes neighboring holes to interfere with each other during lithography. Because of this, holes in a photonic crystal may interfere constructively and print larger or interfere destructively and print smaller than solitary holes. In uniform lattices, this effect is not noticeable, as the illumination energy will be chosen to print the holes in the lattice on target. However, at the boundaries of the lattice, or near defects like a waveguide or cavity, some holes lack neighbors and will therefore print differently than their counterparts in the bulk of the lattice. This phenomenon is described as optical proximity effects (OPE).

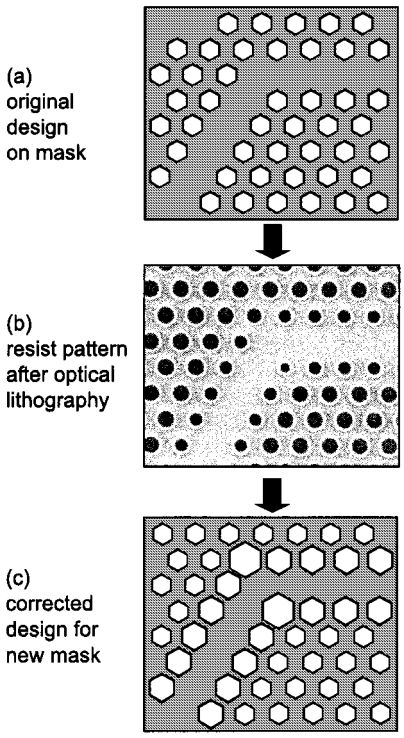

Fig. 6. Exaggerated illustration of OPEs. Although the holes on the reticle are all of the same size (a), the holes in the bulk of the lattice print different than the holes near the waveguide (b), so to correct for this OPC should be added to the mask (c).

To correct for OPE, the features on the mask should be altered. This is illustrated in Fig. 6. Holes near a lattice defect are printed smaller and are, therefore, enlarged on the mask. It is evident that a good understanding of the OPE is necessary to design the structures with optical proximity correction (OPC).

2) Effect in Superdense Lattices: The denser the structures and the smaller the pitch, the stronger the optical proximity effects become. Fig. 7 shows the optical proximity effects for a

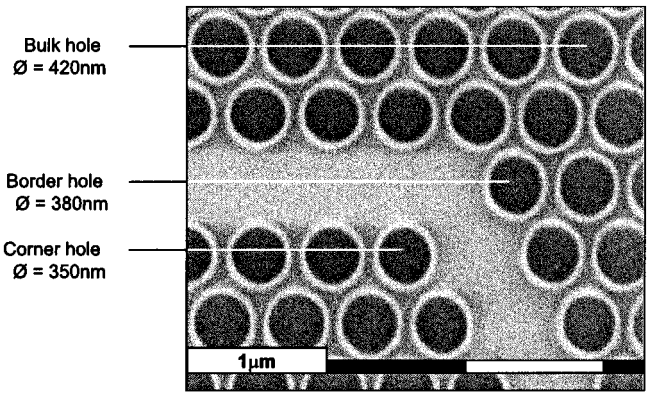

Fig. 7. Measurement of OPEs: 530 nm pitch. Although not noticeable on first sight, the holes in the corners are 70 nm smaller than the holes in the bulk of the lattice.

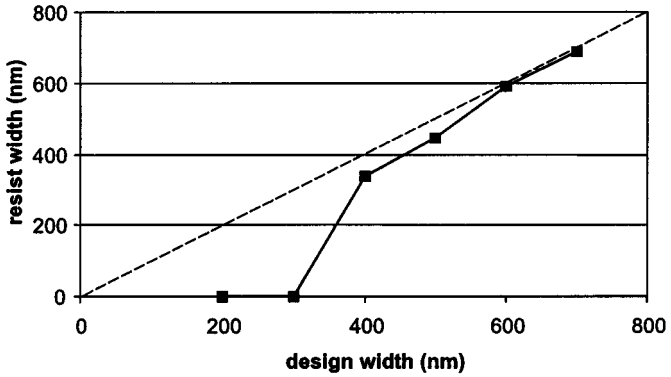

Fig. 8. Measurements of line-hole bias. Resist line width as a function of design line width of a narrow line when printed at the dose-to-target of a superdense triangular lattice (500-nm pitch, 300-nm hole size). The dashed line indicates features printed on target.

lattice with a relatively large pitch of 530 nm, but with holes targeted at 420 nm. In this case, border holes print 40 nm smaller than the hole in the bulk, while the hole in the inner corner prints 70 nm smaller.

Because the functionality of most photonic crystals is determined by the defects like waveguides and cavities, the control of the hole size near the defects is of the utmost importance. Therefore, the new mask structures were included to study the effect of OPE in photonic crystals in more detail and determine the necessary OPC for a variety of situations.

B. Line-Hole Bias

A difference between CMOS structures and PICs is that for CMOS lithography, structures on a mask are always very similar. Contact holes are never printed in the same step as lines. Therefore, the lithography process can be tailored for each type of structures individually. For many PICs, most structures with very different geometries are on the same level of the chip, and are preferably printed together. This is no problem for components that are much larger than the illumination wavelength, but not so for the wavelength-scale features of photonic crystals and photonic wires. Small holes generally need a much higher illumination dose-to-target than a narrow line a few hundred nanometers in width. This means that at the dose-to-target of a photonic crystal, a photonic wire will print much narrower, or even disappear completely. This is generally true for small features against a light background. Fig. 8 gives the width of a narrow line after lithography as a function of the design line width when printed at the dose-to-target for a photonic crystal with 500-nm pitch and 300-nm hole diameter. Also, the incoupling waveguide in Fig. 5(d) is printed almost 50 nm narrower than designed.

To correct for this problem, the lithography should target the features with the highest exposure dose (e.g., small holes), while a bias should be applied on the mask to the features that need less energy to print on target.

VII. Conclusion

First experiments show that deep UV lithography has the potential for the mass fabrication of ultracompact photonic ICs based on photonic crystals or other wavelength-scale features. Lithography and etching experiments with photonic crystals in silicon-on-insulator showed well-defined holes with very little edge roughness.

However, because photonic integrated circuits often contain features with a variety of geometries, and features unlike any features used in CMOS, processing rules valid for a CMOS structures cannot be applied in a straightforward way. Additionally, different features requiring different exposure conditions should be biased on the mask to print on target together.

The dense nature of photonic crystals also gives rise to optical proximity effects. Interference between the images of the individual holes changes the size of the holes. Due to this, holes that lack one or more neighbors will print different. To correct for this, optical proximity corrections should be applied on the mask at the design stage.

Summarized, we can say that deep UV lithography is a good candidate to provide mass-manufacturing capabilities to the world of ultracompact photonic ICs.

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