Photonics Research Gro

Diffractive micro-electromechanical structures in Si and SiGe

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21/08/2013

Contents:

- **Motivation**
- **SiGe based Grating Light Valves**
- **SiGe based 2D movable gratings**
- **Si Photonics MEMS devices**
- **Summary**

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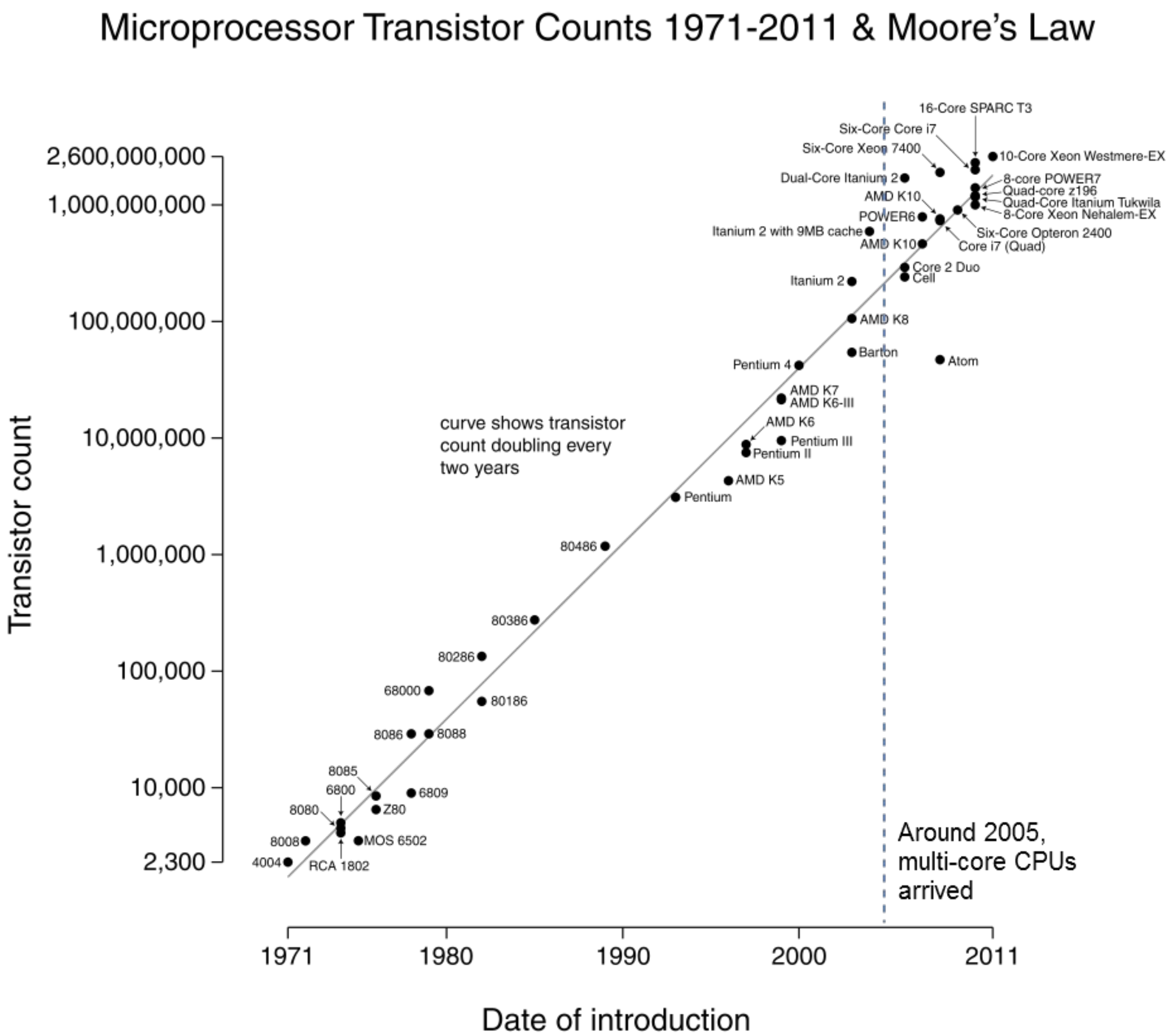
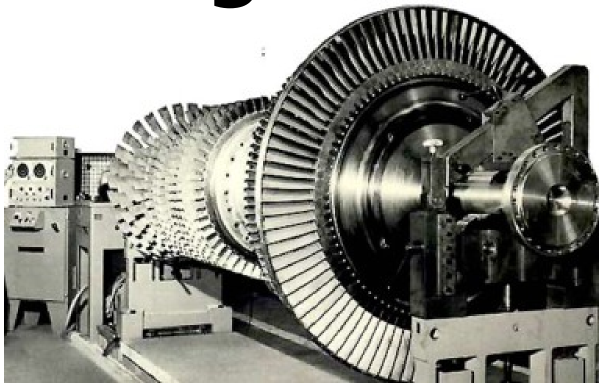
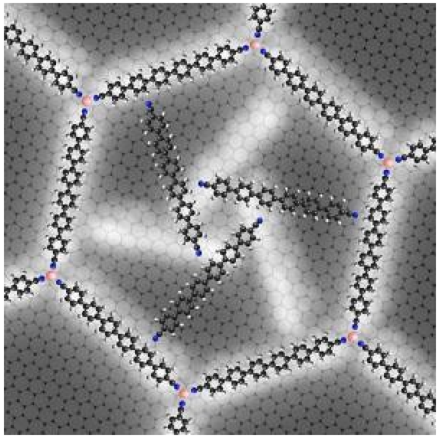
Moore’s Law



Microprocessor Transistor Counts 1971-2011 & Moore’s Law
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
Date of introduction
1971
1980
1990
2000
2011
curve shows transistor count doubling every two years
Around 2005, multi-core CPUs arrived
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
Quad-Core Itanium Tukwila
8-Core Xeon Nehalem-EX
AMD K10
POWER6
Six-Core Opteron 2400
Itanium 2 with 9MB cache
AMD K10
Core i7 (Quad)
Core 2 Duo
Cell
Itanium 2
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
8080
Z80
8008
MOS 6502
4004
RCA 1802

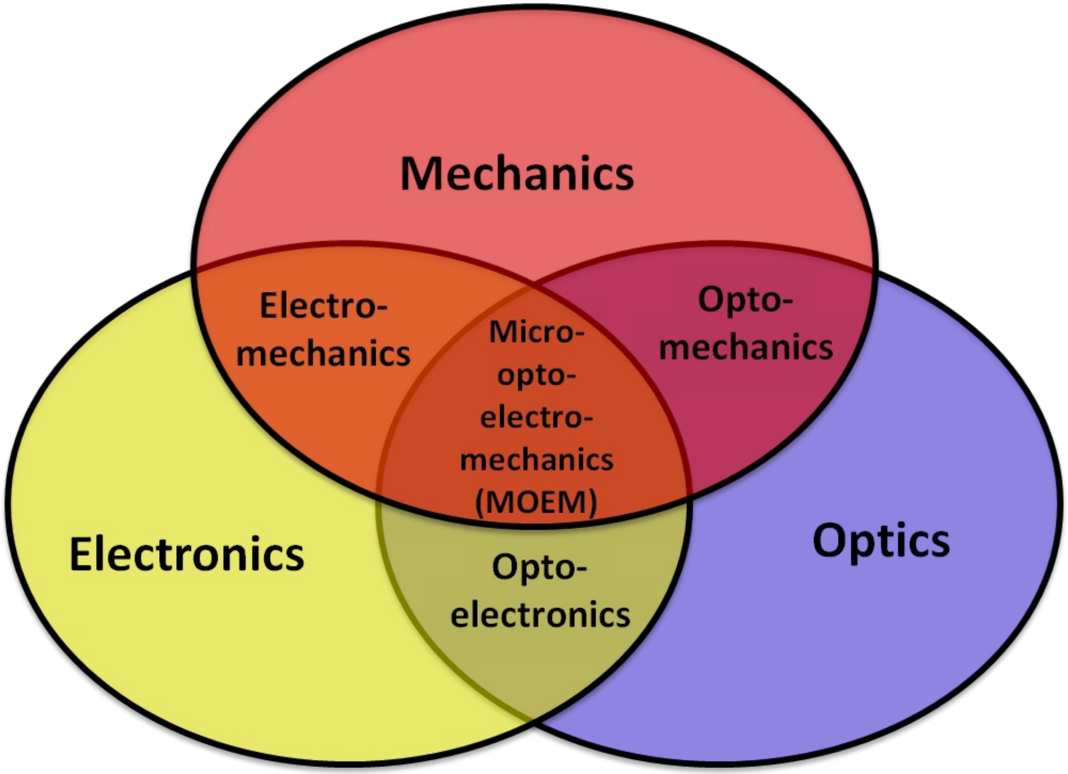
The promise of micro/nanotechnology: Integration

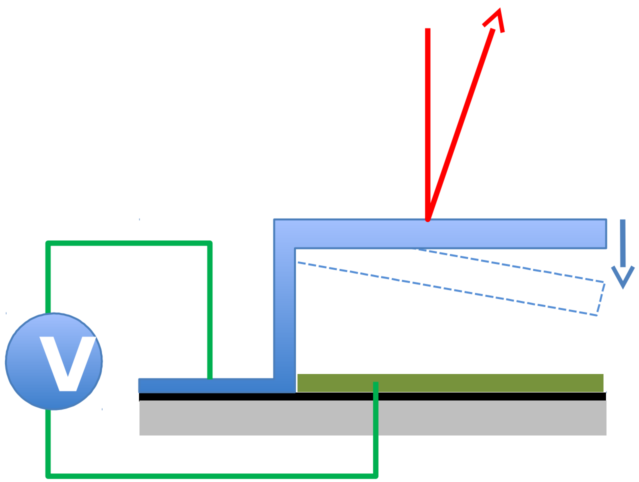




'Micro/ Nano' is an enabling technology; Integration is the key!

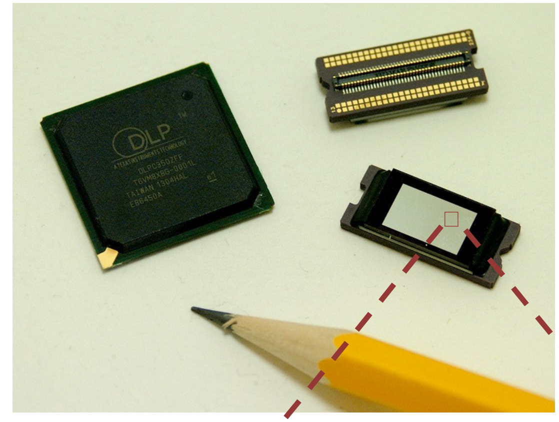
Micro-opto-electromechanical systems (MOEMS)

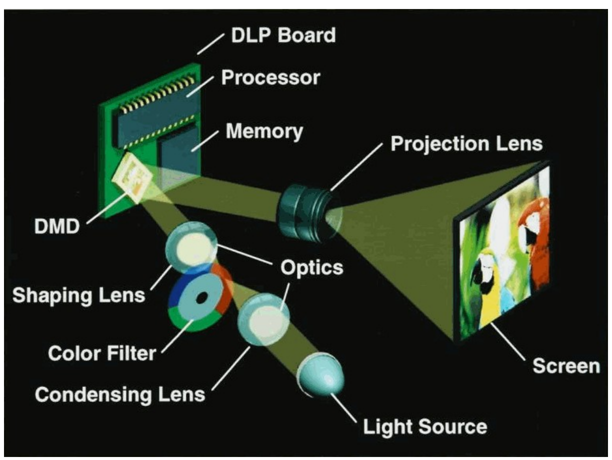


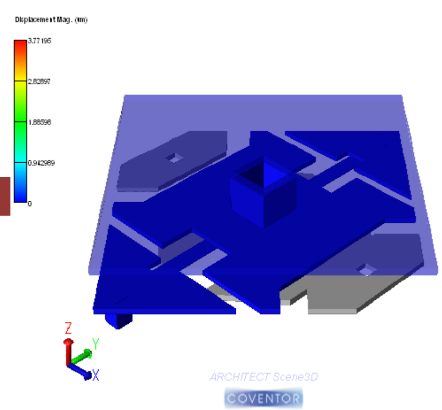


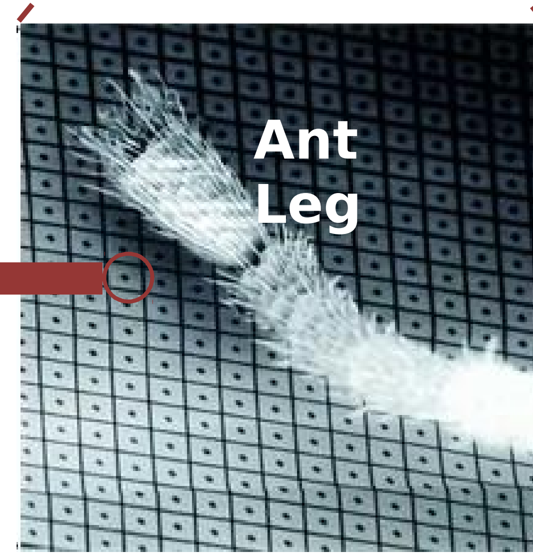
Electrical actuation Mechanical displacement/ deformation Modulation of optical information

Miniaturization in the form of MOEMS



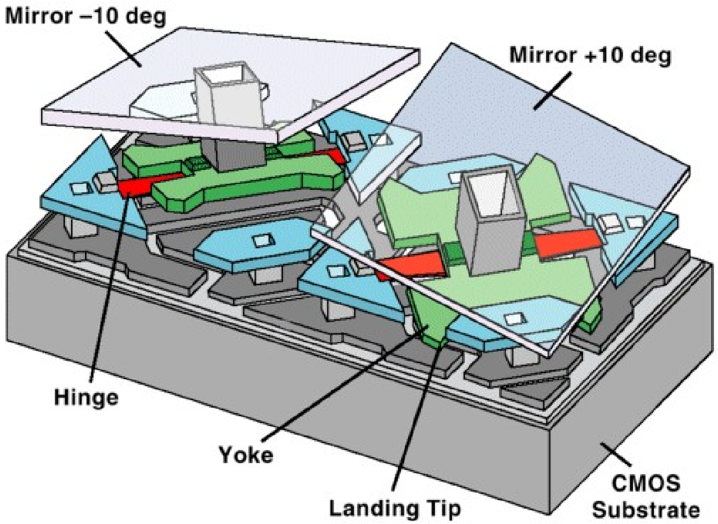


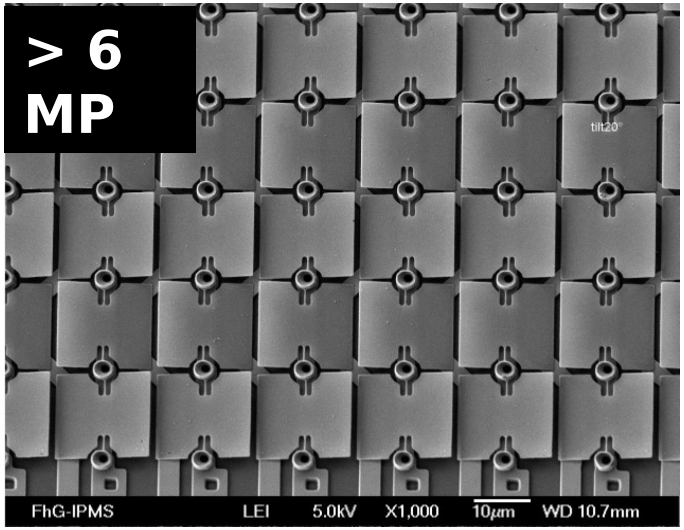


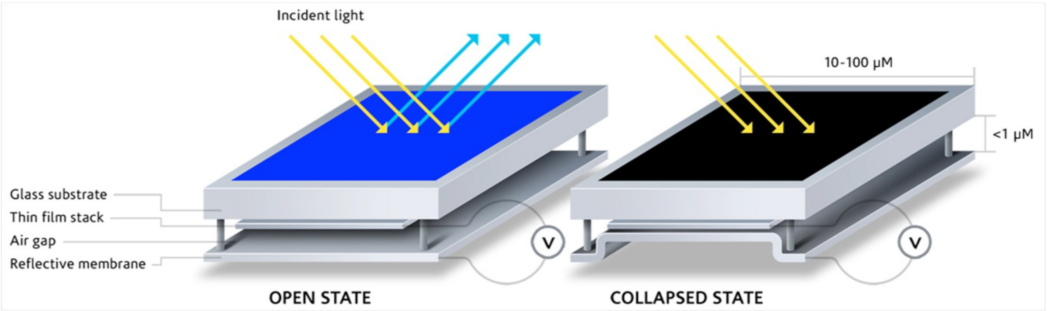


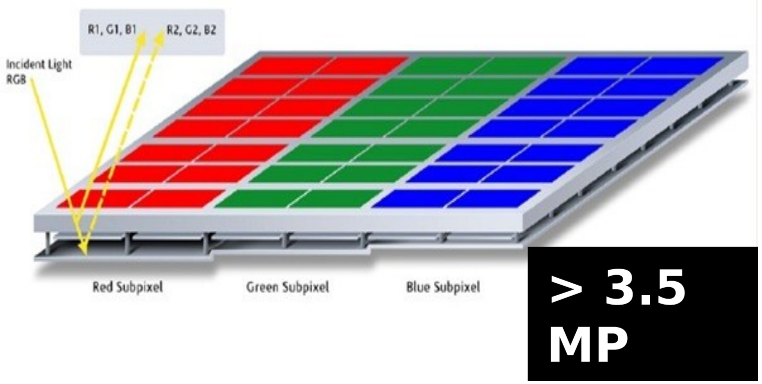
*http://www.coventor.com/mems-solutions/products/mems/scene-3d/

MOEMS devices in large arrays





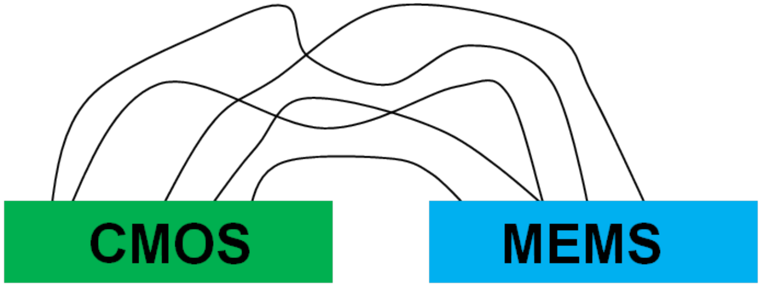


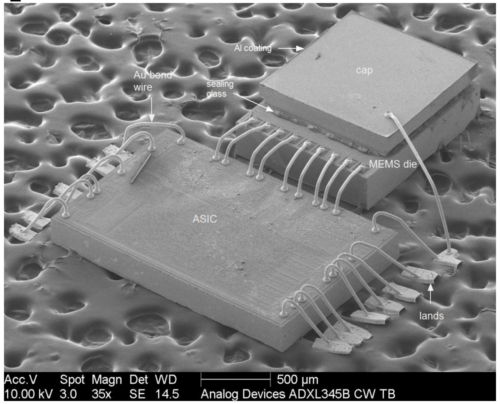


Possibility to set-up large matrices of MOEMS
** Need of electrical actuation mechanism of individual pixels**

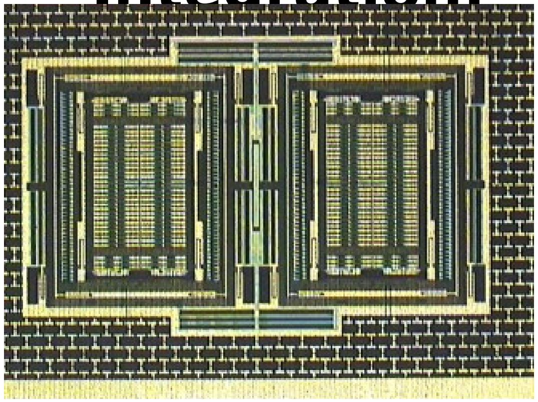
Integration of MEMS and CMOS

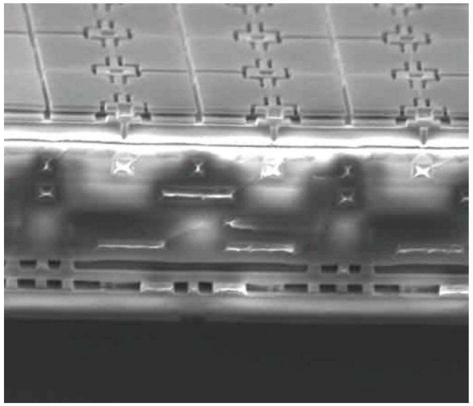
Hybrid Integration:





Monolithic Integration:





GEMINI (Generic Electronics and Microsystems INtegration Initiative)

CMOS Front end

CMOS Back end

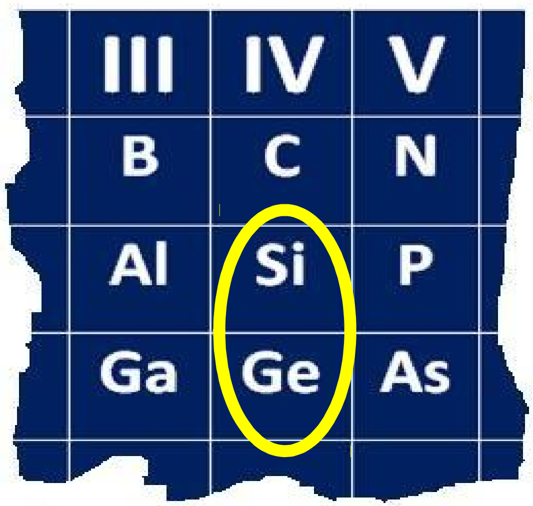
Dicing and packagin

Pre-processing
Any MEMS temperature budget
Complicates IC processing

Modified backend sequences
MEMS process temperature limited
Complicates IC and MEMS processing

Post-metal processing
MEMS process temp. max~ 450° C
‘transparent’ to CMOS

processed at significantly lower process temperatures (≤ 450°C) than Si (≥ 800°C).
➢ Properties are similar to Si and can be tailored by adjusting



Si Deposition temp. ~ 800°C

Monolithic integration by post processing:
✓ Standard IC processing possible.
✓ Newest updates can be introduced without any problems.
✓ Most compact but limited to processing temperature.

SiGe:
Young’s modulus: 120 GPa
Density: 4100 Kg/ m3
Strain Gradient: 7 x 10-4 /µm

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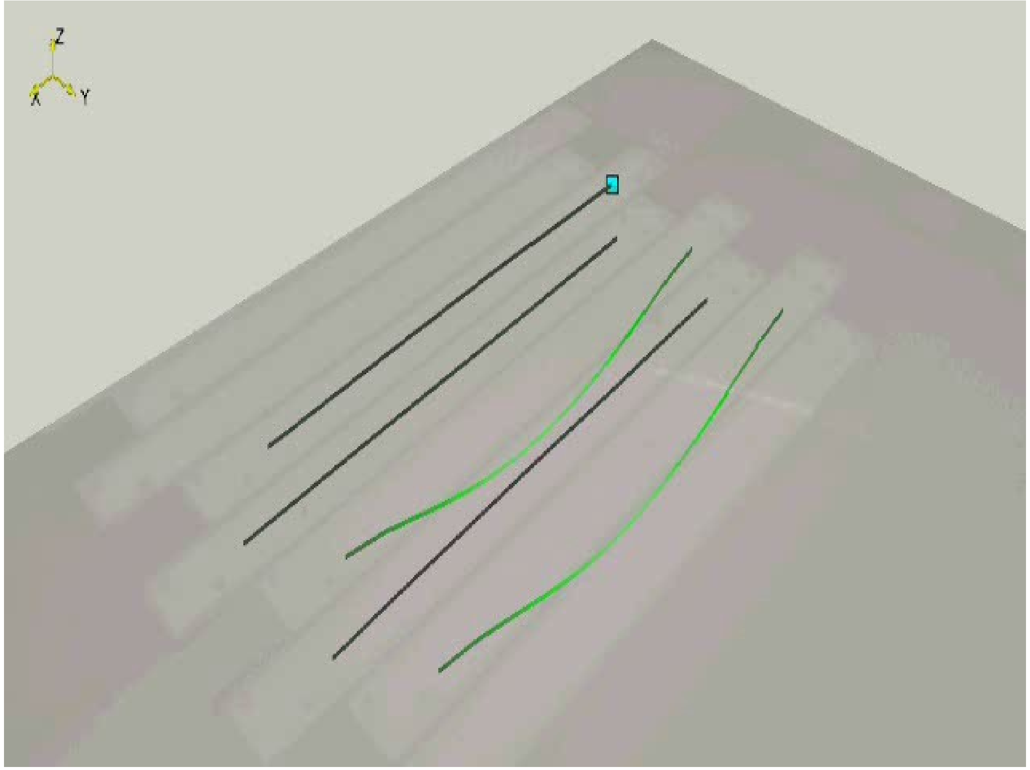
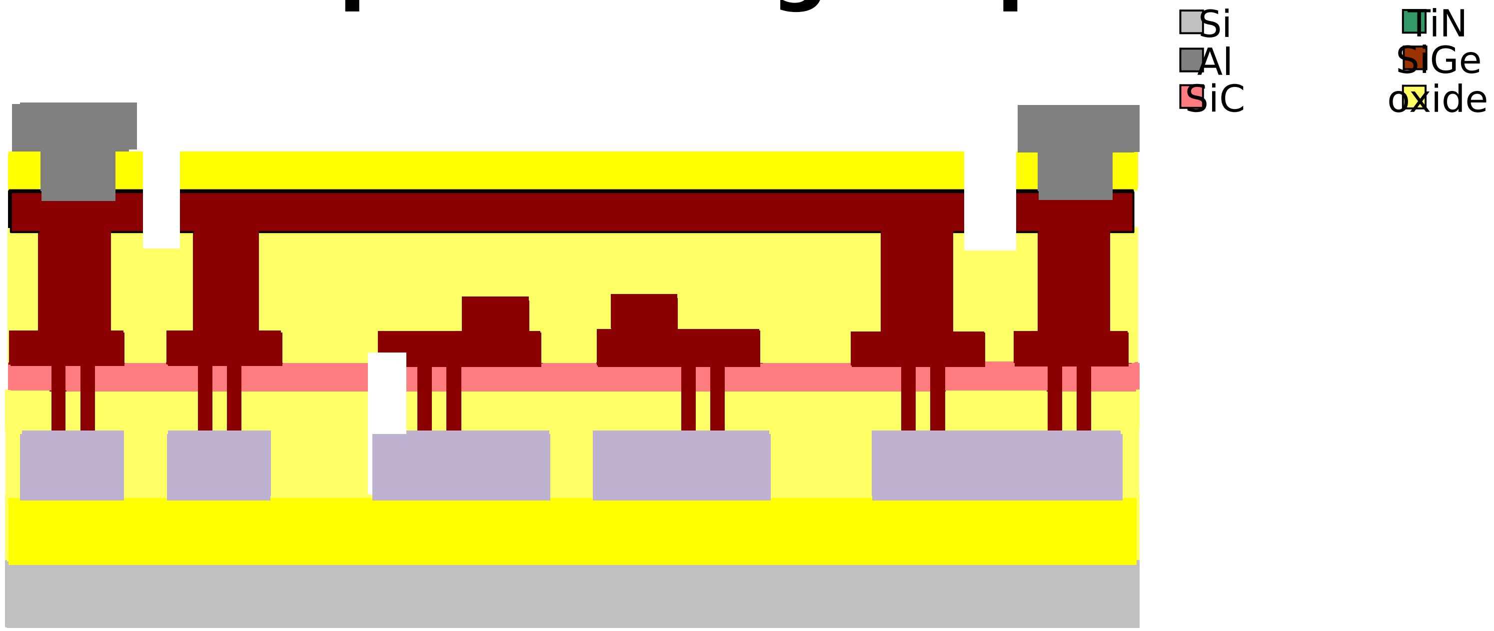
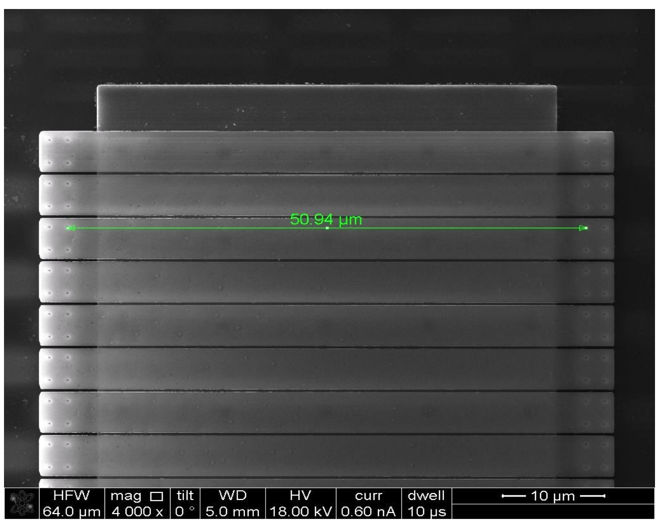
Important parameters to focus on:

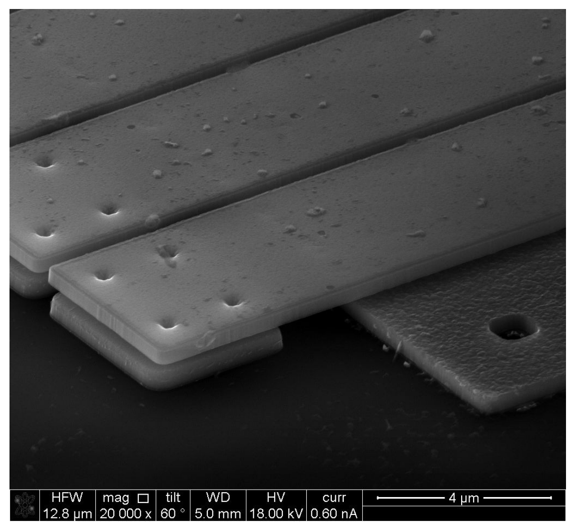


- Optical performance
  - Contrast
  - Diffraction efficiency
- Mechanical performance
  - Resonance frequency
  - Damping nature
  - Settling time

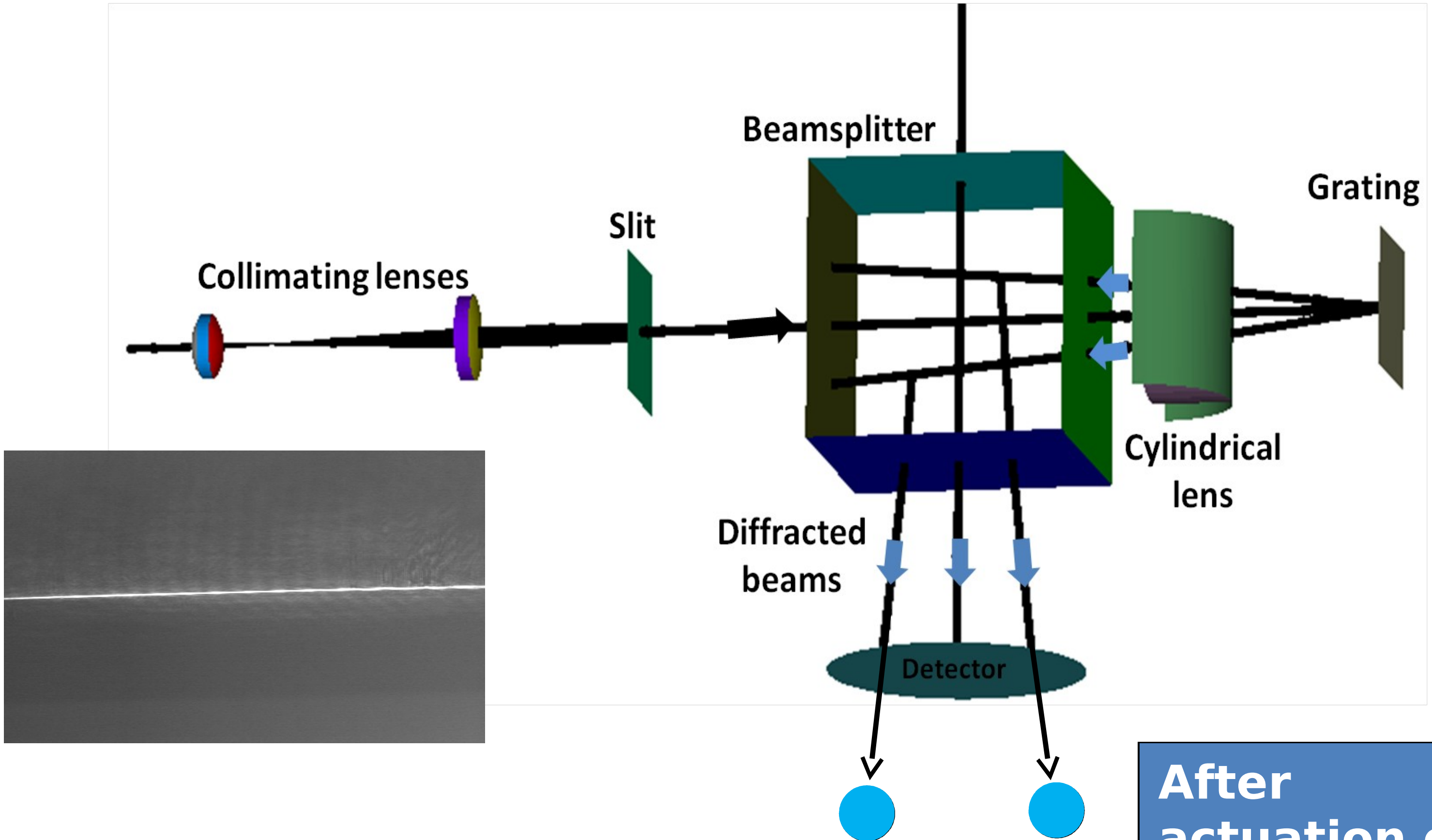
GEMINI SiGe processing steps:







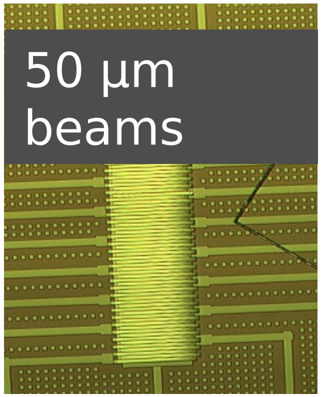
Optical measurement setup:

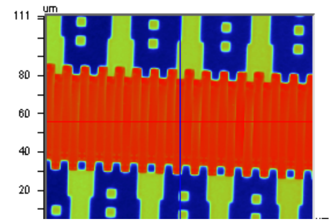


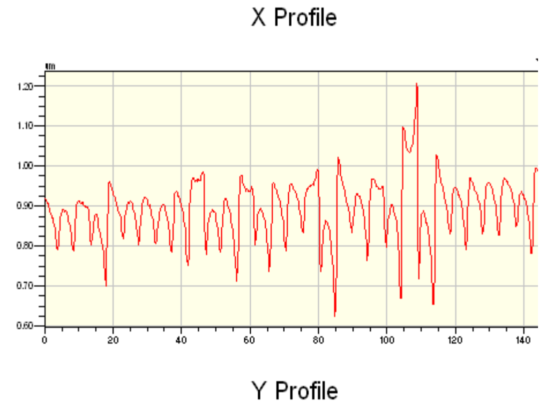
After actuation of the GLV pixels

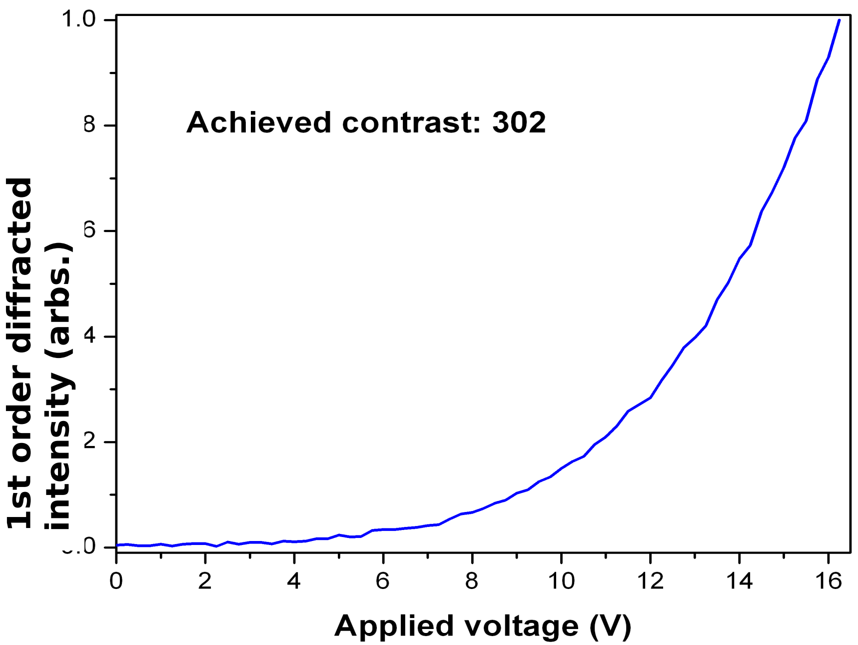
$$\text{Contrast} = \frac{\text{Diffracted power in the } \pm 1\text{st order after actuation}}{\text{Power in the } \pm 1\text{st order before actuation}}$$

Non-uniform flatness of the consecutive microbeams:



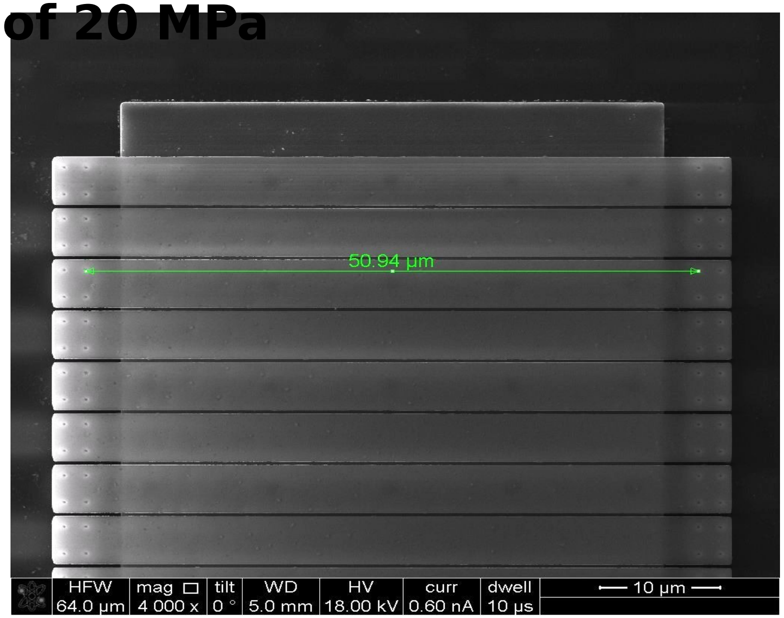


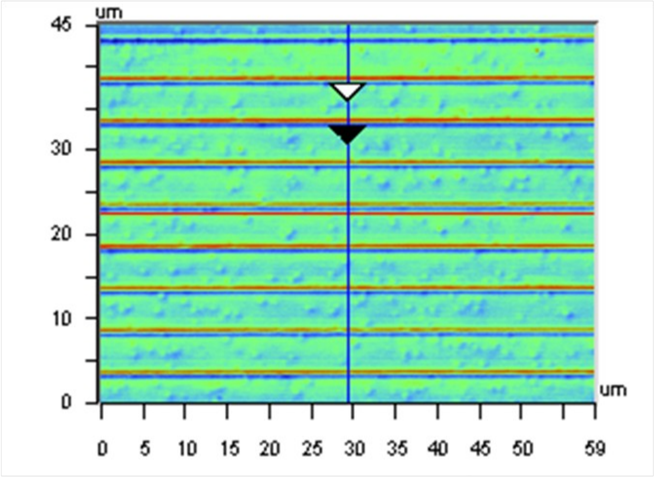


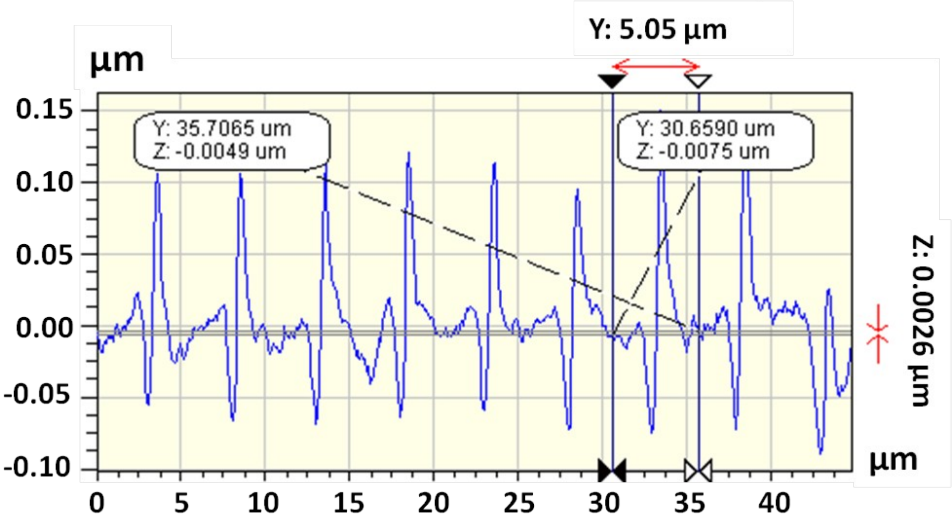


Improved GLV structures with uniform flatness:

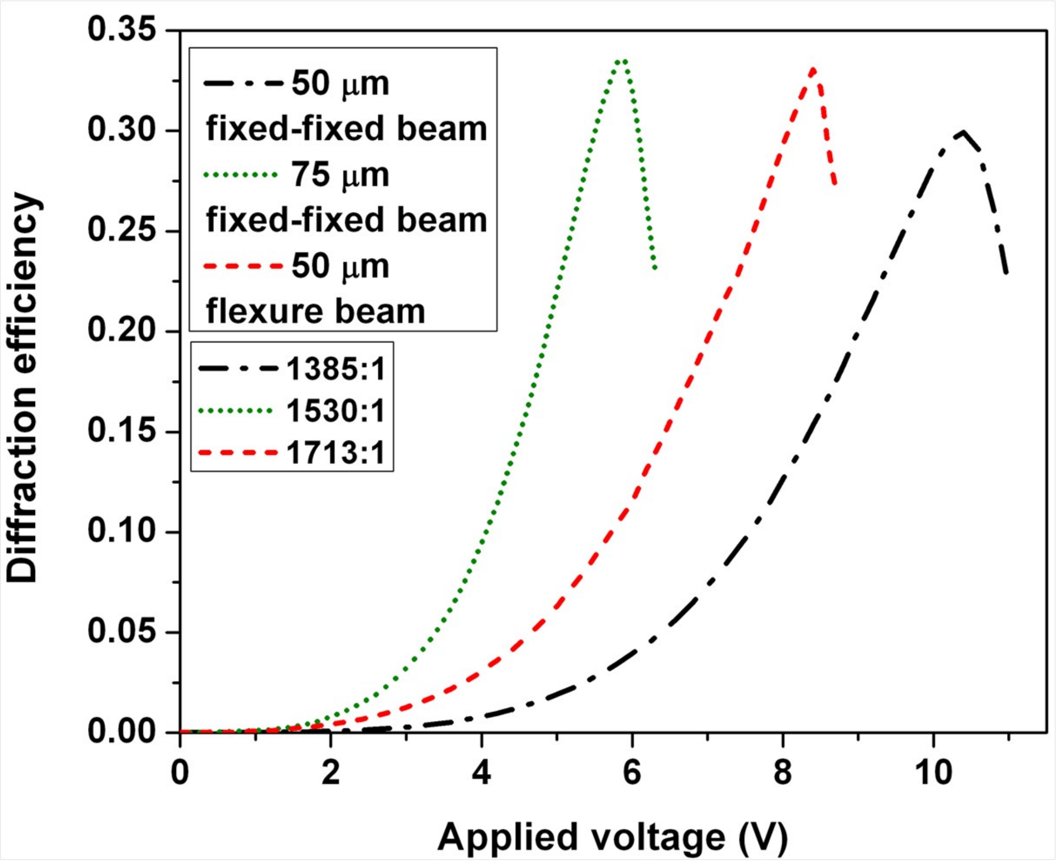
With additional tensile stress of 20 MPa





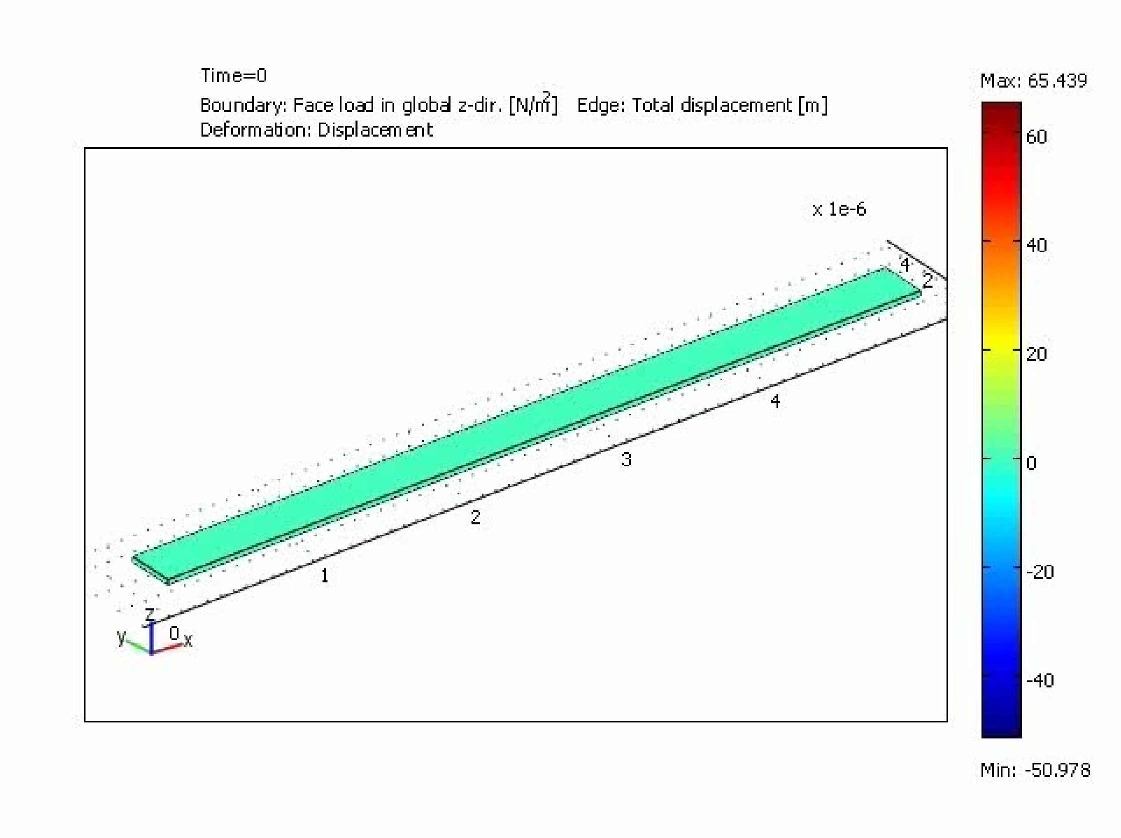


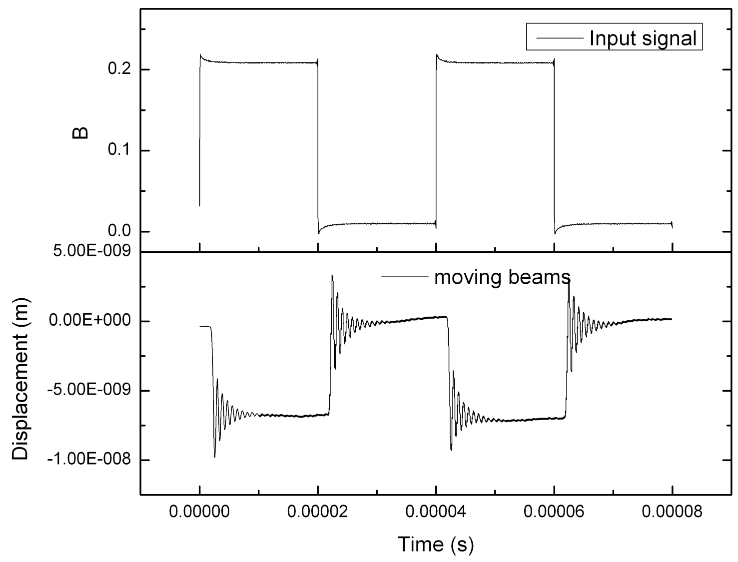
Static optical response:



- Attained High contrast.
- ~ 67% of the incident light was diffracted in the first orders (Max. 72% from theory).

Dynamic behavior of the microbeams

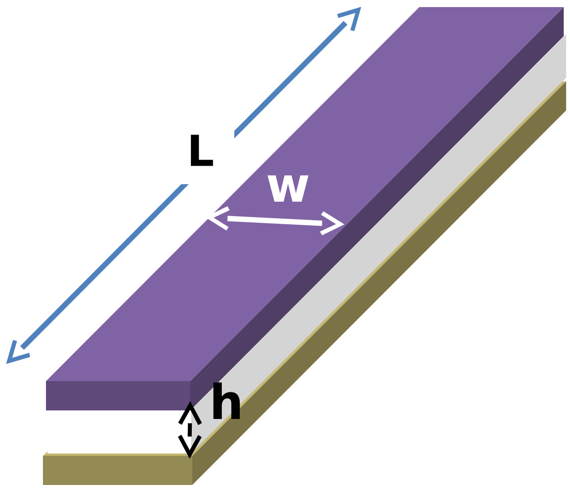


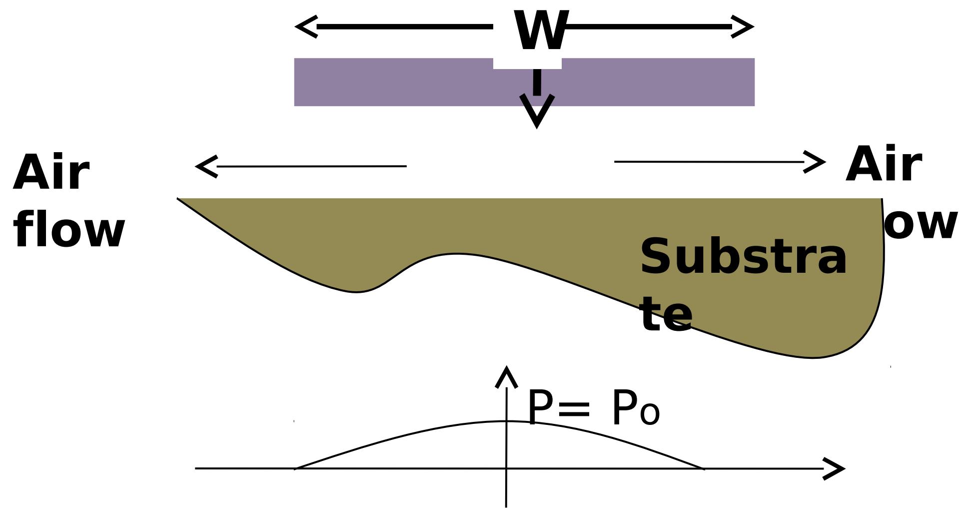


Task:

➢ Decrease the vibration settling time

Squeezed film damping in MEMS:

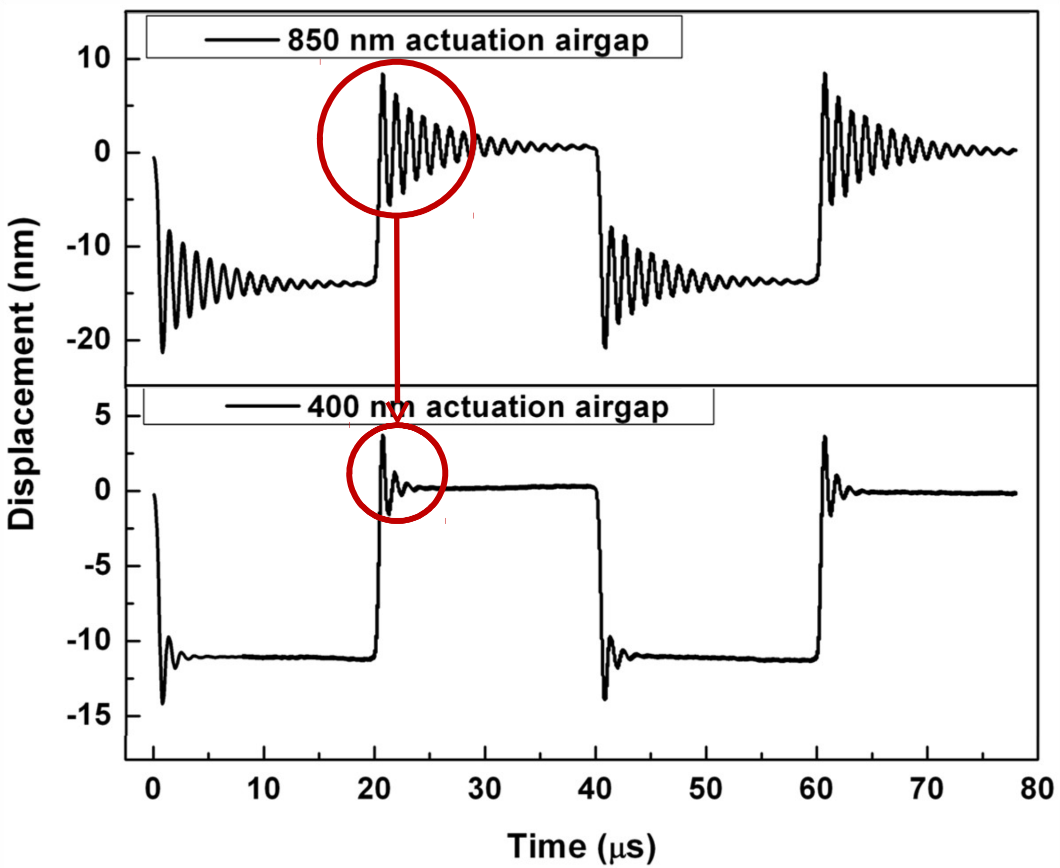


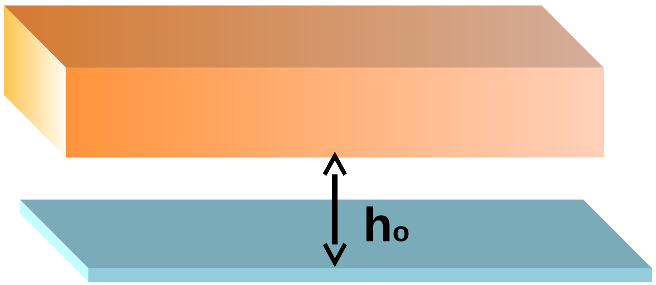


Viscous damping co-eff. C_d ~ μLw3/ h3

Damping variation with sacrificial layer height:

Viscous damping coefficient, $c_d \propto 1/h_o^3$

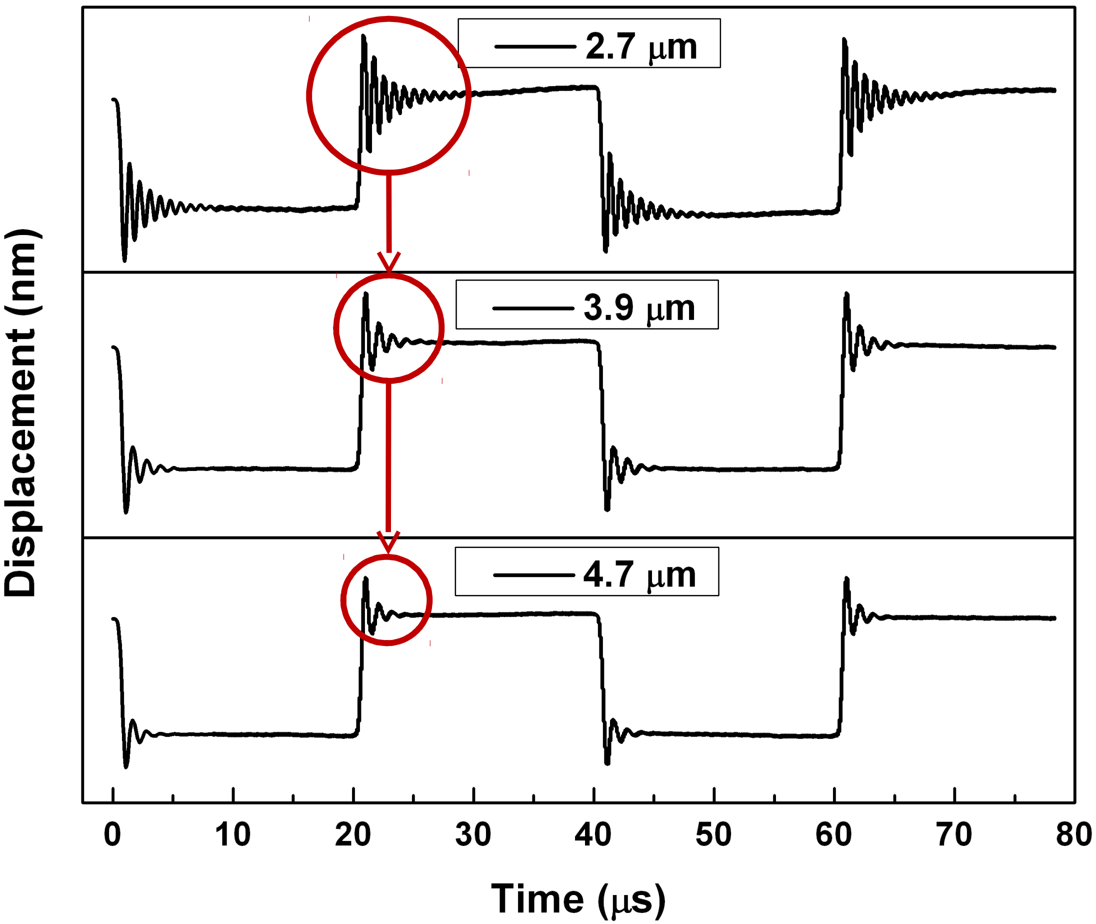




- Viscous damping is dominated by vertical compression of air.
- Driving voltage, $V \propto h_o^{3/2}$
- $h_o/3 > \lambda/4$ (In practice achieved deflection is lower than $h_o/3$.)

Damping variation with width of the microbeams:

Viscous damping coefficient , $c \propto w^3$

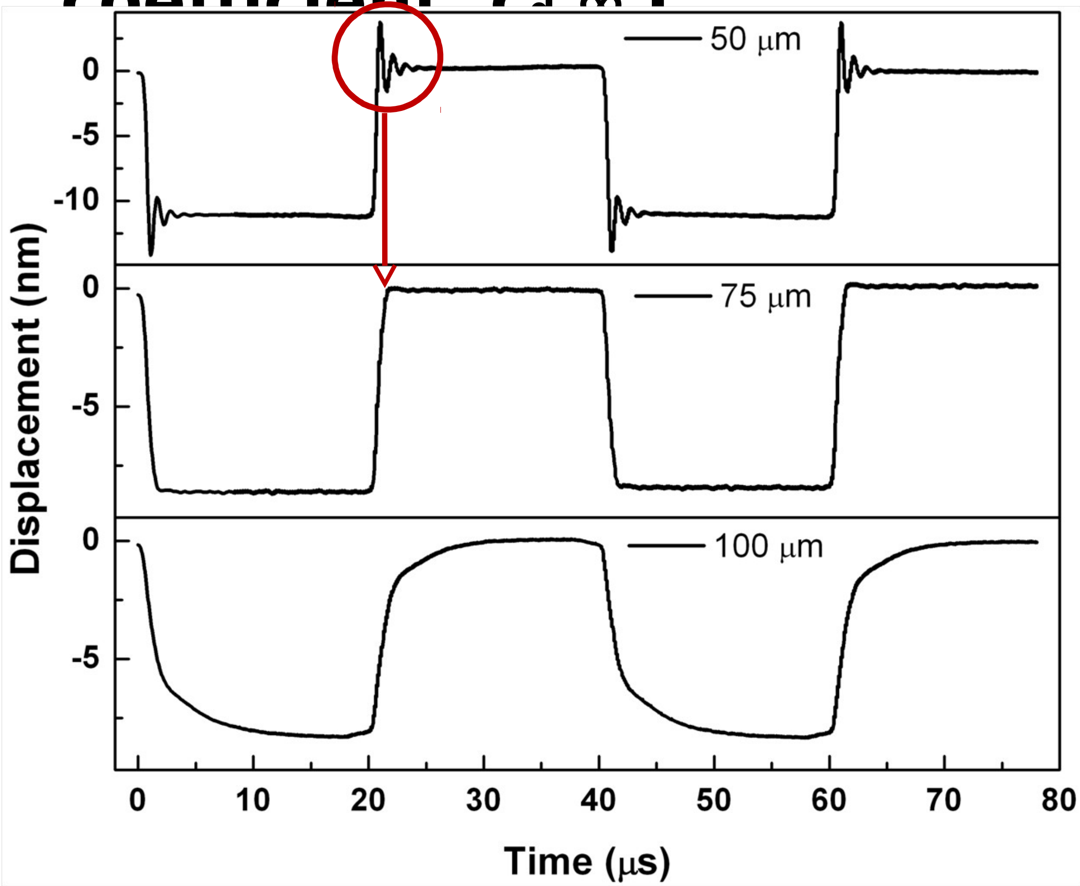


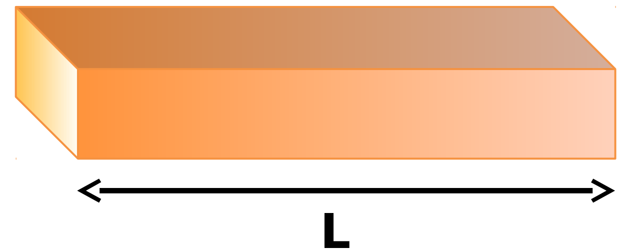
$d \sin\theta = n\lambda$

- d↑ , θ↓
- Inadequate spatial separation of 0th and ±1st order beams

Damping variation with length of microbeams:

Viscous damping coefficient, $c_d \propto L$

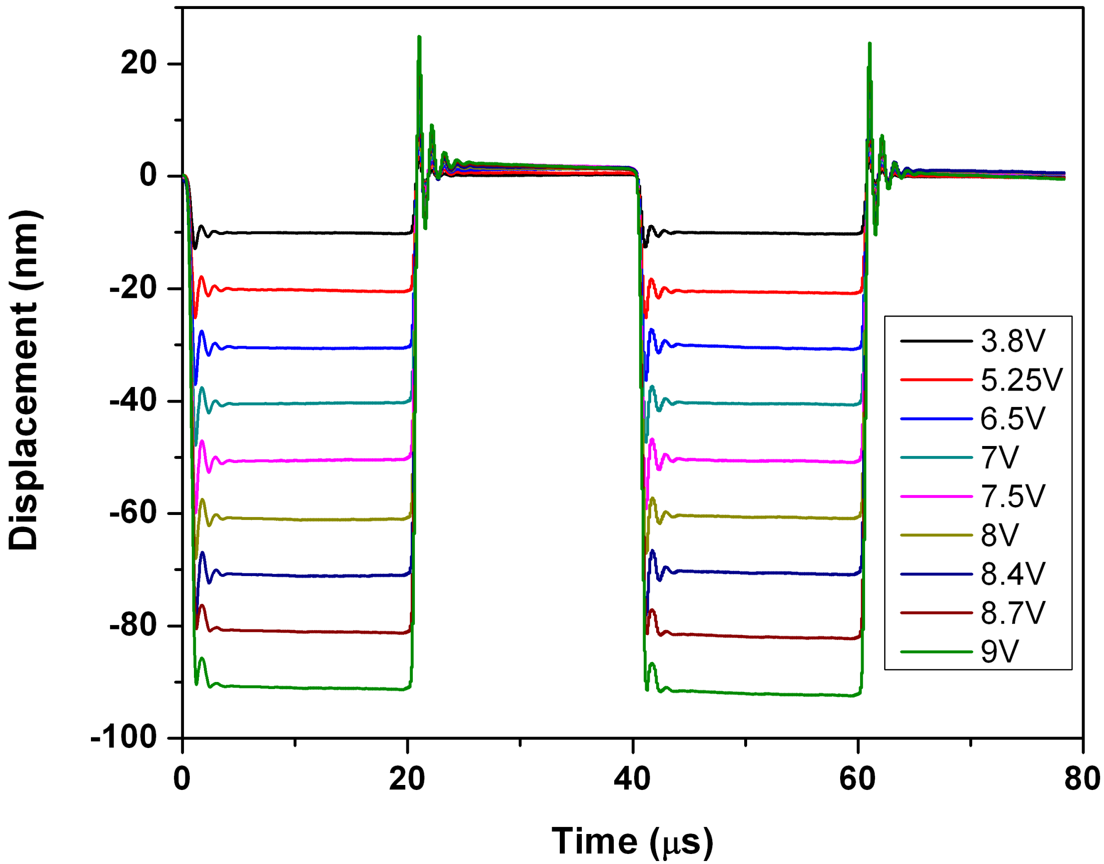




- Driving voltage, $V \propto 1/L^{1/2}$
- L , ωres (shorter GLV devices enable higher modulation rates)

Minimum settling time achieved : 2 μs (< 5 μs)

Analog gray scale:



- PWM not required.
- Analog nature of the GLV device allows it to be programmed to specified intensity level.

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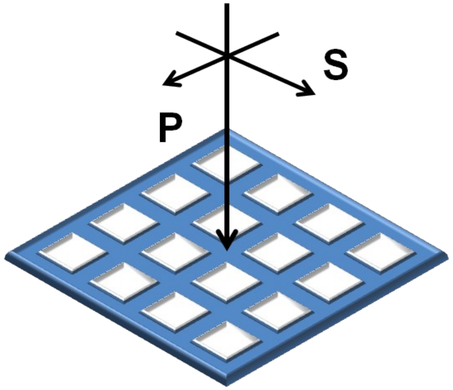
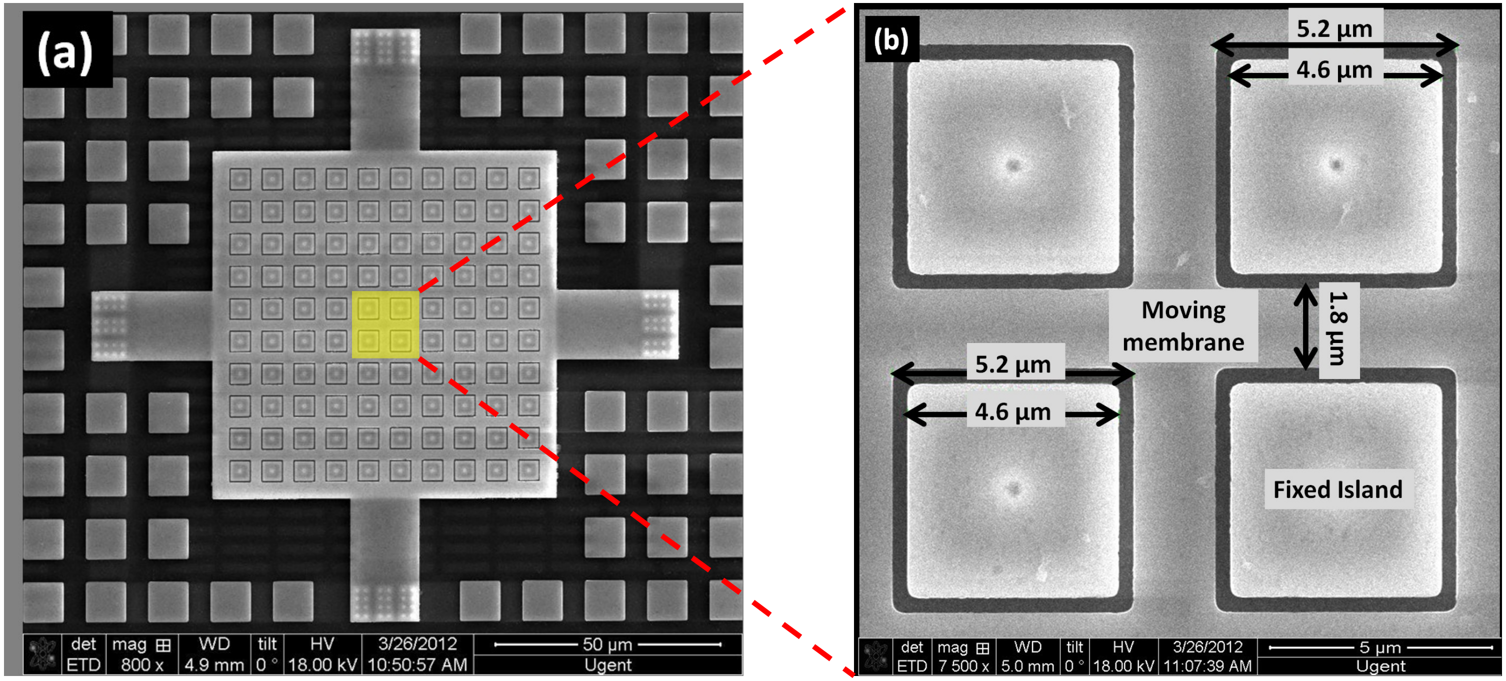
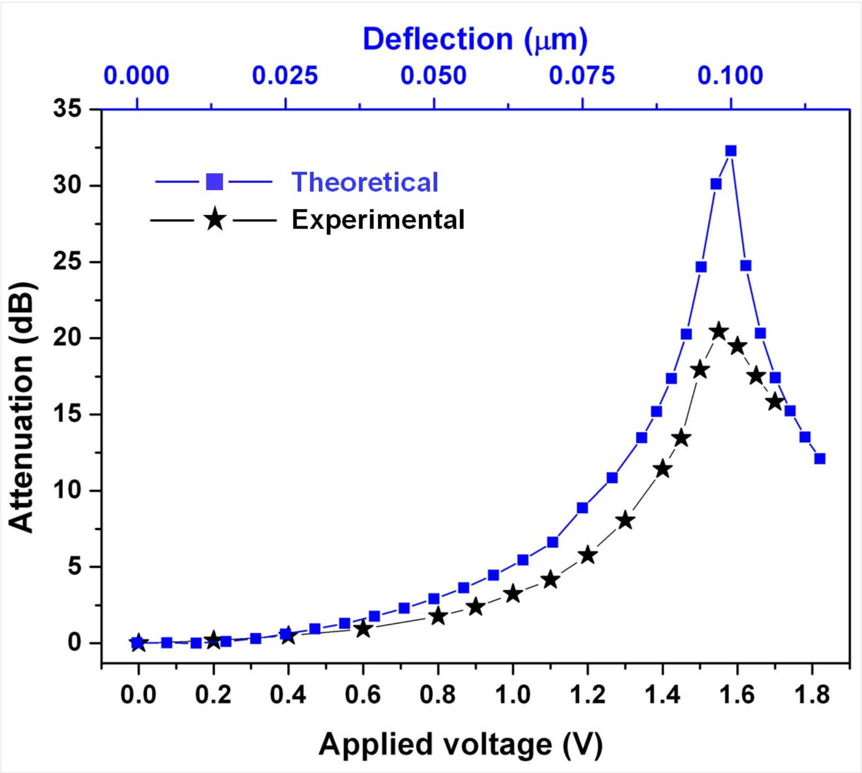
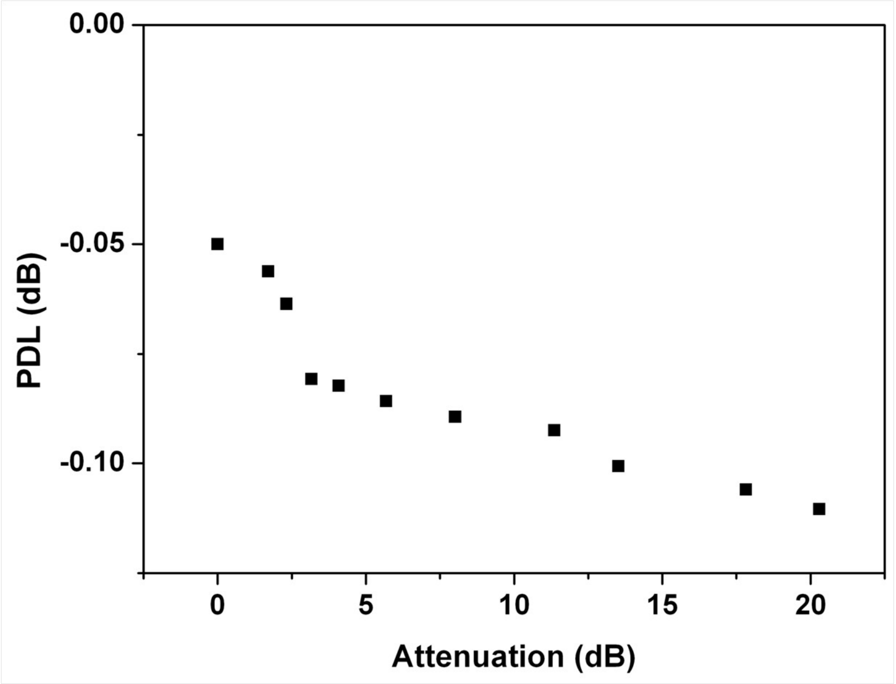
2D movable grating:





Polarization independent attenuation





Application as a variable optical attenuator.

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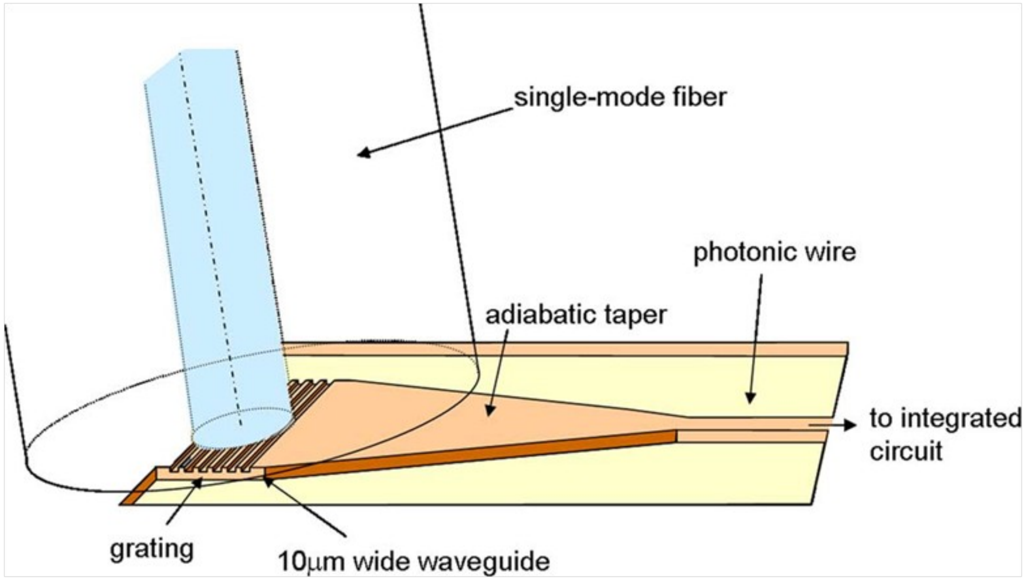
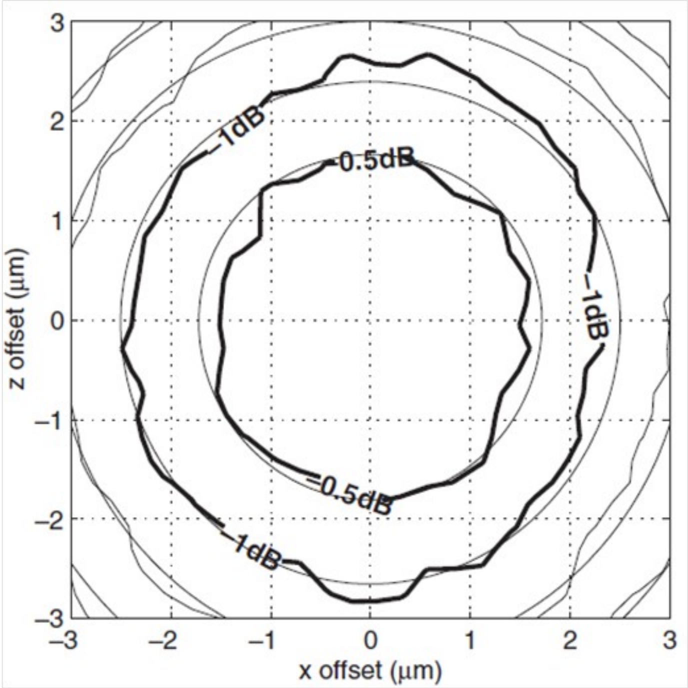
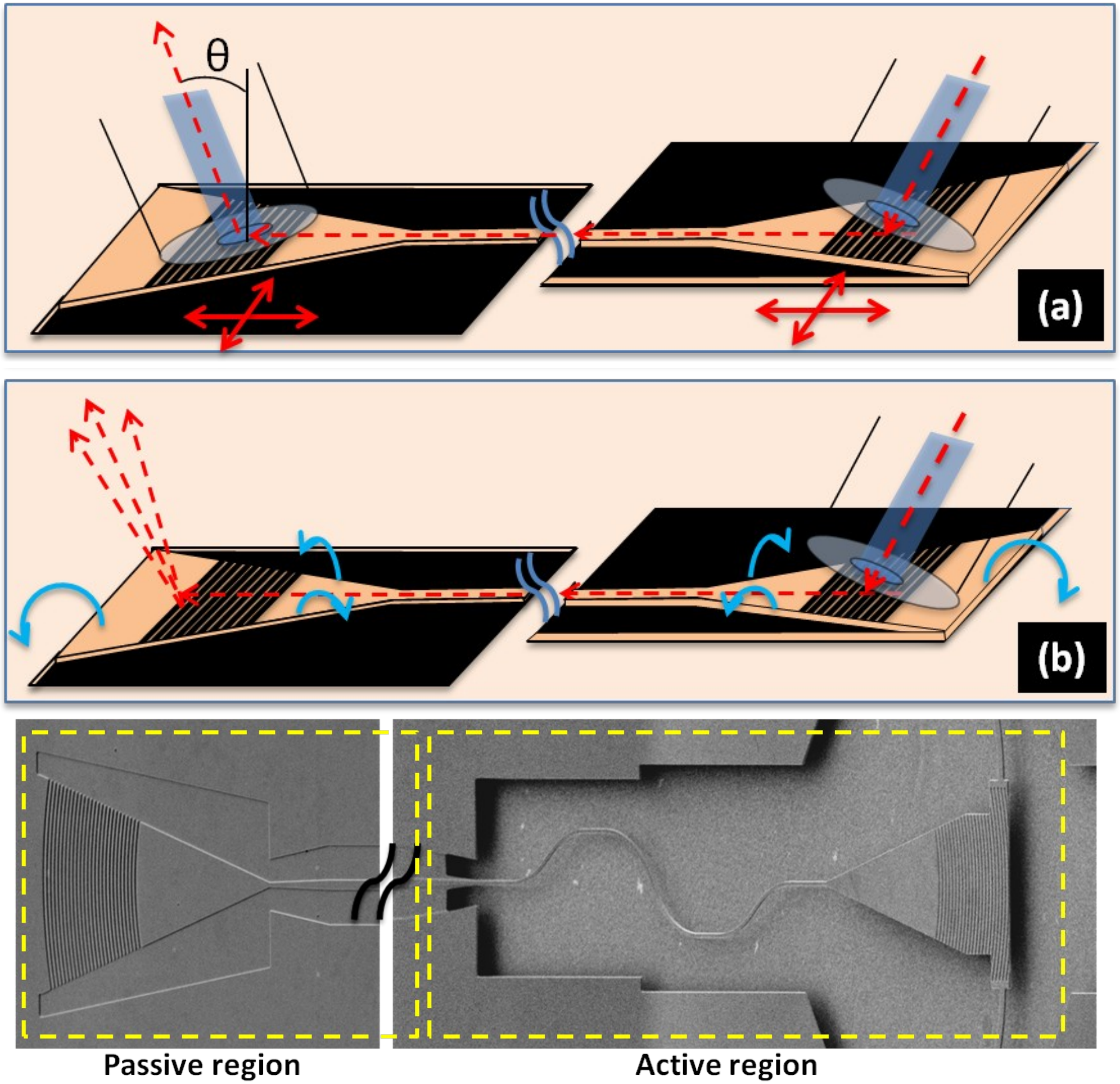
Grating couplers





Waveguide insertion loss tolerance through a grating coupler

Actively alignable grating coupler



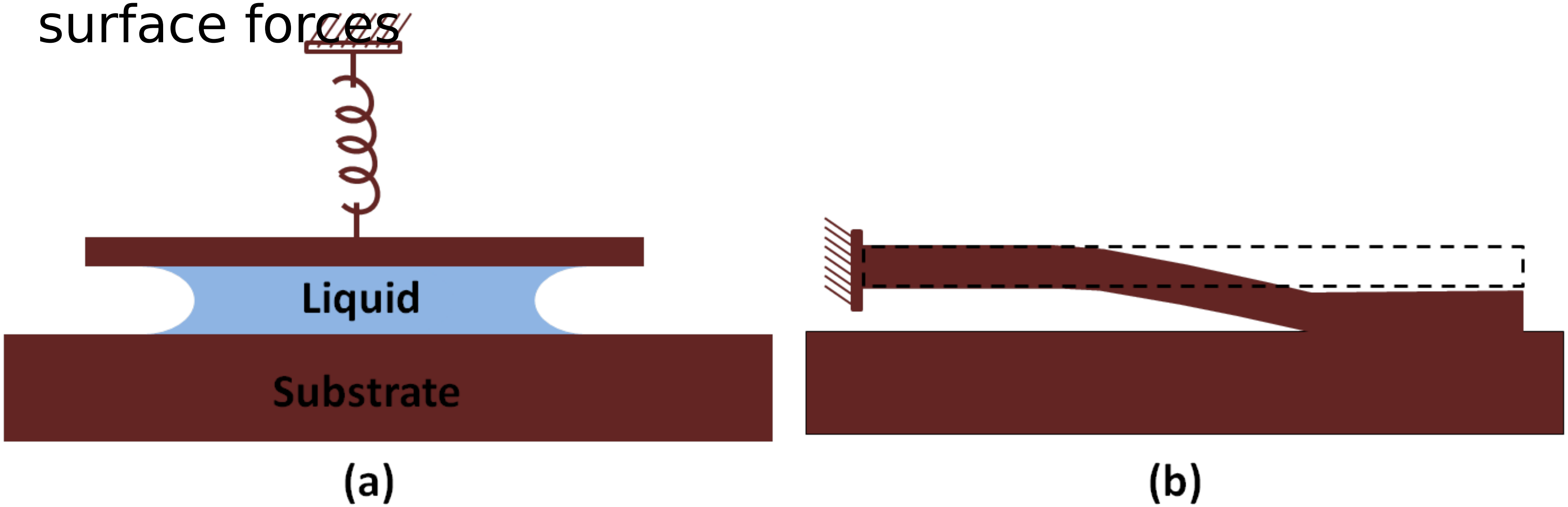
Possibility of mitigating a misalignment of ± 2 µm with accuracy ~ 100 nm

Possibility of steering the light 4-5° with an accuracy of 0.1 °

Sticking in MEMS during release with wet etchants

MEMS:

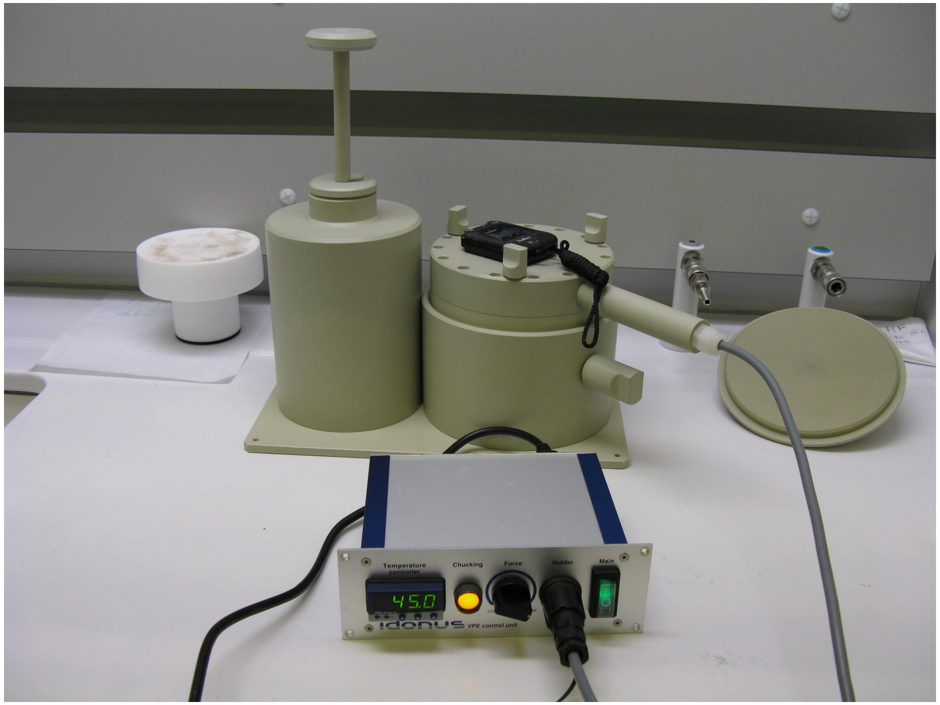
- Large areas with small stiffness
- Small device to substrate gap Highly susceptible to surface forces



Strong attractive capillary forces during dehydration Adhesion of the suspended member during rinsing and dry cycle.

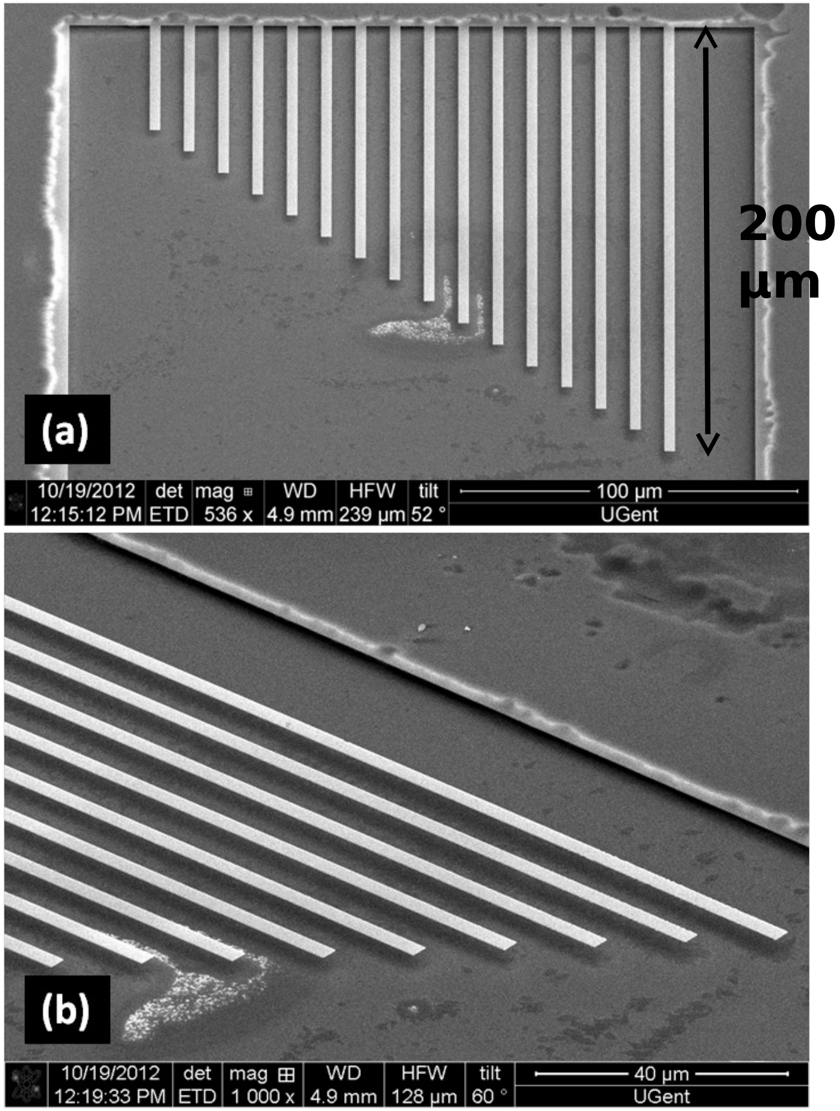
Need of a dry etching process

IDONUS vapor phase etcher (VPE)

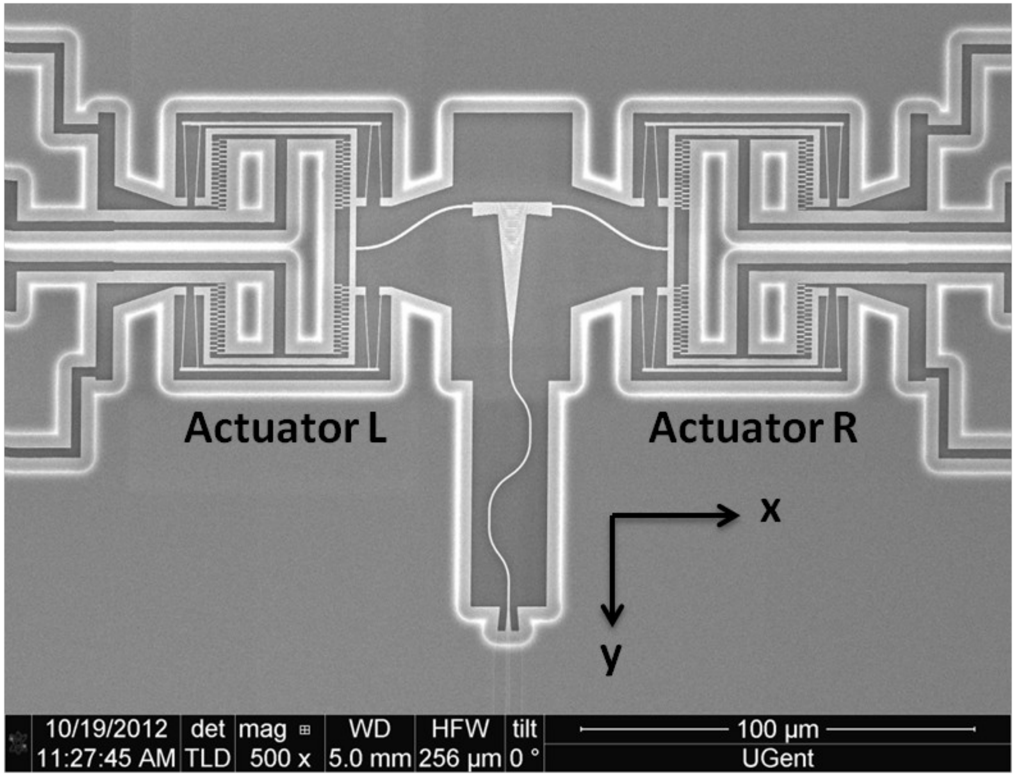


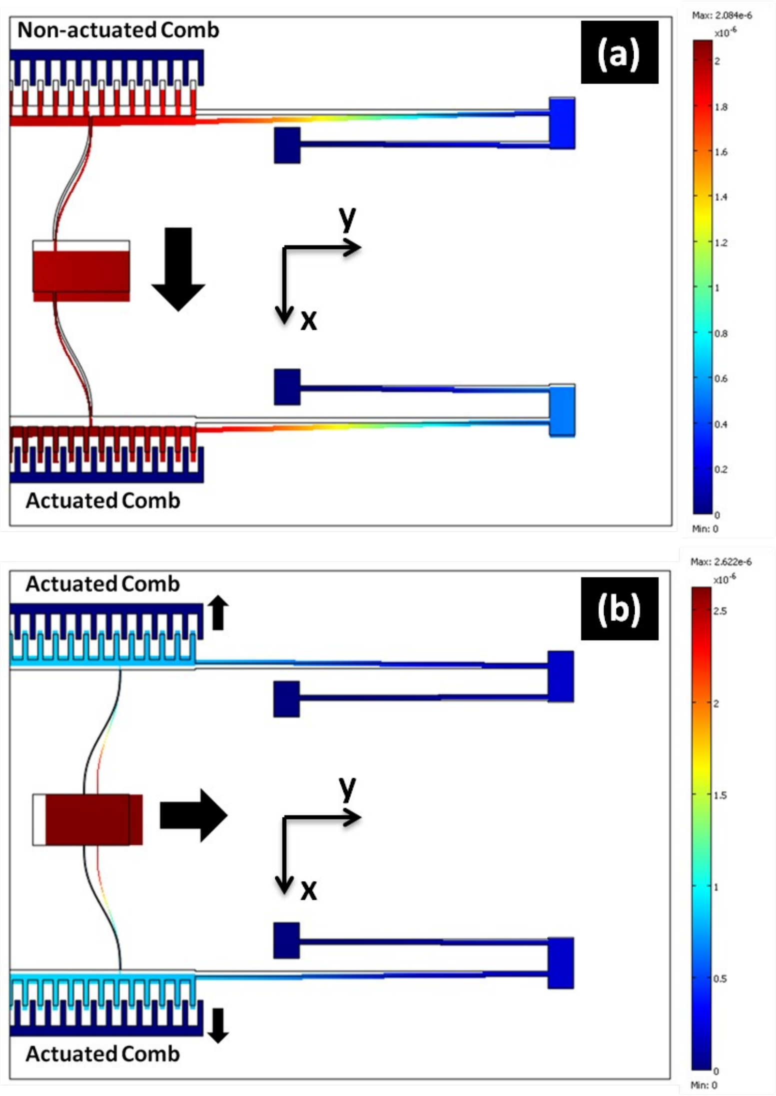
- Quasi dry method and never in contact with liquid.
- $SiO_2 + 2H_2O \rightarrow Si(OH)_4$
  $Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O$
- Water acts as an initiator and reactant of the etching process.
- Temperature control over the amount of reactant water.

Released SOI cantilevers



In-plane moving devices





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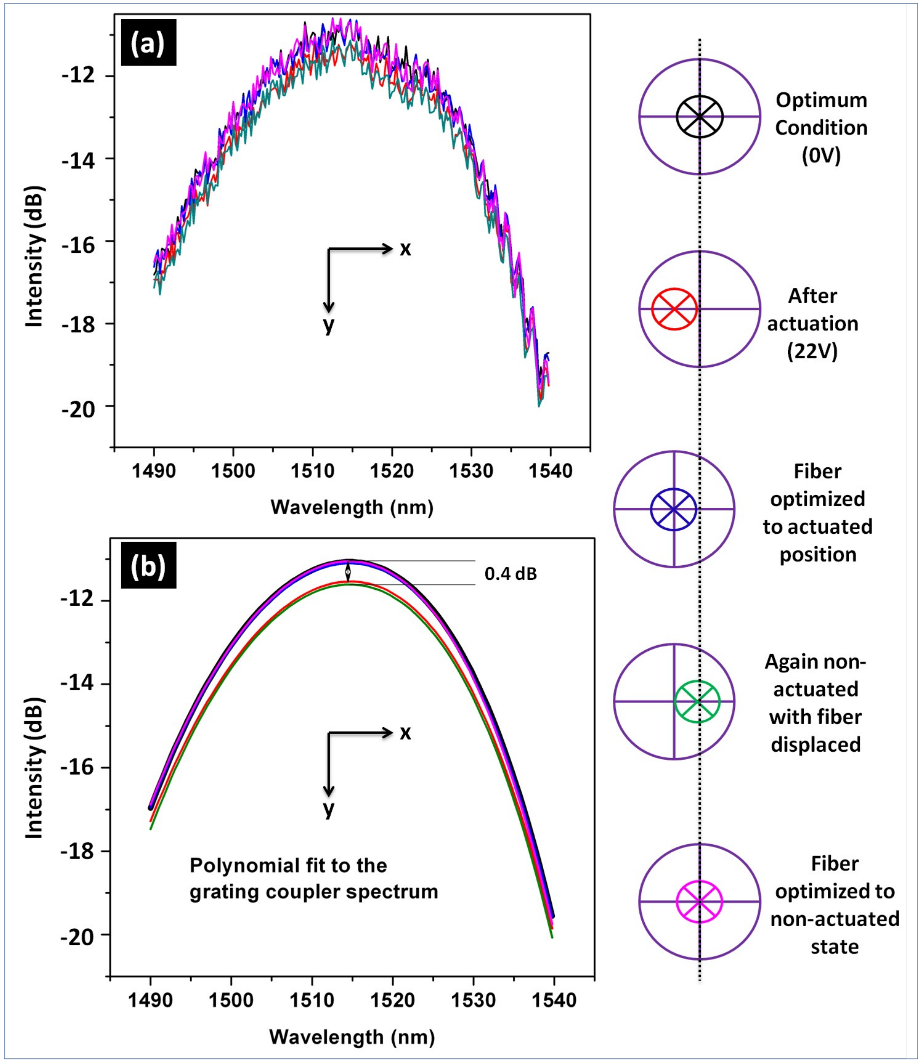
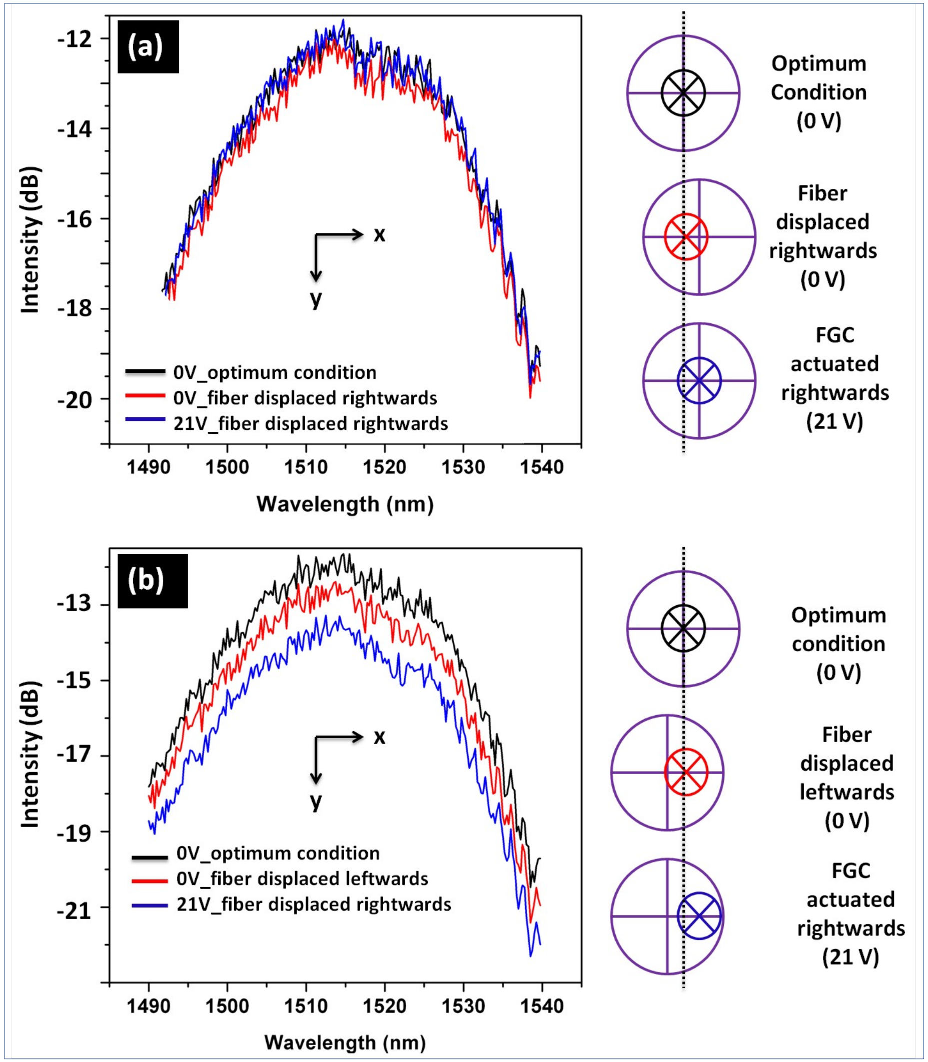
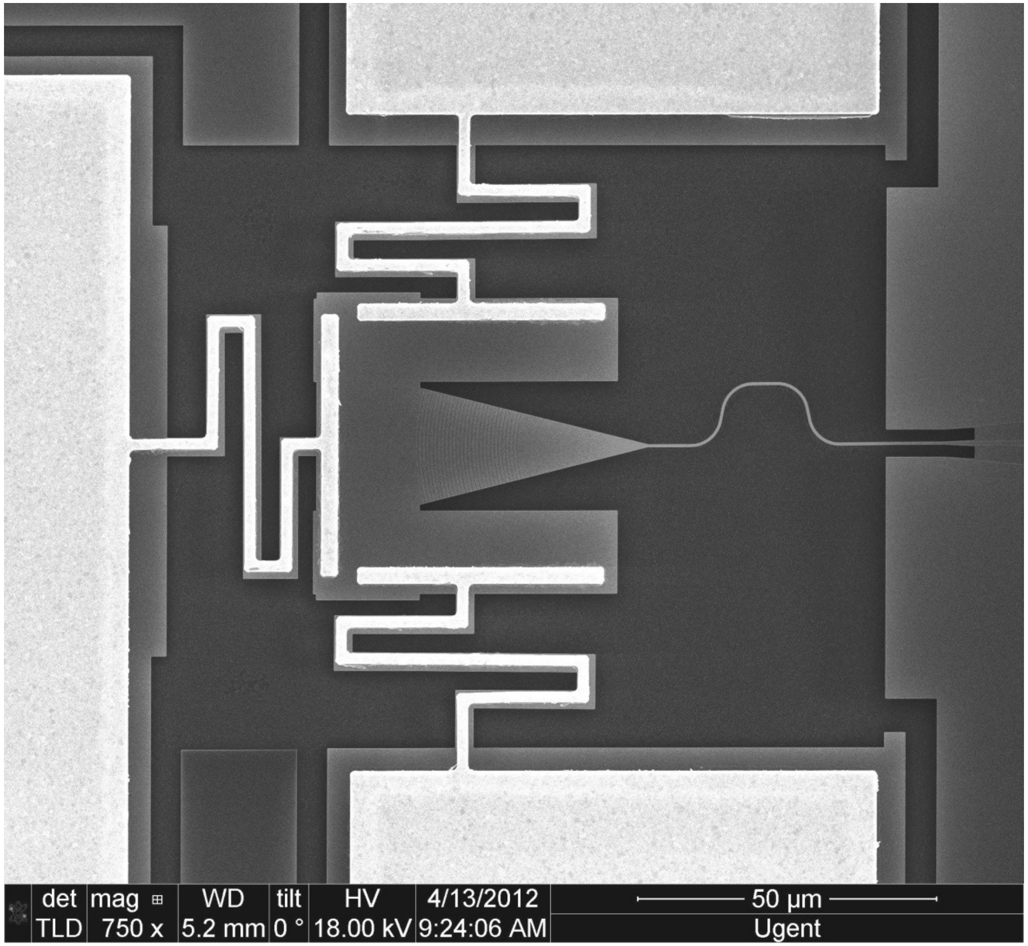
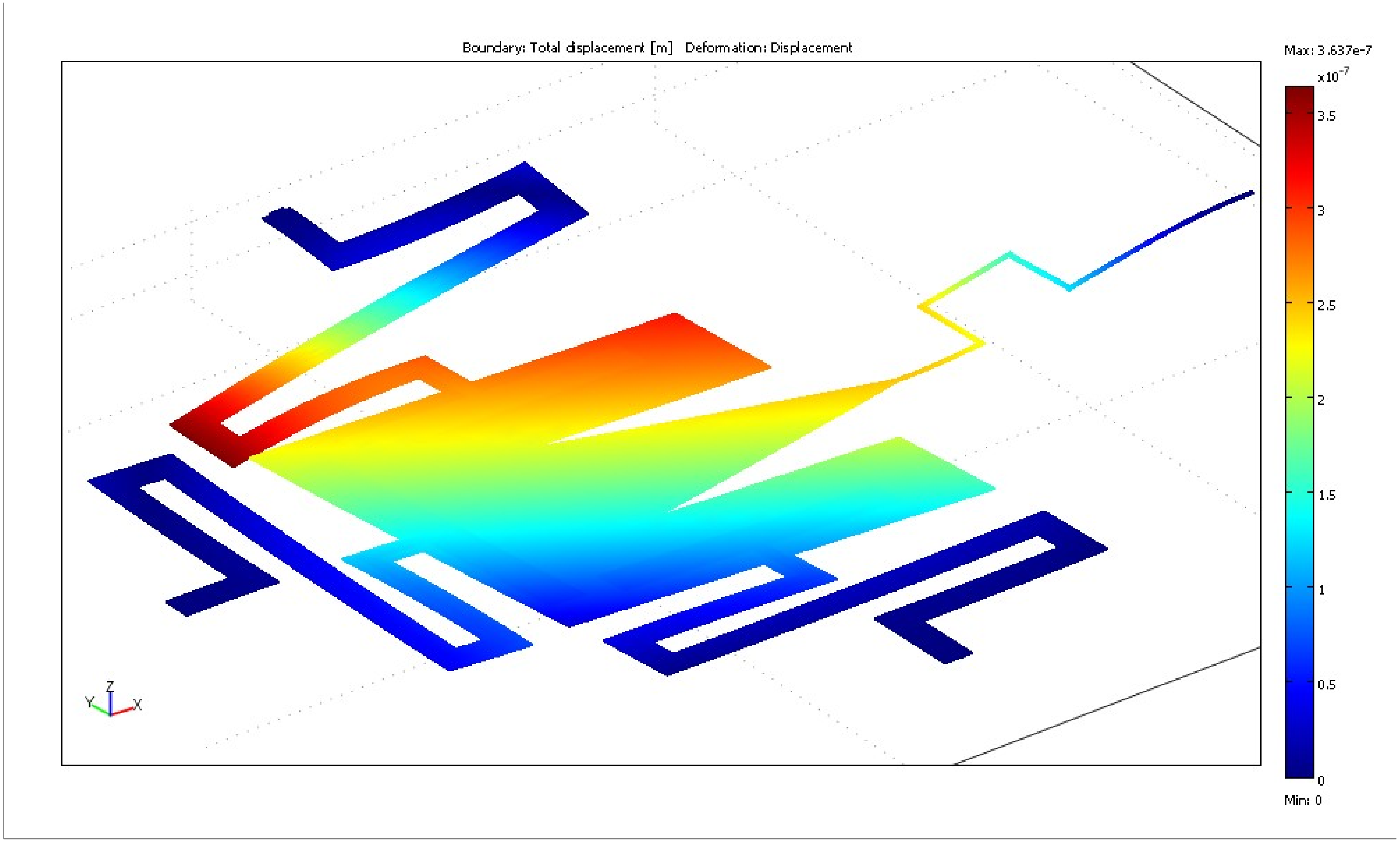




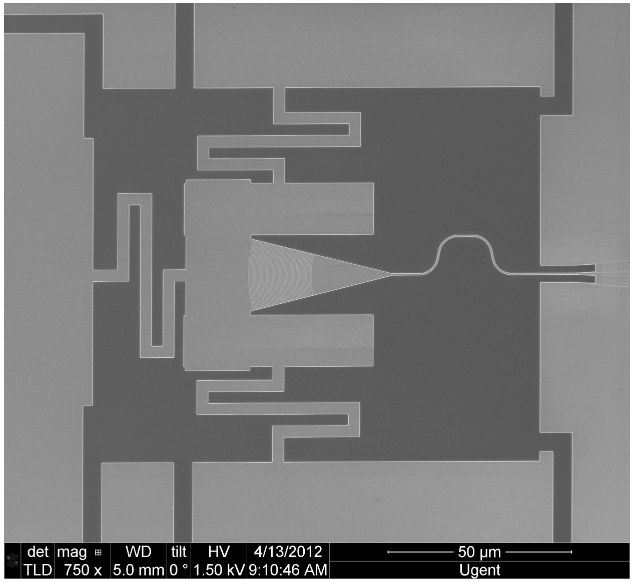
Beam steering using Si-photonic MEMS



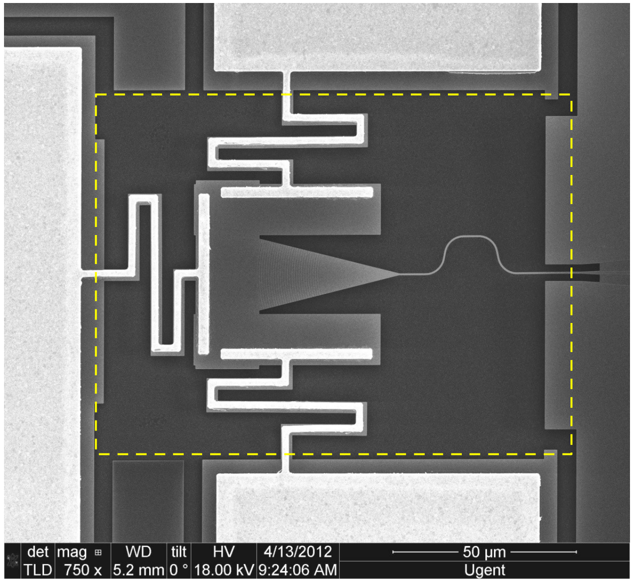
Beam steering using Si-photonic MEMS



Out-of-plane moving devices



Metallization and subsequent under-etching



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- Achieved a contrast of >1500:1 with a settling time of 2 µs for the GLV devices.

- 2D MEMS gratings were demonstrated with 20 dB attenuation with a PDL of 0.11 dB at maximum attenuation. Potential application as a variable optical attenuator (VOA).

- Proved the feasibility of using SiGe in forming high quality MOMES devices that can be integrated in large arrays.

- Demonstrated the possibility of using MEMS structures in Si-photonics platform in solving alignment problems.

Thanks for your attention