FACULTY OF ENGINEERING
AND ARCHITECTURE

Heterogeneous Integration of III-V Semiconductor Light Sources on Low-Refractive-Index Platforms

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Dankwoord

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List of Acronyms

a-Si:H	Hydrogenated amorphous silicon
ADF	Add-drop Filter
AM	Amplitude Modulation
AOM	Acousto-Optic Modulator
APF	All-pass Filter
ASE	Amplified Spontaneous Emission
BCB	Benzocyclobutene
BER	Bit Error Rate
CCW	Counterclockwise
CMP	Chemical-mechanical Polishing
CVD	Chemical Vapour Deposition
CW	Continuous Wave
CW	Clockwise
DBR	Distributed Bragg Grating
DC	Direct Current
DSH	Delayed self-heterodyne
DUT	Device Under Test
DUV	Deep-ultraviolet
DVS-BCB	Divinylsiloxane-bis-benzocyclobutene
EME	Eigenmode Expansion
EO	Electro-optic
ESA	Electrical Spectrum Analyzer
FBMS	Fixed Beam Moving Stage
FDTD	Finite-Difference Time-Domain
FP	Fabry-Pérot
FM	Frequency Modulation
FSR	Free Spectral Range
FWHM	Full Width at Half Maximum
GC	Grating Coupler
HF	Hydrofluoric acid
HSQ	Hydrogen Silsesquioxane
IPA	Isopropyl alcohol
IV	Current-voltage
LI	Light-current
LN	Lithium niobate

LNOI	Lithium niobate-on-insulator
LPCVD	Low-Pressure Chemical Vapour Deposition
MMI	Multimode Interference
MPW	Multi-Project Wafer (run)
MQW	Multiple Quantum Well
MRR	Microring resonator
MZI	Mach-Zehnder Interferometer
NA	Numerical Aperture
OSA	Optical Spectrum Analyzer
PDK	Process Design Kit
PDMS	Polydimethylsiloxane
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PMMA	Polymethylmethacrylate
PSD	Power Spectral Density
PSF	Point Spread Function
QW	Quantum Well
R&D	Research and Development
RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Anneal
SC-DBR	Sidewall-Corrugated Distributed Bragg Grating
SEM	Scanning Electron Microscope
SNR	Signal-to-Noise Ratio
SOA	Semiconductor Optical Amplifier
SOI	Silicon-on-insulator
TE	Transverse electric
TEOS	Tetraethyl orthosilicate
TFLN	Thin-film Lithium Niobate
TOX	Thermal Oxide
UV	Ultraviolet
WDM	Wavelength Division Multiplexing

Samenvatting

1 Inleiding

De sterke groei van geïntegreerde fotonica gedurende de laatste decennia heeft geleid tot het gebruik ervan in een brede waaier van toepassingsgebieden. Mature en performante geïntegreerde fotonische platformen op basis van silicium en indiumfosfide worden nu aangeboden door verschillende gieterijen over de hele wereld. Indiumfosfide heeft het voordeel dat alle actieve functies (lichtopwekking, modulatie en detectie) op één enkel platform worden gecombineerd. Silicium vereist een externe lichtbron, maar kan superieure passieve componenten, performante modulatoren en detectoren aanbieden in een goedkoper en meer schaalbaar platform. De prestaties van deze platforms worden tot het uiterste gedreven voor toepassingen zoals optische communicatie. Om de specificaties van toekomstige toepassingen te halen, moeten echter ook de mogelijkheden van andere materiaalplatforms worden benut. Siliciumnitride is een complementair platform naast silicium en InP dat zeer performante passieve componenten aanbiedt. De grote bandkloof en het brede transparantiebereik maken krachtige geïntegreerde schakelingen bij zichtbare golflengtes en hoge (piek)vermogens mogelijk met optische vermogens tot verscheidene Watts. Andere voordelen zijn ultralage propagatieverliezen en een temperatuursongevoelig gedrag. Afgezien van (energieverslindende) thermo-optische faseverschuivers ontbreekt echter actieve functionaliteit op dit platform. Recentelijk zijn ook dunne-film lithiumniobaatschakelingen met lage propagatieverliezen gedemonstreerd. Hoewel dit platform zeer performante zuivere fasemodulatoren kan aanbieden, blijft de totale bandbreedtedichtheid nog steeds beperkt en is het materiaal volledig uitgesloten uit CMOS-gieterijen, waardoor de commerciële toepassing ervan wordt belemmerd.

Elk van deze materiaalplatformen heeft zijn eigen voordelen en beperkingen. De ideale fotonische geïntegreerde schakeling zou verschillende materialen combineren om de voordelen van elk platform te kunnen benutten. Deze visie ontstond al in de jaren zeventig, maar de uitdagingen in verband met integratie werden al snel duidelijk. Daarom werden circuits op basis van één platform (de lichtbron buiten beschouwing gelaten) met een beperkt

aantal componenten de aanvankelijke norm vanwege hun beperkte fabricagecomplexiteit. Toen fotonische schakelingen op basis van silicium begonnen op te duiken voor toepassingen met grotere volumes, werd de integratie van lichtbronnen op basis van III-V-halfgeleiders door middel van zijkoppeling of flip-chipintegratie bevorderd, in plaats van de schakeling te verbinden met optische vezels. Naarmate de verwachte volumes in tele-/datacomtoepassingen toenamen, werden de ontwikkelingsinspanningen toegespitst op technologisch meer uitdagende integratiestrategieën zoals wafer-to-wafer bonding, die-to-wafer bonding en micro-transfer printing. De meer uitdagende integratiestrategieën werden gerechtvaardigd door de meer kosteneffectieve assemblage van elke module bij grotere volumes. Voor toekomstige toepassingen kunnen de integratiestrategieën voor het combineren van verschillende materialen niet alleen worden bepaald door de kosteneffectiviteit, maar ook door de prestaties en de vereiste functionaliteit. Zo heeft de verrijking van het siliciumnitride-platform met componenten op basis van III-V materialen geleid tot de demonstratie van single-mode lasers met fundamentele lijnbreedtes van minder dan 1 kHz. Het wegnemen van de technologische hinderpalen voor de heterogene integratie van III-V componenten op siliciumnitride en lithiumniobaat zal een grotere functionaliteit met hoge integratiedichtheden en grotere volumes mogelijk maken, waardoor geïntegreerde fotonica op haar beurt nieuwe toepassingsgebieden kan bedienen.

Dit proefschrift beschrijft onze inspanningen voor de heterogene integratie van optische versterkers op basis van III-V materialen op geïntegreerde circuits met siliciumnitride en lithiumniobaat. De gekozen integratietechniek is microtransfer-printen (µTP), die enkele van de voordelen van de wafer bonding en flip-chip integratiebenaderingen combineert. Microtransferprinten is een "pick-and-place"-methode om componenten van hun oorspronkelijke substraat over te brengen op een doelsubstraat. Het overdrachtsproces kan worden geparallelliseerd omdat de positie van de componenten op de bronwafer wordt bepaald door de lithografiemaskers. De integratiestap kan tegen het einde van de processtroom worden uitgevoerd, wat het mogelijk maakt extra functionaliteit toe te voegen aan een reeds ontwikkeld platform. Siliciumnitride en lithiumniobaat hebben lagere brekingsindices ($n \sim 2$ - 2,2) dan InP ($n \sim 3{,}2$), waardoor een directe adiabatische overgang naar de III-V versterker wordt verhinderd. Om deze reden wordt een tussenlaag met een hogere brekingsindex toegevoegd om het verschil te overbruggen. In het eerste deel van dit proefschrift worden III-V versterkers geïntegreerd op siliciumnitride circuits door middel van een tussenlaag van gehydrogeneerd amorf silicium. Er wordt een fabricagestroom ontwikkeld voor een platform dat breed afstelbare, single-mode lasers op siliciumnitride mogelijk maakt, uitgaande van een lege siliciumnitride wafer. Het platform bevat twee golfgeleiderlagen, thermo-optische faseverschuivers en III-V versterkers. Het tweede deel van dit proefschrift bouwt voort op

de verworven kennis en beschrijft de integratie van III-V versterkers op geprefabriceerde en met oxide beklede geïntegreerde schakelingen in lithiumniobaat. Deze fabricagestroom bestaat uit de definitie van een lokale uitsparing in de oxidebekleding en het transferprinten van een kristallijne siliciumlaag, gevolgd door de toevoeging van de III-V versterker. Op beide platforms demonstreren we alleenstaande versterkers en lasers, en hun prestaties en problemen worden besproken.

2 Resultaten

2.1 Meerlagig III-V/a-Si:H/Si_3N_4 platform

Het eerste platform dat werd ontwikkeld, begon met een blanco laag van 300 nm LPCVD Si_3N_4 bovenop 3.3 µm thermisch oxide. Wafers (10 cm diameter) met dit materiaal werden gekocht bij LioniX International. Het proces begint met het deponeren van een laag gehydrogeneerd amorf silicium, gevolgd door twee opeenvolgende stappen van e-beam patroneren en etsen. Op deze manier kunnen risicovolle planarisatiestappen worden vermeden. Na de definitie van deze tweelagige schakeling worden III-V versterkercoupons op de schakeling gemicrotransferprint. Het monster wordt geschaafd door een laag DVS-BCB polymeer te spincoaten, waarna verwarmingselementen worden gedeponeerd en de elektrische contacten worden geopend. Een schematische dwarsdoorsnede met de verschillende onderdelen van het platform is weergegeven in Fig. 1a. De overgang in twee stappen van de Si_3N_4 naar de III-V versterker is weergegeven in Fig. 1b. In het gebied rond de Si_3N_4 golfgeleider wordt de a-Si:H laag verwijderd.
Op dit platform werden verschillende apparaten gedemonstreerd: een zelfstandige versterker, een multimode ringlaser en een single-mode laser. Bouwstenen voor het maken van breed afstelbare single-mode lasers werden ontwikkeld, maar geen werkend apparaat werd bereikt in dit werk. De zelfstandige versterker bereikte klein-signaalversterking tot 13.7 dB bij 1570 nm en een 3-dB versterkingsbandbreedte van meer dan 28 nm. Niettemin, een hoog ruisgetal van 12.3 dB en een roodverschuiving van het versterkingsspectrum wijzen op hoge overgangsverliezen en verhitting in de versterker. De single-mode laser is gebaseerd op een breedbandige DBR reflector gecentreerd rond 1568 nm aan de ene kant, en een add-drop ringspiegel aan de andere kant. Het vrije spectrale bereik van de ring komt overeen met de bandbreedte van de DBR-reflector om ervoor te zorgen dat slechts één gereflecteerde frequentie in de DBR-reflectieband valt. Twee apparaten werden gekarakteriseerd met een verschillende koppelingssterkte aan de ring. De apparaten bereikten een uitgangsvermogen van 0.7 mW voordat de thermische afrol begon. Vermindering van de koppeling naar de ringspiegel verlaagde de geschatte spiegelreflectie met 2 dB en resulteerde in een smallere resonantie.

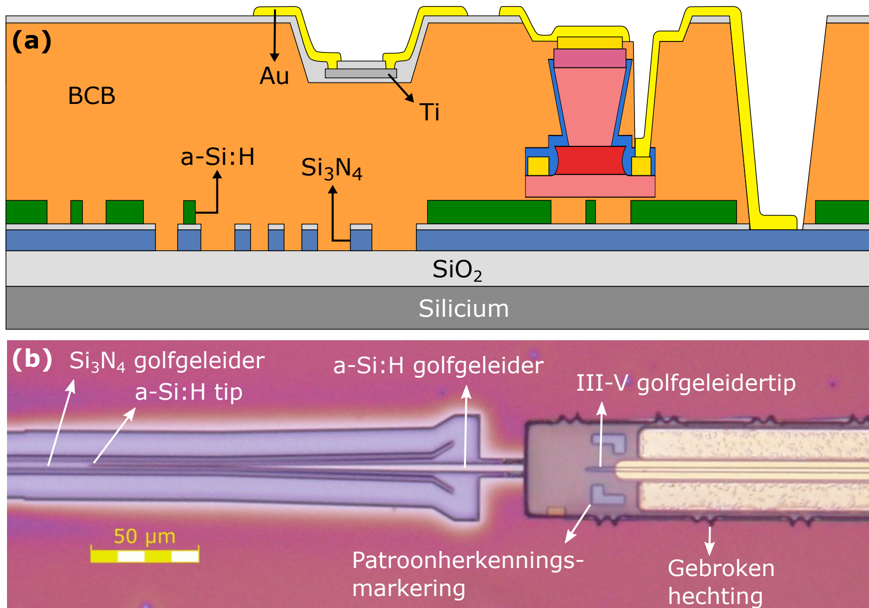

Figure 1: (a) Dwarsdoorsnede met de verschillende onderdelen van het ontwikkelde meerlagige III-V/a-Si:H/Si_3N_4 platform. (b) Microscoopfoto van een overgang van de Si_3N_4 golfgeleider naar de III-V-versterker via de a-Si:H laag.

2.2 Meerlagig III-V/c-Si/$LiNbO_3$ platform

Het tweede ontwikkelde platform ging uit van een reeds ontwikkelde processtroom van onze medewerkers aan de Stanford University. Hun platform bestond uit circuits in lithiumniobaat op een saffieren substraat, met een siliciumoxide topbekleding. De heterogene integratie van de III-V-versterkers gebeurt in dit geval volledig in de back-end. Een lokale uitsparing wordt geëtst in de (niet-geplanariseerde) oxide topbekleding, tot aan de laag lithiumniobaat. De etstijd wordt gecontroleerd om 70 nm van het siliciumoxide op de golfgeleider te laten, waarop een laag van 30 nm alumina wordt opgedampt. Coupons van kristallijn silicium worden gedefinieerd op een 400 nm silicium-op-isolatie sample, en getransferprint in de uitsparing op het doelsample. Golfgeleiders en tapers worden gevormd in het silicium coupon met behulp van elektronenstraallithografie en droog etsen. De opgedampte aluminiumoxidelaag dient als etsstoplaag. Na deze stap worden de III-V-versterkers op soortgelijke wijze als voorheen getransferprint en gecontacteerd. Een schematische dwarsdoorsnede met de verschillende onderdelen van het platform is te zien in Fig. 2.
Op dit platform werden zelfstandige versterkers, ringlasers en breed afstel-

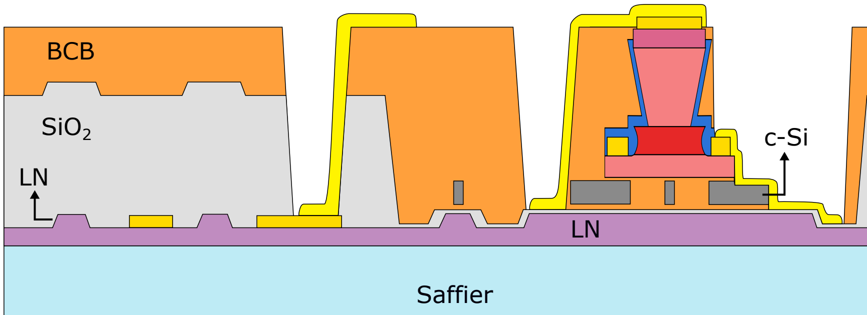

Figure 2: Dwarsdoorsnede met de verschillende onderdelen van het ontwikkelde meerlagige III-V/c-Si/$LiNbO_3$ platform.

bare single-mode laser gedemonstreerd. Het ontwerp van de single-mode laser is gebaseerd op het Vernier-effect, waarbij twee ringresonatoren worden gebruikt als spiegels en frequentiefilters. Het afstellen van de golflengte gebeurde middels het elektro-optisch effect van lithiumniobaat, waardoor voor het eerst een elektrisch gepompte, geïntegreerde afstelbare laser met deze mogelijkheid werd aangetoond. De zelfstandige versterkers toonden een piekversterking bij 1540 nm van 10.6 dB, en een versterkingsbandbreedte die 44 nm overschrijdt. De lagere versterkingspiekgolflengte wijst duidelijk op de betere thermische warmteafvoer in het lithiumniobate platform in vergelijking met het Si_3N_4 platform. Er is geen sluitende verklaring voor de lagere piekversterking in deze versterkers en verdere experimenten zijn nodig. De afstelbare laser bereikt een uitgangsvermogen van 1 mW in één van de vier uitgangen. Ruw elektro-optisch afstellen is aangetoond over een bereik van 21 nm, en fijn afstellen over een bereik van 180 pm. Het fijnafstellingsbereik wordt beperkt door de spanningstoevoer die het elektro-optische effect in de ringresonatorspiegels van de laser aanstuurt.

3 Besluit

In dit proefschrift zijn twee fabricagestromen ontwikkeld voor de integratie van III-V-halfgeleider optische versterkers op platformen die gebaseerd zijn op kernmaterialen met een lagere brekingsindex. In de loop van dit werk werden gelijkaardige ontwikkelingen gepubliceerd door andere onderzoeksgroepen. Hieruit blijkt de trend om over te schakelen op complexere materiaalstapelingen voor het bereiken van hogere prestaties en meer functionaliteit. De in dit werk gedemonstreerde apparaten zijn prototypes met veel ruimte voor verbetering. Niettemin is aangetoond dat de gebruikte methodes flexibel zijn en naar verwachting in de toekomst vele opwindende ontwikkelingen en samenwerkingsverbanden mogelijk zullen maken.

Summary

1 Introduction

The extensive growth of integrated photonics over the past decades has led to its use in a wide range of application domains. Mature and performant silicon and indium phosphide photonics platforms are now offered by several foundries across the world. Indium phosphide has the benefit of combining all active functionalities (light generation, modulation and detection) onto a single platform. Silicon requires an external light source, but can offer superior passive components, performant modulators and detectors in a cheaper and more scalable platform. The performance of these platforms is being pushed to the limits for applications such as optical communications. Nevertheless, in order to reach the specifications of future applications, there is a need to include the capabilities of other material platforms. Silicon nitride is a complementary platform to silicon and InP offering highly performant passive components. Its high bandgap and wide transparency range enable performant integrated circuits at visible wavelengths and high (peak) power operations with up to several Watts of optical power handling. Its further benefits include ultra-low propagation losses and temperature insensitive behaviour. However, apart from (power hungry) thermo-optic phase shifters, active capabilities are missing on this platform. Recently, also thin-film lithium niobate circuits with low propagation losses have been demonstrated. Although this platform can offer highly performant pure phase modulators, the total bandwidth *density* still remains limited and the material is entirely excluded from CMOS foundries, hampering commercial deployment.

Each of these material platforms have their own benefits and limitations. The ideal photonic integrated circuit would combine different materials to be able to exploit the benefits of each platform. This vision originated in the 1970's already, but the challenges related to integration soon became apparent. For this reason, single-platform circuits (not considering the light source) with a limited number of components became the initial standard because of their limited fabrication complexity. When silicon photonic integrated circuits started appearing for deployment in larger volume applications, the integration of III-V semiconductor based light sources through

edge coupling or flip-chip integration was pushed forward, rather than interfacing the circuit with optical fibers. As the expected volumes in tele-/datacom applications increased, development efforts were geared towards more technologically challenging *heterogeneous* integration strategies such as wafer-to-wafer bonding, die-to-wafer bonding, and micro-transfer printing. The more challenging integration strategies were warranted by the more cost-effective assembly of each module at larger volumes. For future applications, the integration strategies for combining different materials can be driven not only by cost-effectiveness, but also by performance and required functionality. For instance, empowering the silicon nitride platform with III-V based components has led to the demonstration of single-mode lasers with sub-kHz fundamental linewidths. Tackling the technological hurdles for heterogeneous integration of III-V components on silicon nitride and lithium niobate will allow for increased functionality with high integration densities and higher volumes, which in turn can enable integrated photonics to serve new application domains.

This dissertation describes our efforts towards the heterogeneous integration of III-V semiconductor optical amplifiers on silicon nitride and lithium niobate integrated circuits. The chosen integration technique is micro-transfer printing (µTP), which combines some of the benefits of the wafer bonding and flip-chip integration approaches. Micro-transfer printing is a pick-and-place method to transfer devices from their native substrate onto a target substrate. The transfer process can be parallelized since the position of the devices on the source wafer is defined by the lithography masks. The integration step can be done towards the end of the process flow, which allows to add extra functionality to an already developed platform. Si_3N_4 and lithium niobate have lower refractive indices (n $\sim$ 2 - 2.2) than InP (n $\sim$ 3.2), inhibiting a direct adiabatic transition to the III-V amplifier. For this reason, an intermediate layer with a higher refractive index is added to bridge the difference. In the first part of this thesis, III-V amplifiers are integrated on silicon nitride circuits through an intermediate layer of hydrogenated amorphous silicon. A fabrication flow is developed for a platform that enables widely tunable, single-mode lasers on silicon nitride, starting from a blank Si_3N_4 wafer. The platform contains two waveguide layers, thermo-optic phase shifters and III-V amplifiers. The second part of this thesis builds on the acquired knowledge and describes the integration of III-V amplifiers on prefabricated and oxide-clad lithium niobate integrated circuits. This fabrication flow consists of the definition of a local recess in the oxide cladding and the transfer printing of a crystalline silicon layer, followed by the addition of the III-V amplifier. On both platforms, we demonstrate standalone amplifiers and lasers, and their performance and problems are discussed.

2 Results

2.1 Multilayer III-V/a-Si:H/Si_3N_4 platform

The first platform that was developed started from a blank layer of 300 nm LPCVD Si_3N_4 on top of 3.3 µm thermal oxide. Wafers (10 cm diameter) with this material were purchased from LioniX International. The process starts with the deposition of a layer of hydrogenated amorphous silicon, followed by two consecutive steps of e-beam patterning and etching. This way, tedious planarization steps can be avoided. After the definition of this bilayer circuit, III-V amplifier coupons are micro-transfer printed onto the circuit. The sample is planarized by spincoating a layer of DVS-BCB polymer, after which heaters are deposited and the electrical contacts are opened. A schematic cross-section showing the different features of the platform is shown in Fig. 1a. The two-step transition from the Si_3N_4 to the III-V amplifier is shown in Fig. 1b. In the area around the Si_3N_4 waveguide, the a-Si:H layer is removed.

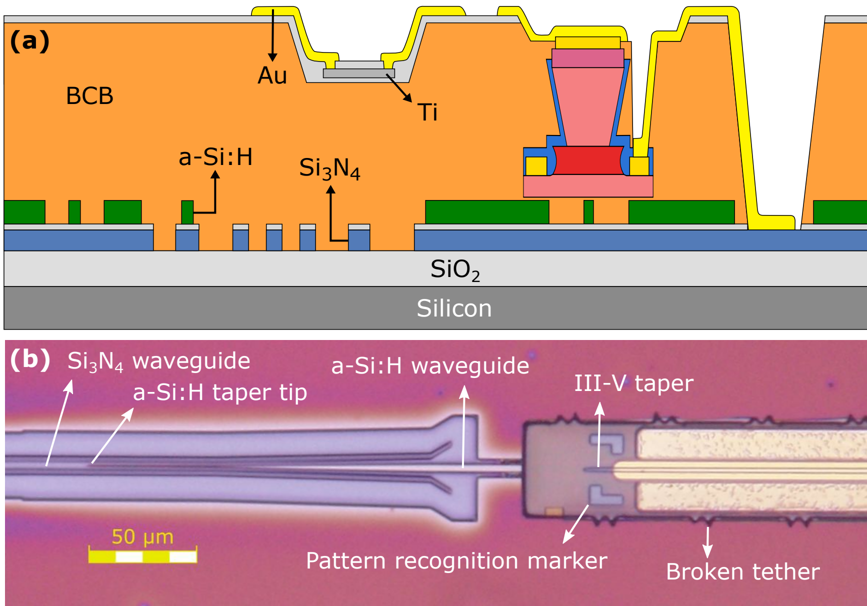

Figure 1: (a) Cross-section showing the different features of the developed multilayer III-V/a-Si:H/Si_3N_4 platform. (b) Microscope image of a transition from the Si_3N_4 waveguide to the III-V amplifier through the a-Si:H layer.

Several devices were demonstrated on this platform: a standalone amplifier, a multimode ring laser and a single-mode laser. Building blocks for making

widely tunable single-mode lasers were developed, but no working device was achieved in this work. The standalone amplifier reached small-signal gains up to 13.7 dB at 1570 nm and a 3-dB gain bandwidth over 28 nm. Nevertheless, a high noise figure of 12.3 dB and a redshift of the gain spectrum indicate high transition losses and self-heating in the amplifier. The single-mode laser is based on a broadband DBR reflector centered at 1568 nm on one side, and an add-drop ring mirror on the other side. The free spectral range of the ring matches the bandwidth of the DBR reflector to ensure that only one reflected frequency falls in the DBRs reflection band. Two devices were characterized with a different coupling strength at the ring. The devices reached output powers of 0.7 mW before the onset of thermal roll-off. Decreasing the coupling to the ring mirror decreased the estimated mirror reflectivity by 2 dB and resulted in a narrower resonance.

2.2 Multilayer III-V/c-Si/$LiNbO_3$ platform

The second developed platform started from an already developed process flow from our collaborators at Stanford University. Their platform consisted of lithium niobate circuits on a sapphire substrate, with a silicon oxide top cladding. The heterogeneous integration of the III-V amplifiers is done entirely in the back-end in this case. A local recess is etched in the (non-planarized) oxide top cladding, down to the lithium niobate layer. The etching time is controlled to leave 70 nm of silicon oxide on the waveguide, on top of which, a layer of 30 nm alumina is evaporated. Coupons of crystalline silicon are defined on a 400 nm silicon-on-insulator sample, and transfer printed in the recess on the target sample. Waveguides and tapers are patterned in the silicon coupon using electron-beam lithography and dry etching. The deposited alumina layer acts as an etch stop layer. After this step, the III-V amplifiers are transfer printed and contacted in a similar way as before. A schematic cross-section showing the different features of the platform is shown in Fig. 2.
On this platform, standalone amplifiers, ring lasers and widely tunable single-mode laser were demonstrated. The design of the single-mode laser is based on the Vernier effect, using two ring resonators as mirrors and frequency filters. The wavelength tuning was done through lithium niobate's electro-optic effect, showing for the first time an electrically pumped, integrated tunable laser with this capability. The standalone amplifiers showed a peak gain at 1540 nm of 10.6 dB, and a gain bandwidth exceeding 44 nm. The lower gain peak wavelength clearly indicates the better thermal heat sinking in the lithium niobate platform compared to the Si_3N_4 platform. There is no conclusive explanation for the lower peak gain in these amplifiers and further experiments are required. The tunable laser reaches an output power of 1 mW in one of its four outputs. Coarse electro-optic tuning is demonstrated over a range of 21 nm, and fine-tuning over a range of 180 pm. The fine-tuning range is limited by the voltage supply that drives

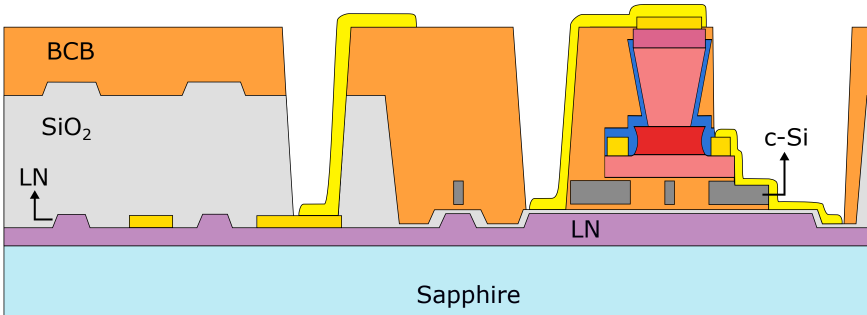

Figure 2: Cross-section showing the different features of the developed multilayer III-V/c-Si/$LiNbO_3$ platform.

the electro-optic effect in the laser's ring resonator mirrors.

3 Conclusion

In this dissertation, two fabrication flows have been developed for the integration of III-V semiconductor optical amplifiers on platforms based on lower refractive index core materials. During the course of this work, similar developments were published by other research groups. This showcases the trend of moving to more complex material stacks for reaching higher performance and more functionality. The devices demonstrated in this work are prototypes with much room for improvement. Nevertheless, the used methods are shown to be flexible and can be expected to enable many exciting developments and collaborations in the future.

1
Introduction

It's not that crazy, it will only take five minutes.
B. Kuyken

The branch of physics studying the properties, behaviour and applications of light has two names: *optics* and *photonics*. The term "optics" sounds probably more familiar to a broader audience and will evoke thoughts of lenses, prisms, refraction etcetera. This branch of science has existed for several hundreds of years and has brought the world (among other things) reading glasses, microscopy and advances in astronomy. On the other hand, the term "photonics" is newer. It is widely accredited to the French physicist Pierre Aigrain who defined it as follows in 1967:

> *"Photonics is the science of the harnessing of light. Photonics encompasses the generation of light, the detection of light, the management of light through guidance, manipulation, and amplification, and most importantly, its utilisation for the benefit of mankind."*

This definition embraces the insights gained since the second half of the 19th century with the development of Maxwell's theory of electromagnetic waves, and the understanding of the quantum-mechanical aspects of light and its interaction with matter. The very name "photonics" indeed refers to a light quantum: the photon. It is no coincidence that this new term was introduced shortly after optical lasers, the first man-made source of (nearly)

perfectly coherent light, were discovered.[1] Lasers proved themselves useful in an immense amount of applications since their discovery and led to the birth of a whole new scientific discipline, which nowadays drives innovation in a wide range of sectors and applications.

1.1 The discovery of the laser

The development of groundbreaking new technologies is often triggered by a military or economic problem. This is very clearly the case for some of the 20$^{\text{th}}$ century's most influential inventions such as nuclear power, computers, or the transistor. The development of the first two was spurred during World War II to gain a military advantage and they only got civil applications after the war. Transistors, on the other hand, were developed to replace large vacuum tubes in electronic circuits, as smaller components often lead to a cheaper product. Even one of the first successes of quantum mechanics, the discovery of the theory of black-body radiation, was incentivized by an economic problem, namely: should the city of Berlin be illuminated by gas or electricity [2]? Solving this problem required the introduction of quantized energy (Planck, 1900) and led to the proposition of the concept of a photon by Einstein in 1905. The introduction of the photon and later on the theoretical prediction of stimulated emission were the first building blocks required for the discovery of the laser.

It is more suitable to speak of the *discovery*, rather than the *invention* of the laser, because in contrast to the previous examples, lasers weren't really supposed to solve a specific problem. Nobody was waiting for them. In spite of (or maybe because of) this, they became a source of wild and unrealistic expectations after the first proposal of the concept in 1958 [3]. Of course, the idea behind a powerful, intense ray of light (a "death ray") had already been introduced by science-fiction writers as early as in 1898, in the book "The war of the worlds" by H.P. Wells. Among others, also an ageing Nikola Tesla had claimed that he had constructed a "teleforce" weapon, capable of shooting planes out of the air from hundreds of kilometers away. Tesla being a renowned inventor at the time, not everyone was quick to dismiss his claims as nonsense. Perhaps as a result of this fantasy, the death ray was referenced in popular news and even by more serious scientific commentators [4–6] after the publication of the first demonstrated laser by Maiman in 1960 [7]. In the movie Goldfinger, which came out in 1964, James Bond is threatened by an "industrial laser cutter" emitting a beam of red

[1] Interestingly, specifying "man-made" is not entirely unnecessary, as naturally occurring lasing has been observed in the atmosphere on Mars and Venus [1].

light powerful enough to cut through metal (and presumably also James Bond). The design of this device was clearly inspired by Maiman's laser. Of course, the scientists in those days also envisioned other potential application areas of lasers, such as communications, healthcare (cutting through tissue, burning tumors), or high-resolution spectroscopy. The large variety of potential applications and the excitement of unveiling new physics is reflected in the widespread interest and many sources of funding for research into the new technology [8]. Indeed, Maiman's device was just the first of five different types of lasers to be demonstrated within only one year [9–12]. Nevertheless, in practice, the first lasers were not capable of satisfying everyone's expectations, and, as they were not developed for a specific purpose, people began to wonder what to do with them. A running joke in the research community was that lasers were "a solution looking for a problem". A striking example of this mindset is perhaps a patent filed by Schawlow - one of the pioneers in the field - describing a laser tool, mounted on a typewriter, to evaporate the ink in case of a spelling error [13]. The grand application of lasers: to make glorified typewriters.

The question what to do with lasers did not stay unsolved for a long time. Within the year, lasers were commercialized by several companies and the technology rapidly improved. Already in 1961, a pulsed ruby laser was used to treat a retinal tumor [14]. The laser replaced a high-intensity Xenon lamp that had been used previously for this kind of procedure. Owing to the high intensity (and small spot size) of the singular laser pulses, the total required energy *and* the duration of the treatment were reduced. These aspects improved the patient's comfort, and in this specific case also allowed to avoid anesthesia.

If initially lasers were replacing incoherent light sources in existing applications, they soon unlocked brand new possibilities. In 1962, the reflection of laser light off the surface of the moon was detected in the first ranging experiment of its kind [15]. Towards the end of the decade, mirrors were installed on the moon during the Apollo and Lunokhod missions to improve the measurement's accuracy. Nowadays, the distance of the moon can be measured with millimeter precision [16]. In 1964, the first CO_2 laser was demonstrated [17]. It was the most powerful continuous-wave laser of its time, and it is still used nowadays for cutting through materials such as biological tissue (in surgery) and sheets of metal (materials processing). The first widely wavelength-tunable dye lasers were demonstrated in 1967 [18]. This type of laser significantly advanced the field of spectroscopy. Finally, two more clusters of critical inventions deserve to be highlighted in this

non-exhaustive list. First: the advent of the **semiconductor** laser diode. Semiconductor optical amplifiers had been suggested already in 1953 by von Neumann [19], years before the first patent by Nishizawa in 1957 [20] and the U.S. patents by Schawlow and others. A major advantage of semiconductors is that they can be pumped with electrical current, instead of a pumping light source such as the flash tube in Maiman's demonstration. Electrically pumped semiconductor laser diodes were first demonstrated in 1962. A few years later, the use of semiconductor heterostructures, capable of confining both the generating carriers and the generated light, was proposed. This invention was awarded with a Nobel prize in the year 2000. The second critical invention was a breakthrough in **fiber optics** technology in 1966, that allowed to reduce the losses over a thousandfold and drastically increase the reach of optical signals in glass fibers to up to 100 km. Also this breakthrough was awarded with a Nobel prize, in 2009. These inventions laid the foundations for optical communications, without which the internet as we know it today would not exist.

1.2 The advent of optical communication

The invention of the semiconductor transistor, which led to the development of the integrated circuit (IC), revolutionized the electronics industry. Integrated circuits miniaturized electronic circuits, which previously consisted of bulky components such as vacuum tubes. However, the main driver of their success is perhaps the fact that integrated circuits could be manufactured in high volumes in assembly lines using photolithography and etching techniques, greatly reducing their cost. As a result of this development, the semiconductor industry boomed and matured. Over the years, higher-purity crystals (silicon, germanium, ...) were grown with increasing wafer diameters, and photolithography and etching techniques were consistently improved. Semiconductor light sources, not only lasers but also LEDs, were able to piggyback off this development in semiconductor growth and processing. These continuous improvements led to the increasing miniaturization of integrated circuits and helped enabling the famous "Moore's law" [21], stating that the number of transistors in integrated circuits doubles every two years.

As computational power increased over the years, also the need for higher capacity communication links grew. Communication using optical signals promised a few fundamental improvements over microwave signals. Inherently, optical signals in the near-infrared (f $\sim 10^{14}$ Hz) have the capacity for much higher bandwidths than microwave signals (f $\sim 10^7 - 10^9$ Hz).

Furthermore, advances in silica optical fiber made guided propagation of optical signals possible with significantly lower losses than copper wires, without suffering from electromagnetic interference. Optical fiber communication technology first appeared in specialised settings, using light emitting diodes switching on and off at MHz speeds [22]. Later on, these LEDs were replaced by AlGaAs/GaAs lasers emitting light in the 800 - 900 nm region. Eventually, development shifted towards lasers operating at longer wavelengths, to benefit from the low chromatic dispersion (at 1300 nm) and low propagation loss (at 1550 nm) of optical fibers. Long-haul optical fiber communications at these wavelengths became commercial in 1984 [23], however, microwave satellite links remained a strong competitor for long-haul, high-volume communications up until 1990 [22]. The battle for market space reached a turning point in 1987 in favour of optical fiber, when the erbium-doped fiber amplifier (EDFA) was invented [24], which allowed for the amplification of optical signals around 1550 nm. This made fiber optics a viable technology for high-capacity trans-oceanic communication channels. Nowadays, submarine optical fibers connect the entire globe, as shown in Figure 1.1. With the fiber infrastructure in place, further improvements were to come from the transmitter and receiver units at both ends of the fiber. The development of these components spurred the field of *integrated photonics*.

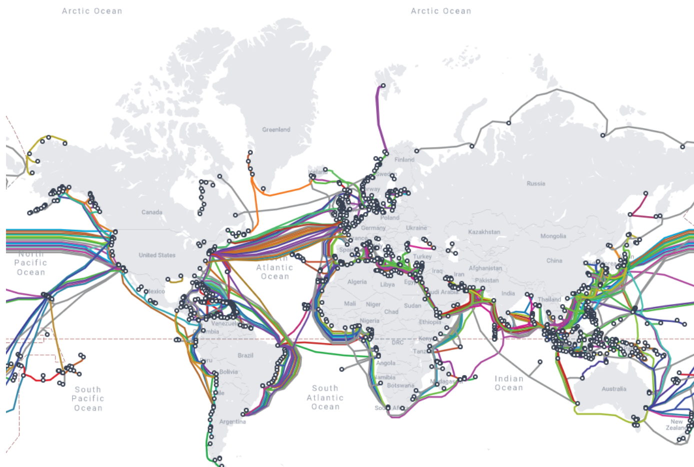

Figure 1.1: Submarine optical fibers across the globe. Reproduced from [25].

1.3 Integrated photonics

Initially, bulk optical components such as lenses and mirrors were used to guide and manipulate laser light. This type of setup is naturally sensitive to environmental influences (mechanical vibrations, humidity ..., temperature drift), from which the laser beam had to be protected. Already soon, it was proposed to apply a similar integration process as with electronic circuits, by employing e.g. dielectric waveguides, fabricated by means of photolitography, doping and/or etching [26]. The idea of the *photonic integrated circuit* (PIC) was born. The main benefits of integrated optics - as it was called then - were expected to be the small form factor and the potential economical scalability towards circuits with complex functionalities. Initially, it was forecasted that PICs would be able to combine a wide range of materials and functionalities by deposition and patterning of different types of layers (see Fig. 1.2) [27]. However, difficulties in fabrication quickly proved troublesome and PICs with a limited set of components became more common.

With the richness in laser sources and wavelengths came a wide range of integrated platforms being investigated. Platforms with a low index contrast such as (doped or etched) silica [26] or Ti-doped lithium niobate [28] provided good coupling with optical fibers, at the cost of large bend radii and hence a limited integration density. They could be used to make passive wavelength multiplexers and filters, and electro-optic modulators in fiber-optic networks [29]. Materials such as silicon nitride and silicon oxynitride could be deposited on oxidized silicon wafers and provided higher index contrasts and hence more densely integrated circuits with low propagation losses down to 0.1 dB/cm [30] in a wide wavelength range spanning from visible wavelengths to above 2 µm. Integrated active components such as lasers, detectors, modulators and switches on epitaxially grown III-V semiconductors were reported to often reach higher efficiencies than their bulk counterparts [27]. While certain advantages of integrated photonics on silicon substrates were already recognized early on, the market push towards telecommunication applications steered most early development efforts towards ferro-electric materials (lithium niobate) and III-V semiconductor platforms such as GaAs and InP [27,31]. Indeed, the first photonic integrated circuits performing more than one function were made on GaAs/InP platforms [32,33]. These circuits contained a single-mode laser and a modulator, for telecommunication links with high data rates.

As photonic integrated circuits started entering the market, more critical views on the push towards fully monolithic system integration arose.

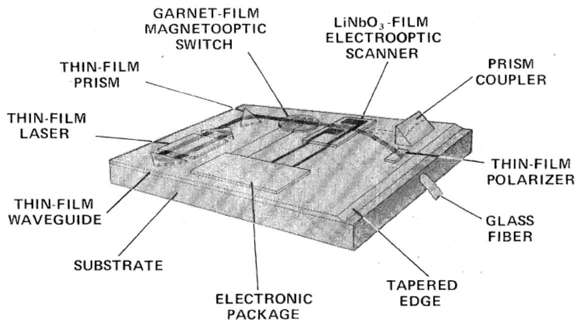

Figure 1.2: Early vision of complex PIC combining a wide range of materials and functionalities on a single substrate. Reproduced from [27].

Although fully monolithically integrated GaAs receivers had been demonstrated, their economic viability was questioned. After taking fabrication costs, testing, packaging and assembly into account, one report concluded that limiting the number of integrated functions per chip to two resulted in a lower cost, compared to fully integrated modules [34]. This conclusion was valid at any production volume, due to the increased chip size and compound yield issues at that time. Co-packaging of several chips was therefore common in the first III-V transceiver products. A later report showed that complex InP PICs with different components (requiring additional processing steps) only became economically viable if they could be made (and sold) in high enough volumes with high yield [35]. A problem persisting until today is that the market demand for specific PICs is usually far below the volume where dedicated process flows become economically interesting. Hence, as a solution, *generic* platforms were to be developed that would allow multiple products to be fabricated at the same time, sharing the production costs [36]. The availability of generic platforms and the need for low volume prototyping during PIC development later led to another cost reduction method, namely the sharing of wafer space between different customers: multi-project wafer runs (MPWs).

The emergence of silicon photonics

Crystalline silicon, despite being "the most thoroughly studied semiconductor in the world" [37], was only proposed as a waveguiding material for integrated photonics in the second half of the 1980s. Its high optical transparency in the 1310 nm and 1550 nm regions, and the potential for low bulk scattering/absorption losses in highly pure crystals showed great

promise for telecommunication applications [38]. The demonstration of excellent electro-optical properties in doped crystalline silicon further propelled the interest in this material [39]. Nevertheless, it was technologically challenging to create single-mode waveguides in a highly pure crystal. Attempts using different substrate configurations were made with varying success, until high quality silicon-on-insulator wafers became available after the development of Smart-Cut® technology by the French company Soitec [40]. The key driver for research into silicon photonics was the fact that it could leverage the immense amount of investment in CMOS fabrication facilities and reach substantially higher volumes at a lower cost than III-V semiconductors. The silicon-on-insulator platform reaches a better trade-off between waveguide loss and bend radius (and integration density) compared to indium phosphide [41]. At the same time, CMOS compatible processes are available for the integration of performant modulators (through doping) [42, 43] and photodiodes (through epitaxial growth of germanium) [44, 45]. While InP and GaAs had been very successful for long-haul applications, silicon promised to be more suitable for targeting mass markets [31]. However, the need for an external light source is a large technological hurdle for many silicon photonic applications up to this day.

Silicon nitride - a complementary platform to SOI and InP

In its early days, research into silicon nitride was motivated by the wide transparency range, including visible wavelengths, and the possibility to process it on silicon substrates [41]. Improvements of the deposition and etching processes lead to the achievement of low propagation losses down to 10 dB/m at visible wavelengths [30]. The low propagation losses and relatively small bend radii allowed to make long delay lines in silicon nitride. For optical biosensing applications, long delay lines allowed to increase the interaction length of light with an analyte and hence increase the sensitivity of the measurement [46, 47]. At telecommunication wavelengths, a further push to ultra-low propagation losses was desired to enable even longer delay lines for optical packet routing (buffering, switching) [41]. The lower index contrast of Si_3N_4 with SiO_2 reduces the sensitivity of passive components in Si_3N_4 to variations in the waveguide dimensions, compared to components in SOI or InP. For this reason, the highest performant on-chip optical filters are made on silicon nitride [48–50]. Furthermore, the fact that silicon nitride is added through a deposition step gives a large degree of freedom to optimize the waveguide geometry for a specific application. Optical powers of several Watts can propagate through silicon nitride waveguides without causing damage, when the material quality is high enough [51]. Thin layers with low confinement allow for these high powers to propagate

with minimal nonlinear signal distortion [52]. On the other hand, thick layers with high confinement allow for a maximal exploitation of optical nonlinearities [49, 51].

Lithium niobate - from bulk to thin films

Low-contrast waveguides in glass and lithium niobate ($LiNbO_3$, LN) crystals were developed early on for their compatibility with fiber optics. Phase modulators in bulk lithium niobate are commonly used even to this day. However, the large mode size requires the modulator's electrodes to be spaced far apart to avoid inducing optical losses. This reduces the overlap between the microwave mode and the optical mode and hampers velocity matching. Higher voltage swings need to be applied to obtain a π phase shift, and the maximal bandwidth remains limited. Having a stronger confinement of the optical mode would allow for more closely spaced electrodes and hence an improved device performance [53]. An initial improvement came from the use of ridge-type waveguides, in combination with doping, to increase the index contrast [54, 55]. The electrodes were then spaced on top of a deposited silicon oxide spacer layer. However, the confinement was still limited to ridges of 9 µm wide and the electrodes had to be several microns thick to achieve velocity matching. High bandwidths up to 100 GHz could be obtained, but the other performance metric, the half-wave voltage-length product ($V_{\pi}L$), remained high, around 10 V·cm. A further step included having a low dielectric layer between the lithium niobate substrate and a thin film of several microns thick [56]. As the material is notoriously hard to etch, polishing and laser ablation methods were used to form a thin layer out of a bonded LN substrate. Reaching submicron film thicknesses reliably was challenging.

Later on, the "ion slicing" technique was developed, which allowed the bonding of high quality, thin (down to several 100 nm) layers of lithium niobate to another substrate such as oxidized silicon [57]. This method resembles the Smart-Cut® method for the fabrication of SOI wafers. It allowed for the fabrication of high-confinement waveguides with good velocity matching and a strong overlap between the microwave and optical modes, resulting in modulators with high bandwidths and low driving voltages. Etching recipes were optimized to result in low propagation losses of the order of 0.2 dB/cm and below [58], approaching the losses of commercially offered silicon nitride [59, 60]. These developments placed thin-film lithium niobate in an overlapping market space, with the added benefit of having the electro-optic (EO) modulation capacity available. On top of that, lithium niobate can not only be doped with titanium, but also with

erbium. Similar to an erbium-doped fiber amplifier, this allows for light generation and lasing in the lithium niobate through optical pumping at room temperature [61,62]. Nevertheless, due to its more recent emergence, component libraries on this platform are not yet reaching the maturity of those on the silicon nitride platforms. Furthermore, its processing requires dedicated tools and cannot scale to high volumes as easily as SOI or silicon nitride.

Table 1.1 shows a qualitative comparison of the strengths and weaknesses of the previously discussed material platforms: InP, Si, Si_3N_4 and thin-film LN (TFLN). The most "complete" standalone platforms, InP and SOI, were able to drive innovation and serve the telecommunication market for several decades. However, for future applications with evermore stringent requirements on PIC performance, it becomes necessary to combine two or more material platforms to overcome their individual limitations. This can be done by assembling multiple chips in a package (*hybrid integration*), or by developing a fabrication flow whereby the different materials are added and processed together on the same substrate (*heterogeneous integration*).

Building block	InP	Si	Si_3N_4	TFLN
Passives	+	++	+++	++
Modulators	+++	++	+	+++
Switches	+++	+++	+	+++
Optical amplifiers	+++	0	0	+
Detectors	+++	+++	0	0
Footprint	++	+++	+ / ++	++
CMOS compatibility	0	++	+ / ++	0
Transparency range	+	++	+++	+++
Power handling	+	+	+++	+++

Table 1.1: Comparison of the strengths and weaknesses of the main integrated photonic platforms. Adapted from [63].

1.4 Hybrid and heterogeneous integration

As laid out in Table 1.1, each integrated photonic platform has its own set of advantages and drawbacks. Combining the strengths of different materials can overcome their individual limitations and increase the functionality of a system. Consider as an example external cavity lasers. Neither SOI, Si_3N_4

or TFLN have a ready solution for electrically pumped light generation to drive the integrated circuit. On the other hand, the propagation losses on III-V platforms limit the performance of passive filters. Initial external cavity lasers used III-V chips with anti-reflective coatings for edge-coupling to bulk diffractive elements [64, 65]. Those diffractive elements were later replaced by tunable filters and delay lines in SOI [66, 67] or Si_3N_4 [68, 69] to achieve a higher degree of integration, while reducing the laser's phase noise. Several integration techniques exist, each with their own pros and cons. Some of them are outlined below, from the point of view of integrating III-V based light sources onto other platforms.

Edge-coupling

Edge-coupling or butt-coupling is technologically the least complicated way to combine two chips into one circuit. Waveguides on both chips are terminated by the chips' facets, which are brought in close proximity to each other. Figure 1.3a shows a hybrid III-V/Si_3N_4 device being characterized. Reflections at the facet can be minimized by inclining the waveguides under an angle, and/or by applying an anti-reflective coating. To maximize transmission, the modal shapes at both facets should match as closely as possible. The benefits of edge-coupling are that each chip can be processed independently on its own substrate for maximal performance, and that proper surface coating can allow efficient coupling between waveguides with diverse modal indices (e.g. InP and Si_3N_4 [68–70]). Drawbacks are the limited integration density - although this can be partly mitigated using arrays of devices - and the increased device footprint. The chip assembly requires highly accurate alignment tools and can only be performed on singular dies, which slows down the integration process and drives up the module's price. While an excellent option for applications with low to medium volumes, requiring a limited number of sources and detectors, edge-coupling is less suitable for serving high-volume markets.

Photonic wire bonding

Photonic wire bonding is a relatively new technique for realizing hybrid interconnects. It is based on a two-photon polymerization process in a negative tone photoresist, upon illumination by a focused pulsed laser [72], followed by a development step, after which only the exposed path remains. Due to the nonlinear nature of the two-photon absorption process, the resolution is enhanced to below the diffraction limit of the pulsed laser. Photonic wire-bonding relaxes the alignment requirements in chip interconnects compared to edge-coupling, speeding up the pick-and-place

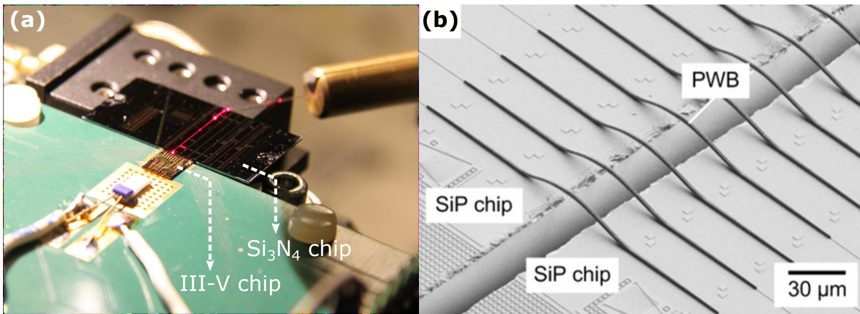

Figure 1.3: Images of (a) an edge-coupled III-V/Si_3N_4 device under characterisation and (b) a detailed view of photonic wire bonds connecting two silicon photonic circuits (adapted from [71]).

process. The precise location of the waveguides can be determined using machine vision after their moderately precise placement, after which the wire bond path is calculated and exposed by the laser. Initial demonstrations showed around 1.6 dB insertion loss for an interconnect between two SOI waveguides [72], which was later improved to 0.7 dB [73]. Another group demonstrated an interconnection between III-V lasers and III-V photodiodes on separate chips, with 10 dB loss [74]. The technique has also been picked up for commercial use [75]. Figure 1.3b shows an array of photonic wire bonds connecting two silicon photonic circuits on different chips. As an interconnect technology, photonic wire bonding is a very versatile technique, with the potential to speed up hybrid integration processes and to increase the interconnect density.

Flip-chip integration

Flip-chip integration is a method for interconnecting chips by adding solder bumps onto the electrical contact pads, and placing an external chip upside down onto the host, with aligned pads. It's a pick-and-place method that can be used to eliminate electrical wire bonding. In integrated photonics, flip-chip integration can be used to place a singulated III-V laser or amplifier into a recess in an SOI/Si_3N_4 integrated circuit [76,77]. Not only should the electrical contacts be aligned in this case, but also the optical facets of the III-V die and the waveguide on the host chip should be aligned both vertically and horizontally. The vertical alignment depends on the thickness of the III-V die, the depth of the recess and the thickness of the solder bumps. The waveguide facets can be horizontally aligned using alignment markers

and machine vision [76,78] or through active alignment. In the latter case, either the gain chip is pumped and the device output is monitored [79], or a continuous optical backscattering measurement is done during the alignment [77]. Vertical alignment with an accuracy of $\pm$ 10 nm was demonstrated by adding pedestals in the recess for mechanically contacting the III-V die [80]. The impact of misalignment can be reduced somewhat by expanding the mode on both facets as much as possible.

Compared to the edge-coupling method, flip-chip integration offers some advantages. The external die is integrated on the same substrate, which reduces the system footprint and packaging costs, while keeping a good thermal contact between the III-V die and the silicon substrate. The coupling interfaces are also no longer limited to the chip edges. A recess can be defined anywhere on the chip, allowing also light coupling on both ends of the III-V chip [76]. Furthermore, although it's a serial pick-and-place method, the III-V dies can be integrated on the silicon wafer prior to the chip singulation. Despite improving on several aspects of the edge-coupling method, the serial nature of the process is prohibiting for high-volume applications.

Wafer-to-wafer and die-to-wafer bonding

The previous integration methods were all examples of *hybrid integration*, or the assembly of finished separate dies into one circuit. The opposite strategy is to include the different materials early on in the process and leverage as much as possible from wafer-scale processing: *heterogeneous integration*. Wafer-to-wafer bonding, as the name suggests, consists of the transfer of an unprocessed substrate onto another one that is patterned and planarized, as shown in Fig. 1.4a. In integrated photonics, bonding of one or more III-V wafers onto a silicon substrate is a common example [81,82]. After annealing, the wafers are held together by strong covalent bonds. Following the bonding step, the III-V devices are defined with lithographic alignment precision relative to the underlying waveguides. Nevertheless, III-V wafers are currently limited in size to 100 mm (InP, although wafer bonding of a 150 mm InP wafer has been shown [83]) or 150 mm (GaAs), whereas silicon wafers are commonly 200 mm or even 300 mm in diameter. In wafer-to-wafer bonding, inevitably this will lead to a loss of material. For high-volume applications, or when the needed amount of III-V material per PIC is limited, it is more economical to bond separated dies to the host wafer. This way, not only can the whole host wafer be used, but it also becomes possible to integrate multiple types of materials/III-V stacks on the same circuit [84,85].

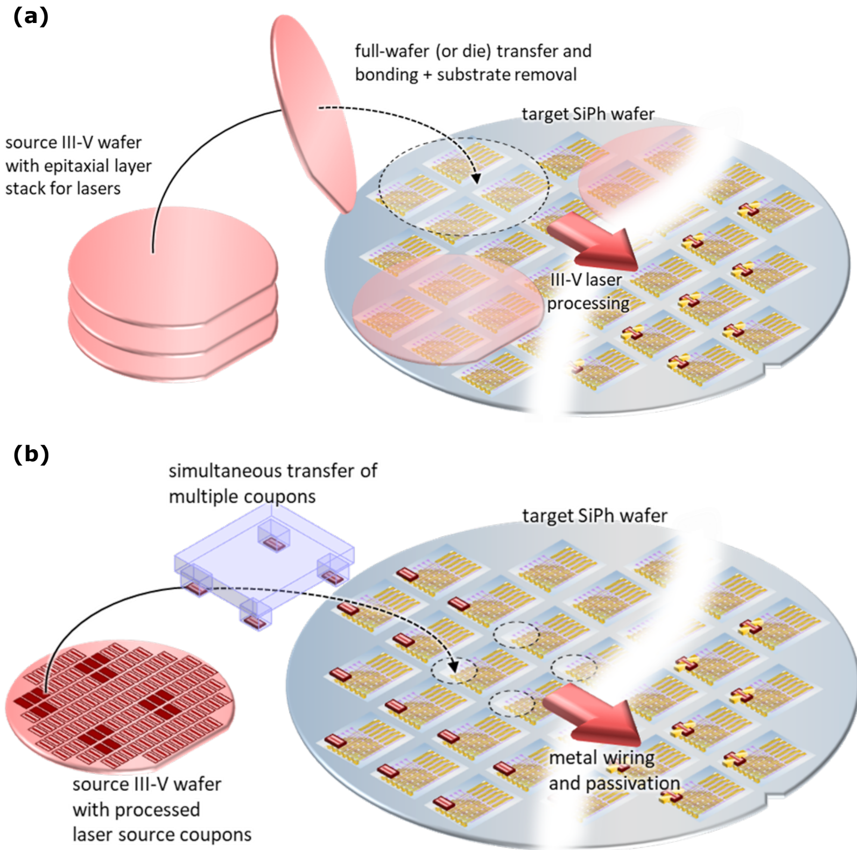

Figure 1.4: Schematic representation of (a) the wafer bonding process and (b) the micro-transfer printing process. In the wafer bonding process, more processing is required on the III-V material after its integration on the silicon wafer.

The key advantages of these methods are that they allow to reach high volumes and high integration densities, while making the chip packaging less complicated and hence cheaper. The drawbacks are related to device cost, yield and performance. Firstly, separate processing tools are needed for the processing of III-V materials on the larger silicon wafers due to incompatibility both with CMOS processes and typical III-V processing tools (wafer size). This significantly increases the initial investment into this technology. Partly because of this, it is only economically viable at

high enough volumes. Secondly, the added number of processing steps has a negative impact on the final device yield. The impact will depend on the maturity of the process and the quality of the III-V material. This issue is exacerbated when a circuit comprises multiple III-V components. Finally, extraction of excess heat from non-radiative recombination and Joule heating is less efficient on substrates with an insulating SiO_2 layer below the device layer, and has its impact on high-power operation of heterogeneous devices. Nevertheless, bonded heterogeneous devices with outputs of several tens of milliwatts have been demonstrated already on SOI (50 mW) [86] and Si_3N_4 (25 mW) [87].

Micro-transfer printing

Micro-transfer printing is an integration technique combining some of the advantages of wafer bonding and flip-chip integration. It is based on the switchable adhesion from a device of interest to an elastomeric stamp [88]. The adhesion to the stamp increases with the stamp's peeling velocity owing to its viscoelasticity. Provided that the adhesion of the device to its native substrate can be sufficiently reduced, the device's adhesion to the stamp can be kinetically turned on or off. This process was introduced to integrated photonics for the heterogeneous integration of active III-V devices on silicon photonic circuits [89–91]. The area on the source substrate can be densely populated with active devices, reducing material waste. Stamps can be patterned to pick up single devices or arrays, providing a route to high printing throughputs. A schematic drawing of the transfer of arrays of III-V components to a host substrate is shown in Fig. 1.4b. Similar to flip-chip integration, the III-V processing can be done in dedicated foundries, and the devices can be integrated in a recess defined at the back-end-of-line. On the other hand, similar to wafer bonding, transfer printing can enable adiabatically coupled devices and all processing steps can be performed on wafer-scale. This combination of properties makes it an interesting candidate for the back-end integration of a wide variety of materials, including e.g. lithium niobate, which is strictly incompatible with CMOS foundry processes [92]. State-of-the-art transfer printing tools have an alignment accuracy of 1.5 µm (3σ), making it necessary to incorporate some tolerance to misalignment into the design. This is in contrast to flip-chipped devices, where (slow) active alignment is a possibility. While in some demonstrations, III-V coupons are micro-transfer printed directly on a deposited gold surface [93], in others, an adhesive polymer layer is used to improve the printing yield [90, 91, 94]. The polymer layer improves the adhesion of the III-V coupon, but increases the thermal impedance of the device as well.

Micro-transfer printing has been used to demonstrate both adiabatically coupled [91, 95] and facet-coupled [89, 94, 96] lasers on silicon. However, the reported output powers are still lower than the best results using wafer bonding and flip-chip bonding.

1.5 Applications of hybrid and heterogeneous devices

The first commercial appearance of photonic integrated circuits was in long-haul communications. Indeed, optical technologies can offer fundamentally higher bandwidths than microwave technologies, and they become more cost effective when the bandwidth-distance product is high enough. As data rates in all parts of the communication network are ever growing, the tipping point for using optical technologies hence keeps moving to shorter distances. Although innovation in electrical technologies has not stopped, it is prospected that optical technologies will penetrate deeper into the network, down to chip-level interconnects in datacenters, as shown in Fig. 1.5 [97]. Nevertheless, a more widespread deployment of photonic integrated circuits implies their fabrication and assembly at high volumes. The original optical transceiver modules for long-haul communications were made from hybridly assembled III-V chips, as the economical case for fully integrated transceivers was not always obvious [34]. As volumes grew and technologies matured, the balance of cost-effectiveness inevitably tipped over to fully integrated III-V chips, and later on to hybrid III-V/SOI chips [66]. Since then, large investments have been made (e.g. by Intel) into heterogeneous integration based on III-V-on-SOI wafer bonding [98]. Their dedicated process flow for III-V devices on top of 300 mm silicon wafers offers a viable path towards high volumes.

The example of optical transceiver modules is one where the used integration method was updated every time to allow reaching higher production volume at a sufficiently low cost. For other applications, heterogeneous integration can become essential to reach certain performance targets. Carrier-based phase modulators on silicon, for example, are compact, performant, and readily fabricated using CMOS processes, and as such have been essential building blocks for optical communications. However, they come with fundamental trade-offs regarding insertion loss and linearity due to their free-carrier-based nature. Heterogeneous integration is heralded as a necessary step to reach the required specifications of future high-bandwidth transmitters [99].

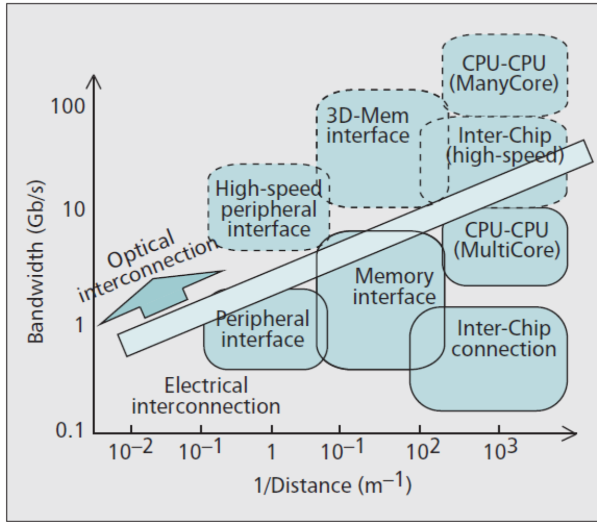

Figure 1.5: Use cases for optical interconnect technologies at decreasing distances. Reproduced from [97].

While silicon and indium phosphide has been the workhorses of integrated photonics at telecom wavelengths, more recently silicon nitride has been gaining more traction due to its superior passive performance. Applications requiring ultra-low insertion losses of several centimeters of propagation length, a more temperature insensitive operation, or high power operation, can benefit from silicon nitride's properties. Examples are LiDAR, quantum computers, or lasers with ultra-low phase noise. Most packaged device demonstrations using silicon nitride chips use edge-coupled light sources [68, 100]. More recently, also flip-chip integration has been used [77, 78]. However, the methods for heterogeneous integration of III-V materials on silicon cannot be readily reused due to the high refractive index difference. As a solution, the cointegration of silicon and Si_3N_4 in multilayer circuits has come up as a way to bridge this index difference. This method was first applied for the integration of photodiodes [101], and later on (also during the course of this work) for laser integration [102, 103]. Varying cross-sections of these multi-layered circuits have been used. Some start with an LPCVD nitride circuit, on top of which an SOI wafer is bonded [87]. In this dissertation, the use of deposited amorphous silicon on top of the silicon nitride is proposed [103, 104]. Again others start from a patterned SOI wafer, followed by the deposition of several layers of PECVD silicon

nitride [105,106]. Finally, another group used a silicon-rich Si_3N_4 deposition to cover the refractive index gap between a Si_3N_4 circuits and a quantum-dot-based light source [107]. The previous examples all demonstrated III-V integration in the multilayer stack, however still several other groups have combined silicon and silicon nitride in a multilayered circuit for enhanced passive capabilities [108–113]. In some cases, the two layers are used for separate components, and in others both layers are used to enhance one building block, such as a grating coupler, or a waveguide crossing. A wide variety of layer stacks has been demonstrated, each for a specific purpose. The order of the integration (SOI first or Si_3N_4 first) depends on the purpose and the technological difficulties. Thick silicon nitride layers may be desired to reach higher confinement, or to make more compact circuits, however this is technologically challenging to achieve using LPCVD. Furthermore, while LPCVD nitride offers the lowest propagation losses, it is deposited at temperatures exceeding 1000°C, making it a front-end process incompatible with any doped components in an underlying silicon layer. For this reason, thick silicon nitride layers can only be added on top of the silicon in a back-end process, using PECVD.

1.6 Research objectives

This initial aim of this PhD project was the development of widely tunable lasers with potentially low phase noise, based on the heterogeneous integration of III-V semiconductor-based light sources on a low-loss silicon nitride platform. At a later stage, through a collaboration with Stanford University, a similar fabrication process was developed for the heterogeneous integration of lasers on a thin-film lithium niobate platform. The dissertation consists of the following work packages / developments:

1. The development of a fabrication flow for rapid prototyping of III-V-on-Si_3N_4 lasers and amplifiers. An intermediate layer of hydrogenated amorphous silicon (a-Si:H) is used to bridge the refractive index difference between silicon nitride and the III-V component. This choice was motivated by the simplicity of the process. The III-V components are integrated using the micro-transfer printing technique.

2. The addition of heaters to the fabrication flow to add wavelength tuning capabilities. Adhesion issues of the heaters on a BCB layer have been addressed by investigating the influence of the heater's top and bottom cladding. The maximal power dissipation has been significantly increased after adding a SiO_2 encapsulation around the heaters.

3. The design and characterization of components in the multilayer circuit. This includes ring resonators, delay lines and interlayer transitions. A cut-back method was used for the characterization of the quality of the a-Si:H layer, the propagation losses in the Si_3N_4 layer, and the influence of the available top claddings in our cleanroom.

4. The fabrication and characterization of a III-V-on-Si_3N_4 amplifier, multi-mode laser, single-mode laser and widely tunable laser. The widely tunable laser failed to work and a root cause was identified through the characterization of separate test structures.

5. The development of an updated fabrication flow for the integration of III-V-on-$LiNbO_3$ lasers, starting from an oxide-clad LN circuit. A back-end compatible process was developed, starting with the local opening of the oxide cladding to expose the LN waveguides. The deposition of a-Si:H was replaced by the micro-transfer printing of a block of crystalline silicon onto an exposed LN waveguide in a recess.

6. The fabrication and characterization of III-V-on-$LiNbO_3$ amplifiers, ring lasers and widely tunable single-mode lasers. Electro-optic wavelength tuning was demonstrated through lithium niobate's Pockels effect.

The key results of this dissertation are the demonstration of amplifiers and lasers on both platforms. Specifically on lithium niobate, we showed the first demonstration of electro-optic wavelength tuning in an integrated laser. Further improvements and optimization are definitely possible. The work described here will soon be outdated, but it may serve as a first building block for future work.

1.7 Outline of the thesis

This dissertation consists of two main parts. The first part covers the development of the multilayer integrated platform of III-V components, hydrogenated amorphous silicon and silicon nitride. First, the fabrication process is described in Chapter 2. Then, Chapter 3 gives an overview of the design of the layer stack and the characterization of some of the passive components on this platform. Finally, fabricated amplifiers and lasers on this platform are characterized in Chapter 4. This ordering should not be mistaken for a chronological order of the work. Some design parameters in Chapter 4 will appear suboptimal based on the knowledge of the previous

chapters, since these results were obtained during the many design and fabrication iterations, of which only the synthesis is described in Chapters 2 and 3. In the second part, the developed fabrication methods are taken a few steps further for the integration of III-V components on a cladded lithium niobate integrated circuit. In Chapter 5, the fabrication flow of this back-end process is described, followed by the characterization of the fabricated devices in Chapter 6. Chapter 7 presents a conclusion to the dissertation and an outlook on future work and developments.

Contributions from colleagues: Some parts of this dissertation are the results of work from other colleagues, but still mentioned for the sake of completeness. Specifically, the processing of the III-V amplifier coupons was done by (now Dr.) Bahawal Haq. The development and processing of the SOI coupons was done by Stijn Poelman and Stijn Cuyvers.

1.8 Publications

This dissertation has led to the following publications in conferences and international peer-reviewed journals.

1.8.1 Publications in international journals

K. Van Gasse, L. Bogaert, L. Breyne, J. Van Kerrebrouck, S. Dhoore, **C. Op de Beeck**, A. Katumba, C. Y. Wu, H. Li, J. Verbist, A. Rahim, A. Abassi, B. Moeneclaey, Z. Wang, H. Chen, J. Van Campenhout, X. Yin, B. Kuyken, G. Morthier, J. Bauwelinck, G. Torfs, G. Roelkens, "Analog radio-over-fiber transceivers based on III-V-on-silicon photonics," *IEEE Photonics Technology Letters*, **30**(21), pp. 1818-1821 (2018)

J. Zhang, G. Muliuk, J. Juvert, S. Kumari, B. Haq, **C. Op de Beeck**, B. Kuyken, G. Morthier, D. Van Thourhout, R. Baets, G. Lepage, P. Verheyen, J. Van Campenhout, A. Gocalinska, J. O'Callaghan, E. Pelucchi, B. Corbett, A. J. Trindade, G. Roelkens, "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing," *APL Photonics*, **4**, p. 110803 (2019)

C. Op de Beeck, B. Haq, L. Elsinger, A. Gocalinska, E. Pelucchi, B. Corbett, G. Roelkens, B. Kuyken, "Heterogeneous III/V-on-Si_3N_4 amplifiers and lasers via microtransfer printing," *Optica*, **7**(5), pp. 386-393 (2020)

E. Vissers, S. Poelman, **C. Op de Beeck**, K. Van Gasse, B. Kuyken, "Hybrid integrated mode-locked laser diodes with a silicon nitride extended cavity,"

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1.8.2 Publications in international conferences

G. Roelkens, J. Zhang, G. Muliuk, J. Goyvaerts, B. Haq, **C. Op de Beeck**, A. Liles, Z. Wang, S. Dhoore, S. Kumari, J. Juvert, J. Van Campenhout, B. Kuyken, D. Van Thourhout, B. Corbett, A. J. Trindade, C. Bower, R. Baets, "III-V/Si PICs based on micro-transfer printing", in *2019 Optical Fiber Communications Conference and Exhibition*, (USA, 2019), paper W4E.6.

C. Op de Beeck, L. Elsinger, B. Haq, G. Roelkens, B. Kuyken, "Towards the integration of C-band amplifiers on silicon nitride via transfer printing", in *Frontiers in Optics + Laser Science APS/DLS*, (USA, 2019), paper FTu5C.6.

C. Op de Beeck, L. Elsinger, B. Haq, G. Roelkens, B. Kuyken, "Heterogeneously Integrated Laser on a Silicon Nitride Platform via Micro-Transfer Printing", in *Frontiers in Optics + Laser Science APS/DLS*, (USA, 2019), paper FTu6B.1.

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J. Zhang, **C. Op de Beeck**, B. Haq, J. Goyvaerts, S. Cuyvers, S. Kumari, G. Muliuk, A. Hermans, E. Gocolinska, B. Corbett, A. Jose Trindade, C. Bowers, J. Van Campenhout, G. Lepage, P. Verheyen, B. Kuyken, D. Van Thourhout, G. Morthier, R. Baets, G. Roelkens, "Micro-Transfer-Printing for III-V/Si PICs", in *2020 Asian Communication and Photonics Conference*, (China, 2020), paper T4G.3.

C. Op de Beeck, G. Roelkens, B. Kuyken, ”Single-Mode Heterogeneous III-V-Si_3N_4 Laser”, in *European Semiconductor Laser Workshop 2020*, (Online, 2020).

S. Cuyvers, B. Haq, **C. Op de Beeck**, S. Poelman, A. Hermans, Z. Wang, G. Roelkens, K. Van Gasse, B. Kuyken, ”Ultra-Dense III-V-on-Silicon Nitride Frequency Comb Laser”, in *European Conference on Optical Communication*, (Online, 2020), paper TH1L-4.

T. Vanackere, M. Billet, **C. Op de Beeck**, S. Poelman, G. Roelkens, S. Clemmen, B. Kuyken, ”Micro-Transfer Printing of Lithium Niobate on Silicon Nitride”, in *European Conference on Optical Communication*, (Online, 2020), paper Mo1C-5.

D. Maes, G. Roelkens, M. Zaknoune, **C. Op de Beeck**, S. Poelman, M. Billet, M. Muneeb, S. Lemey, E. Peytavit, B. Kuyken, ”Heterogeneous Integration of Uni-Travelling-Carrier Photodiodes using Micro-Transfer-Printing on a Silicon-Nitride Platform”, in *2021 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference* (Online, 2021), paper CK-4.3.

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I. Luntadila Lufungula, A.Shams-Ansari, **C. Op de Beeck**, S. Cuyvers, S. Poelman, G. Roelkens, M. Loncar, B. Kuyken, ”Two-step transfer printed single mode DFB laser on LN”, in *Annual Symposium of the IEEE Photonics Society Benelux Chapter* (Belgium, 2021).

S. Cuyvers, A. Hermans, S. Poelman, **C. Op de Beeck**, B. Haq, G. Roelkens, K. Van Gasse, B. Kuyken, ”III-V-on-Silicon-Nitride Mode-Locked Lasers”,

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I. Luntadila Lufungula, A.Shams-Ansari, D. Renaud, **C. Op de Beeck**, S. Cuyvers, S. Poelman, G. Roelkens, M. Loncar, B. Kuyken, ”Universally printable single-mode laser on low-index platforms”, in *2022 Conference on Lasers and Electro-optics* (USA, 2022).

I. Luntadila Lufungula, A.Shams-Ansari, D. Renaud, **C. Op de Beeck**, S. Cuyvers, S. Poelman, G. Roelkens, M. Loncar, B. Kuyken, ”On-chip electro-optic frequency comb generation using a heterogeneously integrated laser”, in *2022 Conference on Lasers and Electro-optics* (USA, 2022).

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2

Process development for multilayer III-V/a-Si:H/Si_3N_4 platform

Anything will lase if you hit it hard enough.
Arthur L. Schawlow

2.1 Introduction

This chapter deals with the fabrication aspects of the first developed multilayer platform. First, the material choice is motivated by expanding on the different deposition methods and the material options. This is followed by a brief highlight of the final platform's cross-sections. Next, the development of the E-beam lithography and etching process is described, with special attention to the process calibration of the circuit's critical features (gratings, taper tips, and directional couplers). After elaborating on the patterning procedure, the process steps are discussed in chronological order. First, the definition of the bi-layered a-Si:H/Si_3N_4 circuit, followed by the heterogeneous integration of the III-V amplifier. Next, all metallization steps for heaters and electrical contacting/routing are covered. For the heaters, a small study on the influence of the cladding on the breakdown power levels. Finally, the chapter concludes with possible improvements of this stack.

2.2 Choice of materials and deposition methods

Chemical vapour deposition Chemical Vapour Deposition (CVD) is a common deposition method in the semiconductor industry for the deposition of thin films. It's a process whereby volatile precursor gases react or decompose on a target substrate, forming a thin layer. Two variants of this technique are highlighted here: plasma-enhanced CVD (PECVD) and low-pressure CVD (LPCVD). In both processes the reaction chamber is kept at a low pressure ranging from a few mTorr to about 1 Torr [114]. The low pressure is needed to avoid unwanted reactions occuring in the gas phase.

LPCVD The name LPCVD is reserved for when the energy to break down the precursor gases into radicals and to initiate the film growth is purely thermal. The required temperatures depend on the process but can range from 400°C to 800°C and above [114]. The wafers are to be kept at a very uniform temperature to achieve a uniform film growth. The number of loaded wafers is kept constant to keep the deposition rate stable over multiple runs. The deposition occurs on both sides of the wafers. LPCVD processes yield conformal layers with high breakthrough voltages, low optical losses and often low etch rates. However, the high temperatures are prohibitive for the use of photoresists, and exceed the thermal budget of e.g. doping profiles, which can be destroyed by diffusion. This typically limits LPCVD processes to the front-end. Heating the chamber to the required high temperatures is furthermore both time and energy consuming. Another issue is that the deposited layers often have a high intrinsic stress, on top of the stress that arises from having a different thermal expansion coefficient than the substrate. This stress limits the thickness of these layers to avoid cracks and excessive wafer bowing, unless tricks are applied. Although single-wafer LPCVD systems exist, typically several wafers are loaded simultaneously. Larger reactors, capable of loading up to 150 wafers at once, compensate for the time lost during heating and the typically slow deposition rates, but are only useful for high volumes [115].

PECVD In a plasma-enhanced CVD process, the decomposition of the precursor gases into reactive radicals (a plasma) is assisted by strong radio-frequency radiation. This allows for the deposition of layers at strongly reduced temperatures (<400°C), making this process more suitable for depositions on doped targets. In a PECVD chamber, usually a single die or wafer is loaded on the bottom electrode, which doubles as a heater, hence the thin film is only deposited on one side of the wafer. This configuration is also much more practical in low-volume R&D environments. Deposition

rates in PECVD are typically higher than for LPCVD and maintenance is much less time-consuming than for LPCVD reactors. A drawback is that the layer thickness uniformity, density and optical losses are typically inferior to those of LPCVD depositions.

Silicon Silicon occurs in a monocrystalline, polycrystalline or amorphous form. Monocrystalline silicon (c-Si) is by far the most commonly used starting material for integrated circuit processing. Although some growth methods start from poly-crystalline silicon, it is generally grown by bringing molten high-purity silicon into contact with a seed, from which a continuous crystal starts to form. After the growth, the material is sliced into wafers. Obtaining thin layers of c-Si on an underlying silicon oxide layer in a reliable manner proved difficult. Several methods were developed, such as heteroepitaxial growth, doping of bulk c-Si with very high oxygen concentrations, or wafer bonding and etching back a full c-Si wafer [116]. However, all methods came with problems such as defects, limited control over the layer thickness or highly stressed layers. The development of Smart-Cut® technology in the nineties led to the availability of silicon-on-insulator wafers with pure c-Si thin films of a well controlled thickness [40].

An amorphous silicon (a-Si) layer with a high refractive index of n=3.73 can be deposited on a target wafer by sputtering a crystalline Si target with highly energetic Xe particles [117]. However, pure amorphous silicon contains a lot of dangling bonds which will cause high optical absorption losses. These dangling bonds can be partially passivated by the incorporation of hydrogen. To distinguish this material from the pure a-Si, it is called hydrogenated amorphous silicon (a-Si:H). Hydrogenated amorphous silicon can also be deposited at relatively low temperatures (180°C - 300°C) with PECVD using a silane (SiH_4) precursor gas [118]. The PECVD process at 180°C that is used in our cleanroom creates a very dusty plasma, requiring both mechanical (wiping/vacuum cleaning) and chemical cleaning of the reaction chamber. Silane is also used for the deposition of poly-crystalline silicon (poly-Si) layers. The difference in deposition conditions is mainly the temperature. Poly-Si is often deposited in an LPCVD process at 580°C - 630°C. The higher temperature allows for mobility of the Si atoms and the local formation of crystalline order. Higher temperatures lead to more nucleation sites, which results in a smaller grain size. Similarly, by annealing amorphous silicon at elevated temperatures, poly-crystalline Si can be obtained [119]. In contrast to undoped c-Si, both a-Si:H and poly-Si will suffer from bulk light scattering. In a-Si:H, depending on the deposition conditions, light will scatter on voids and defects, whereas in poly-Si, scattering

happens on the multiple grain boundaries.

Silicon nitride PECVD silicon nitride has a significantly higher hydrogen content than LPCVD Si_3N_4, leading to absorption peaks. Particularly for this work, it induces absorption at 1520 nm. The general layer quality is also lower in PECVD, leading to a higher background optical loss. On the other hand, PECVD Si_3N_4 can be made very thick by alternating between two process conditions that result in layers with compressive and tensile stress. High-temperature annealing can reduce the hydrogen content in the material, but this will also affect the stress in the material. LPCVD silicon nitride is typically limited to layer thicknesses around 300 - 400 nm before the onset of stress-induced cracks [120, 121]. Thicker layers would enable dispersion engineered waveguides and a higher confinement, e.g. for nonlinear optics. Some groups mitigate this problem by introducing crack barriers: trenches etched (or manually scribed) into the underlying silicon oxide [120, 122]. This however only results in "nearly crack-free" LPCVD Si_3N_4 layers and does not solve the problem with wafer bow on larger wafers. The term *photonic Damascene process* has been coined for a variant of the crack barrier method, where the waveguides are defined during the crack barrier etch [123]. The crack barriers/waveguide openings are then filled by the conformal deposition of a thick Si_3N_4 layer. After the deposition, the excess material is polished away, leaving a smooth top surface. The optical losses in this method can be further reduced by reflowing the etched silicon oxide, leading to smoother sidewalls [124]. Other researchers developed a *twist-and-grow* process whereby the wafers are rotated 45° in between LPCVD deposition steps of 365 nm Si_3N_4 [125]. This rotation re-distributes the uniaxial strain and prevents excessive wafer bow. Using this technique, the researchers deposited 800 nm thick LPCVD Si_3N_4 layers on a 200 mm wafer [51]. In principle, this can also be scaled towards 300 mm wafers.

Silicon oxide Silicon (di)oxide can be grown by oxidation of a silicon substrate, or through chemical vapour deposition. When a silicon substrate is exposed to an oxidizing agent at elevated temperatures (typically 800°C - 1200°C), the silicon molecules react with the oxygen and form silicon oxide. In this process, a part of the substrate is consumed. The oxidizing agent can be pure oxygen (dry oxidation) or clean water steam (wet oxidation). The growth rate in this process decreases as the layer thickness grows, since the oxygen atoms have to diffuse through the already formed SiO_2 layer to reach the substrate. This puts a practical limit to the layer thicknesses that are typically grown with this method, although it is possible to grow

8 µm [63,126] or even 15 µm [127] thick layers. Wet oxidation is 5 - 10 times faster than dry oxidation as water molecules are smaller than O_2 molecules and can hence diffuse faster [114]. Thermal silicon oxide (TOX) offers the highest optical quality: low absorption and low Rayleigh scattering. However, thermal oxide is typically only available as the bottom cladding. To achieve ultra-low losses, a silicon wafer with a thick layer of thermal oxide can be bonded on a planarized sample [127].

For the CVD deposition of silicon oxide, there are two possible chemistries: silane (SiH_4) and tetraethyl orthosilicate (TEOS, $Si(OC_2H_5)_4$). They can both be used in LPCVD, as well as in PECVD reactors. The silane-based PECVD process has the advantage of the lowest possible process temperature (200°C - 400°C), making it compatible with back-end operations in a CMOS line. However, residual hydrogen impurities and other defects will increase the optical losses in this material. Absorption at telecom wavelengths caused by the hydrogen impurities can be avoided by using deuterated precursors [128]. The difference in atomic mass shifts the absorption bands out of the region of interest. The TEOS chemistry leads to more conformal layer depositions with a higher optical quality compared to silane, especially when depositing using LPCVD. Nevertheless, stress will also limit the achievable crack-free SiO_2 thickness that can be deposited using LPCVD to around 1500 nm [121].

DVS-BCB Divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or short, BCB) is a polymer that is often used as an adhesive layer in heterogeneous integration processes. Layer thicknesses ranging from several microns, or when diluted with mesitylene, several tens to hundreds of nanometers, can be applied to a sample through spincoating. It can be cured at relatively low temperatures (<300°C) into a glass-like layer with a refractive index of n=1.54. It features several attractive properties for use in photonic heterogeneous integration such as low moisture absorption, good thermal stability, high degree of planarization and low optical loss. On the other hand, its thermal conductivity is about 4 times lower than that of silicon oxide. The optical losses depend on the curing atmosphere. The presence of oxygen or nitrogen will induce losses as shown later in Section 3.2.2.

The lowest optical losses in a multilayer platform will be achieved if it is possible to combine LPCVD Si_3N_4 and c-Si layers, ideally clad with TEOS-based LPCVD SiO_2 and thermal oxide and patterned using deep-UV (DUV) lithography. Using thicker layers of Si_3N_4 will allow reducing the thickness and influence of the oxide claddings. A thinner buried oxide layer will

lead to a lower thermal resistance to the substrate, which is important for integrated active components such as III-V amplifiers. LPCVD processes are not available in our cleanroom, but 10-mm wafers with LPCVD Si_3N_4 on thermal oxide can be commercially purchased from Lionix BV. PECVD Si_3N_4 is available in our cleanroom, but the losses around 1550 nm are of the order of 1-2 dB/cm. Waveguide patterning will be done using electron-beam lithography to allow for faster and more flexible prototyping. For the first part of this work, the combination of deposited a-Si:H on LPCVD Si_3N_4 is chosen over PECVD Si_3N_4 on c-Si for multiple reasons. First, the main goal is to demonstrate lasers with a silicon nitride cavity. Having low losses in the silicon nitride layer is hence more important than reducing the losses in the c-Si/a-Si:H layer, which will be only a few millimeters long. Second, a low-index Si_3N_4 waveguide deposited on silicon cannot work without first etching the silicon and planarizing the wafer. Planarization steps are tedious and best avoided. Depositing a-Si:H is chosen over wafer bonding c-Si for simplicity, and with the idea in mind that ideally, the process could be implemented in the back-end. Depositing a-Si:H in a recess is much less troublesome than bonding a small piece of c-Si in a recess. At a later stage in the project, the a-Si:H deposition was replaced by the microtransfer-printing of small c-Si coupons.

2.3 Developed multilayer III-V/a-Si:H/Si_3N_4 platform

Figure 2.1 shows a schematic cross-section of the developed multilayer platform. It features two main waveguiding layers (Si_3N_4 and a-Si:H) and a transition between them. Both layers are patterned using electron-beam lithography. Titanium heaters can be placed at arbitrary distances from the waveguides by locally etching back the cladding. The cladding material around the waveguides is DVS-BCB. The platform includes a heterogeneous integration flow for III-V semiconductor-based amplifiers. To achieve the ultimate goal of dense integration of functionality, all electrical connections can be routed to an array of wire-bonding pads. To avoid issues with the adhesion of gold on the BCB cladding, a via through the BCB cladding down to the insulating Si_3N_4 layer is added. This will increase the yield of the wire-bonding process.

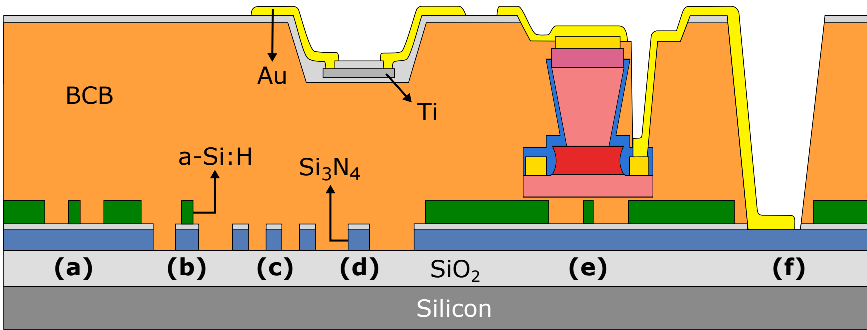


Figure 2.1: Cross-section showing the possible features of the developed multilayer platform. (a) Wire waveguide in the a-Si:H layer. (b) Waveguide transition between the a-Si:H layer and the Si_3N_4 layer. (c) Wire waveguides in the Si_3N_4 layer. (d) Titanium heaters in a silicon oxide encapsulation, placed at an arbitrary distance above the Si_3N_4 waveguide. (e) III-V semiconductor optical amplifier integrated on an a-Si:H waveguide. The layer stack of the amplifier is shown in Section 2.6. (f) Isolated contact pad on the Si_3N_4 layer, for wire bonding.

2.4 Circuit definition using E-beam lithography

E(lectron)-beam lithography is a maskless, direct-write lithographic technique, based on the switchable solubility of an electrosensitive resist in a developing agent. It offers high resolution patterning at the cost of a lower throughput as compared to deep-ultraviolet (DUV) lithography. It is therefore mostly used for low-volume applications such as mask fabrication or research and development. A schematic drawing from an E-beam column, including some of the typical components, is shown in Fig. 2.2. In this work, the circuit definition was carried out using Raith's 50 kV E-beam system Voyager [129]. The electron gun is a field emission source which is able to provide high currents for fast patterning of larger structures. This current can be reduced for slower patterning with higher accuracy and resolution. A beam blanker blocks the electron beam when no patterning should be done, e.g. while moving between two structures. A pair of electron lenses is used to adjust the focal plane of the beam. The aperture size can be tuned to have more current levels available. A stigmator allows to minimize astigmatism to obtain a circular beam. This is necessary to have the same line widths for a horizontal and a vertical scan. High-speed deflectors send the beam to the locations on the wafer as defined by the pattern.

A design to be patterned will be fractured in smaller components by the software of the E-beam and divided in pixels. During exposure, each pixel is

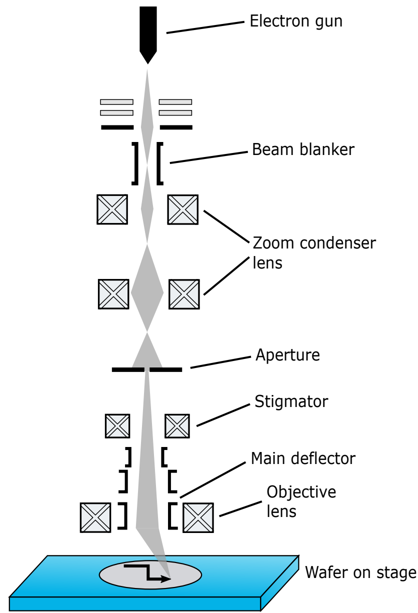


Figure 2.2: Schematic drawing of some of the components in an electron beam column, edited from [130].

illuminated during the time needed to achieve a certain exposure dose. For the Voyager, the standard pixel size is 5 nm × 5 nm, but it can be lowered to 3 nm × 3 nm for higher accuracy patterning. The critical dimensions of the features in the design should be multiples of the pixel size, however the distance between different features can be more accurate. The address grid of the system is 1 nm. This is for instance important when patterning grating couplers: the period can be chosen with an accuracy of 1 nm, however the fill factor should be snapped such that the exposed region has a length which is a multiple of 5 nm. The software uses a vector scan algorithm to pattern all features, meaning the beam is directed only to features which have to be exposed. For sparser designs, this algorithm allows a shorter patterning time as compared to a line scan technique, where the beam scans over the whole writefield and the beam blanker turns the beam on and off when required.
In order to obtain an optimal pattern, four steps are to be carried out prior to the patterning.

Beam current measurement: Accurate knowledge of the current is needed in order to estimate how much time is required per pixel to receive the desired dose.

Sample leveling: The surface to be patterned should be as horizontal as possible such that the whole design is patterned with a focused beam. The depth-of-focus of the electron beam is a few microns, so a modest topography on the sample can be tolerated.

Focus and stigma correction: The beam should be focused on the sample's surface and astigmatism should be minimized. These parameters are usually optimized together.

Deflection distortion correction: When the electron beam is deflected far away from the center of the writefield, the error on the beam's position on the sample increases due to nonlinear behaviour of the deflector. If uncorrected, patterns at the edges and corners of the writefield will be distorted, and stitching errors will occur when patterns cross writefield boundaries. A calibration procedure should be carried out where a pattern is observed at different positions relative to the beam center (by moving the sample holder with high precision) and comparing the distorted image with the original pattern. A lookup table is then created which maps the distorted writefield onto a rectangular writefield. Any residual error will be noticeable in the

form of stitching errors.

Electrosensitive resists can be subdivided into two families, based on their reaction to the exposure. For *positive tone* resists, the exposed parts become soluble in the developer. In a photonic integrated circuit, this means that the trenches next to the waveguides have to be patterned. *Negative tone* resists behave in the opposite way, they become insoluble in the developer after exposure. With this type of resist, only the waveguide cores need to be patterned. Most of the sample surface will be etched, with only the waveguides sticking out. This inverse topography is less suitable for heterogeneous integration if it is not planarized. For micro-transfer printing, a planarization step can still be avoided by defining a large flat area next to the waveguide to support the heterogeneously integrated component.
In this work, the E-beam circuit definition is done using the positive tone AR-P 6200 resist. Two varieties with different concentration are used: AR-P 6200.09 and AR-P 6200.13. The former offers layer thicknesses below 320 nm, for shallow etches or metal marker deposition by lift-off. The latter can offer layer thicknesses up to 650 nm, for deep etches with low selectivity. A thin (approx. 70 nm) layer of a conductive polymer (Electra 92, or AR-PC 5090) is spincoated on top of the resist to avoid charging of the sample during exposure, which can deform the pattern. The standard exposure dose used for waveguides and other components using this resist is 160 $\mu C/cm^2$. Before development, the conductive polymer is removed by rinsing the sample with deionized water. Samples are developed for 60 seconds in n-amyl acetate at room temperature and the development is stopped by submerging the sample in isopropyl alcohol (IPA). The sample is inspected for patterning errors. If no visible errors are seen that jeopardize the circuit's operation, the sample is etched using reactive ion etching after a short 10 second etch in a low pressure oxygen plasma (See Table A.1). This oxygen plasma will etch the resist anisotropically to remove any pedestals at the bottom of the resist features (so-called *tail-cutting*) and any residual traces of resist in the developed areas. This is mostly important when only a partial etch is needed, but it is included in the standard practice.

2.4.1 Resolution and proximity effect

The resolution limit of conventional optical lithographic techniques is ultimately the diffraction limit, which inhibits the observation of two sub-wavelength structures with a separation d below

$$d = \frac{\lambda}{2 \cdot \mathrm{NA}} = \frac{\lambda}{2n \sin\theta}, \tag{2.1}$$

where NA is the numerical aperture of the imaging system, θ is the half-angle of the focal spot and n the refractive index of the medium between the focal spot and the imaging system. In air, the theoretical resolution limit is hence $\lambda/2$, however practical imaging systems cannot achieve this. For deep-UV lithography at 248 nm or 193 nm, this puts the practical resolution limit above 124 nm or 97 nm. The resolution can be pushed down by filling the air gap between the UV source's optics and the sample surface with a (transparent) material with a higher refractive index. This technique is called *immersion lithography*. Extreme-UV lithography, using a wavelength of only 13 nm, can overcome the resolution problem of deep-UV, but it comes with disadvantages of its own.

As theorized by De Broglie, also particles with mass such as electrons exhibit wave-like properties. The wavelength of an electron depends on its energy and hence the acceleration voltage of the imaging column in the scanning electron microscope or e-beam lithography tool:

$$\lambda_{\mathrm{el}} = \frac{h}{\sqrt{2m_e \cdot e \cdot V_a}}, \tag{2.2}$$

leading to a wavelength around 10 pm for a 50 kV acceleration voltage. Clearly, the diffraction limit is not the limiting factor of the resolution in e-beam lithography. Practical limits on the resolution are imposed by proximity effects and the used resist and development process. Proximity effects arise from the interaction of the electron beam with the resist and the substrate. Each electron will undergo multiple scattering events, significantly broadening the exposed area of the resist. The point-spread function (PSF) of the dissipated electron energy can be simulated using Monte-Carlo simulations, calculating the trajectories of a large number of electrons. This PSF is modeled as the sum of two (or sometimes three) Gaussians, representing the effects of, respectively, forward scattering in the resist, backward scattering from the substrate, and a combination of other scattering mechanisms [131, 132]. The forward scattering spread has a decay length of the order of several to several tens of nanometers. On the other hand, the backward scattering contribution is spread out over several to several tens of micrometers. An example of the two-Gaussians approximation of the PSF is plotted in Fig. 2.3a, using typical values [131]. Fig. 2.3b shows a schematic drawing of the origin of both contributions. The proximity effect needs to be taken into account when designing critical features that are not isolated on a design. In a photonic integrated circuit with a positive resist, the proximity effect will cause thinning down of features next to large exposed areas. On the other hand, a lower dose factor is sufficient to clear the resist in the middle of a large exposed area. Fig. 2.4 shows the influence

of the dose factor and the proximity effect on a structure, patterned in the positive AR-P 6200.13 resist. The narrow waveguide trenches and corners in Fig. 2.4a are clearly underexposed, however in the center of the larger exposed area, the lower dose factor is compensated by the proximity effect.

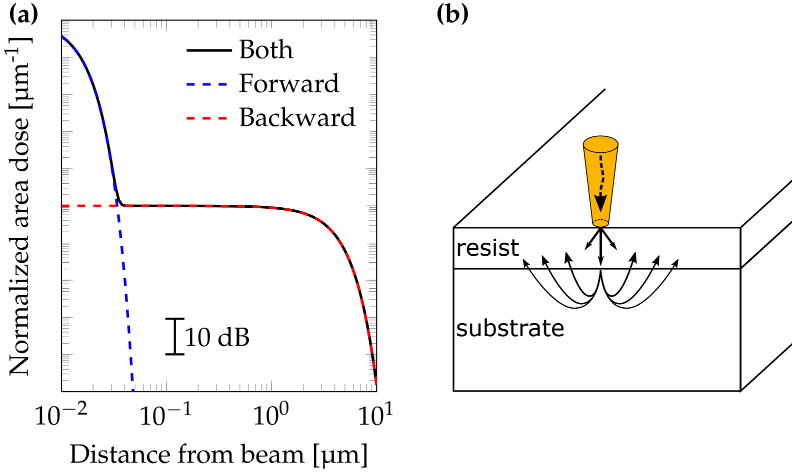


Figure 2.3: (a) Approximation of a typical PSF of the electron exposure distribution using two Gaussians with decay lengths of 10 nm (forward scattering) and 3 µm (backward scattering). (b) Schematic drawing of the origin of the two scattering mechanisms.

The second factor determining the resolution is the combination of the used resist and development process [133]. Two figures of merit are typically used to describe the performance of this step: the sensitivity and the contrast. The sensitivity of the resist is the required electron-beam dose (in units of $\mu C/cm^2$) to achieve the desired effect after development. For a positive tone resist, this means the dose to clear the resist after development, whereas for a negative tone resist it indicates the required dose to prevent dissolution in the developer. The contrast γ of the resist is determined by the highest dose that does not affect the resist after development (D_0) and the lowest dose at which the resist's solubility is completely inverted (D_{100}):

$$\gamma = \frac{1}{\log \frac{D_{100}}{D_0}}. \tag{2.3}$$

A resist with a high sensitivity will have a low D_{100}-value. A higher sensitivity allows for a higher throughput of the patterning. A high contrast

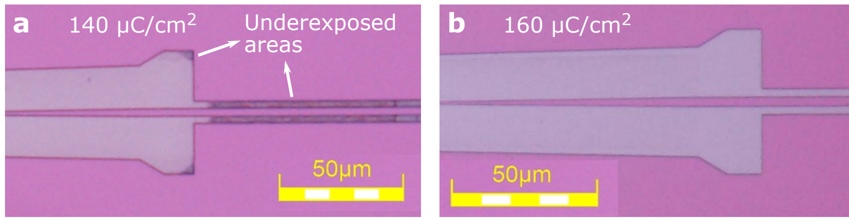


Figure 2.4: Influence of the proximity effect on a structure with large and smaller exposed area, defined in AR-P 6200.13 resist. (a) Structure exposed with a dose of 140 $\mu C/cm^2$. (b) Structure exposed with a dose of 160 $\mu C/cm^2$.

will favour the definition of small features in the design, since the tail of the PSF will have less influence on the developed structure. The parameters to sweep in the optimization process are the area dose, the chosen developer, the development time and the temperature at which the development takes place. Typically, however, the sensitivity and contrast cannot be increased simultaneously and a compromise has to be found [134]. Feature sizes below 10 nm have been reported using polymethylmethacrylate (PMMA) [135] or hydrogen silsesquioxane (HSQ) resist [136]. Sidewall corrugated distributed Bragg gratings (SC-DBRs) with corrugations down to 40 nm are feasible with AR-P 6200.13 before becoming visibly limited by the resolution of the combination of the resist, the patterning, and the development used in this work.

2.4.2 Design adjustments for E-beam patterning

The proximity effect can be counteracted in the software of the E-beam tool, if the PSF of the beam is known for the combination of the used resist and material stack on the substrate. However, the developing and etching process can still alter the size of the designed components. Therefore, rather than counteracting the proximity effect, the effect of the total process (exposure, development and etching) on the feature sizes is studied and counteracted already in the design phase. This is called *mask biasing*. The reactive ion etching (RIE) chemistry based on CF_4, SF_6 and H_2 allows for anisotropic etching with straight sidewalls of a-Si:H, Si_3N_4 and SiO_2. The same behaviour can thus be expected for the waveguides in the a-Si:H and Si_3N_4 layer. In our platform, with fully etched waveguides, trenches of 3 μm are typically used. These thin down the waveguide around 30 nm on each side, as can be seen on the scanning electron microscope (SEM) image of a

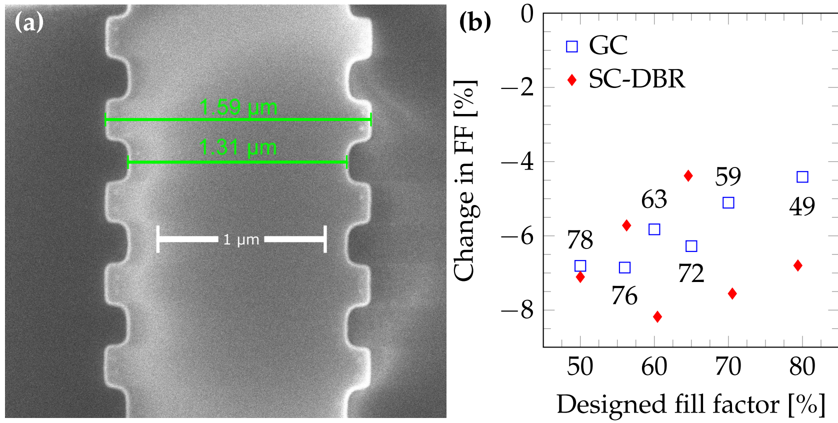


Figure 2.5: Influence of the combination of exposure and development process on the dimensions of the resulting structures. (a) Offset on waveguide width on a distributed Bragg reflector with designed average width of 1.5 µm. (b) Offset on fill factor in grating couplers (GC) with a 1.18 µm period and sidewall corrugated DBRs with a 480 nm period. The numbers in the graph indicate the absolute (positive) change of the width of the etched parts of the grating coupler, in units of nanometer.

DBR grating in Fig. 2.5a. This DBR was designed with a width of 1.5 µm and a corrugation depth of 140 nm. The corrugation depth is preserved, however the average waveguide width is reduced to 1.45±0.005 µm, a reduction of 45-55 nm. For straight waveguides, this is not so critical. Also the influence of this effect on for instance multimode interference (MMI) couplers will be minimal. More care should be taken when designing gratings, directional couplers or ring resonators, and adiabatic tapers with fine tips.

Grating couplers and sidewall corrugated DBRs

For gratings, although the period will remain unaffected, the fill factor will change. For grating couplers on this silicon nitride platform, with a period of 1.18 µm, the fill factor decreases between 4% and 7%, as shown in Fig. 2.5b. The deviation becomes smaller for larger designed fill factors, i.e. when the etched areas become thinner, both relatively and in absolute numbers. For sidewall corrugated DBRs with a period of 480 nm and a corrugation of 100 nm on each side, the trend is less clear. As the corrugation depth decreases, the corrugations become less rectangular. Corrugations down to 40 nm are feasible. For very weak corrugations, different grating designs with ”posts” in the trench can be more suitable [137].

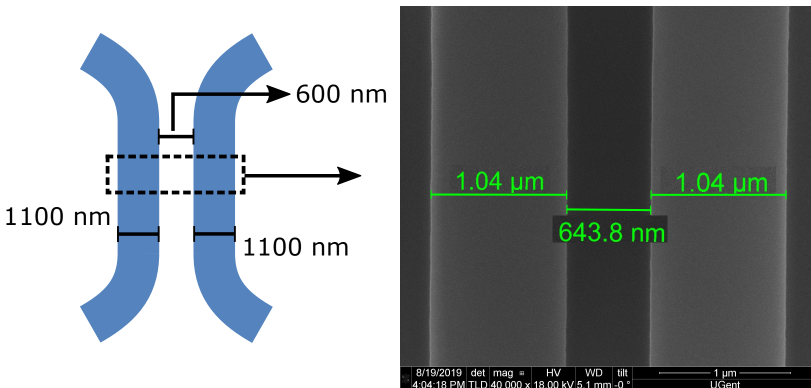


Figure 2.6: Change of dimensions of the waveguide width and the gap in a directional coupler. Left: the designed parameters. Right: measured dimensions on a SEM image.

Directional couplers and ring resonators

In directional couplers or ring resonators, the coupling waveguides will narrow down and their separation will increase. An example of the change in waveguide dimensions and gap size of a directional coupler is shown in Fig. 2.6. The waveguides become 60 ± 5 nm more narrow and the gap is 40 - 45 nm wider than designed. This feedback can be used in simulations for a better estimation of the coupling coefficient.

Adiabatic tapers

Thin taper tips will become thinner than designed. In principle, this is often a helpful feature. However one aspect that should be considered in this case is the adhesion of the resist to the substrate. During development, rinsing or blow-drying, forces are exerted on the developed structures, which can cause them to collapse or deform. Especially long and narrow tapers are at risk for this. The tapers in the a-Si:H layer were initially designed to be 160 µm long with taper tip widths of 120 nm and 150 nm. To allow enough space to pattern the Si_3N_4 waveguide afterwards, a wide window is opened up around the tapers. The effective dose at the boundaries of the taper will be higher than for normal waveguides and the taper tips will be thinned down more than expected, making them too thin to withstand the forces of fluid motion during development. As a result, the taper tips would come loose and bend during development, as shown in Fig. 2.7a.
In general it was found that resist adhesion deteriorates after every cycle

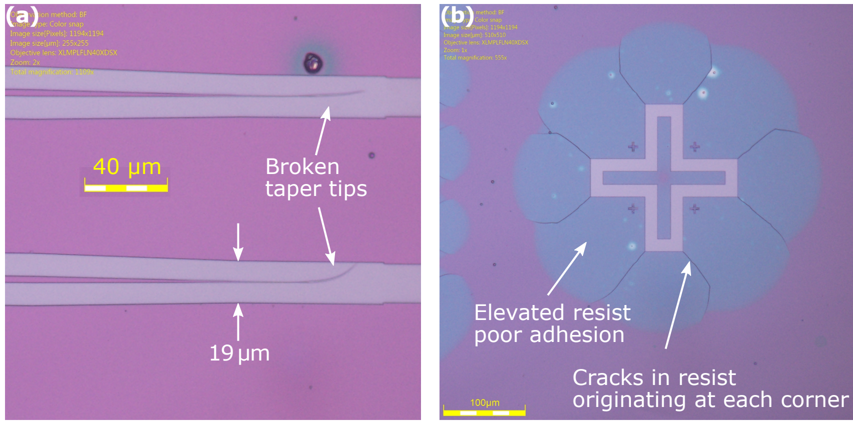


Figure 2.7: (a) Collapsed and bent tapers in the a-Si:H layer, due to proximity effect and poor resist adhesion. (b) Resist coming loose and cracking at each corner due to adhesion problems.

of spincoating, exposure and development. Fig. 2.7b shows a result of a poor resist adhesion on the whole sample. This sample had been exposed once for the definition of the metal markers and twice for the definition of the a-Si:H waveguide layer, including a first failed attempt (shown in Fig. 2.7a). In the purple regions, the resist adhesion is fine. Profilometer measurements showed that in the blue regions, the resist was elevated. At corners of patterned features, cracks would appear in the resist. Some of those cracks could be several hundreds of microns long, allowing whole blocks of resist to shift and destroy the pattern. After experiencing these problems, a 20 minute cleaning step in oxygen plasma (PVA TePla Gigabatch) was introduced to the standard practice before each patterning step.

Two more adjustments were made to the process to improve the reliability of the taper tip patterning in particular. Firstly, the exposure dose was lowered to 140 $\mu C/cm^2$ around the taper tip to compensate the proximity effect of the wide exposed area around the tip, as shown in Fig 2.8a. Only a narrow strip of 1.5 μm at the edges is kept at 160 $\mu C/cm^2$ to avoid underexposed corners such as in Fig. 2.4a. Secondly, the taper tips were no longer designed to be 120 nm or 150 nm, but rather 200 nm wide. This, together with the general adhesion improvement, allows to prevent swaying of the resist during development. The resist is then thinned down in the RIE using a higher pressure oxygen plasma recipe, which etches the resist more isotropically than the original tail-cutting recipe (see Table A.1). The designed tip of

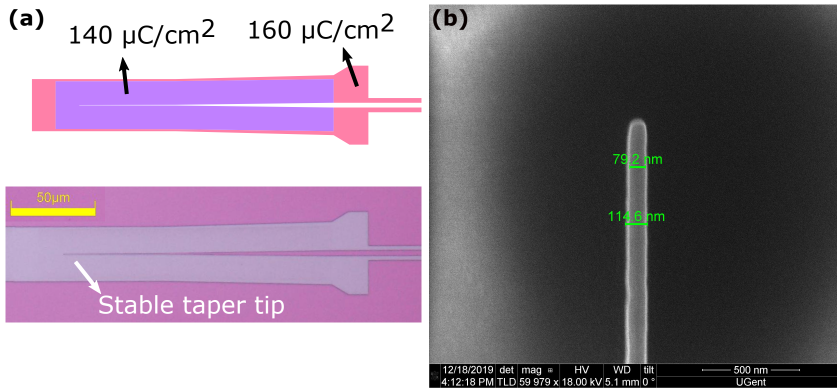


Figure 2.8: (a) Adjustment of the dose factor for the taper definition and microscope image of the patterned taper. (b) SEM image of a stable taper tip after all improvements in the processing and design.

200 nm can be reduced to a width below 120 nm in this way, as shown in the SEM image in Fig. 2.8b. A drawback of this method is that it limits the achievable functionality that can be patterned reliably in the a-Si:H waveguide layer in one exposure step.

2.4.3 Fixed beam moving stage writing mode

In the regular E-beam patterning mode, the beam is deflected within a writefield to all pixels that need to be exposed. As discussed before, the deflection distortion must be minimized in order to obtain a reliable pattern at the edges of the writefield. For structures extending beyond a single writefield, this correction is even more critical, since the circuit can be interrupted at the writefield edge by distortion errors. However even after a successful distortion correction, the patterns crossing the writefield boundary will still suffer from so-called *stitching errors*. This consists of a thin slice of resist at the writefield boundary which did not receive the required dose. Sometimes this effect is reduced or removed by the tail-cutting plasma, but in general it will cause excess losses in the waveguides. This prevents the patterning of long optical delays of more than a few centimeters, which are critical in the design of low-noise laser cavities.
A second patterning mode is available to circumvent this issue: the Fixed beam moving stage (FBMS) mode. In this mode, the beam spirals around its central point with a maximal radius that can be set in the software. The wafer holder underneath then moves the sample continuously, allowing

to pattern structures of centimeters to tens of centimeters long without stitching errors. With a positive E-beam resist, the use of this mode is limited to structures that can be written with a trench of constant width: straight and bent waveguides and tapers. Directional couplers, ring resonators, MMI couplers and gratings all require the regular patterning mode.

2.4.4 Overlay

In order to align the exposures of the Si_3N_4 and the a-Si:H, suitable markers should be added that are clearly visible in the E-beam system during alignment. One method is to deposit metal markers in a first step and align both exposures to the same markers. Metal markers offer a modest contrast, sufficient for high accuracy alignment with < 150 nm offset even when covered by a thick resist layer, as shown in Fig. 2.9a. A drawback is the need for two extra steps (metal deposition and lift-off) to be added to the process. Problems during the lift-off can result in metal particles contaminating the surface to be patterned. A faster method is to add markers in the first exposure step. Since the top waveguide layer (a-Si:H) has sufficient contrast in SEM with the layers below (SiO_2 and Si_3N_4) and since the etch is deep enough, this can also offer a clear contrast in a SEM microscope. However, for the E-beam patterning, the marker will be covered by a thick layer of resist, which strongly reduces the contrast of the marker as shown in Fig. 2.9b. A workaround for this problem is to do first a coarse alignment on these markers and expose the area around them. Subsequently, the sample is taken out of the E-beam system and developed. The dark erosion of non-exposed parts is very limited, allowing to reuse the remaining resist for the patterning of the circuit. After developing, the thin layer of conducting polymer is added again and the sample is loaded in the E-beam system again. Now, the visibility of the markers is no longer reduced by the thick resist layer and the contrast is sufficient for high-accuracy alignment, as shown in Fig. 2.9c. There are two benefits of using the latter method. First, it is faster. It takes approximately 1 hour to go through the process of finding the markers, exposing and developing them and reloading the sample in the Voyager, as compared to the metal deposition and lift-off which requires a full day. Second, the alignment accuracy increases since the markers are automatically aligned with the first exposure, as opposed to the first method where the alignment error accumulates in the subsequent exposures.

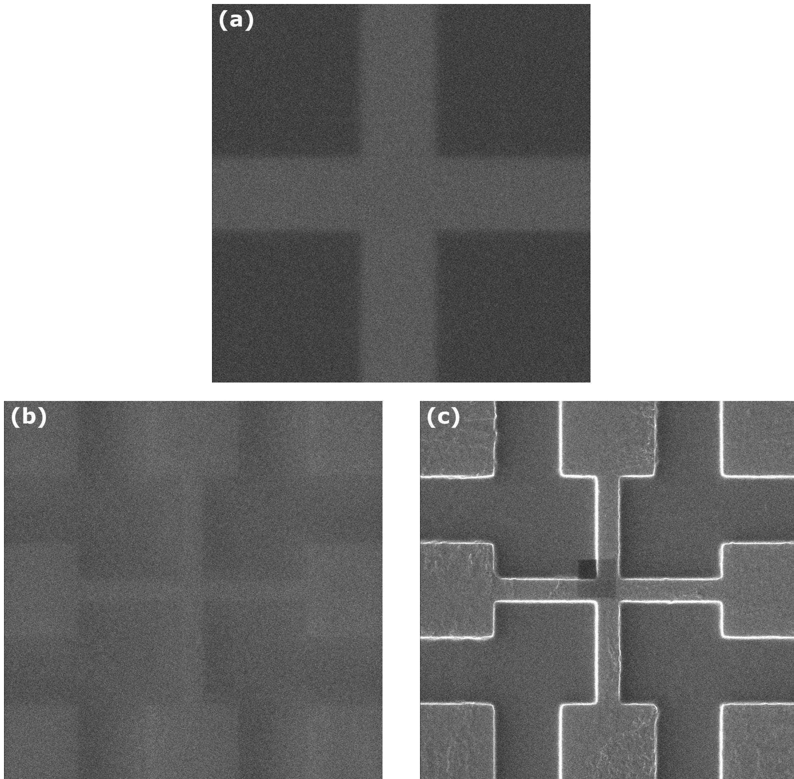


Figure 2.9: Comparison of the visibility of different alignment markers in the Voyager. (a) A 50-nm-thick gold cross on Si_3N_4, covered with a 600-nm-thick AR-P 6200.13 resist layer. This image was recorded with a field of view of 10 µm and a pixel dwell time of 3 µs. (b) A marker etched through a 400-nm-thick a-Si:H layer into the underlying SiO_2 layer with a 600-nm-thick AR-P 6200.13 resist cover. (c) The same marker, without the resist cover. These images were recorded with a field of view of 10 µm, a pixel dwell time of 3 µs and identical contrast and brightness settings.

2.5 Multilayer stack processing

The core material of choice for ultralow-loss integrated waveguides is LPCVD deposited Si_3N_4. The Si_3N_4 material used in this work was purchased from LioniX International [59], which commercially offers 300 nm thick LPCVD Si_3N_4 on 100 mm single-side polished silicon wafers. They are thermally oxidized up to a desired oxide thickness. This thickness should be carefully chosen to simultaneously minimize substrate leakage and the thermal impedance, and maximize grating coupler efficiency at the central wavelength of interest, 1550 nm in our case. For the initial tests on the platform, wafers with a standard oxide thickness of 8 µm were used. For the next wafer batches, the oxide thickness was optimized to 3.3 µm. Following the thermal oxidation, the wafers are loaded in an oven in batches of 10 wafers for the deposition of the silicon nitride layer. A layer of 300 nm Si_3N_4 is then deposited using low-pressure chemical vapour deposition (LPCVD). After the deposition, an extra annealing step at 1150°C in an N_2 environment is done to allow residual hydrogen impurities to escape, reducing the strength of the absorption peak at 1520 nm. The layer thickness uniformity of the LPCVD process is superior to what can be achieved with PECVD processes. A layer thickness map, shown in Fig. 2.10, was constructed from a series of ellipsometry measurements on one of the wafers. The layer thickness is uniform within ± 3 nm on a large part of the wafer.

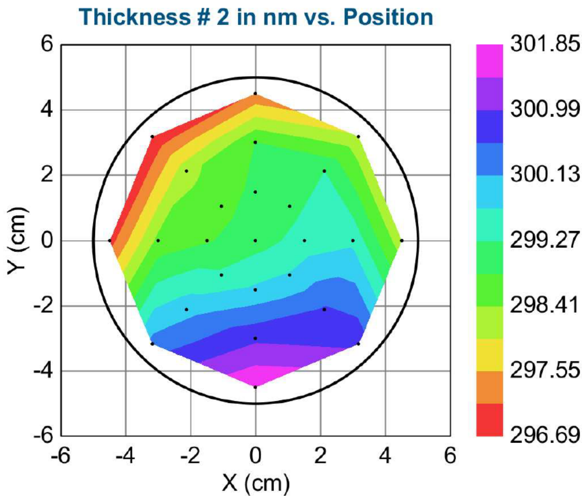


Figure 2.10: Layer thickness uniformity of the LPCVD deposited Si_3N_4.

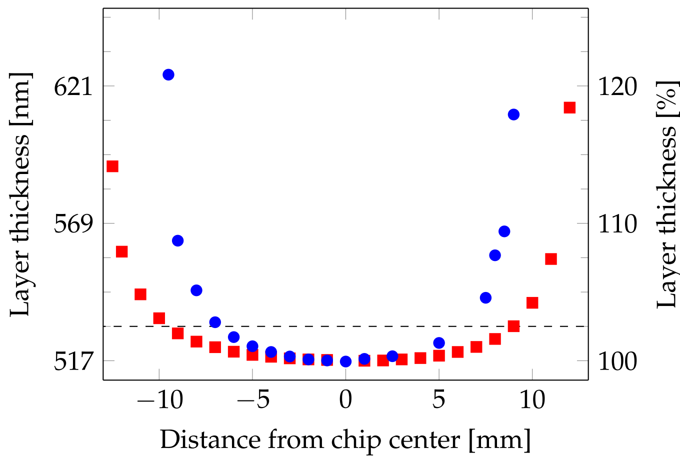


Figure 2.11: Uniformity of PECVD a-Si:H deposition on a 20 x 25 mm^2 sample. The measured thickness on the sample is shown on the left axis. The thickness relative to the center is shown on the right axis. The dashed line indicates a 2.5% deviation, corresponding to 10 nm absolute deviation on a 400 nm target thickness.

The preceding steps are carried out by LioniX International. All further processing is performed in the cleanroom facilities at Ghent University. A wafer dedicated for the multilayer platform is cleaned using a rinse with acetone and IPA, followed by 15 minutes oxygen plasma cleaning (PVA TePla Gigabatch). Subsequently, the wafer is loaded in a PECVD chamber (Advanced Vacuum Vision 310-PECVD). An intermediate layer of silicon oxide is deposited at a temperature of 270°C, prior to the final deposition of the hydrogenated amorphous silicon layer at 180°C. After the layer depositions, the wafer is cleaved into individual samples, typically 25 x 25 mm^2, for further processing. Doing the depositions on wafer scale improves the layer thickness uniformity. Fig. 2.11 shows the relative layer thickness when the a-Si:H is deposited on a sample of 20 x 25 mm^2. For a targeted layer thickness of 400 - 420 nm, it is necessary to stay more than 3 mm away from the sample edge in order to have an absolute deviation less than 10 nm.

In this process flow, all layers are deposited prior to any patterning steps. This allows to avoid tedious planarization steps. The circuit is patterned in a top-down fashion using two electron-beam lithography steps, as shown in Fig. 2.12. In a first exposure step, the a-Si:H layer is patterned. In this step, the micro-transfer printing sites and the tapers for coupling to the

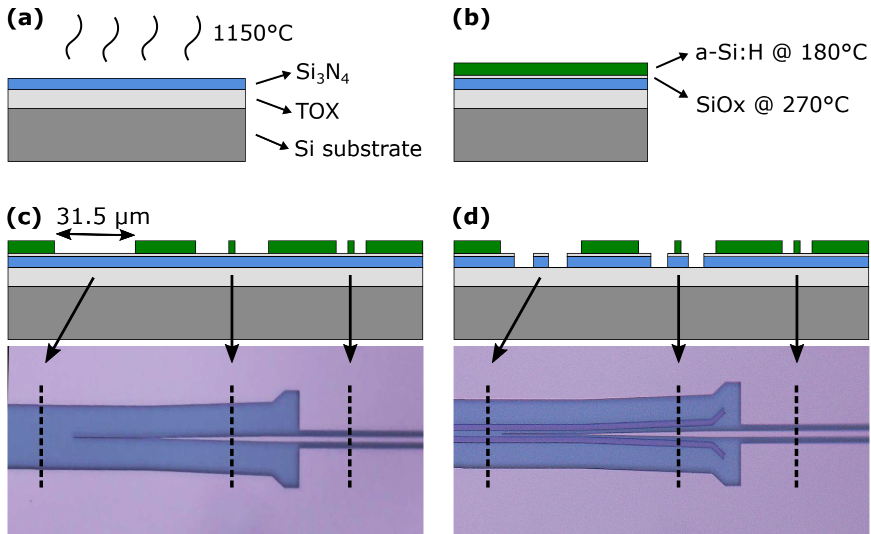


Figure 2.12: Target sample preparation steps and different waveguide cross-sections. (a) Starting stack of LPCVD Si_3N_4 on thermal oxide. (b) Deposition of SiO_2 and a-Si:H layers with PECVD. (c) First exposure and patterning of a-Si:H layer. (d) Second exposure and patterning of Si_3N_4 layer.

Si_3N_4 layer are defined. In the same step, a large area is also cleared where afterwards the Si_3N_4 waveguides will be patterned. The topography of the sample at the micro-transfer printing sites remains flat, apart from the two trenches that define the a-Si:H waveguide. This is needed in order to support the III-V coupon, which is 40 µm wide (as opposed to the a-Si:H waveguide which is 3 µm wide). A 600-nm-thick layer of AR-P 6200.13 resist is used for this step. This accommodates the extra O_2-plasma step for the thinning down of the taper tips (as explained in Sec. 2.4.2) and the overetching of the a-Si:H layer. The etching is done in a reactive ion etcher (Advanced Vacuum Vision 320-RIE). All etching recipes details are given in the appendix, in Table A.1. The a-Si:H waveguide is etched with an anistropic etch recipe. The target is to leave around 30 nm of SiO_2 on top of the Si_3N_4; enough to have a safety margin before attacking the Si_3N_4 top surface, without adding too much extra etching time in the second patterning step. In order to control and monitor the etch depth, 60 x 60 μm^2 squares are added in the design, which can be used for real-time reflectometry during the etching, and profilometry and white light interferometry after the etching.

In the second exposure, the Si_3N_4 layer is patterned. This step typically takes several hours as several multi-centimeter cavities need to be written. The Si_3N_4 features will be located in the etched recesses in the a-Si:H layer. Hence, after aligning the coordinate system in the E-beam software to the markers on the sample, the on-chip beam optimization is done in the 60 x 60 μm^2 squares. The resulting pattern is etched in two steps. First, the remaining oxide is etched away using the anisotropic recipe with SF_6 in about one minute. Then, the silicon nitride is overetched using the anisotropic etch recipe without SF_6. After removing the resist, the sample is cleaned for 20 minutes in oxygen plasma (PVA TePla Gigabatch), and it is ready for the micro-transfer printing process.

The E-beam resist does not follow the sample topography conformally. The actual resist thickness will be higher in the recesses, although the resist cover on features in the middle of a recess will be lower. In order for the process to be repeatable, the resist should be thick enough to protect the a-Si:H pattern. However, even in the case when the taper is etched at the tip, this should not endanger the coupling efficiency. The same spincoating speed as the first exposure is used, resulting in a 600-nm-thick resist layer on the sample surface. This leads to a sufficiently thick cover on the a-Si:H pattern. This can be assessed using white light interferometry and profilometry. The profile of the resist at three points in an a-Si:H taper is shown in Fig. 2.13, indicating that the thickness of the resist decreases significantly towards the taper tip.

It was explained that the first exposure step of the a-Si:H layer requires the patterning of both large areas, where the Si_3N_4 waveguides will come afterwards, and very fine features (i.e. the taper tips). The patterning of the tapers and waveguides requires the use of a low current with a high resolution, in order to obtain a high-quality pattern. However, this would be impractically slow for the purpose of opening up the larger areas. Therefore, the first exposure of the a-Si:H layer is done using two different current modes, one with a low current of 0.45 - 0.5 nA for the high-resolution patterning, and one with a much higher current of 9 - 13 nA to speed up the writing of the larger areas. Both modes need to be calibrated and optimized separately. Either the optimization and alignment process is repeated for each mode, or the modes are internally aligned such that they have the same focal plane. The second method offers some advantages. Using the high-current mode for imaging on the sample can be cumbersome due to excessive charging and even damaging the resist layer. Furthermore it requires a longer active time from the operator. In the second method, both

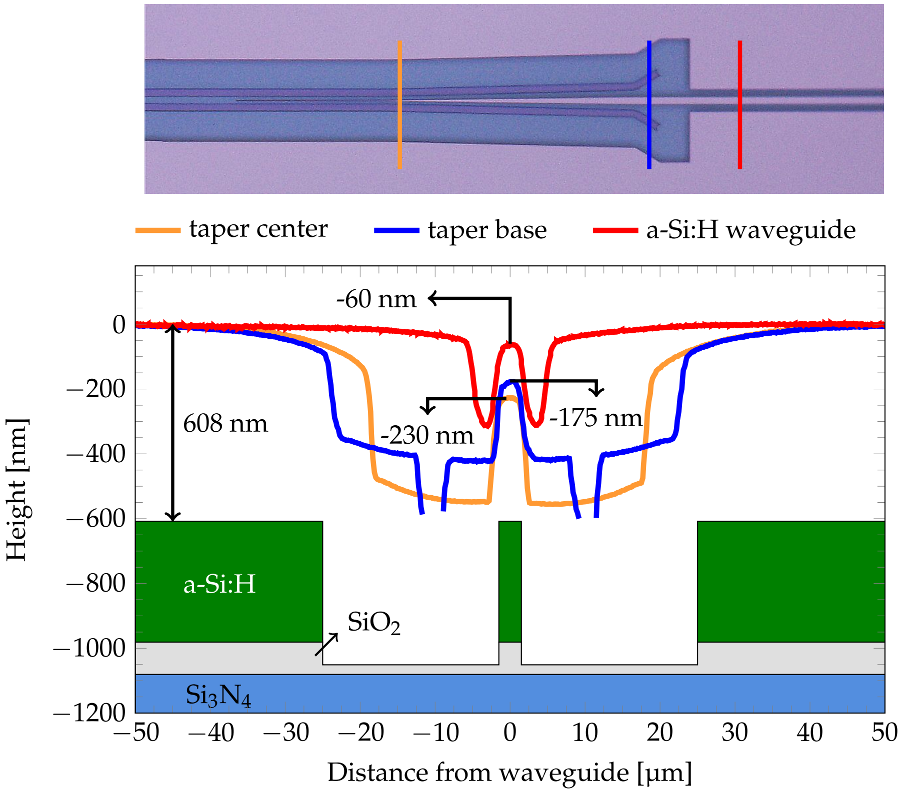


Figure 2.13: Resist cover of the a-Si:H features before the Si_3N_4 etching. The underlying layers are drawn for the cross-section at the base of the a-Si:H taper. The locations of the resist topography measurements are indicated on the image of the taper above.

modes are focused on the same Z-plane consecutively and the settings for the E-beam optics are saved for both of them. A lateral shift in the XY-plane will still be present when shifting between the modes, but this can be also counteracted in the software. The software allows for automatic switching between modes during the patterning. This enables overnight exposures without requiring supervision or intervention from the operator.

2.6 Heterogeneous integration of III-V semiconductor optical amplifiers

The heterogeneous integration process for the semiconductor optical amplifiers (SOAs) has been previously described in [103] and is mostly repeated here. An introduction to the concept of micro-transfer printing was given in Chapter 1.

The process of micro-transfer printing starts with the definition of active devices (referred to as *coupons*) on a III-V wafer (the *source* wafer). These active devices can then be transferred to a non-native substrate, the *target* wafer. The III-V source wafer is densely populated with arrays of SOA coupons of various lengths. Around 1000 SOAs with different lengths fit on 1 cm^2 of the III-V wafer in this design. One source wafer can thus be used to add amplifiers to a great number of target wafers. The layer stack needed for the active devices on the source is epitaxially grown on a 50 nm InGaAs on top of 500 nm InAlAs release layer, which can be etched with a high selectivity against InP (Fig. 2.14a). The definition of the devices starts with the patterning and formation of the III-V SOA mesa and the active region using optical contact lithography and a mixture of dry and wet etch processes (Fig. 2.14b). The sidewalls of the multiple-quantum-well layer and the p-InP mesa are passivated using a layer of PECVD-deposited silicon nitride. A lift-off process is used to deposit Ni/Ge/Au contacts on the n-InP cathode. The wafer is then planarized using divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or BCB). The InGaAs contact layer is opened up and Ti/Au contacts are deposited on the anode. To define the coupon boundaries, the BCB and n-InP layer are patterned in a dry etching step, exposing the release layer next to the coupons. The exposed release layer is patterned and openings are etched down to the InP substrate in a dry etching step. The devices are then covered with a patterned photoresist encapsulation, which is resistant to the release layer etchant (Fig. 2.14c). The photoresist is attached to the III-V substrate with thin tethers, while leaving the release layer accessible for the etchant to be able to underetch

the coupons. The release layer is then etched in a $FeCl_3$:H_2O solution at 7°C, leaving the coupons suspended by means of the encapsulation (Fig. 2.14d). The release layer etch reduces the adhesion strength of the active device to its substrate to the mechanical strength of the weakest point in the tethers. After the release layer etch, the coupons are ready to be micro-transfer printed onto the target wafers.

After processing the source and target samples, the active devices can be micro-transfer printed onto the a-Si:H landing sites. Different amplifier lengths are available. The total coupon size of the longest available amplifier is 1186.5 µm x 47.5 µm. On this coupon, the total length of the active layers is 1148 µm, consisting of a central straight section of 700 µm long and 3.2 µm wide, and two adiabatic tapers, each 224 µm long. The source and target wafers are loaded into an X-Celeprint µTP-100 tool, after spincoating a thin adhesive BCB layer on the target wafer (Fig. 2.14e). A solution of four parts mesitylene and one part BCB 3022-46 is used. An elastomeric polydimethylsiloxane (PDMS) stamp with a single 1200 µm x 50 µm post can be used to pick up a single coupon from the III-V source wafer. The stamp is laminated against a coupon, followed by a rapid upward acceleration, during which the adhesion of the coupon to the stamp increases and the tethers break at their weakest point. This is schematically shown in Fig. 2.14f and the broken tethers are visible on the fabricated device in Fig. 2.15. Printing a coupon on the target wafer happens in the opposite way. The coupon is laminated against the target, after which the stamp is retracted slowly, leaving the coupon behind on the target (Fig. 2.14g). An extra shear force can be applied during the retraction to facilitate the release of the stamp. Both steps are carried out at room temperature. The printing process of III-V devices on photonic integrated circuits typically requires careful alignment. Markers for digital pattern recognition are therefore defined on the source coupon and near the target printing site. The markers on the coupon are visible on the device in Fig. 2.15. State-of-the-art micro-transfer printing tools offer an alignment accuracy of ± 1.5 µm (3σ) for printed arrays and < 1 µm for single coupons at the time of writing. Although the process shown here is sequential, dedicated stamps can be fabricated with posts matching the design of the source and target wafers to parallelize the micro-transfer printing process. After the transfer printing, the photoresist encapsulation is removed and the adhesive BCB layer is cured at 280°C. This is the highest temperature needed for the post-processing of the micro-transfer printed coupons. Afterwards, the sample is planarized with a thick layer of BCB (Fig. 2.14h) and cured again at 280°C.

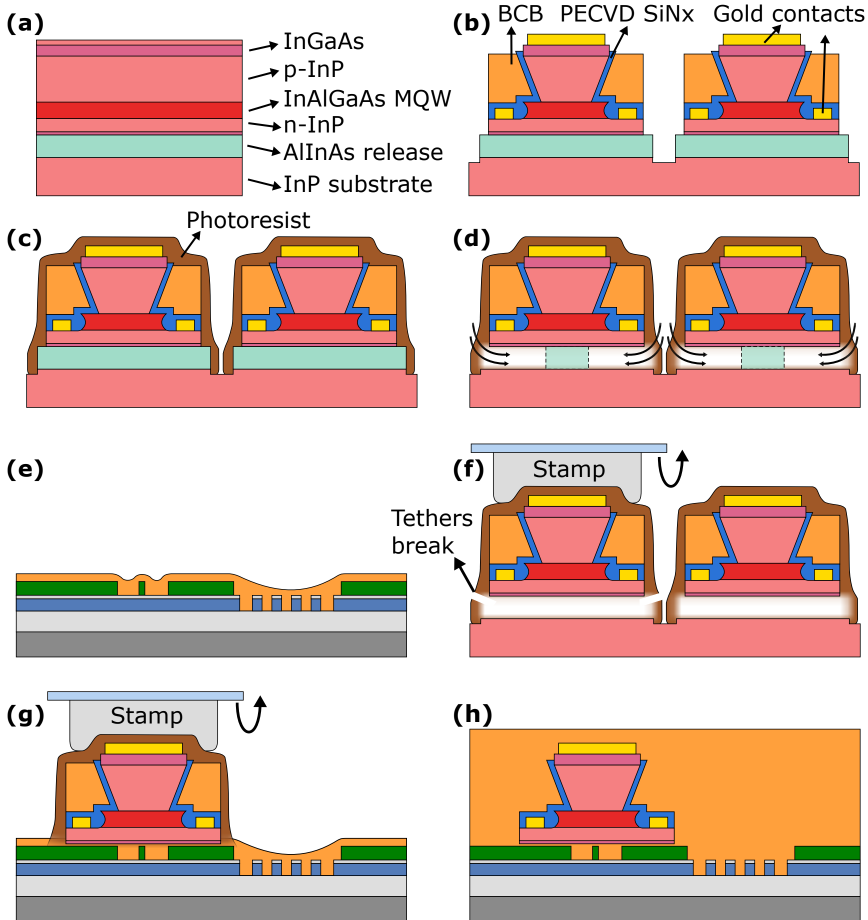


Figure 2.14: Schematic drawing of the heterogeneous integration flow for SOAs on the a-Si:H-on-Si_3N_4 target circuit. (a) III-V epitaxial layers on the source wafer. (b) Device definition on source wafer. (c) Coupon encapsulation with photoresist and tether definition. (d) Release layer etch. After this step, the coupons are ready for transfer printing. (e) Spincoating adhesive BCB layer on target circuit. (f) Coupon picked from source wafer. (g) Coupon printed on target circuit. (h) Strip encapsulation in O_2-plasma and planarize sample with thick BCB cladding layer.

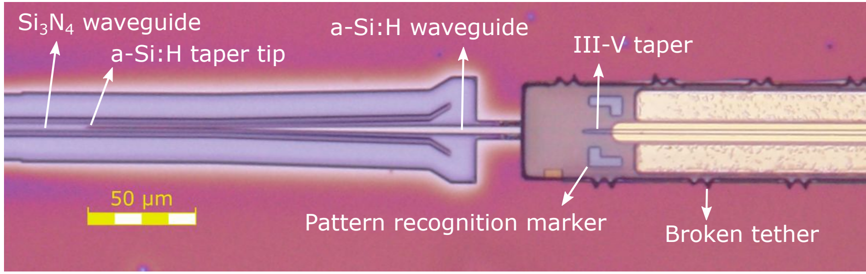


Figure 2.15: Optical microscope image of a micro-transfer printed SOA coupon on an a-Si:H-on-Si_3N_4 circuit.

This integration technique combines the advantages of two established integration approaches: (heterogeneous) wafer bonding [81] and (hybrid) flip-chip integration [76]. Wafer bonding allows for high-throughput integration of active devices on the host substrate, however the dense cointegration of different material stacks is not trivial. Furthermore, the III-V devices can only be tested after finishing the fabrication, leading to a compound yield issue. For flip-chip integration, active devices can be characterized prior to the integration, however typically these devices need anti-reflective or highly reflective coatings on their facets, resulting in a high cost. Furthermore, the pick-and-placing of the devices is a sequential process, lowering the throughput significantly. Micro-transfer printing combines the advantages of both methods. Devices can be fabricated on wafer scale and electrically pre-tested on their native substrate. Dense arrays of active devices can be printed in a parallel way, leading to a high throughput. Additionally, it is possible to cointegrate diverse material stacks in a dense way on a single target substrate. The pre-testing can be done for each individual coupon, provided that it contains sufficiently large contact pads. A faster method consists of estimating the contact resistance of the anodes and cathodes over the whole wafer using transmission line measurements. In this work, the latter method was used for the electrical pre-testing of the coupons.

2.7 Heater definition

In order to tune the lasing frequency of the tunable lasers, heaters are placed above the frequency selective mirrors. These can be DBR gratings, or micro-ring resonators (MRRs). Through the thermo-optic effect, the resonance wavelengths of the mirror are shifted. A tunable laser has two limits to its tunability: the gain bandwidth of its active medium and the maximum

dissipated power in the heaters. For ring resonators, the heater needs only to be able to dissipate enough power to establish a 2π phase shift in the ring. An extra phase tuning element is also needed in the cavity to align one of the laser's longitudinal modes with the resonance wavelength of the frequency selective mirror. Heaters are typically made from a metal with a higher resistance than the contacts. This is to ensure that most of the power is actually dissipated in the heater and not in the metal interconnects. In this work, titanium heaters are used. The failure mechanism of the heaters is rooted in adhesion problems. At elevated temperatures, the heater can locally delaminate from the material below. This in turn increases the local temperature of the heater since the thermal resistance also increases because of the delamination. Finally the delaminated heater burns and there is no more current flow possible. In order to boost the power handling capabilities of the heaters, the choice of the top and bottom cladding around the heater was investigated. The seven different combinations that were tested are listed in Table 2.1. In all combination, a thick layer of BCB of around 2.7 µm separates the heater from the underlying SiO_2 or Si_3N_4 layers. Samples B_1 and B_2 have the same cladding configuration, but on a different substrate.

Type	A	B_1	B_2	C	D	E	F	G
SiO_2 top clad.					■	■	■	■
SiO_2 bottom clad.				■			■	■
BCB top clad.		■	■	■	■			■
Multilayer stack	■	■						
Oxidized Si			■	■	■	■	■	■

Table 2.1: Different combinations of heater claddings.

Ring heaters with a length of approximately 630 µm were tested with all seven cladding combinations. The heaters are identical to the ones used in the laser design, with a width of 5 µm and a radius of around 100 µm.

Experiment 1: Influence of BCB top cladding

The heaters on samples A and B_1 were tested on the multilayer stack, with a BCB layer of around 2.7 µm between the heater and the Si_3N_4 waveguide layer, and a 3.3 µm thermal SiO_2 layer underneath. The heater itself consisted of 100 nm Ti with 15 nm Au on top. The thermo-optic shift of the microring resonances was measured as a function of the dissipated power. Both samples showed a resonance shift of -17 pm/mW. The reso-

nance shows a blueshift since the negative thermo-optic coefficient of the BCB dominates the response. The heaters on sample A burned at 70 mW dissipated power (corresponding to a 1.19 nm resonance shift), whereas the heaters on sample B_1, which had a BCB top cladding, burned only at 120 mW dissipated power (corresponding to a 2.04 nm resonance shift). The power handling capability is clearly improved by adding the top cladding, without a trade-off in efficiency. The free spectral range of the ring is 2.05 nm around 1560 nm, meaning that the heater without BCB cladding cannot provide a 2π phase shift. However, the BCB top cladding may not be a reliable solution when 2π phase shifts are required for longer periods of time.

Experiment 2: Influence of SiO_2 bottom cladding

The other combinations (B_2 till G) were tested on silicon substrates with 3 µm thermal SiO_2 and also around 2.7 µm BCB on top. On those samples, the heaters consisted of 130 nm Ti with 20 nm Au on top. Samples B_2 and C allow to check if a layer of 60 nm SiO_2 below the heater can increase the damage threshold. The result is shown in Fig. 2.16: there is no clear difference in the power handling capacity between the samples with and without a thin SiO_2 layer below the heater. Each voltage level was sustained for 10 seconds before increasing in order not to overestimate the power level at which the heaters burn.

Experiment 3: Combinations with SiO_2 top cladding

Samples D-G all have in common that a layer of $\sim$240 nm SiO_2 is deposited on top of the heater. The samples are loaded into the PECVD at room temperature and brought to the deposition temperature of 270°C after evacuating the chamber. The results of the four different combinations (with/without SiO_2 below the heater, with/without extra BCB on top) is shown in Fig. 2.17. Fig. 2.17a shows the dissipated electrical power as a function of the applied voltage. Each voltage level was sustained for 10 seconds. Fig. 2.17b shows a clear distinction between samples D and E, where the heater is deposited directly on BCB, and between samples F and G, where the heater is completely encapsulated by SiO_2. The former samples still seem vulnerable to burning. This seems to be prevented by the full oxide encapsulation of the heater at least up to an applied voltage of 21 V, which was the limit of the measurement equipment. In this configuration, the resistance of the heater first starts decreasing, then increases up to a power dissipation around 200 mW before dropping again.

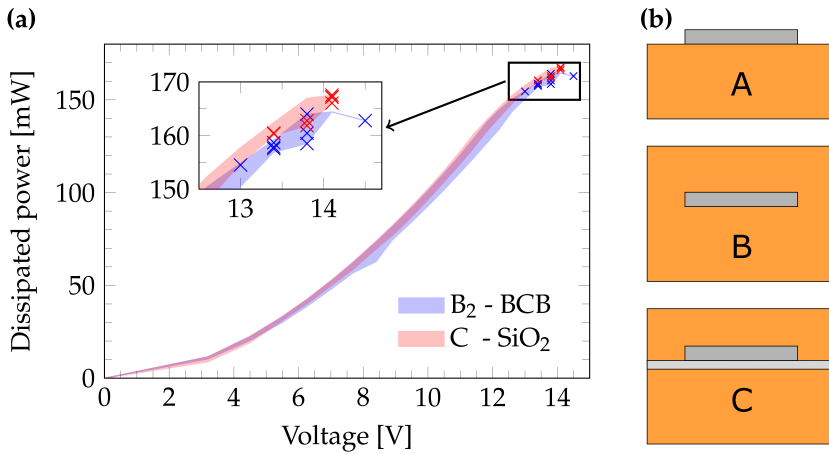


Figure 2.16: (a) Influence of bottom cladding on heater power handling. The shaded areas indicate the data range of the eight heaters on each sample. The cross markers indicate the highest power a heater could reach before burning. Inset: the final range of the data in more detail. (b) Heater cross-sections from the different samples.

The configuration of sample F, with oxide below and above the heater, but without extra BCB, will be used in the final platform. The heaters are placed in a local recess in the BCB cladding, shown in Fig. 2.18a, which allows to place them at an arbitrary distance above the Si_3N_4 waveguide layer. This distance will determine the trade-off between heater efficiency (the induced phase shift per unit of dissipated power) and losses induced by the proximity of the metal to the optical mode. Keeping the excess waveguide loss to a minimum is critical to ensure that the ring resonator mirrors operate as expected.

2.8 Electrical contacting

After the placement of the heaters, the final steps are to open up all electrical contacts (Fig. 2.18b) and to deposit a thick layer of gold (800 nm - 1 µm) for routing and probing (Fig. 2.18c). In order to ensure that the gold layer covers the topography of the sample, the vias to the electrical contacts are defined using a positive lithography process. This allows to reflow the photoresist after developing with a baking step at an elevated temperature, creating slanted sidewalls in the photoresist. This slanted profile is then transferred into the underlying BCB layer, minimizing the risk of an insufficient step

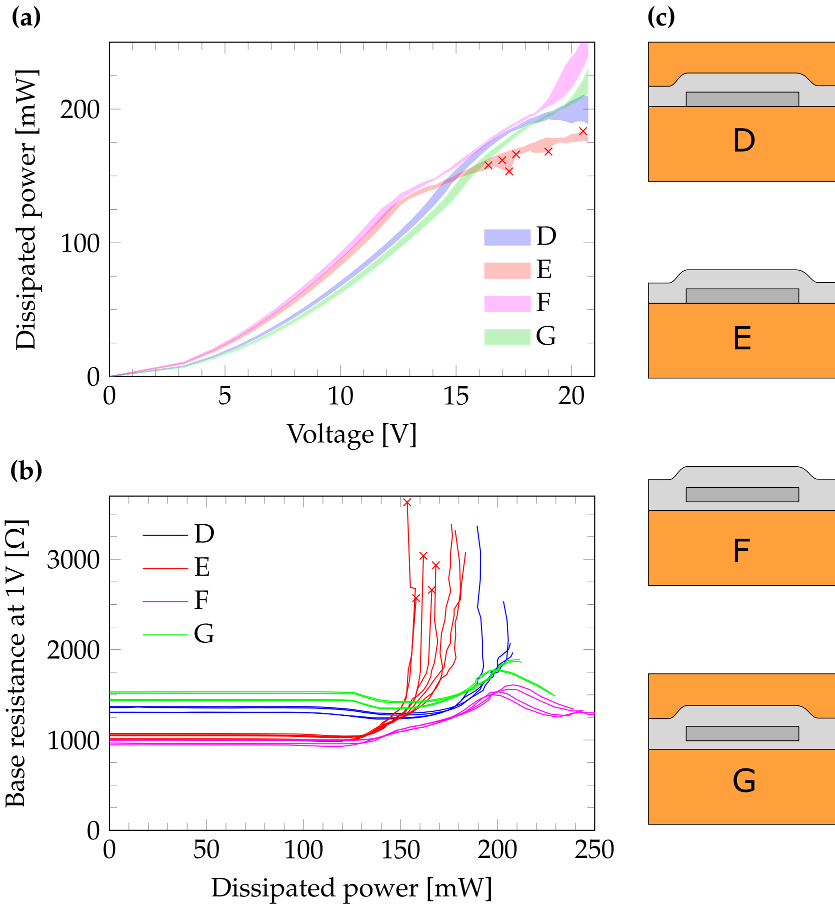


Figure 2.17: Influence of top cladding on heater power handling. The cross markers indicate recorded breakdown points. (a) Power dissipation a.f.o. applied voltage. (b) Resistance change at 1V after each data point. (c) Heater cross-sections from the different samples.

coverage of the metal. Firstly, the shallow vias are defined: the oxide cover of the heaters is locally opened up for electrical contacting, and the BCB cover on top of the III-V amplifier coupons is etched back until the P-contacts are exposed. Afterwards, deeper vias are etched towards the N-contact of the III-V amplifier, and down to the insulating Si_3N_4 layer, onto which the wirebonding pads are placed. The Si_3N_4 layer is chosen for this purpose to avoid adhesion problems during the wirebonding, which could occur when the pads would be placed on BCB. When all vias are opened, a thick layer of gold is deposited and the sample is ready for measurement.

2.9 Future improvements

The process flow as presented here allows for the integration of amplifiers and thermal phase shifters onto a silicon nitride waveguide circuit. Both components have been tested and demonstrated separately. However, an attempt to combine their functionality in order to make a widely tunable laser has failed. Persistent issues with the contact resistance of the amplifiers have made the use of a rapid thermal annealing step an often necessary part of the process flow. In this step, the sample is placed in an H_2/N_2 environment and heated up to a temperature of 380°C or even 430°C for 30 seconds, which sometimes improves the resistance and reduces the self-heating of the amplifiers. The presence of the oxide layer on top of the BCB cladding becomes a risk during such thermal treatments, as the adhesion between the two layers can be unreliable. The oxide layer can delaminate and make further processing on the sample very cumbersome. The heaters themselves seem to survive the high temperatures and they don't delaminate, perhaps because they are placed in a local recess. The delamination should also not have an impact on the waveguide losses, however any grating coupler covered by the delaminated oxide is rendered useless.

Suggestions for future improvement of this process flow are:

- Removing the SiO_2 cladding for the heaters everywhere outside of the local heater recesses.
- Adding electrical contacts to the amplifiers prior to the processing of the heaters to avoid exposing the latter to thermal treatments.

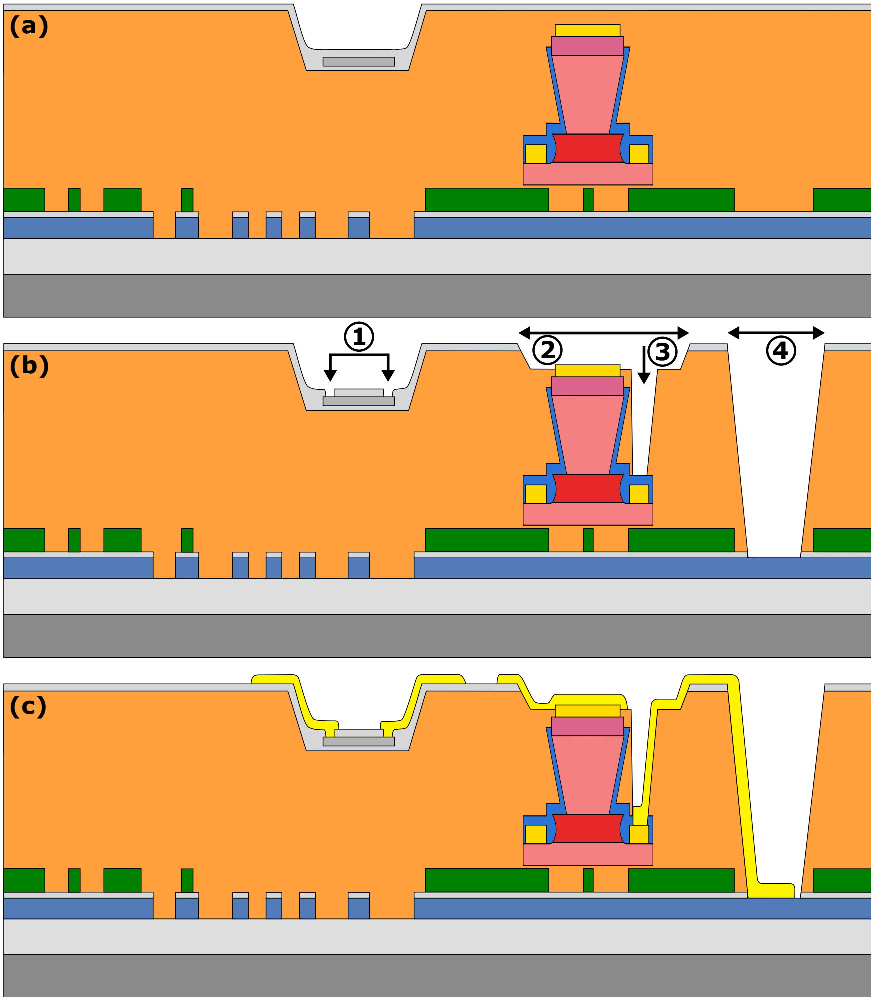


Figure 2.18: Final post-processing on the multilayer platform. (a) Placement of oxide-clad titanium heaters in a recess, at an arbitrary distance from the waveguide. (b) Etching vias for electrical contacting. ① Heater contacts. ② Amplifier P-contact opening. ③ Amplifier N-contact opening. ④ Wire-bond pad opening. (c) Final metallization.

3

Components for multilayer III-V/a-Si:H/Si_3N_4 platform

Bijna weekend!
Monday vibe, E. Vissers, 2018 - present

3.1 Introduction

This chapter deals with the design and characterization of the building blocks of the multilayer III-V/a-Si:H/Si_3N_4 platform that was described in the previous chapter. First, the waveguide losses in both layers are characterized. The influence of the cladding on the waveguide losses is clearly shown. Second, the III-V amplifier coupon is briefly described with some attention to the shape of the taper. As these coupons were developed for a different project, their design was fixed. Given this boundary condition, an appropriate thickness and design for the a-Si:H layer is then chosen, to allow efficient coupling between all layers. The next section zooms in on one critical building block for tunable lasers - ring resonators - and the optimization of their design. Finally, in a thermal analysis, the used material stack is compared to the more commonly used silicon-on-insulator stack.

3.2 Waveguide losses

3.2.1 a-Si:H waveguide losses

For the initial feasibility study, the waveguide losses of as-deposited a-Si:H were measured. A 500-nm-thick layer was deposited on a silicon substrate with 3 µm thick layer of thermal oxide. To distinguish between the losses arising from sidewall scattering and those originating from bulk defects and the top surface, two experiments are done. In a first experiment, narrow (650 nm wide) waveguides are swept in length. Secondly, the waveguide width is swept for a fixed waveguide length of 3 mm. The results are shown in Fig. 3.1. The losses in narrow 650 nm wide waveguides are remarkably high, estimated at 23-25 dB/cm. For single-mode waveguides (350 nm wide), the losses are even higher. However, the losses drop significantly for waveguide widths exceeding 2 µm. This indicates that the sidewall roughness is prohibitive for components in the a-Si:H layer requiring single-mode waveguides. Even for very wide waveguides, the waveguide loss remains around 5 dB/cm, indicating a contribution from top surface scattering, bulk scattering on voids and defects, and potentially absorption losses. The precise origin of the losses has not been investigated, nor has an attempt been made to reduce the top surface scattering through chemical-mechanical polishing (CMP), since for the envisioned devices there is only a need for wide a-Si:H waveguides of less than 2 mm, limiting the propagation loss in those waveguides to around 1 dB.

3.2.2 Si_3N_4 waveguide losses

The optimal waveguide geometry and technology depends on the application. For routing, higher index contrast waveguides with tighter bending radii are more suitable. On the other hand, reducing the index contrast and having a large optical mode (in non-absorbing materials) is the best way to avoid the onset of nonlinear effects and to obtain low propagation losses if the roughness on the core/cladding interfaces cannot be sufficiently minimized [127]. In order to obtain high quality factor resonators with high confinement Si_3N_4 waveguides, surface roughness must be addressed [49]. Integrated photonic platforms more often than not include a top cladding layer covering the waveguides. A top cladding protects the circuit from contamination such as dust or humidity, and can also be used to add extra functionality to the platform. For instance, heaters can be placed above the waveguide without inducing too many losses, and metal contacts can easily be rerouted to wire bonding pads. For low-loss waveguide platforms, a high quality top cladding is important. Even though a top cladding will reduce

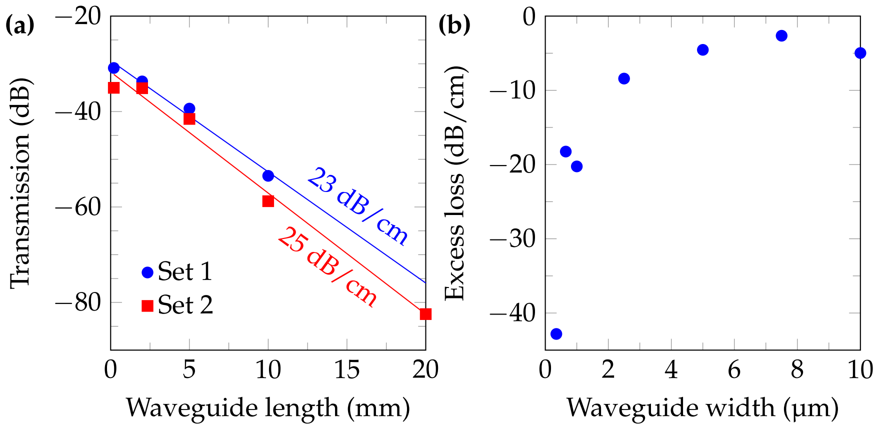


Figure 3.1: Waveguide losses in the a-Si:H layer. The a-Si:H thickness was 500 nm in this experiment. (a) Length sweep of 650 nm wide waveguide. (b) Sweep of the waveguide width, with a fixed waveguide length of 3 mm.

scattering losses from the sidewalls and top surface of the waveguides, it may add absorption losses. The ideal claddings in terms of absorption are thermally grown silicon oxide, or LPCVD deposited silicon oxide. Silicon nitride waveguides clad with these oxides have been demonstrated with losses down to below 1 dB/m around 1550 nm [127]. This ultra-low loss was limited by absorption features corresponding to the overtone of a resonance of an N-H bond, originating from the silicon nitride. In deposited oxide claddings, residual hydrogen impurities cause absorption losses if they are not removed through thermal annealing steps. Another more exotic solution is to use precursor gasses where the hydrogen is replaced with deuterium. The difference in atomic mass shifts the wavelengths of the absorption features away from the wavelength region around 1550 nm [128].

For the characterization of the silicon nitride layer, the waveguide losses are first measured without cladding, to assess the sidewall roughness and the material quality. Three sets of waveguide spiral pairs of 2 cm and 12 cm long are used to extract the propagation loss in the waveguides. The waveguides are 1.5 µm wide and support only one quasi-transverse electric (TE) mode. All spirals have the same number of 90° bends, so all excess loss in the long spirals can be attributed to 10 cm of straight waveguide. A measurement of the propagation loss of unclad waveguides, before and after the wafers were annealed at 1150°C, is shown in Fig. 3.2a. An absorption peak at 1520 nm originating from the hydrogen impurity is clearly present in the material before annealing. Further away from the absorption peak,

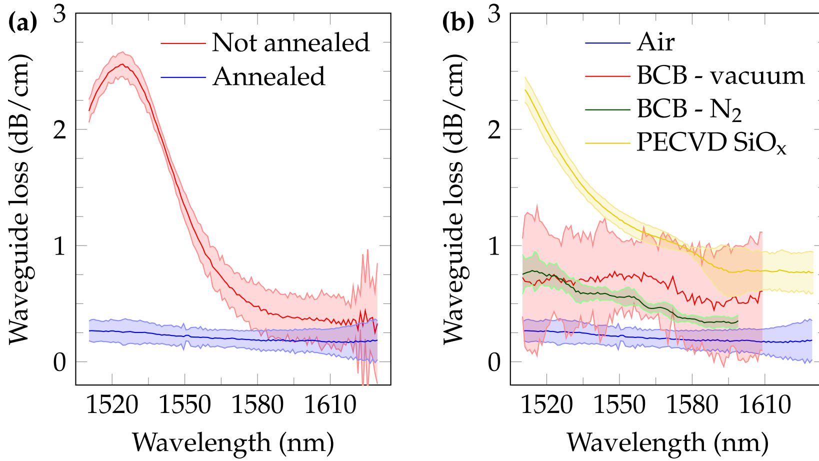


Figure 3.2: Influence of (a) annealing and (b) cladding on the propagation losses in fully etched 300-nm-thick LPCVD Si_3N_4 waveguides. The shaded areas indicate the 95% confidence interval.

the propagation losses saturate at a value of around 0.35 dB/cm, whereas the loss in the annealed material is 0.22 $\pm$ 0.05 dB/cm, almost independent of the wavelength.

The available top claddings in our cleanroom at the time of this work were PECVD deposited silicon oxide with a silane precursor, and DVS-BCB. BCB is a polymer that is applied to the sample through spincoating, followed by a curing step. The curing step takes place in an oven, in which the temperature is ramped up to a desired temperature (280°C in this work) over the course of a few hours, to let the solvent evaporate from the BCB before the onset of the vitrification of the polymer. After the curing, the BCB layer has a refractive index of 1.54. The atmosphere in which the curing takes place influences the BCB's properties. Curing in an atmosphere containing oxygen can cause oxidization of the BCB [138]. Since the used oven cannot be evacuated sufficiently to prevent this, the effect of purging the atmosphere with N_2 during the curing was also investigated. The waveguide losses measured with these claddings are shown in Fig. 3.2b. The (single-mode) waveguide width in BCB cladding is 1.5 µm, whereas it is 1.1 µm for oxide-clad waveguides. The first cladding to be investigated was BCB, cured in vacuum, since this was commonly used in the processes for heterogeneous integration on silicon-on-insulator (SOI). This cladding yielded an estimated loss of 0.6 - 0.7 dB/cm. This measurement, unlike the others reported here,

was done using several waveguides of 1 cm, 2 cm, 4 cm and 8 cm, resulting in wider confidence intervals. The measurement of the loss of the BCB, when cured in a nitrogen-purged atmosphere, resulted in a more accurate estimate. The addition of nitrogen appears to lower the base loss to around 0.35 dB/cm. However, it introduces an absorption peak around 1520 nm, which increases the losses to about 0.75 dB/cm. The PECVD deposited oxide results in the highest base loss and furthermore contains a strong absorption feature at a wavelength below the measured range. Moreover, thicker layers (around 1 µm) exhibited a significant roughness on the top surface, in the form of sharp spikes of 50-100 nm high. An attempt was made once to investigate if a thermal annealing step at 900°C for several hours could improve the losses, however instead they increased to about 6 dB/cm. This cladding was not investigated further.

3.3 III-V semiconductor optical amplifier

The III-V waveguides used in this project are described in detail in [139], where they were integrated on a 400 nm SOI platform. Its layer stack consists of multiple InAlGaAs quantum wells (MQW), sandwiched between n-doped and p-doped indium phosphide (InP), respectively below and above the quantum wells. The III-V waveguide taper was designed to be tolerant to lateral misalignment. Two taper designs were made: one for full coupling, with a double inverted taper, and one for partial coupling, where the silicon waveguide has a constant width throughout the whole III-V coupon length. Simulations indicate that the design with a partially coupled III-V waveguide tolerates more misalignment and generally gives a higher coupling efficiency. For this reason and for simplicity, the a-Si:H waveguide in this work also keeps a constant width. A microscope image of a transfer printed coupon (Fig. 3.3a) shows the transition region from the a-Si:H to the III-V waveguide. First, the a-Si:H mode hits a 260 nm thick slab of n-InP, followed by the tapered stack of the MQWs and the p-InP. The latter is called the III-V 'mesa'. Schematic cross-sections of the different stacks are shown in Fig. 3.3b. The shape of the mesa taper is shown in Fig. 3.3c. The tip is designed to be 500 nm wide. A cross-section of a transfer printed amplifier coupon on an a-Si:H waveguide with a constant width of 3 µm is shown in Fig. 3.3d. The amplifier has a lateral offset of around 600 nm.

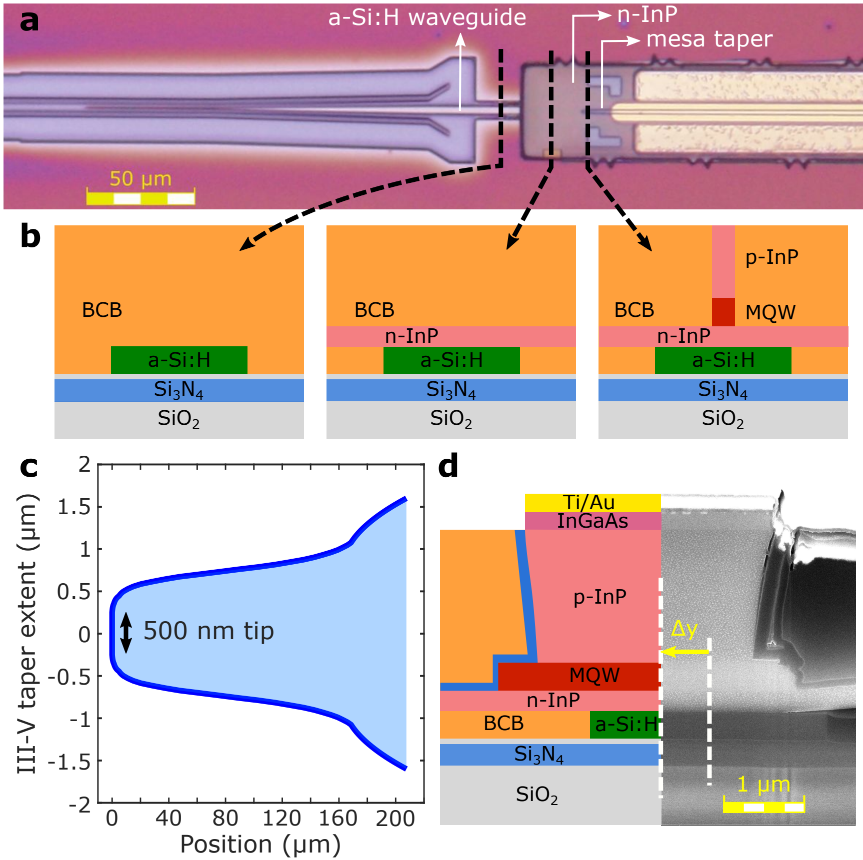


Figure 3.3: (a) Microscope image of a transfer printed III-V waveguide on an a-Si:H waveguide. (b) Schematic drawing of the different cross-sections in the a-Si:H-III-V transition. (c) Shape of the III-V waveguide taper, from [139]. (d) Focused ion-beam cross-section at the center of a III-V waveguide transfer printed on an a-Si:H waveguide, with a schematic overlay. The dashed white lines indicate the extent of the lateral misalignment Δy.

3.4 Choosing the thickness of the a-Si:H layer

The targeted thickness of the intermediate layer of hydrogenated amorphous silicon is subjected to boundary conditions, both in the design and in the fabrication. In Chapter 2 it was already explained that mechanical deformation of the E-beam resist imposes a lower limit on the achievable taper tip widths. This lower limit will be higher when the resist layer is thicker, as the aspect ratio of the resist feature cannot increase indefinitely. The a-Si:H layer can hence not be too thick as this would hamper the taper definition. As the refractive index of PECVD-deposited a-Si:H is expected to be around the same value as crystalline silicon, a thin a-Si:H layer will be beneficial for coupling to and from the Si_3N_4 layer. On the other hand, a thicker layer will cause less losses in the transition towards the III-V component.

The experimental determination of the refractive index of the deposited a-Si:H layer initially had an confidence interval of 1.4%, leading to an estimation between 3.35 and 3.4. This small error does not significantly alter the design of the Si_3N_4-a-Si:H transition, but it can have a large impact on the transition to the III-V waveguide. Also the confinement in the final hybrid a-Si:H/III-V mode, and hence on the expected gain per unit length, are affected by this parameter. Figure 3.4 shows the coupling efficiency from the a-Si:H mode to the mode at the III-V taper tip for different thicknesses and widths of the a-Si:H waveguide. The colored regions indicate the uncertainty of a-Si:H's refractive index between 3.35 and 3.40. The coupling efficiency is calculated as the product of the transmission of the a-Si:H mode at the n-InP slab and the transmission at the III-V taper tip (see Fig. 3.3b). Based on this simulation, the constant a-Si:H waveguide width can be set to be 3 µm. As expected, thicker a-Si:H layers with higher refractive indices result in a better coupling to the III-V mode at the tip. The a-Si:H layer thickness should be around 400 nm or more to avoid too many losses at these interfaces, as this can also result in higher spurious reflections, which can destabilize the amplifier.

The reported confinement in III-V amplifiers bonded on SOI by Van Gasse et. al. was 0.7% per quantum well [86]. This value allowed for high output powers over 50 mW with up to 27 dB gain. To be on the safe side, the chosen a-Si:H thickness should allow for higher gain to compensate the losses occurring in the transitions. The simulated confinement per quantum well (QW) for varying a-Si:H thicknesses and refractive indices are shown in Fig. 3.5 for BCB bonding layer thicknesses of 20 nm and 40 nm. From previous experience, it is expected that the BCB bonding layer will not exceed 40 nm.

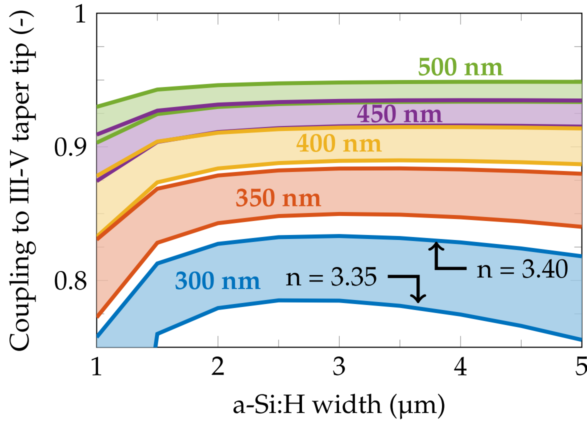


Figure 3.4: Coupling efficiency between the a-Si:H mode and the III-V waveguide taper tip, calculated as the product of the power coupling at the n-InP edge and at the mesa taper tip.

The a-Si:H waveguide width is fixed here at 3 µm. A thickness of around 400 nm would lead to a confinement per QW higher than 0.9% within the uncertainty of the refractive index of the a-Si:H, for the expected BCB bonding layer thickness, and with some tolerance on the precise deposited thickness. The dashed/dotted lines indicate how the confinement changes upon lateral misalignment of the a-Si:H waveguide and the SOA coupon and shows that this will not lead to a problematic decrease in confinement.

3.5 Interlayer taper between Si_3N_4 and a-Si:H waveguides

The transition between the Si_3N_4 and the a-Si:H waveguide layer is done using a piecewise linear taper. A schematic depiction of the used taper design is shown in Fig. 3.6. In the first part of the taper, the mode shape changes significantly as the light moves up to the a-Si:H layer. It is therefore important to make this transition long enough in order not to excite higher order modes or the odd supermode. The second part consists of a mere adiabatic broadening of the a-Si:H waveguide to reduce the scattering loss of this waveguide. The tip of the taper should be narrow enough to avoid scattering, while remaining reproducible. In Section 2.4.2, it was shown that taper tip widths of 100 - 120 nm are still stable and reproducible albeit with some uncertainty of the width. The refractive index of the a-Si:H is set

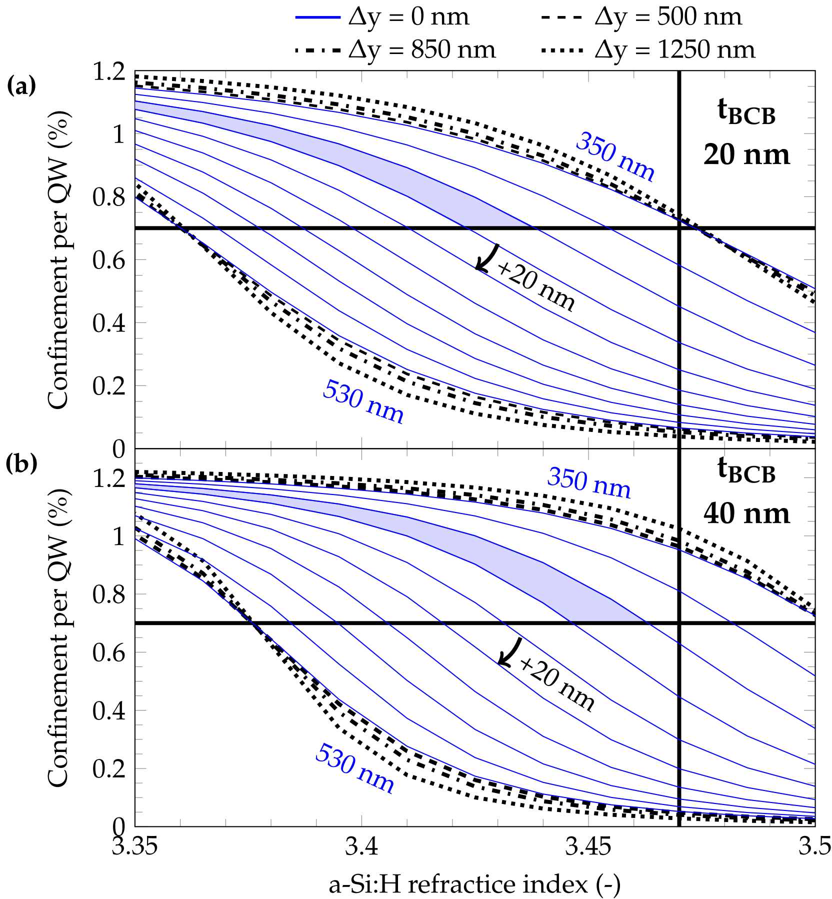


Figure 3.5: Dependence of the confinement of the hybrid a-Si:H/III-V mode in the amplifier on the thickness and refractive index of the a-Si:H layer for a BCB bonding layer thickness of (a) 20 nm and (b) 40 nm. The full blue lines indicate the confinement for increasing a-Si:H thicknesses with 20 nm increments. The black dash(-dotted) lines indicate how the behaviour changes upon lateral misalignment of the SOA coupon. The thick horizontal line indicates a confinement of 0.7%, as reported by Van Gasse et. al. [86]. The thick vertical line indicates the refractive index of crystalline silicon. The blue shaded areas indicate where the target thickness of 400 nm ±10 nm gives a confinement above the minimal value of 0.7%.

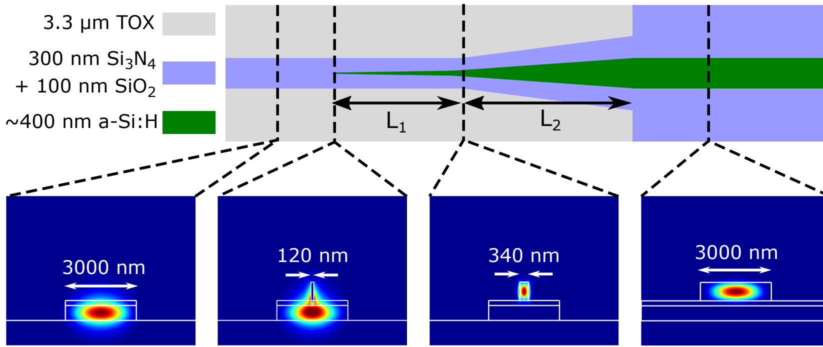
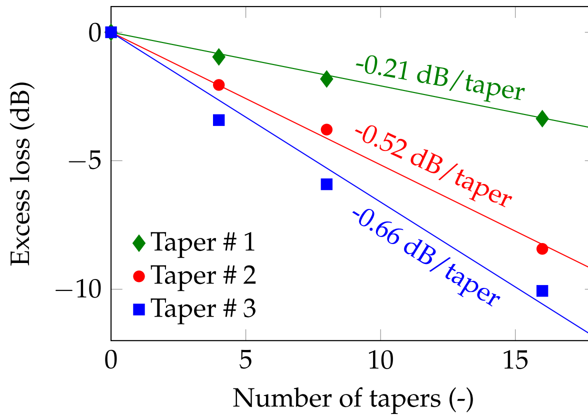


Figure 3.6: Layout of the interlayer taper between the Si_3N_4 and the a-Si:H layer.

at $n = 3.4$ in the design. The modal overlap of the fundamental mode at a 120-nm-wide taper tip is 98.6% with a 100 nm SiO_2 spacer layer on the Si_3N_4, and 96.7% without the spacer layer. The reflection of the taper tip was simulation using 3D finite-difference time-domain (FDTD) simulations, assuming perfect alignment of the taper to the Si_3N_4 waveguide. On the side of the Si_3N_4 waveguide, -50 dB is reflected back into the fundamental TE mode. In the a-Si:H waveguide, the reflection is -41 dB. When the a-Si:H waveguide becomes 340 nm wide, the mode has transitioned completely from the Si_3N_4 to the a-Si:H. This is the first part of the linear taper with length L_1, as indicated in Fig. 3.6. In a first design, this parameter was fixed at 60 μm, followed by an adiabatic broadening length L_2 of 100 μm. Eigenmode expansion (EME) simulations show that this configuration leads to a coupling efficiency (within the a-Si:H taper) over 99% , for lateral taper misalignments up to 200 nm.

The losses of the transition, as shown in Fig. 3.7, were measured after the full platform processing, using several identical Si_3N_4 waveguides with increasing numbers of pairs of a-Si:H tapers on them. Measurements of two varieties of the taper, with a different tip width, indicate that the loss per 60 μm + 100 μm long taper is 0.52 dB/taper when the tip was 100 nm, and 0.66 dB/taper with a 120 nm wide tip. The influence of the width of the tip is clearly noticeable, however the losses still appear to be limited by scattering on the rough a-Si:H. The best way to reduce the losses is to keep the taper as short as possible, on the limit of adiabaticity. A shorter design, with L_1 and L_2 both 30 μm long and a tip width designed to end up



#	Tip	L_1	L_2
1	100 nm	30 µm	30 µm
2	100 nm	100 µm	60 µm
3	120 nm	100 µm	60 µm

Figure 3.7: Measured excess loss per taper, extracted from identical Si_3N_4 waveguides with increasing numbers of taper pairs at fixed intervals. The table below summarizes the dimensions of the tapers as shown in Fig. 3.6.

at 100 nm, offers a significant improvement. The measured loss per taper was reduced to 0.21 dB, corresponding to a total transmission over 95%.

3.6 Ring resonators

A simple, yet powerful component in photonic integrated circuits is the ring resonator. Topologically it can be seen as a directional coupler where one of the outputs is redirected to one of its inputs, resulting in a cavity with a small footprint. At resonant wavelengths, optical power builds up in the ring and a dip occurs in the transmission spectrum, accompanied by a nonlinear phase shift. Ring resonators can be used for channel filtering in wavelength-division-multiplexing (WDM) systems [140, 141], for optical modulators [142, 143], to create optical time delays [144, 145], or for sensing applications [146–148]. Furthermore, they are an essential component to achieve integrated, tunable and low-noise lasers [68, 69, 100, 149–151]. When low propagation losses can be achieved, the intensity of light can be enhanced by several orders of magnitude in a near-critically coupled ring. This property can be taken advantage of to enhance e.g. nonlinear

effects [49,152,153] or the sensitivity of optical biosensors, while keeping a small footprint [146]. A disadvantage of ring resonators is that they are very sensitive to interwafer and intrawafer variations in the device layer thickness and the coupler geometry, which can result in a varying optical response between topologically identical devices, especially on high-index-contrast platforms such as silicon-on-insulator [154].

3.6.1 Parameter extraction from ring resonators

Ring resonators can also be used as a compact test to assess waveguide losses, if the excess losses arising from radiation and scattering at the coupler are negligible. It is important to have a model to estimate the coupling to and from the ring resonator and the losses in each roundtrip. The two most common configurations of the ring resonator are the all-pass filter (APF), where the resonant frequencies are dissipated in the ring, and the add-drop filter (ADF), where part of the resonant frequency power is coupled out to another waveguide. These two topologies are shown in Fig. 3.8. All-pass filters are the easiest to characterize, so they are ideally suited to create a model for the coupling coefficient and to assess the waveguide losses. The transmitted power through an all-pass ring resonator (or *notch* filter) is [154]:

$$T_n = \frac{a^2 - 2ra\cos\phi + r^2}{1 - 2ar\cos\phi + (ra)^2}, \tag{3.1}$$

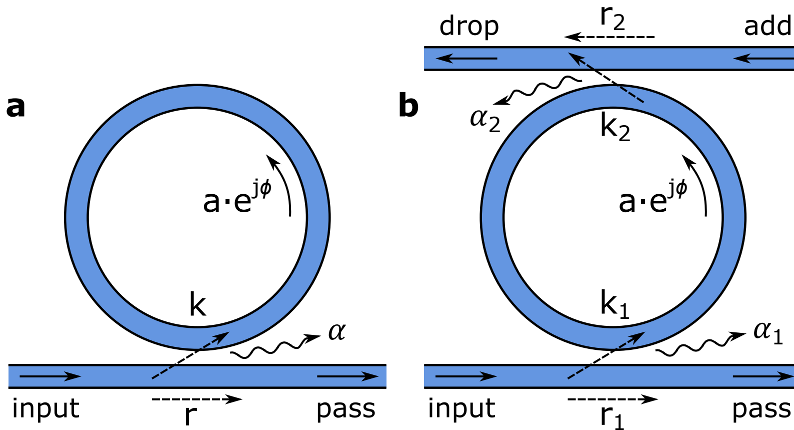


Figure 3.8: Schematic drawing of (a) an all-pass filter and (b) an add-drop filter, with their relevant parameters and port names.

where a is the amplitude loss per rountrip, r is the amplitude transmission - or self-coupling coefficient - at the bus-ring coupling section, and ϕ is the accumulated phase over one roundtrip in the ring. When the accumulated roundtrip phase at a certain wavelength is a multiple of 2π, constructive interference occurs and the light intensity builds up in the ring at that wavelength. The fraction of this light that couples out to the bus waveguide will interfere destructively with the transmitted field, resulting in a dip in the transmission. This is shown in the measurement of an APF ring resonance in Fig. 3.9a. The width of the resonance decreases with lower roundtrip losses or lower cross-coupling. When the roundtrip loss and the transmission coefficient are exactly equal, the power build-up in the ring is maximal and the transmission at resonance drops to zero. An extra loss factor α is drawn in the schematics of Fig. 3.8 at the coupling section. This serves as a reminder that the losses in a ring can have different origins. For instance, excess losses at the coupler, such as mode conversion losses, will be absorbed in the factor a during the data fitting, potentially leading to an overestimation of the actual propagation loss in the ring. Other imperfections at the coupler can also occur, such as the two local supermodes experiencing a different loss. This can cause a distortion of the resonance shape [155].

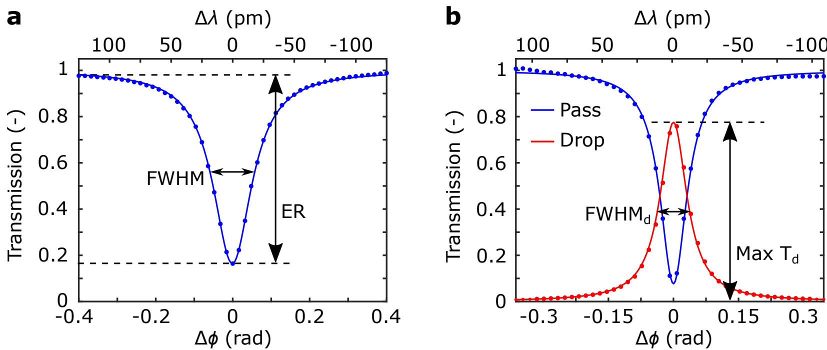


Figure 3.9: Measured and fitted response of (a) an all-pass filter and (b) an add-drop filter, with some spectral features of interest. FWHM: Full-Width at Half-Max; ER: Extinction Ratio; T_d: transmission at the drop port.

The counterpart of r is k, the cross-coupling coefficient. This can be related to the coupling constant of the ring and bus waveguide in the same way as for a directional coupler:

$$|k|^2 = \sin^2(\kappa_0 + \kappa L), \tag{3.2}$$

where L is the straight length of the coupling section, with a unit-length coupling coefficient κ, and κ_0 accounts for the spurious coupling in the bends near the coupling section. Coupling sections with a high wavelength dispersion will result in resonators with a very wavelength-dependent behaviour.

In order to extract useful information from the measurements of these rings, the wavelength and the roundtrip phase in the ring need to be linked to each other, such that Eq. (3.1) can be used. For a ring resonator with length L, we can write the following expressions for the roundtrip phase:

$$\phi = \beta \cdot L = \frac{2\pi n_{eff}}{\lambda} \cdot L \tag{3.3}$$

$$\phi_{res} = 0 = \frac{2\pi n_{eff,0}}{\lambda_0} \cdot L \tag{3.4}$$

$$\Rightarrow \phi - \phi_{res} = 2\pi L \left(\frac{n_\lambda}{\lambda} - \frac{n_0}{\lambda_0} \right) = 2\pi L \frac{\lambda_0 n_\lambda - \lambda n_0}{\lambda \lambda_0} \tag{3.5}$$

This expression can be rewritten using the following approximations:

$$\lambda \approx \lambda_0 \Rightarrow \lambda\lambda_0 \approx \lambda_0^2 \tag{3.6}$$

$$n_\lambda = n_0 + (\lambda - \lambda_0) \cdot \frac{\partial n}{\partial \lambda} \tag{3.7}$$

Plugging these expressions into Eq. (3.5), we obtain [156]:

$$\phi(\lambda) = -\frac{2\pi}{\lambda_0^2} n_g (\lambda - \lambda_0) \cdot L \tag{3.8}$$

The group index n_g can be accurately simulated and also extracted from the free spectral range (FSR) of the resonances. The conversion from wavelength to phase around resonance can be done with high accuracy. With some precaution, these equations allow to extract a and r from the fitting of the resonance. Examination of Eq. (3.1) shows that a and r can be interchanged without changing the formula. The fitting is only able to extract pairs of values for them and it is up to the data analyst to determine which of the two values corresponds to the loss and to the transmission. However, if multiple resonances are fitted over a wide wavelength range, it is possible to untangle the parameter pairs in most cases. For the wavelengths and

waveguide dimensions used here, the transmission coefficient r will decrease with increasing wavelengths, since the modes become less confined to the waveguide cores and hence more strongly coupled. In weakly dispersive waveguides, such as the on Si_3N_4-platform used here, this decrease is approximately linear. A more general approximation that remains valid in more dispersive waveguides such as on SOI, is given by [157]

$$r \simeq |\cos(c_0 + c_1\lambda)|, \tag{3.9}$$

where c_0 and c_1 are fitting constants. Another possibility is to sweep the separation between the ring and the bus waveguide. Except in the limit of very small gaps, the roundtrip loss in the ring is not affected by the coupling [156]. This information can also help to distinguish the two parameters a and r.

An example of a parameter extraction from a set of ring resonators with increasing gaps is shown in Fig. 3.10. The rings have a radius of 100 µm and are clad with BCB, cured in an N_2-environment. The bus and ring waveguide are both designed with a width of 1360 nm. The coupling section consists of a straight bus waveguide and a ring with a constant radius. While the coupling coefficient clearly changes for different gaps, the estimated loss remains roughly the same. The pronounced absorption peak at 1520 nm arises both from the silicon nitride core (before annealing) and from the N_2-cured BCB cladding, as reported in chapter 2. This indicates that ring resonators can serve as a compact probe for absorption peaks. On the other hand, the variance of the data is larger than what would be ideal for an accurate assessment of the propagation loss. The data also show that the wavelength dependence of the coupling can be satisfactorily fitted with a linear model. These linear fits can then be used to create a model of the coupling strength versus the designed gap, as shown in Fig. 3.11, and facilitate a more accurate design in the next fabrication iteration.
The preceding analysis assumes unidirectional operation of the ring resonator, which is a theoretical approximation. In real devices, small perturbations of the ring waveguide are inevitable. Waveguide sidewall roughness acts as a distributed source of backreflections and the transition from the ring waveguide to the coupling interface with the bus waveguide can be considered as a lumped reflection point [158]. These backreflections can cause coupling of the clockwise and counterclockwise propagating modes. If the Q-factor of the ring is high enough and the backreflected light can build up sufficiently, the resonance peaks of the rings split into two overlapping peaks, each corresponding to one of the counterpropagating modes. In high-index contrast platforms such as silicon-on-insulator, resonance split-

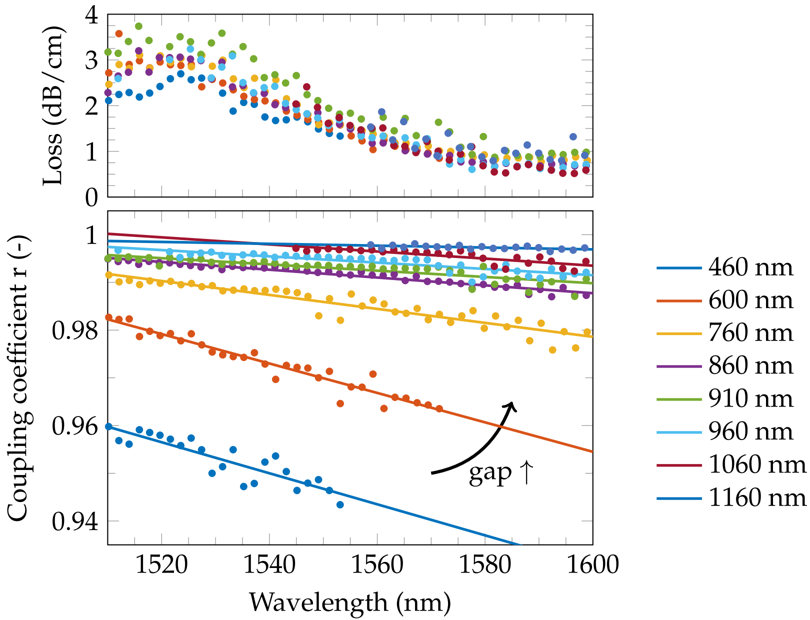


Figure 3.10: Extraction of the loss (up) and coupling coefficient (down) from a sweep of all-pass ring resonators with increasing gaps before the annealing of the silicon nitride. The rings have a radius of 100 µm and are clad with BCB, cured in an N_2 environment. The bus and ring waveguide widths in this case are designed 1360 nm wide.

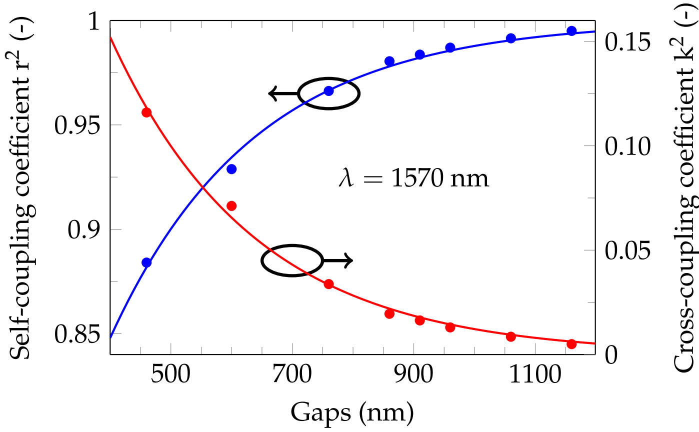


Figure 3.11: Fitting of an exponential model to the coupling coefficient data at 1570 nm, extracted from the linear fits in Fig. 3.10. The cross-coupling coefficient is calculated as the complement of the self-coupling, under the assumption of negligible losses at the coupling section. Note: the gaps on the x-axis are the *designed* gaps. The actual gaps will be wider due to the fabrication process.

ting can already be seen for Q-factors around $8 \cdot 10^4$ [154]. For rings with lower sidewall scattering losses, such as on the Si_3N_4-on-insulator platform, resonance splitting occurs at higher Q-factors. If the Q-factor is sufficiently high, e.g. > 10 million [68], a strong reflection occurs at resonance, enough to act as a frequency selective mirror for lasing. These ultra-high Q-factors are however difficult to achieve.

Although all-pass filter rings are very useful for monitoring waveguide losses because of their small footprint and short required E-beam writing time, add-drop filter rings are more robust component to construct frequency selective mirrors for widely tunable lasers. The power transmission at the pass- and the drop-port is, respectively [154]:

$$T_p = \frac{r_2^2 a^2 - 2r_1 r_2 a \cdot \cos\phi + r_1^2}{1 - 2r_1 r_2 a \cdot \cos\phi + (r_1 r_2 a)^2} \tag{3.10}$$

$$T_d = \frac{(1 - r_1)^2 (1 - r_2)^2 a}{1 - 2r_1 r_2 a \cdot \cos\phi + (r_1 r_2 a)^2} \tag{3.11}$$

The expression for the transmission at the through-port is the same as in the case of an all-pass ring, except the outcoupling at the drop-port has to be included in the roundtrip losses: $a \to r_2 a$. A measurement of the

through- and drop-ports around resonance is shown in Fig. 3.9b. To achieve critical coupling, an asymmetric coupling is needed. A similar resonant suppression of the output at the drop port is not possible. At resonance, the output at the drop port is strongest. The parameter extraction from add-drop filters is a little bit more involved than that from all-pass filters and in the most general case it requires measurement of both the through-port and drop-port transmission. From the resonances in the through port, the parameters that can be extracted are the transmission coefficient r_1 and the product $r_2 a$. For a full parameter extraction from the measurement of this port, extra assumptions are needed such as $r_1 = r_2$. Again, the fitting will return two numbers which must be mapped to their corresponding parameter with care. For the fitting of the drop-port resonances, the two transmission coefficients r_1 and r_2 can be interchanged, however the roundtrip loss a can be assessed. A more rigorous method is to optimize the fit for both ports simultaneously.

3.6.2 Losses induced by the coupling section

As mentioned above, the interface of the ring with its feeding waveguide(s) is a perturbation of the mode in the ring and hence extra light may be lost due to scattering or reflection at this point. Several coupling section designs have been tested for rings with a radius of 100 μm and waveguide widths of 1.5 μm to assess their impact on the roundtrip loss. They are graphically shown in Fig. 3.12. A convenient method to compare the different coupler designs is presented in [159]. The linewidth and power at the drop port (equivalent to the reflection bandwidth and strength, when used as a mirror) of all resonances of several rings with a varying gap can be shown on a scatter plot and compared to theoretical curves representing a constant loss a and a varying coupling strength r. The results for add-drop rings processed on blank Si_3N_4-on-insulator, clad with vacuum-cured BCB, are shown in Fig. 3.13a. The full lines show theoretical curves of a constant loss that approach the fitted data. Two coupling sections appear to perform better than the rest: the rings with adiabatically changing curvatures (Fig. 3.12b) and those with a symmetric coupling section without a straight extension (Fig. 3.12e). In these rings, the measured propagation loss is close to that of a straight waveguide in vacuum-cured BCB, indicating low excess losses. In the other configurations, a significant amount of excess loss appears to be induced by the coupling sections. In order to see if these results are still valid for the design of laser cavities, the same experiment was repeated on a sample where the extra layers of 100 nm SiO_2 and 400 nm a-Si:H were deposited. These deposited layers were first removed with the same dry

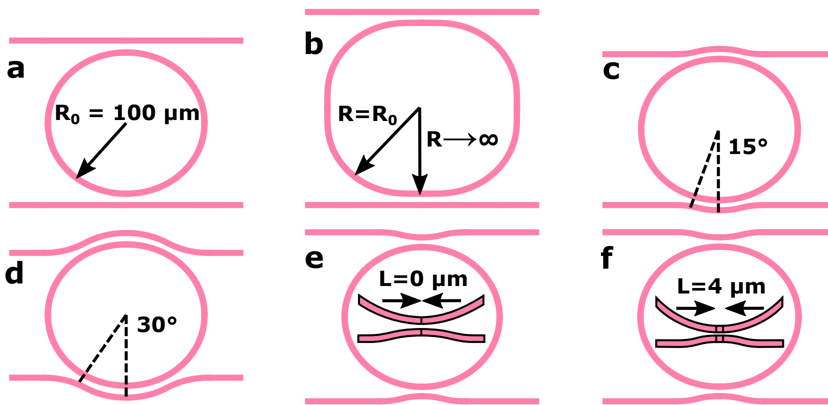


Figure 3.12: Different coupling section designs for the ring resonators. All bus and ring waveguides are 1.5 µm wide. (a) Standard design with a straight bus waveguide and a constant ring curvature. (b) Adiabatic change of the curvature in the ring from straight to the target curvature over an angle of 5 degrees. (c) Bus waveguide wrapped around a ring with constant curvature, spanning a 15° arc. (d) Wrapped bus waveguide spanning a 30° arc. (e) Symmetric coupling section. (f) Symmetric coupling section with a straight extension of 4 µm.

etching recipes that are used in the fabrication steps described in Chapter 2. A small amount of SiO_2 is left on top of the Si_3N_4 layer. The roughness on the waveguide's top surface, introduced by the dry etching process, could potentially increase the propagation losses. The results are shown in Fig. 3.13b. It is clear that the performance of the two best designs does not deteriorate noticeably. The design with the symmetric coupling section from Fig. 3.12e will be used in laser cavity design later on. Its measurement results are shown in more detail in Figs. 3.13c and 3.13d.

3.6.3 Add-drop ring resonators as frequency selective mirrors

Add-drop rings can be used as frequency selective mirrors when connecting the input- and drop-ports with a splitter or a 1x2 MMI, as shown in Fig. 3.14a. In this case, an extra filter is needed to ensure that lasing can only happen at one of the resonances. Tuning of the lasing wavelength will be limited by the FSR of the ring. However, tuning of a single Si_3N_4 ring is difficult to achieve over a range of more than a few nm due to Si_3N_4's low thermo-optic

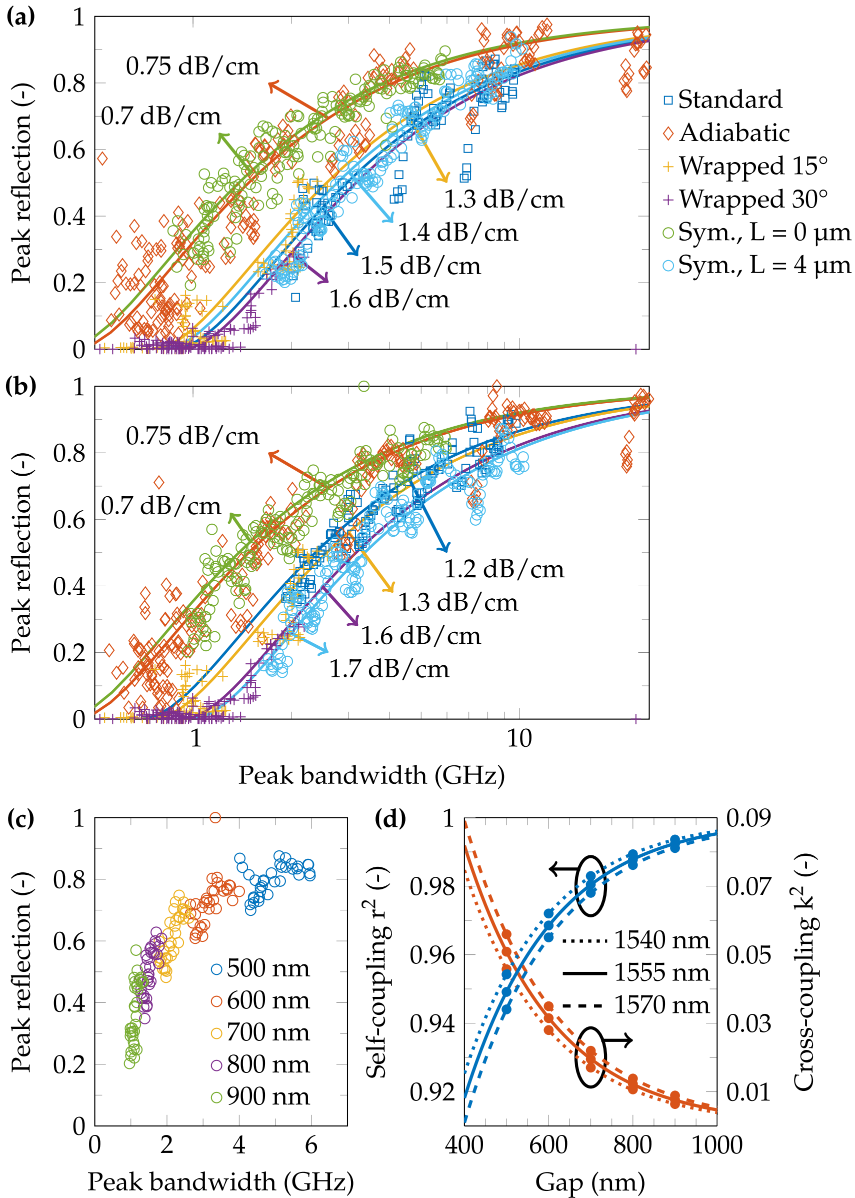


Figure 3.13: Comparison of add-drop rings with different coupling sections. Peak bandwidth is the FWHM width of the resonances. Peak reflection is the power transmission to the the drop port. (a) Results of rings on blank Si_3N_4 sample. (b) Results of rings on Si_3N_4 sample with deposited and subsequently etched SiO_2 and a-Si:H layers. (c) Detailed view of the results for different gaps with the best design: the symmetrical coupling section without straight extension. (d) Coupling coefficient data extracted for the best design.

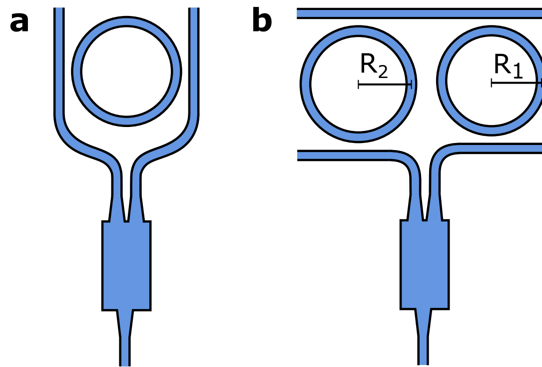


Figure 3.14: Frequency selective mirror based on add-drop ring resonators. (a) Single-ring mirror. (b) Double-ring Vernier mirror.

coefficient. Therefore, two rings with slightly offset FSRs are used to exploit the Vernier effect, as shown in Fig. 3.14b. The three main design parameters for the application of these types of mirror in narrow-linewidth lasers are the resonance bandwidth, the reflection/transmission and the (combined) FSR. Low resonance bandwidths can always be achieved by undercoupling the rings, however this adversely affects the reflection of the mirror. The reflection of the mirror in Fig. 3.14a equals the fraction of light coupled to the drop-port, reduced by any excess insertion loss at the splitter. Since the transmission to the drop port, Eq. (3.11), is symmetric in r_1 and r_2, it will always be maximal when the ring is designed symmetrically with $r_1 = r_2$. This also prevents excess loss in the 1x2 MMI combiner. The reflection of the mirror is maximal using critically coupled or overcoupled rings. The resonance bandwidth must be sufficiently narrow to ensure single-mode lasing operation of the laser. The reflectivity of the mirror must be high enough to ensure that the laser reaches threshold at all. Ultimately, the achievable roundtrip loss in the ring resonators will determine how optimal both parameters can be designed.

Since we intend to use these add-drop mirrors as parts of the lasing cavity, we also investigate the group delay of these rings. Group delay is defined as the derivative of phase with angular frequency and corresponds to a travelled length divided by the group velocity:

$$T_g = \frac{\partial \phi}{\partial \omega} = L\frac{\partial \beta}{\partial \omega} = \frac{L}{c}\frac{\partial(\omega \cdot n_{eff})}{\partial \omega} = \frac{L}{c}\left(n_{eff} + \omega\frac{\partial n_{eff}}{\partial \omega}\right) \tag{3.12}$$

$$\Rightarrow L = T_g \cdot v_g = \frac{\partial \phi}{\partial \omega} \cdot v_g \tag{3.13}$$

However, for ring resonators, the effective phase delay between the in- and output of the ring is different from the phase delay of a single roundtrip, and as such also the group delay is different. An effective length can be ascribed to the ring, based on the aforementioned definition of group delay. Consider now the effective phase delay of the ring, φ. The ring's group delay can still be defined as:

$$T_g = \frac{\partial \varphi}{\partial \omega} \tag{3.14}$$

We can relate the ring's effective group delay to the group delay of a single roundtrip as follows:

$$T_g = \frac{\partial \varphi}{\partial \phi} \cdot \frac{\partial \phi}{\partial \omega} = \frac{\partial \varphi}{\partial \phi} \cdot T_{g,1}, \tag{3.15}$$

where ϕ is again defined as the accumulated phase during one roundtrip. The group delay of the ring equals the group delay of a single roundtrip multiplied by a factor $\partial\varphi/\partial\phi$. This can also be considered as an increase of the effective length of the ring, which makes it easier to calculate the total cavity length when designing a laser cavity:

$$L_{eff} = \frac{\partial \varphi}{\partial \phi} \cdot L_{ring} \tag{3.16}$$

In Appendix B, the expression for this multiplicative factor is derived for the effective phase delay at the drop port, resulting in the following expression for the effective length of an add-drop ring resonator *at resonance*:

$$L_{eff,d} = \frac{1 + ar_1r_2}{2(1 - ar_1r_2)} \cdot L_{ring} \approx \frac{1}{1 - ar_1r_2} \cdot L_{ring}, \tag{3.17}$$

where the approximation is valid in the limit of low losses and near-critical coupling.

3.6.4 Expanding the free spectral range - the Vernier effect

To achieve a wide wavelength tuning range, two add-drop ring resonators are used in a Vernier configuration. The rings are designed with slightly different free spectral ranges. Efficient reflection of the light back into the

laser cavity is only possible when the resonances of both rings are aligned. The total free spectral range of the combined two rings will satisfy the following conditions:

$$\mathrm{FSR}_{\mathrm{tot}} = m \cdot \mathrm{FSR}_1 \tag{3.18}$$

$$\mathrm{FSR}_{\mathrm{tot}} = (m+1) \cdot \mathrm{FSR}_2, \tag{3.19}$$

where m is an integer. Rearranging these terms to eliminate m, we see that this mechanism extends the total free spectral range of the mirror to

$$\mathrm{FSR}_{\mathrm{tot}} = \frac{\mathrm{FSR}_1 \cdot \mathrm{FSR}_2}{|\mathrm{FSR}_1 - \mathrm{FSR}_2|}. \tag{3.20}$$

A schematical illustration of the Vernier effect is shown in Fig. 3.15.

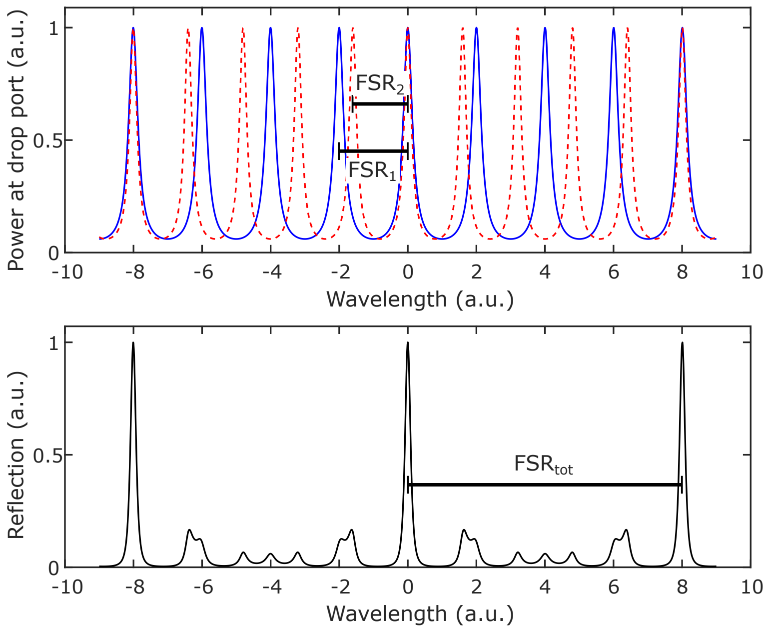


Figure 3.15: Illustration of the Vernier effect using two cascaded add-drop ring resonators. (top) Simulated spectra of the power at the drop-port of two add-drop ring resonators with a different radius. (bottom) Combined reflection of the mirror.

By designing the rings with almost the same radius (and hence FSR), the combined FSR can in principle be extended arbitrarily. However, a practical

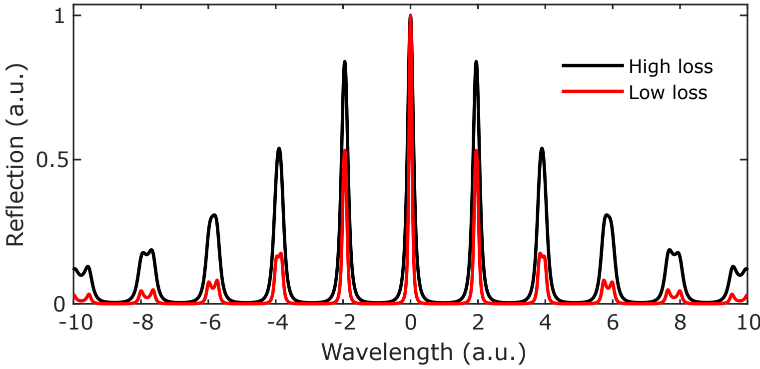


Figure 3.16: Schematic illustration of the impact of roundtrip losses in the ring resonators on the performance of a Vernier mirror. Lower roundtrip losses lead to more narrow resonance peaks and faster peak splitting, resulting in a better side-peak rejection.

limit to the FSR originates from the finite spectral width of the resonances. As the difference in free spectral range is reduced, also the suppression of the peaks adjacent to the central peak goes down, until there is not enough suppression anymore to ensure single-mode operation of the laser. For this reason, when a wide total FSR is required, the losses in the rings should be low enough to allow for enough side-peak suppression, while still having a high peak reflection. A schematic drawing of this effect is shown in Fig. 3.16, where two Vernier mirrors with the same FSR but different losses are compared. The peak power in the Vernier mirror with low roundtrip losses drops much faster than in the case with high losses. Low roundtrip losses in the add-drop rings leads to more narrow resonances, causing the product of slightly misaligned peaks to drop faster.

3.7 Thermal impedance of the target substrate

Active components on the a-Si:H-on-Si_3N_4 stack will suffer from a higher thermal impedance to the substrate, as compared to typical SOI platforms, due to the thicker buried oxide layer. A two-dimensional finite element solver (COMSOL) was used to simulate the effect of power dissipation in an SOA on the temperature elevation. The a-Si:H-on-Si_3N_4 platform is compared to the 400-nm-SOI platform commonly used in our research group. Radiation and convection are ignored, only thermal conduction

is taken into account in order to compare the thermal impedance to the substrate. The equation to be solved is then:

$$\overrightarrow{q} = -k\nabla T \quad (3.21)$$

$$\nabla \cdot \overrightarrow{q} = \begin{cases} Q, & \text{within the heat source} \\ 0, & \text{outside the heat source,} \end{cases} \quad (3.22)$$

where $\overrightarrow{q}$ is the heat flux density (W/m^2), Q is the generated heat per unit volume (W/m^3), k is the thermal conductivity of the material (W/m·K) and ∇T is the temperature gradient (K/m). The approximation is made that all of the electrical power is dissipated in the quantum well layer, hence the heat is generated only in that layer. The top and side of the simulation area are set to an insulating boundary condition. The bottom of the simulation window, in the substrate, is set as a heat sink with a fixed temperature of 20°C. The simulation window is taken large enough to avoid influence of the boundary conditions on the simulation results. The substrate is included up to a depth of 20 µm and the simulation window is 80 µm wide.

Material	Thermal conductivity (W/m·K)	Reference
Silicon	130	COMSOL
a-Si:H	1 - 5	[160–162]
SiO_2	1.4	COMSOL
Si_3N_4	20	COMSOL
BCB	0.29	[163]
InP	68	[164,165]
$(Al_{0.9}Ga_{0.1})_{0.47}In_{0.53}As$ - transition	14.39	[166]
$(Al_{0.7}Ga_{0.3})_{0.47}In_{0.53}As$ - SCH	11.00	[166]
$(Al_{0.25}Ga_{0.75})_{0.3}In_{0.7}As$ - QW	7.71	[166]
$(Al_{0.45}Ga_{0.55})_{0.51}In_{0.49}As$ - barrier	8.17	[166]
MQW average	8.01	
SCH-transition average	12.18	
InGaAs	4.82	[166]

Table 3.1: Thermal conductivities used in thermal simulations.

The only material parameter needed in this equation is the thermal conductivity, which is listed in Table 3.1 for the materials used in the simulation. The values for the quaternary III-V materials were calculated using interpolation formulas, starting from the binary III-V components [166]. It is worth noting that the thermal conductivity of a-Si:H is almost two orders

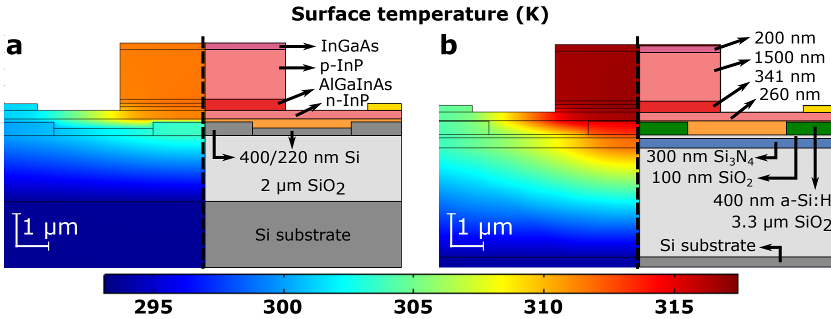


Figure 3.17: Comparison of the thermal behaviour of integrated amplifiers on (a) a 400 nm SOI stack and (b) our a-Si:H-on-Si_3N_4 platform. The BCB bonding layer is 20 nm thick in both cases.

of magnitude smaller than that of crystalline silicon, similar to that of SiO_2. Amorphous silicon can be deposited in several different ways, all of which result in a highly disordered structure with similar thermal properties [162]. One report confirms that PECVD-deposited a-Si:H is no exception [161]. Heat transport in solids happens either through phonon propagation or free electron displacements. The contribution of the latter is generally low due to the low carrier mobility in amorphous semiconductors [160], whereas phonon propagation is hindered by the lack of crystalline order, hence reducing the ability to carry heat. The thermal conductivity of a-Si:H in the simulation is 3 W/m·K.

As a heat source, an electrical power dissipation of 200 mW is taken, assuming a device length of 1 mm. The resulting temperature profiles are shown in Fig. 3.17, together with an overlay of the material stack. The amplifier stack and the BCB bonding layer of 20 nm are the same in both simulations. The AlGaInAs layer consists of a 111 nm thick MQW layer, sandwiched by two separate confinement heterostructure layers, each 115 nm thick. Both temperature profiles are plotted on the same scale. The maximal temperature elevation on the SOI platform is 18.7°C, whereas on the a-Si:H-on-Si_3N_4 platform it is 24.5°C: an increase of 31%. The main reason is the thicker buried oxide layer in the a-Si:H-on-Si_3N_4 platform. However, due to their low thermal conductivity, the a-Si:H and Si_3N_4 layers also don't spread the heat as efficiently as the partially etched SOI layer. From the temperature elevation, the thermal impedance of both devices can be calculated as

$$Z_t = \frac{\Delta T}{\Delta P} = \frac{T_{max} - T_0}{P_{el}}, \tag{3.23}$$

where ΔT is the temperature elevation, T_{max} is the maximal temperature and T_0 is the substrate temperature. The power dissipated through Joule heating is given by ΔP. In devices with a high wall-plug efficiency, the optical output power should be subtracted from the electrical input power P_{el}. However, in our devices this can be ignored. The calculated thermal impedances are then 93.5 K/W on 400-nm-SOI and 122.5 K/W on a-Si:H-on-Si_3N_4. The value for SOI is comparable, but slightly lower, than a simulation reported for a 220-nm-SOI stack [96].

4

Heterogeneously integrated III/V-on-Si_3N_4 lasers

The laser is a solution seeking a problem.
Theodore Maiman

4.1 Introduction

In this chapter, the results from the integration of III-V amplifiers on a silicon nitride platform are discussed. A standalone amplifier, a multimode laser, and a single-mode laser will be demonstrated. The fabrication steps for these devices have been previously described in Chapter 2 and the performance of the platform's passive components has been shown in Chapter 3. The characterization of the standalone amplifier can be used to construct a black box model in the design of the laser. The behaviour of the multimode laser unveils some laser dynamics that can be taken into account. Finally, the single-mode laser is a first step towards heterogeneously integrated, widely tunable lasers on silicon nitride with low noise. Parts of this chapter have been previously published in [103, 167].

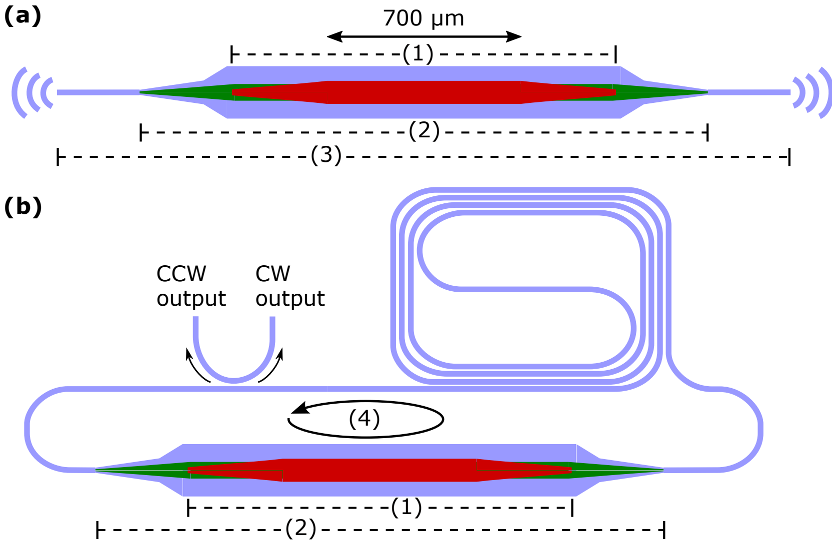


Figure 4.1: Layout of the heterogeneously integrated amplifier (a) and the multimode ring laser (b). The III/V SOAs in both devices have the same length. The dashed lines indicate possible spurious cavities of which the FSR is calculated in Table 4.2.

4.2 III/V-on-Si_3N_4 amplifier

A standalone III/V-on-Si_3N_4 amplifier can be characterized by adding grating couplers on each side for transmission measurements. The processed sample is placed on a temperature-controlled chuck, which is set to a temperature of 20°C. Each device under test (DUT) is accompanied by a nearby reference Si_3N_4 waveguide to calibrate the grating coupler efficiency. Reflections at the grating coupler can perturb the amplifier's operation and even cause spurious lasing if the gain surpasses the roundtrip loss. Two-dimensional FDTD simulations indicate that the reflection in the waveguide at the grating coupler is smaller than -20 dB.

The extracted optical output on one end of the device is collected by an optical spectrum analyzer (OSA, Anritsu MS9740A), which also acts as a power meter for the alignment of the fibers at the grating coupler interface. For the measurement of the gain of the amplifiers, an optical input from a tunable semiconductor laser source (Santec TSL-510) is sent through a polarization controller and injected on the other side of the device. The layout of the III/V-on-Si_3N_4 amplifier is shown in Fig. 4.1a. The devices

are electrically contacted using DC probes. A low-noise current source and voltage meter (Keithley 2400 Sourcemeter) is used to control the applied bias current on the device. Both devices have a differential series resistance of 10 Ω at 80 mA. This bias current level corresponds to a current density in the active layers of 2.11 kA/cm^2.

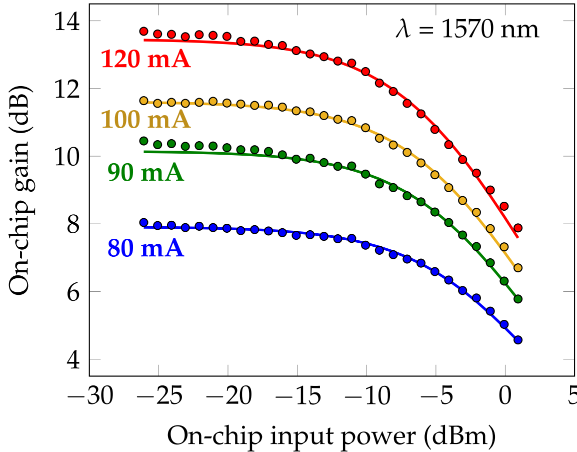


Figure 4.2: On-chip gain of the III-V-on-Si_3N_4 amplifier at 1570 nm as a function of on-chip optical input power for different bias currents. The onset of gain compression is visible. The solid lines represent the fit to the gain compression model.

Three parameters are swept to characterize the amplifier: the bias current, the optical input power and the wavelength. Fig. 4.2 shows the gain compression as a function of optical input power at a wavelength of 1570 nm, for different bias currents above transparency. At low input power levels, the gain reaches 13.7 dB for a current of 120 mA. We measure a maximum on-chip output power of 7.6 mW for an input power of 1.24 mW and 120 mA bias current. The gain compression can be approximated with the following simple relationship [168]:

$$G(P_{in}) = G_0 \frac{1 + P_{in}/P_{sat}}{1 + G_0 P_{in}/P_{sat}}. \tag{4.1}$$

Equation (4.1) can be used as a model to fit the small-signal gain G_0 and the material gain saturation power P_{sat} for each bias current. At higher input power levels, the gain will decrease, eventually approaching 1 as $P_{in} \gg P_{sat}$. For a high enough small-signal gain G_0, the material saturation power indicates at which input power level the gain is reduced *to* 3 dB. It can be

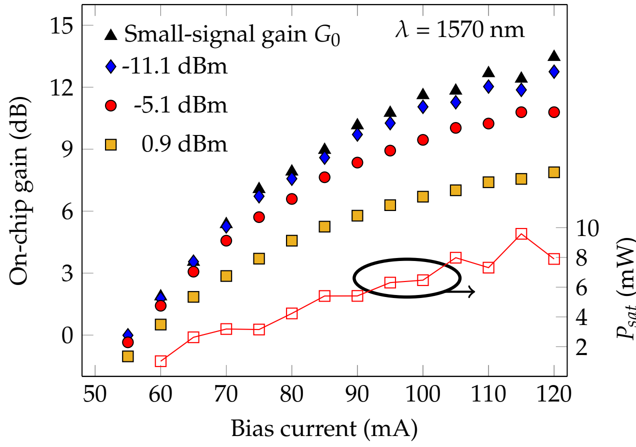


Figure 4.3: On-chip gain of the III-V-on-Si_3N_4 amplifier at 1570 nm as a function of bias current for three on-chip optical input levels. The fitting parameters G_0 and P_{sat} - extracted from the fits in Fig. 4.2 - are shown.

readily related to the input saturation power $P_{in,sat}$, at which the gain is reduced *by* 3 dB using equation (4.1):

$$P_{in,sat} = \frac{P_{sat}}{G_0 - 2} \tag{4.2}$$

The results of these fits are plotted in Fig. 4.3, together with the optical gain at 1570 nm for several optical input powers P_{in}. The fits indicate that the saturation power reaches 8 mW at 120 mA. Higher gains and saturation powers can be achieved using longer devices with dedicated III-V epi-stacks and optimized waveguide cross-sections [86,168]. Longer amplifiers will result in an increased small-signal gain, but will not necessarily result in higher output powers, due to gain saturation. The saturation power P_{sat} is described by [168]:

$$P_{sat} = \frac{hc}{\lambda} \cdot \frac{\sigma_{xy}}{a\tau\Gamma}, \tag{4.3}$$

where hc/λ is the photon energy, σ_{xy} is the cross-sectional area of the quantum wells, Γ is the confinement factor of the optical mode in the pumped quantum wells, a is the differential gain, and τ is the carrier lifetime. The on-chip noise figure indicates the degradation of the signal by the addition of shot noise and randomly phased amplified spontaneous emission (ASE)

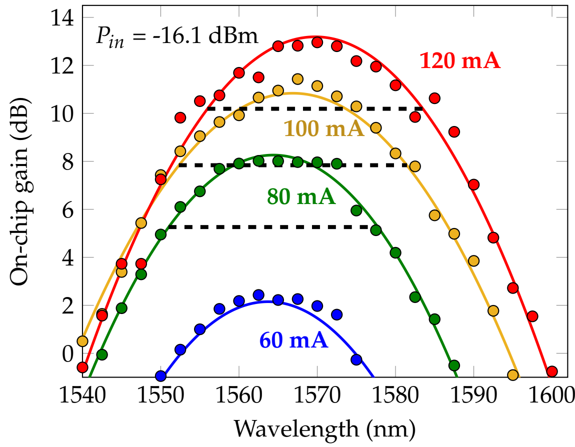


Figure 4.4: The wavelength dependence of the gain of the III-V-on-Si_3N_4 amplifier at different bias currents, for an optical input level of -16.1 dBm. The dashed lines indicate the 3-dB gain bandwidth. The gain peak shifts to higher wavelengths for higher currents, indicating the effect of self-heating.

to the signal [139]:

$$F_{\text{shot}} = 1/G \tag{4.4}$$

$$F_{\text{ASE}} = \frac{2\lambda^3}{Gc^2h}\frac{P_{\text{ASE}}}{\delta\lambda}, \tag{4.5}$$

where λ is the pump wavelength and G the on-chip gain. The power spectral density of the ASE is calculated by dividing the ASE power P_{ASE} by the integrated wavelength range $\delta\lambda$. For a low on-chip optical input power level of -11 dBm, the noise figure of the amplifier is 10.6 dB at a bias current of 100 mA and 12.3 dB at 120 mA.

Finally, the wavelength dependence of the gain was measured for different input currents. This result is shown in Fig. 4.4. The wavelength dependence of the gain can be described using the following relationship:

$$G(\lambda) = G_p \cdot \exp\left[-A(\lambda - \lambda_p)^2\right]. \tag{4.6}$$

The solid lines in Fig. 4.4 represent the fits of Equation (4.6) to the measured data, from which the peak wavelength λ_p, peak gain G_p and the 3-dB bandwidth of the gain can be extracted. The latter is indicated by the dashed black lines. The amplifier has a 3-dB gain bandwidth of 28 nm at a bias current of 100 mA. The peak wavelength of the gain shifts from 1564.4

nm at 80 mA to 1569.7 nm at 120 mA. This redshift indicates self-heating, which can be explained by the higher thermal insulation between the device and the substrate in this material stack (3.3 µm TOX), as compared to active devices integrated on SOI, which typically only has 2 µm of TOX below the waveguide layers. Indeed, the same SOAs integrated on SOI show a clear blue-shift of the gain at elevated currents [139].

4.2.1 Spurious reflections in the III/V-on-Si_3N_4 amplifier

Spurious reflections around the heterogeneous III-V-on-Si_3N_4 amplifier create weak Fabry-Pérot (FP) effects, which lead to a variation in the measured gain. This gain ripple can be observed in the spectrum of the amplified spontaneous emission spectrum of the amplifier and can be used to assess the strength of the reflections. Fig. 4.5a shows the gain ripple of the amplifier at a bias current of 100 mA at 20°C. The inset shows in more detail the gain ripple around 1570 nm. The presence of oscillations with different periods indicates multiple spurious reflections in the cavity. The strongest reflections originate from discrete scattering points such as the grating couplers and the taper tips. The lengths and group indices of the different waveguide layers in the device are listed in Table 4.1. With this knowledge, the free spectral range of the spurious cavities can be calculated:

$$FSR = \frac{c}{2 \cdot n_g L} \qquad \text{for Fabry-Pérot cavities} \tag{4.7}$$

$$FSR = \frac{c}{n_g L} \qquad \text{for ring cavities} \tag{4.8}$$

These formulas are based on the definitions of the length from Fig. 4.1, where for the Fabry-Pérot cavities, only the physical length of the cavity is counted instead of the total roundtrip length. The estimated free spectral ranges, corresponding to the Fabry-Pérot cavities between the taper tips on the III-V coupon, between the a-Si:H taper tips, and between the grating couplers in the Si_3N_4 layer, are given in Table 4.2.

Layer	n_g	Length (µm)
III-V amplifier	3.5	1148
a-Si:H	3.53	474
Si_3N_4 (amp.)	1.91	1199
Si_3N_4 (las.)	1.91	11810

Table 4.1: Waveguide lengths and group indices in each layer.

Number	L_{opt} (mm)	FSR (GHz)
(1)	4.018	37.3
(2)	5.691	26.3
(3)	7.981	18.9
(4)	28.248	10.7

Table 4.2: Optical length and FSR estimation of the cavities in Fig. 4.1.

The spectrum of the gain ripple between 1550 nm and 1590 nm is shown in Fig. 4.5b. Multiple peaks are indeed visible. The arrows indicate that the estimation of the FSRs in Table 4.2 is accurate. The remaining peaks are caused by reflections on other pairs of those points. The amplitude of the gain ripple can be related to the absolute reflectivity using the Hakki-Paoli method [169]. Although there is no dominant source of reflections, we will perform the analysis as if only one spurious cavity is present. We can then write the following relationship between the amplitude of the ripple, the mirror loss and the amplification in the amplifier,

$$\frac{\sqrt{r}+1}{\sqrt{r}-1} = \frac{1}{\sqrt{R_1 R_2} e^{-\alpha L}} \tag{4.9}$$

where r is the ratio of the upper and lower envelope, or simply the amplitude of the ripple on a logarithmic scale, R_1 and R_2 are the reflectivities of the cavity mirrors and $e^{-\alpha L}$ is the loss (or gain) of a single pass in the cavity. At 100 mA, the small-signal gain is 11.6 dB, or 14.5. The amplitude of the largest ripple is 2.3 dB, or 1.7. We can then solve equation (4.9) for the product $R_1 R_2$. The result is an estimated reflection of -20.4 dB for one cavity mirror. It is clear that the amplifier demonstrated here cannot start lasing due to the spurious reflections, however it has to be taken into account for future optimizations. The scale on the vertical axis in Fig. 4.5b is left dimensionless. With proper scaling, the strength of the peaks in the fast-Fourier transformed (FFT) spectrum could be related to the reflectance, however this would only be valid if the gain were constant across the whole spectrum.

4.3 III/V-on-Si_3N_4 multimode laser

To demonstrate the potential of the amplifier, a laser cavity was formed by connecting the outputs of an amplifier with a 1-cm-long waveguide in the Si_3N_4 layer. A directional coupler is used to extract around 17% of the power circulating in the cavity. A schematic layout of the laser is shown

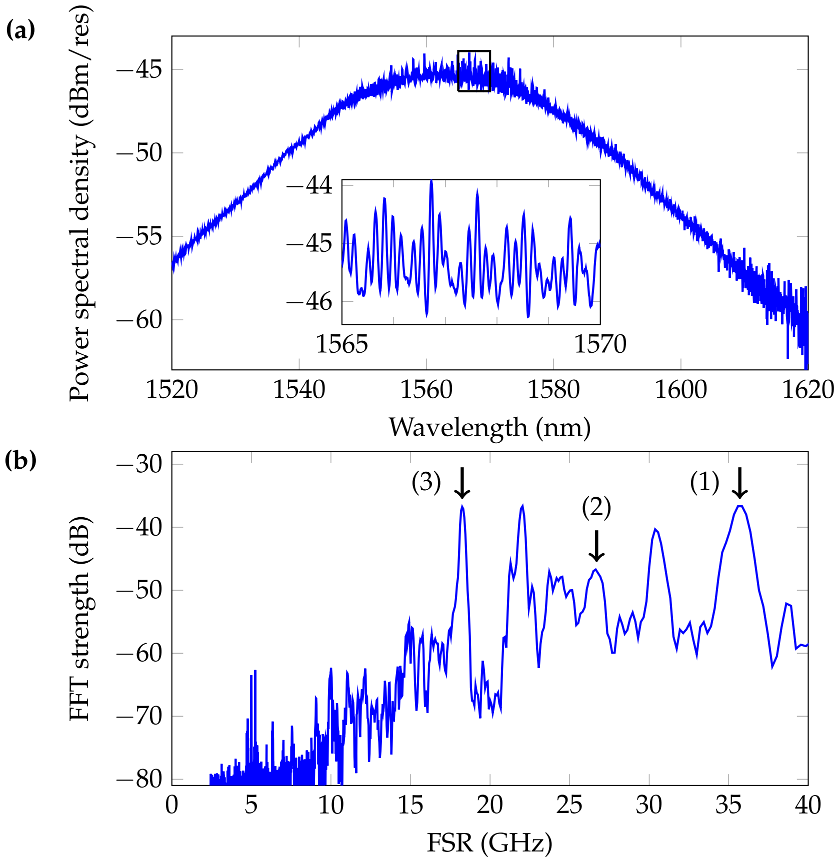


Figure 4.5: Analysis of the amplified spontaneous emission spectra from the amplifier at 20°C. (a) ASE spectra of the amplifier at 100 mA. The inset shows a detailed view of the gain ripple around 1570 nm. Multiple oscillation periods are visible. (b) Spectral distribution of the gain ripple. The arrows indicate the spurious Fabry-Pérot cavities calculated in Table 4.2.

in Fig. 4.1b. No spectral filters were added in this first demonstration, so the laser is strongly multimode with a free spectral range of 10.7 GHz as calculated in Table 4.2. For the characterization of the laser, the same measurement setup is used, except the tunable laser input is replaced by a second optical power meter (HP 8153A Lightwave Multimeter). The laser is characterized by measuring the optical output power and spectrum as a function of bias current at three different temperatures: 15°C, 20°C and 25°C. The measured voltage and single-sided on-chip optical output power

at all three temperatures are plotted against the bias current in Fig. 4.6. The differential series resistance is the same at each temperature. It can be observed that the lasing threshold increases with temperature: from 59 mA at 15°C, over 63 mA at 20°C to 69 mA at 25°C. At threshold, the loss and gain of a longitudinal mode in the cavity match. The gain is reduced at higher temperatures. Thermal roll-off occurs at an electrical power dissipation around 230 mW. Reducing the series resistance will allow to pump the device with higher current densities. Single-sided on-chip optical powers up to 350 µW are reached. This sub-milliwatt value can be explained by the combined effects of a low output coupling, cavity losses and variability in the transfer printing alignment accuracy, which leads to a varying coupling efficiency between the III-V and the a-Si:H waveguides. Lasing spectra below and above threshold at 20°C are shown in Fig. 4.7. Just above threshold, the estimated slope efficiency is 0.015 W/A and only one lasing peak is prominent, with around 18 dB side-mode suppression. At higher bias currents, more modes start lasing. The laser can be made single-mode by adding a spectral filter in the Si_3N_4 cavity [102].

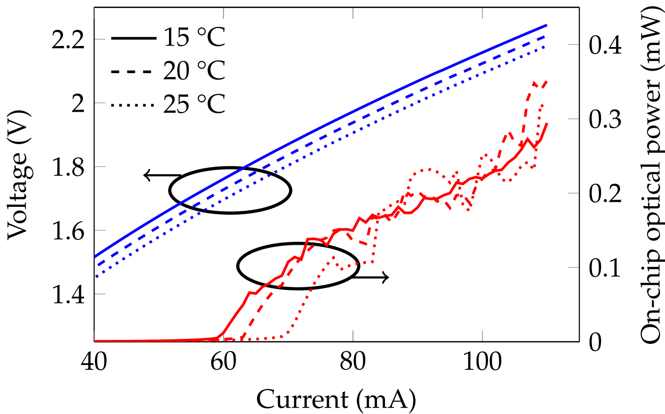


Figure 4.6: LIV curves of the multimode laser. The estimated slope efficiency just above threshold at 20°C is 0.015 W/A.

4.3.1 Spurious reflections in the III/V-on-Si_3N_4 ring laser

After the initial characterization of the laser, an electrical contact of the device was damaged due to a defect in the post-processing of the coupon. This increased the series resistance of the device, causing more resistive heating and degrading the performance of the device. At 20°C, thermal

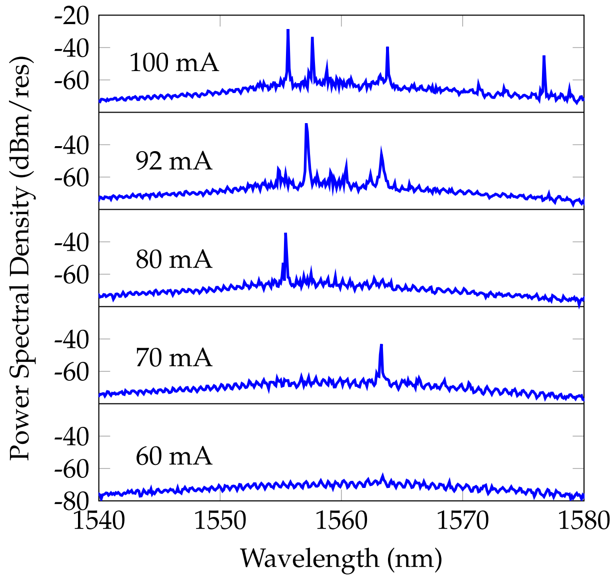


Figure 4.7: Spectra of the device below and above threshold at 20°C, recorded with a resolution of 30 pm.

roll-off limits the gain before threshold can be reached. The sub-threshold amplified spontaneous emission from both outputs is measured with a high resolution to extract its frequency components and thus identify the sources of spurious reflection. This is shown in Fig. 4.8. Contrary to the amplifier, the gain ripple of the laser's outputs contain a predominant oscillation, with a period of 10.7 GHz, matching the FSR of the total ring cavity including the silicon nitride waveguide, as listed in Table 4.1. The feedback through the silicon nitride waveguide is >18 dB stronger than the feedback caused by spurious reflections in the cavity. The peaks corresponding to the total cavity roundtrip, the reflections at the a-Si:H taper tips and those at the III-V taper tips, are indicated with arrows in Fig. 4.8.

From the sub-threshold spectra, it can be observed that the clockwise propagating mode (CW) carrier about 7 dB more optical power than the counterclockwise propagating mode (CCW). However, the same spectral features are present in their spectrum. This indicates that the counterpropagating modes become coupled due to the spurious reflections. By actively cooling the laser to 12.5°C or below, the heating of the damaged electrical contact is partly counteracted and the device can reach threshold. Spectra were recorded with high resolution for a bias current of 92 mA at two different

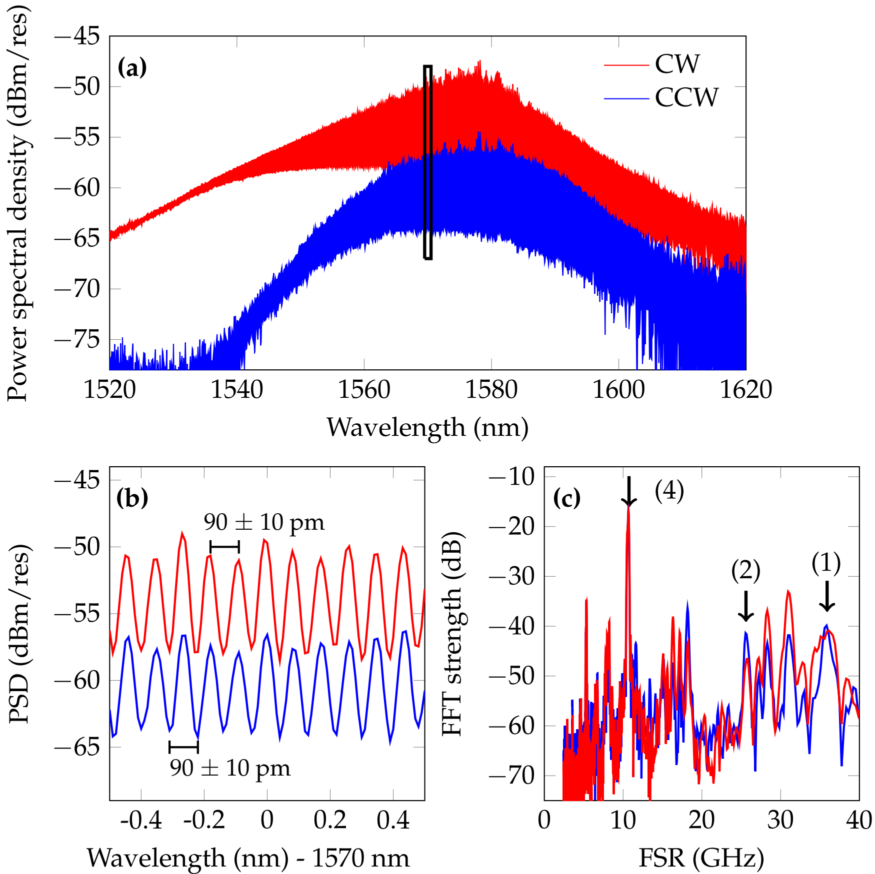


Figure 4.8: Analysis of the sub-threshold amplified spontaneous emission spectra from the damaged laser at 20°C. (a) ASE spectra at 100 mA. (b) Detailed view of the gain ripple around 1570 nm. The dominant oscillation has a period of 90 ± 10 pm. (c) Spectral distribution of the gain ripple. The arrows indicate the spurious Fabry-Pérot cavities calculated in Table 4.2.

temperatures. Those spectra are shown in Fig. 4.9. From these plots it is again confirmed that the mode spacing matches the FSR of the total cavity including the silicon nitride. It can also be noted that at a higher temperature, the spectrum is centered around a higher wavelength: the peak shifts from 1560.3 nm at 10.3°C to 1563.0 nm at 12.4°C. This can be expected since there is no filter present in the cavity to select a single longitudinal mode.

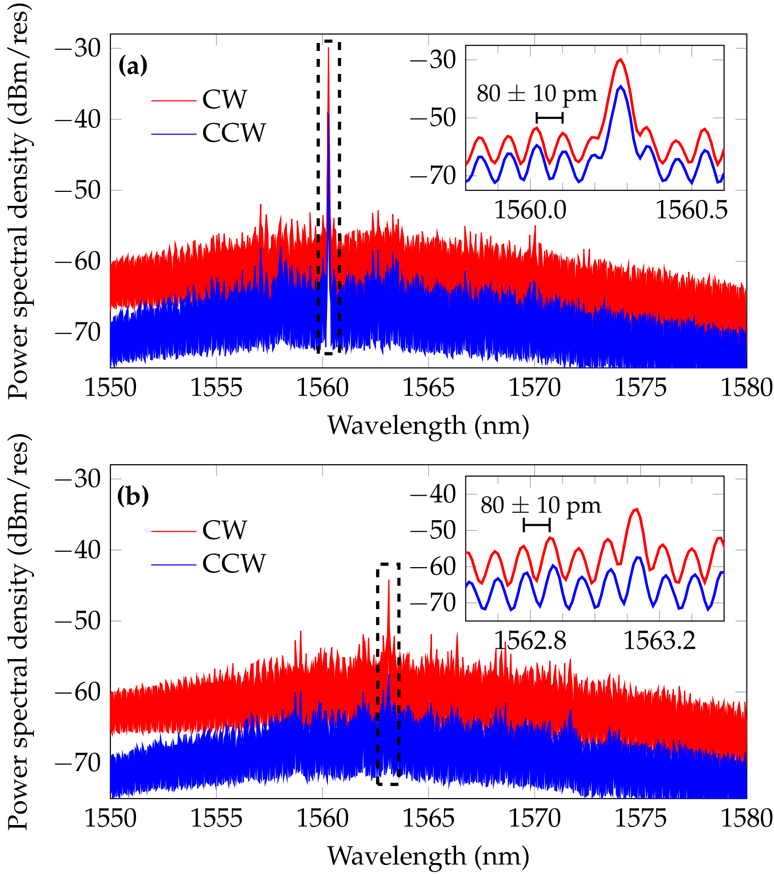


Figure 4.9: Lasing spectra for a bias current of 92 mA at 10.3°C (a) and 12.4°C (b). The insets show a detailed view of the spectrum around the peak wavelength. The measured longitudinal mode spacing is indicated.

4.4 III/V-on-Si_3N_4 single-mode laser

4.4.1 Laser design

A laser cavity was designed for single-mode lasing with cavity mirrors, optical delay and spectral filters in the Si_3N_4 layer. A 1348-µm-long optical amplifier with a 900-µm-long central section provides the gain. A schematic layout of the laser is shown in Fig. 4.10. On one side, the amplifier is connected to a broadband distributed Bragg reflector (DBR) grating by a 5-mm-long single-mode Si_3N_4 waveguide. The DBR mirror is designed to

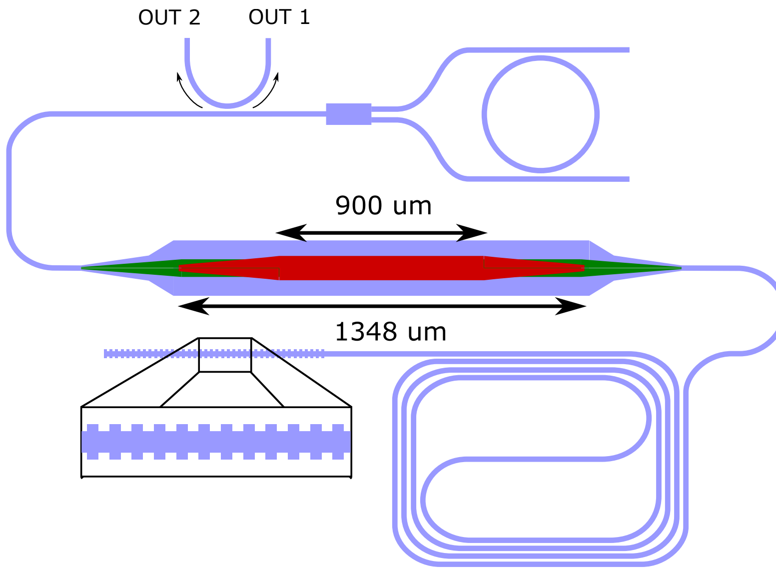


Figure 4.10: Schematic layout of the heterogeneously integrated single-mode laser. The III/V SOA has a longer central section of 900 µm.

have a reflection band of 4 nm wide around a central wavelength of 1570 nm. On the other side of the amplifier, an add-drop ring resonator acts as a spectral filter, reflecting only narrow frequency bands. The ring resonator is designed with a 50 µm radius to have a free spectral range of 4.1 nm, such that only one of its resonances lies within the reflection band of the DBR. Furthermore, the width of the resonance has to be sufficiently narrow to avoid two longitudinal modes to start lasing. The longitudinal mode spacing in the cavity is estimated to be 76 pm or 9.3 GHz at 1570 nm. A directional coupler between the ring resonator mirror and the amplifier extracts 20% of the optical power. From the ratio between the two outputs, the reflectivity of the add-drop mirror can be assessed. The gap between the bus waveguide and the ring was varied in order to test multiple points on the reflection-bandwidth curve of the ring resonator. In the remainder of this section, we will discuss the results of two devices with gaps of 600 nm (”Device A”) and 700 nm (”Device B”), corresponding to targeted power coupling coefficients of 3% and 1.5%.

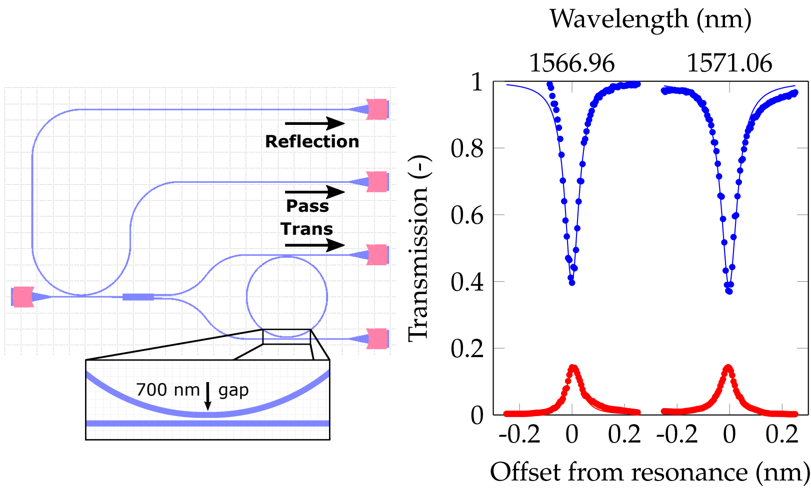


Figure 4.11: (a) Test structure for measuring the mirror losses of device B, with a bus-ring gap of 700 nm. (b) Normalized transmission and reflection data and their fits. The fitting parameters are listed in Table 4.3.

4.4.2 Test structure feedback

The performance of this laser is strongly dependent on the characteristics of the ring resonator mirror. Losses in the mirror will result in an increased cavity roundtrip loss and less frequency selective filtering. A separate structure with a topologically identical mirror accompanied each laser. The characterization of the mirror of device B will be presented here. The test structure is shown in Fig. 4.11a. The **original purpose** was to test the full mirror including the 1x2 splitter. A directional coupler extracts a small fraction of the light for measurement. The power in the Pass channel is compared to the power in the Trans channel to determine the power coupling in the directional coupler. This information is then used to compensate for the directional coupler at the output of the Reflection channel. The resonance spectra of the transmitted and reflected light are fitted simultaneously with one set of fitting parameters. **However, in practice**, the uncertainty on the grating coupler probing and spurious Fabry-Pérot effects due to reflections at the grating couplers make it difficult to normalize the reflection data using the information from the Pass channel. Hence, in the fitting, a relative vertical shift between the transmitted and reflected power of the data is allowed. This does not endanger the fitting, as only the shape of the resonances is important, but it removes all information about the excess losses in the 1x2 splitter, making this test structure needlessly complicated.

	k^2 (%)	α (dB/cm)	BW_R (pm)	T_g (ps)	L_{eff} (mm)	T_D (dB)
Res. 1	1.83	8.5	65	40.4	6.3	-8.34
Res. 2	2.14	9.9	74	34.5	5.4	-8.58

Table 4.3: Fitting parameters for the two characterized resonances of device B's ring resonator mirror test structure. Explanation: k^2: power coupling coefficient; α: fitted propagation loss in the ring; BW_R: bandwidth of the reflection at the drop port; T_g: group delay at resonance; L_{eff}: effective waveguide length added to the cavity by the ring; T_D: power transmission to the drop port.

The measured resonances and their fits to the model from Section 3.6 are shown in Fig. 4.11b. The targeted FSR of 4.1 nm was achieved very accurately. The results of the fits are listed in Table 4.3. The bandwidth at the drop port is 65 - 74 pm, similar to the estimated longitudinal mode spacing. The losses are estimated at 8.5 - 9.9 dB/cm instead of the expected 1.1 dB/cm. This is probably due to a combination of scattering losses at the straight bus-ring interface, and radiation losses due to a too tight bending radius. These design parameters later appeared suboptimal, as shown before in Chapter 3. From these parameters, also the group delay of the ring can be estimated and hence the waveguide length which is virtually added to the cavity by the ring. The high losses of the rings limit this to around 5-6 mm. Finally, the return loss of the ring, the power in the drop port, is around -8.5 dB, without including the losses incurred by the 1x2-splitter.
Similar to the analysis in Sec. 4.2.1, we can extract the optical length of the amplifier coupons with 900 µm long central sections, and the optical length of the total a-Si:H-III/V hybrid waveguide, by Fourier transforming subthreshold ASE spectra from a straight amplifier on the chip. The result is an optical length of 6.5 mm, or the equivalent of 3.4 mm of Si_3N_4 waveguide. With this information, we can attempt to estimate the longitudinal mode spacing in the cavity more accurately. The equivalent length of the cavity, if it consisted only of Si_3N_4 waveguides, is:

$$L_{\text{tot}} = L_{\text{ring}} + 2 \cdot (L_{\text{rout}} + L_{\text{a-Si:H-SOA}} + L_{\text{cav}}) + L_{\text{DBR}}, \quad (4.10)$$

$$L_{\text{tot}}(\text{mm}) = 6 + 2 \cdot (0.5 + 3.4 + 5) + 0.5 = 24.3 \text{ mm}. \quad (4.11)$$

The contribution of the mirrors is only counted once, whereas the length in between is counted double. For the DBR mirror, the approximation is made that the light travels halfway the DBR and then back, as it is not the major

contributor to the cavity length. This results in a longitudinal mode spacing (at 1570 nm) of:

$$FSR_{\text{cav}} = \frac{\lambda^2}{n_g \cdot L_{\text{cav}}} = 53.1\ \text{pm} = 6.45\ \text{GHz}. \tag{4.12}$$

This is a lower limit of the mode spacing, at resonance. Off-resonance, the group delay in the ring decreases. This lower limit is smaller than expected, but not smaller than half the ring mirror bandwidth, which should guarantee at least 3 dB side-mode suppression when the lasing mode is aligned with the ring resonance.

4.4.3 Laser output characterization

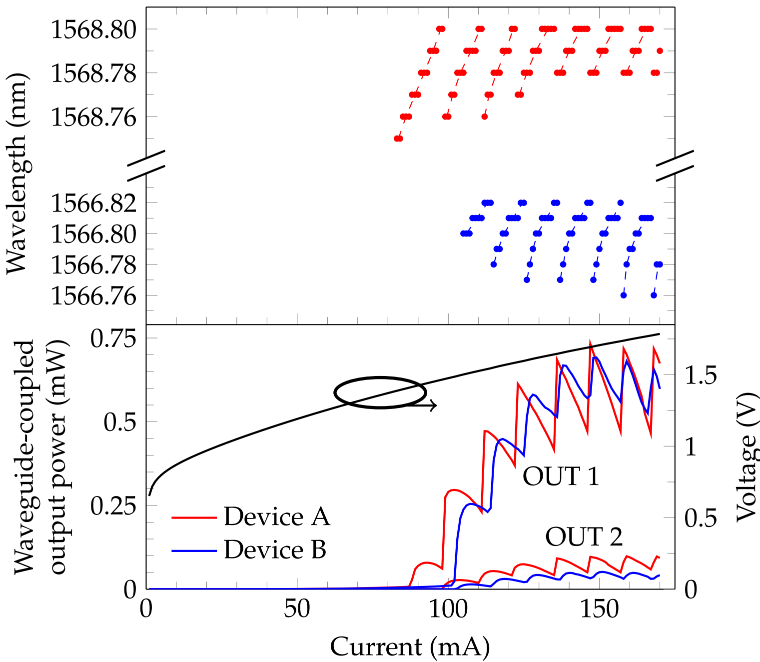


Figure 4.12: Characterisation of the single-mode laser. (down) Light-current (LI) curves of the two outputs of both devices and the current-voltage (IV) curve of device B. (up) Lasing wavelengths of both devices. The dashed lines serve as a guide to the eye.

For the characterization of this laser, the same measurement method is used as for the multimode laser in Section 4.3. The laser is characterized

by measuring the optical output power and spectrum as a function of bias current at 20°C. The measured voltage and on-chip optical output power are plotted against the bias current in Fig. 4.12, as well as the recorded lasing wavelengths. The output power from the main output waveguide reaches 732 µW at 147 mA for device A and 691 µW at 149 mA for device B. Given the estimated outcoupling efficiency of the directional coupler of 20%, the estimated steady-state output power of the amplifier in the cavity is 3.66 mW and 3.45 mW for devices A and B respectively. Mode-hopping takes place every 7-14 mA, due to plasma dispersion and thermal effects on the refractive index in the amplifier. The modes hop maximally 60±10 pm, which confirms our estimation of the FSR of the cavity. The slope efficiency is difficult to assess from the simple bias current sweep, as the roundtrip phase of the lasing mode is not controlled and the precise offset of the longitudinal relative to the ring's resonance will influence the return loss of the mirror and hence the output power of the laser. As mentioned before, the mirror's reflection loss, which includes any insertion loss in the 1x2-splitter, can be estimated from the ratio of the powers measured at both outputs, taking into account that 20% of the light is extracted from the cavity before reaching the mirror:

$$R_{MRR} = \frac{P_{\text{out,2}}}{0.8 \cdot P_{\text{out,1}}} \tag{4.13}$$

Figure 4.13 shows the return loss of the two devices calculated using Eq. (4.13). As expected, device A has a lower reflection loss as it has a smaller gap and higher power coupling, which results in a higher power at the drop port. The ring resonator in device A will have a wider resonance width. This is also clear from the fact that when the mode hops, the new lasing mode in device A is already very close to the resonant wavelength (i.e. the point with lowest return loss), whereas in device B it is still further away. The return loss of the mirror in device B is 1.5 - 2 dB lower than the return loss of the ring. This difference can be attributed to a small error in the calculation of Eq. (4.13) and the excess losses of the 1x2-splitter, which are suffered twice.

Lasing spectra of both devices showing a single peak at a bias current of 158 mA and 20°C are shown in Fig. 4.14a. The reflection band of the DBR, spanning from 1565 nm to 1569 nm, can be discerned in the ASE background on the optical spectrum. The difference in lasing wavelength stems from a small variation in the ring radius; the ring resonator in device A has a radius of 51 µm, as opposed to the 50 µm radius in device B. This variation was introduced to reduce the risk of the ring resonances being out of the DBR's reflection band. Figure 4.14b shows the RF spectrum of the beat note

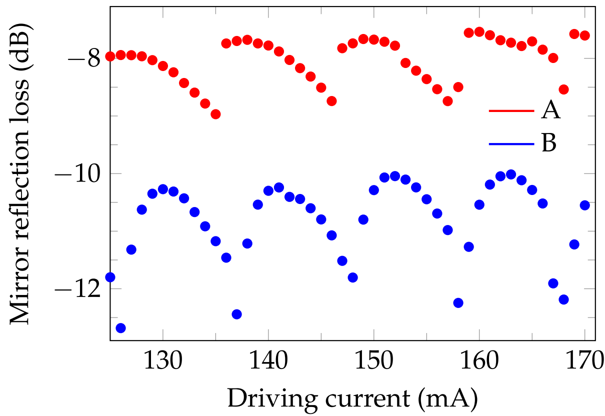


Figure 4.13: Reflection loss of the microring resonator mirror for the two measured devices. As expected, device A with stronger power coupling has a lower return loss.

of device B with a with an external laser. If multiple adjacent longitudinal modes would be able to start lasing, extra peaks would be expected with a spacing of around 9 GHz. Only one peak is visible in the spectrum with a signal-to-noise ratio of >30 dB, showing that any side-mode is suppressed at least 15 dB optically.

4.5 Widely tunable, low-loss, single-mode III/V-on-Si_3N_4 laser

The last piece of the puzzle is a single-mode laser featuring wavelength tuning over a wide range, preferably with a low fundamental phase noise for a highly coherent output. This is a relevant component for coherent communications with a complex modulation format.

4.5.1 Laser design

A schematic drawing of the design of the single-mode widely tunable laser is shown in Fig. 4.15. On one side of the amplifier, a Vernier ring resonator mirror is used to reflect a single longitudinal mode. Heaters are added on top of both ring resonators for thermal tuning of the lasing wavelength over the whole free spectral range of the mirror. On the other side of the amplifier, a Sagnac mirror acts as a broadband, partially reflecting mirror. The transmission through the Sagnac mirror is the output port of the laser.

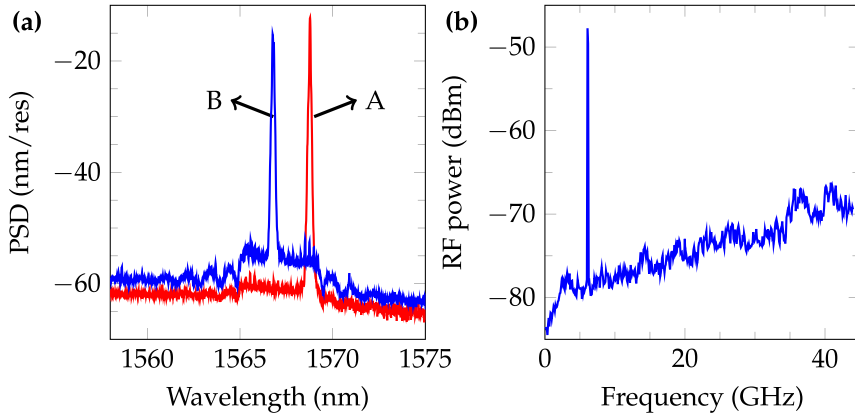


Figure 4.14: (a) Lasing spectra of the two lasers at a bias current of 158 mA. The reflection band of the DBR grating can be discerned in the ASE background. The difference in lasing frequency between the two devices originates from an intentional small offset in the ring radius. (b) Electrical spectrum of the beat note between device B and an external laser, showing only one peak above the noise floor with over 30 dB extinction.

The waveguides at the side of the Vernier mirror that contain the rejected light can be used to monitor the resonance frequencies of the individual rings. A waveguide spiral acting as a delay line is included between the amplifier and the Sagnac mirror to prolong the photon lifetime in the cavity and reduce the fundamental linewidth. On top of this spiral, another heater is added to fine-tune the roundtrip phase of the lasing mode. The delay line is added at the side of the Sagnac mirror to have more balanced losses on either side of the amplifier, as the Vernier mirror is expected to have a higher return loss.

Vernier mirror design

The Vernier ring mirror should have a total FSR of 40 nm and the losses should be as low as possible to have both a low return loss and a narrow bandwidth at the peak wavelength. The bus waveguides of the rings are designed symmetrically, i.e. with the same bending radius as the rings, to minimize the losses. This is based on the results from Section 3.6.2. Given the group index of the ring waveguide (W_{WG} = 1.5 µm, n_g = 1.91) and a bending radius of 100 µm, the free spectral range of one ring will be 2.05 nm around 1570 nm. A total Vernier FSR of around 40 nm could then be achieved by increasing the radius of the second ring by 5% (roughly the

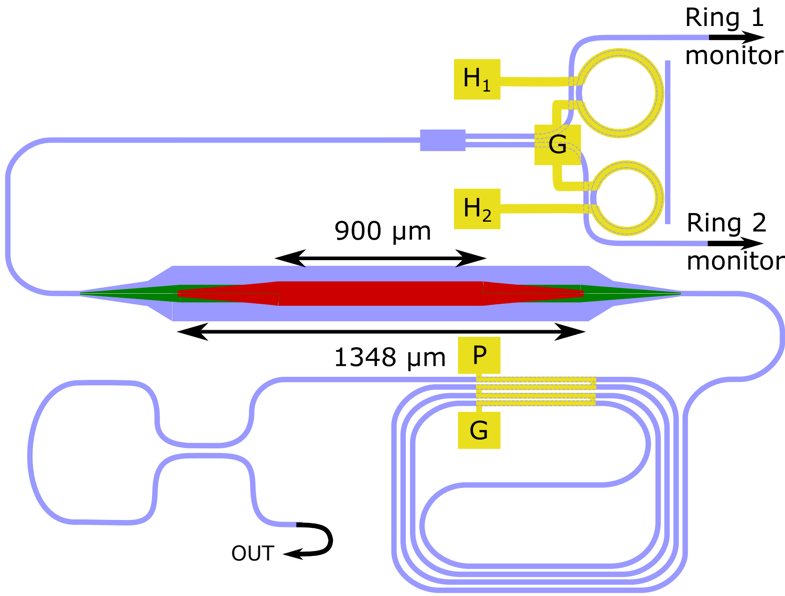


Figure 4.15: Schematic layout of the heterogeneously integrated tunable laser. The design features only one output through the use of a Sagnac mirror. Heaters are included on the ring resonators to tune the lasing wavelength, as well as on the Si_3N_4 waveguide to fine-tune the phase of the lasing mode.

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ratio of the ring's FSR to the desired total FSR) to 105 µm. This is obvious from Eq. (3.20):

$$\mathrm{FSR_{tot}} = \frac{\mathrm{FSR} \cdot \mathrm{FSR} \cdot 1.05}{0.05 \cdot \mathrm{FSR}} = 21 \cdot \mathrm{FSR} \simeq 43 \text{ nm}. \tag{4.14}$$

Two mirrors are designed, with different gaps between the bus waveguides and the rings. The design from Fig. 3.12e is used, of which the relevant measurement data are plotted in Figs. 3.13c and 3.13d. Add-drop rings with gaps of 600 nm and 700 nm have a return loss between 1 dB and 3 dB, with a reflected bandwidth of 2 - 4 GHz. In a Vernier configuration the return loss would then be between 2 dB and 6 dB. Figure 4.16 shows the characteristics of a Vernier mirror for a range of coupling coefficients and three different propagation losses, simulated with Lumerical's INTERCONNECT software. The simulation results indicate that the reflected bandwidth of the Vernier mirror will be in the range 1.5 GHz - 2 GHz, with side-peak rejections well over 10 dB. The Vernier mirrors with 600 nm and 700 nm gaps will have a group delay of respectively 200 ps and 291 ps, which is a delay equivalent

to respectively 3.1 cm and 4.6 cm Si_3N_4 waveguide (single-pass).

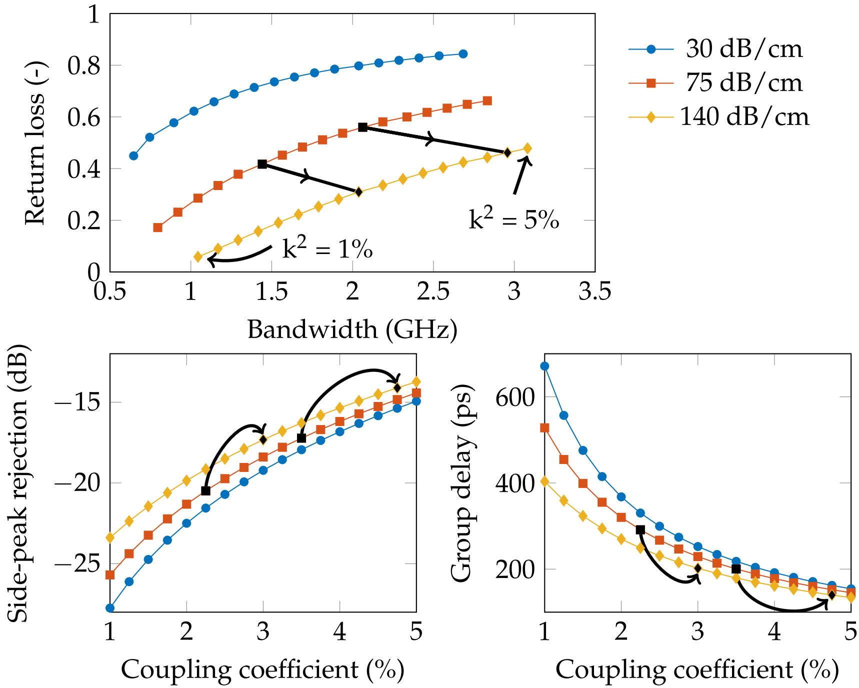


Figure 4.16: Simulated Vernier mirror characteristics for three propagation loss values: in air cladding, in BCB cladding (from Fig. 3.13) , and as measured in the final device (see Section 4.5.2). The arrows connecting the blackened points indicate the change from design to the measured situation.

Cavity design

The long Si_3N_4 cavities of the laser are usually wound up in a spiral for compactness. This introduces a number of bends in the cavity. At the interface between the straight and the bent waveguide, there is a small modal mismatch. The overlap between the two modes is 99.703% for waveguides of 1.5 µm wide in BCB cladding and a bend radius of 100 µm. Every bend has two interfaces with a straight waveguide and hence after every bend only 99.407% of the power remains, corresponding to a loss of 1 dB per 38 bends. In the used design, also shown in Fig. 4.15, a spiral with N windings has $8N + 2$ bends. Spirals with 2, 3 and 4 windings will suffer respectively 0.5 dB, 0.7 dB and 0.9 dB excess losses because of the bends. To prevent this

excess loss, adiabatic bends are implemented, which taper the mode from a straight waveguide to a bend radius of 100 µm over an arc of 15°.

4.5.2 Test structure feedback

Vernier mirror measurement

Figure 4.17 shows a resonance around 1570 nm of test add-drop rings with gaps of 600 nm and 700 nm. The expected behaviour of a perfectly aligned Vernier mirror can be estimated from the fitting results of the drop port. On a logarithmic scale, the expected behaviour of the Vernier is simply twice the response of the drop port of the single ring. This is indicated by the dashed black lines. The fitting parameters and the targeted parameters (from Fig. 3.13) are listed in Table 4.4. Both the coupling coefficient and the propagation loss are higher than expected, leading to a wider response and a higher return loss. This could either be due to process variations, or to the presence of the metal heater above the ring. A test structure for the Vernier mirror with gaps of 600 nm was also characterized and the FSR of 40 nm was confirmed. Although heaters were present on the test structure, it was only characterized as is. Around 1550 nm, the resonances of the two add-drop rings were almost perfectly aligned. This resonance and its two neighbours are shown in Fig. 4.18. From the splitting in the two neighbouring peaks, we can assess that the resonances in the center are still around 15 pm misaligned. Nevertheless, already just over 10 dB of suppression is achieved with a bandwidth of approximately 25 pm (3.1 GHz). This corresponds well with the value simulated in Fig. 4.16.

	k^2 (%)	α (dB/cm)	RL_R (dB)	BW_R (GHz)	RL_V (dB)	BW_V (GHz)
600 nm (targeted)	3.5	0.7	-1.2	3.2	-2.3	2.1
600 nm (measured)	4.8	1.3	-1.6	4.7	-3.1	3.0
700 nm (targeted)	2.3	0.7	-1.7	2.3	-3.4	1.4
700 nm (measured)	3.1	1.4	-2.5	3.3	-5.0	2.1

Table 4.4: Fitting parameters for the characterized resonances of the ring resonator test structures. Explanation: k^2: power coupling coefficient; α: fitted propagation loss in the ring; RL_R: return loss of the ring; BW_R: bandwidth of the reflection at the drop port; RL_V: return loss of the Vernier mirror; BW_V: reflected bandwidth of the Vernier mirror

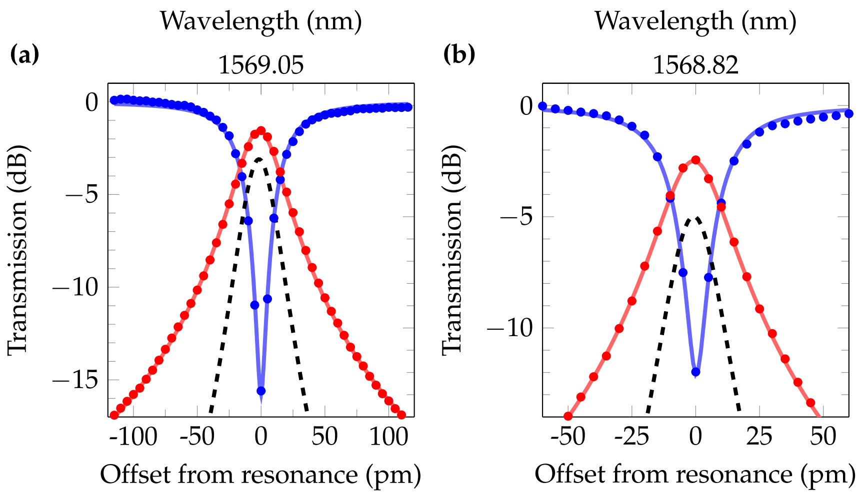


Figure 4.17: Fitted resonances from test add-drop rings with gaps of (a) 600 nm and (b) 700 nm. The dashed black line indicates the expected behaviour of the Vernier mirror, based on the behaviour of the drop-port.

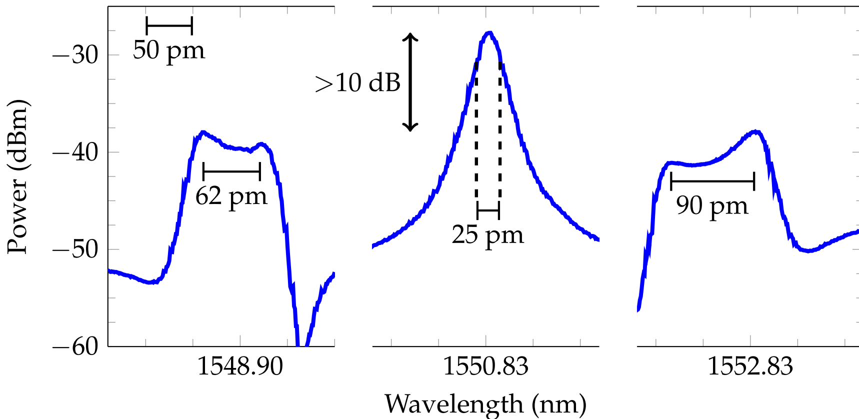


Figure 4.18: Spontaneously aligned resonance and its neighbours in the Vernier mirror with 600 nm gaps. The two resonances forming the central peak are still around 15 pm misaligned. The bandwidth of the central peak is now around 25 pm (3.1 GHz) and could decrease a bit when the misalignment is counteracted. The side-peak rejection is over 10 dB.

Heaters

A simple all-pass ring resonator with a heater on top was used as a test structure for the heater (Fig. 4.19). Its tuning efficiency was almost three

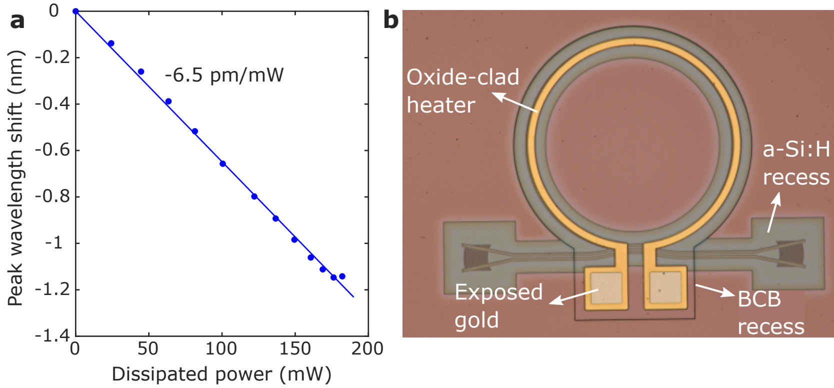


Figure 4.19: (a) Resonance tuning of the heater as a function of dissipated electrical power. (b) Microscope image of the test structure for the heater, before the deposition of thick gold contacts.

times lower than in the first experiment, described in Section 2.7, where it was -17 pm/mW. This is most likely due to the extra safety margin in the thickness of the BCB layer between the Si_3N_4 waveguide and the heater. It was targeted to be between 2.8 µm and 3 µm to avoid excess losses in the ring caused by the proximity of the metal. The heater showed linear behaviour up till around 180 mW dissipated power. The total resonance shift is around 1.1 nm, which corresponds to a shift just over half of the FSR of the ring. This limits the tuning range of the laser and could prevent lasing altogether if the resonances of the Vernier mirror are aligned too far off the gain peak of the amplifier. The contour of the recess in the BCB cladding around the heater is visible in the microscope image. The darker yellow colour of the gold on the heater originates from its silicon oxide top cladding. On the contacts, this oxide is locally removed.

4.5.3 Laser characterization

After finishing the fabrication, the IV-curves of the amplifiers were measured (see Fig. 4.20). The resistance, which ideally goes down to 5 Ω, stayed at 16 Ω at a voltage of 2.5 V for the two best devices. For the others, the resistance was even higher. The two best devices were tested and the output from the control channels at the Vernier mirror was sent to an optical spectrum analyzer to align the mirror near the expected gain peak wavelength of 1570 nm. The limited tuning range of the rings did not allow to align the resonances near the gain peak and no lasing was observed. A

rapid thermal anneal (RTA) to 430°C was performed to try and improve the contacts. However, this step caused delamination of the oxide which was left on the BCB layer, which made it impossible to probe the grating couplers in further experiments.

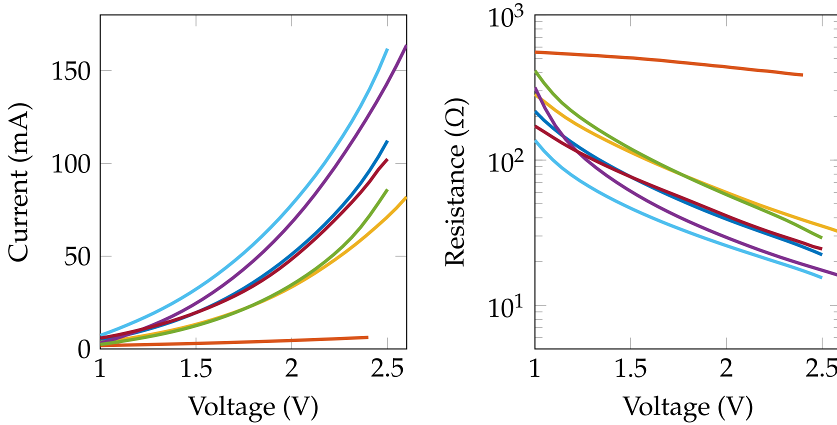


Figure 4.20: Electrical characterization of the III-V amplifiers.

4.5.4 Conclusion

The relationship between the separation of heaters from the Si_3N_4 waveguide, their efficiency and the propagation loss should be further investigated to improve the reliability of the heaters for tuning over the full FSR of the ring resonators. Despite the widespread delamination of the oxide layer, due to its bad adhesion to the underlying BCB, the heaters were not damaged. This is probably due to the fact that the heaters were placed in a local recess. Delamination starting elsewhere on the chip seems not to be able to continue over the recess edges. Nevertheless, the removal of the oxide layer where it is not needed, and especially above the optical in- and outputs, should be implemented in future runs.

5

Back-end integration of Si waveguides and III/V amplifiers on lithium niobate

The illiterate of the 21st century will not be those who cannot read and write, but those who cannot learn, unlearn, and relearn.
Alvin Toffler

5.1 Introduction

In this chapter, we describe the process for the heterogeneous integration of III/V amplifiers on oxide-clad thin-film lithium niobate ($LiNbO_3$, LN) waveguides using two steps of micro-transfer printing. After defining local recesses in the oxide cladding down to the waveguide layer, a block of crystalline silicon is micro-transfer printed on the LN. An interlayer taper is defined in this coupon using E-beam lithography for a higher accuracy alignment. At this point, the sample is ready for the transfer printing of the III-V SOA. Since we start from a fully cladded target sample, this can be considered as a generic and flexible process for any waveguide platform with core refractive indices around 2 and medium-high index contrasts. In contrast to the thin-film LN-on-insulator (LNOI) material stack, which is

commercially available, the substrate in this work is sapphire (Al_2O_3). This platform was developed by our collaborating partners at the Laboratory for Integrated Nano-Quantum Systems (LINQS) at Stanford University [170]. The sapphire substrate has a lower refractive index than the LN, making an intermediate oxide layer such as in LNOI or SOI unnecessary. This improves the thermal resistance to the substrate and yields very good microwave properties of transmission lines on the LN layer. This in turn is important to maximally exploit the second order nonlinearity of the LN. A schematic cross-section of the platform is drawn in Fig. 5.1. It contains rib waveguides in the LN layer and electrodes to apply an electric field over some waveguides. For the integration process, we add the functionality of an extra silicon waveguide layer in a local recess. On top of this Si layer, III-V SOAs can be transfer printed. Vias are also added for the electrical contacting of the electrodes on the LN layer.

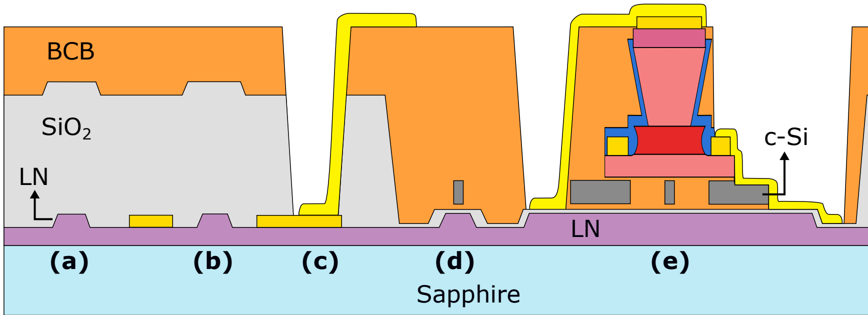


Figure 5.1: Cross-section showing the possible features of the platform after back-end integration. (a) Rib waveguide in the LN layer. (b) Rib waveguide with electrodes for electro-optic phase shifting. (c) Via to contact the phase shifter electrodes. (d) Waveguide transition between the LN layer and the c-Si layer. (e) III-V semiconductor optical amplifier integrated on a c-Si waveguide. The layer stack of the amplifier is shown in Section 2.6. The last two features are located in a local recess in the oxide top cladding.

5.2 Preparation of SOI coupons for micro-transfer printing

Instead of using hydrogenated amorphous silicon, which can suffer from varying material quality and layer thicknesses, coupons of crystalline silicon can be micro-transfer printed onto the target. This offers the benefit of a more uniform and higher quality intermediate layer for the amplifier. This

in turn will result in a more reproducible behaviour of the amplifiers. As a starting point we used wafers with a 390 nm thick layer of SOI on a 2 µm thick buried oxide. The fabrication of the blank SOI coupons does not consist of many steps. First, the coupon boundaries and tethers are defined, as shown in Figs. 5.2a-5.2b. The coupons are 1670 µm by 46 µm. The tethers connect the coupon to the rest of the non-etched SOI, which acts as a support structure. The smallest feature in this design, a part of the tethers, is 750 nm. The patterning can hence be done with a high-current mode in the E-beam, or even using a high-resolution contact lithography mask. Using reactive ion etching, the pattern is etched through the SOI layer into the underlying oxide (Fig. 5.2b). Consequently, the silicon oxide layer is etched away using vapour-phase hydrofluoric acid (HF) etching at 40°C during 4 hours (Fig. 5.2c). As this etch is isotropic, also 23 µm of silicon oxide is etched underneath the support structure on either side of the coupon. The stability of the support structure puts an upper limit to the density of coupons, unlike in the case of III/V coupons, where the tethers are connected to the substrate. The coupons can be picked up by pressing on them with a PDMS stamp with a width of 60 µm, 14 µm wider than the coupon itself (Fig. 5.2d). This relaxes the alignment tolerance during pick-up.

5.3 Preparation of the target substrate

The target substrate consists of oxide-clad lithium niobate rib waveguides, sitting directly on a sapphire substrate. Lithium niobate is an electro-optic material with a uniaxial birefringence. This means that the refractive index of light polarized along its optic axis (the extraordinary refractive index, n_e = 2.13) is different from light polarized perpendicular to the optic axis (the ordinary refractive index, n_o = 2.21). Sapphire has a lower refractive index of 1.74 (all values at 1550 nm), hence, there is no need for a buried oxide layer such as on silicon substrates. The starting wafers were fabricated by NGK Insulator. The lithium niobate layer thickness increased towards one edge of the sample, ranging from 450 nm to 510 nm, and the etch depth of the rib waveguides was around 280 nm. The waveguides are patterned in a negative process, i.e. the waveguides are exposed and everything else will be etched away. This is the opposite of the integration process on a-Si:H-on-Si_3N_4 (Section 2.5), where the topography of the sample featured local holes instead of local extrusions. In order to offer support for the SOI and III/V coupons, the transfer printing sites are designed as 80 µm wide slabs. The electro-optic effect can be used to induce a change in LN's refractive index, proportional to an applied voltage. To this end, metal electrodes

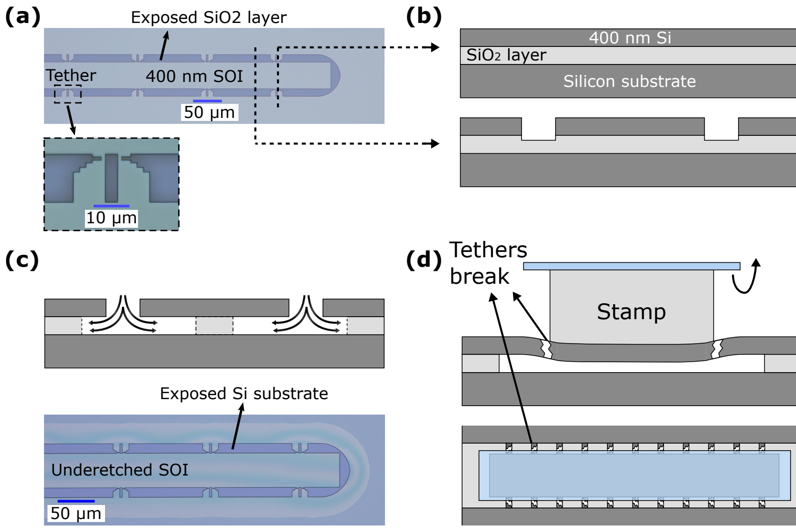


Figure 5.2: SOI coupon source sample preparation steps. (a) Patterning the SOI layer to expose the buried oxide. (b) Cross-sections of a coupon with and without a tether. (c) Underetching the coupon with hydrofluoric acid. (d) Picking up the SOI coupon. The tethers break when the stamp is pressed against the sample's surface.

are placed around some waveguides in the circuit. Finally, the sample is clad with silicon oxide, but not planarized, so the topography of the LN waveguide layer is still present on the top surface of the silicon oxide. A schematic cross-section of the described sample with the relevant features is shown in Fig. 5.3a. These samples were fabricated by collaborators from the Laboratory for Integrated Nano-Quantum Systems (LINQS) at Stanford University.

In order to prepare these cladded samples for the heterogeneous integration of III/V amplifiers, a few processing steps are needed. First, local recesses are etched around the alignment markers (for visibility in the E-beam) and around the transfer printing location, using a thick positive photoresist (AZ 10XT 520 CP, 6.3 µm and RIE etching (Fig. 5.3b). The etching is monitored in order to leave a layer of around 70 nm of SiO_2 cladding on top of the lithium niobate at the transfer printing site. On the alignment marker, all oxide is removed. Second, a layer of 40 nm aluminum oxide is evaporated on the sample to serve as an etch-stop layer later on, to protect the exposed LN waveguides during the etching of the SOI coupon (Fig. 5.3c). Subsequently,

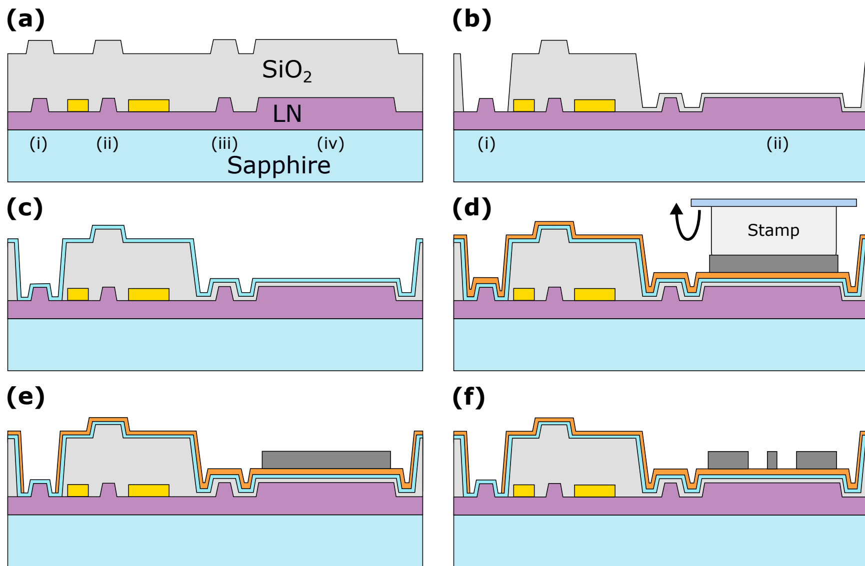


Figure 5.3: Target sample preparation steps. (a) The starting point is a non-planarized, oxide clad sample featuring (i) alignment markers, (ii) rib waveguides with electrodes for electro-optic tuning, (iii) waveguides for transitioning to the Si waveguide layer, and (iv) transfer printing sites. (b) Local recess definition around (i) alignment markers (opened completely) and (ii) TP sites ($\pm$70 nm SiO_2 left). (c) Evaporation of AlO_x etch-stop layer. (d) Spincoating adhesive BCB layer and micro-transfer printing SOI coupon. (e) Opening up the alignment markers for a better contrast in the E-beam. (f) Patterning the SOI coupon.

a thin adhesive layer of BCB is spincoated on the sample and loaded in the X-Celeprint µTP-100 tool, together with the source sample of the SOI coupons. The target sample is heated to 70°C to improve the adhesion of the coupon. SOI coupons of 1670 µm by 46 µm are then printed in the opened recesses (Fig. 5.3d). The lateral alignment of the coupons to the target waveguides is less critical in this step and can be done manually without needing any alignment markers. The longitudinal alignment remains important in order to fit the desired pattern on it afterwards. After printing all coupons, the sample is placed in an oven to cure the adhesive BCB layer at a temperature of 280°C. Afterwards, the BCB is stripped from the E-beam alignment markers to improve the visibility in the E-beam (Fig. 5.3e). Prior to the spincoating of resist for the E-beam patterning, the sample is cleaned in oxygen plasma (PVA TePla Gigabatch) for 20 minutes to improve the resist

adhesion. For the alignment of the waveguide on the SOI coupon to the underlying LN waveguide, the same method is used as for the alignment of the two waveguide layers in the a-Si:H-on-Si_3N_4 platform. A layer of 500 nm of AR-P 6200.13 resist is spincoated on the target sample, followed by a thin layer of conductive polymer (Electra 92). In a first coarse alignment step, the resist covering the alignment markers is exposed, after which the sample is unloaded from the E-beam chamber and developed. After clearing the resist from the alignment markers, a new layer of conductive polymer is spincoated and the sample is loaded in the E-beam chamber again. The exposed alignment markers offer sufficient contrast to align the exposure of the SOI waveguides to the underlying LN waveguides (Fig. 5.3f). After exposure and development, the silicon, and to a much lesser extent the exposed aluminum oxide, are etched using an anisotropic RIE etching recipe. The etch-stop layer allows to safely overetch the SOI waveguide.

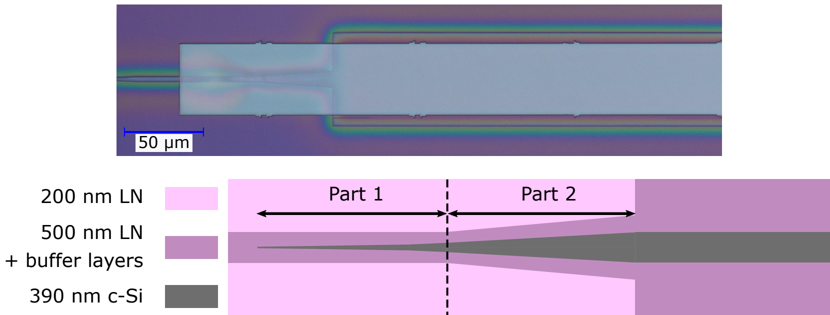


Figure 5.4: (a) c-Si coupon transfer printed on the lithium niobate taper and slab. (b) Layout of the originally designed LN-Si interlayer taper.

The transition between the lithium niobate and the silicon layer has a similar design as the Si_3N_4-a-Si:H transition. Initially, the LN waveguide is 3 µm wide at the taper tip of the Si waveguide, and it becomes wider to accommodate the broadening of the Si. However, as the length of the Si coupon was fixed at 1740 µm (due to a lack of other coupon lengths available at the time), there was an upper limit to the possible taper length. A microscope image of a transfer printed Si coupon on a lithium niobate taper and slab is shown in Fig. 5.4a. The initial taper design consisted of two parts, similar to the taper in Section 3.5: a first part where the mode transitions from a 3 µm wide LN waveguide to a single-mode Si waveguide of 370 nm wide over a length of 50 µm, and a second part where the Si waveguide broadens

to 3 µm, accompanied by a broadening of the LN waveguide, as shown in Fig. 5.4b. The length restriction of the taper made it necessary to shrink the length of the broadening from the initially designed 50 µm to 30 µm and shift the first part of the taper away from the coupon edge.

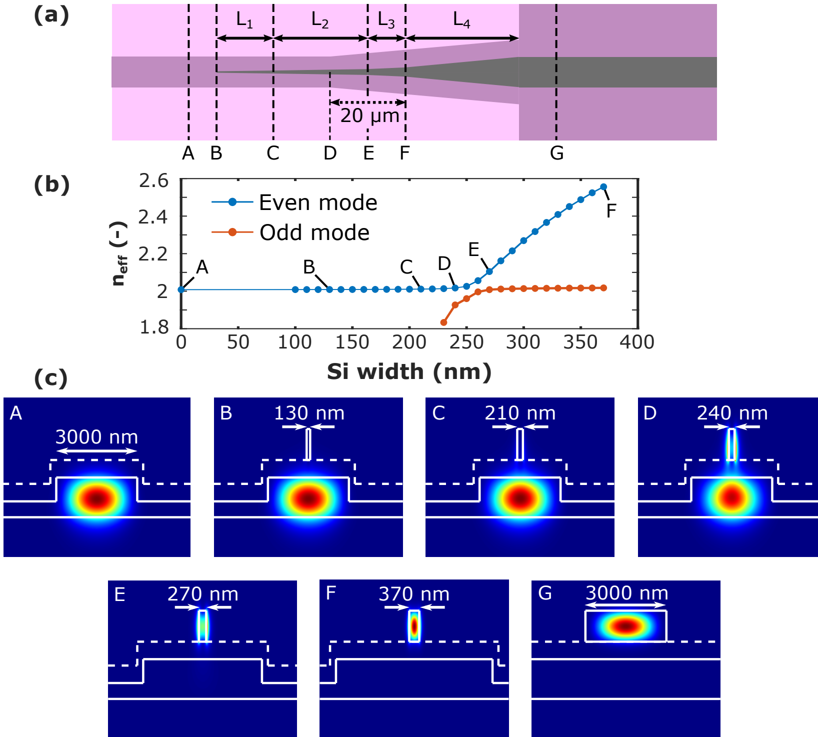


Figure 5.5: LN-Si transition details. (a) Layout of the fabricated LN-Si interlayer taper. (b) Evolution of the effective index of the hybrid LN/Si supermodes in a BCB cladding, showing the phase matching point at a Si width around 260 nm. (c) Mode profiles along the taper. The dashed lines indicate the extent of the SiO_2, AlO_x and BCB layer around the LN waveguide prior the transfer printing of the Si coupon.

The actually used design is shown in Fig. 5.5a. The first part of the taper consists of three distinct tapering angles. First, there is a fast transition from the tip (designed to be 130 nm wide) to a Si width of 210 nm over a length L_1 of 15 µm. Next, the tapering is done slower, over a length L_2 of 25 µm to a Si width of 270 nm, to avoid exciting the odd supermode around the phase matching point. The effective indices of the hybrid LN/Si supermodes are shown in Fig. 5.5b. The phase matching point lies around 260 nm, still in

the slow tapering region. Finally, over a length L_3 of 10 µm the Si width is expanded to 370 nm, where the mode is fully confined in the Si waveguide. The final broadening to a width of 3 µm is done over a length L_4 of 30 µm, which we can assume to be safe from the experimental results of the Si_3N_4-a-Si:H transition. The premature broadening of the LN waveguide compared to the original design does not impact the taper performance. The mode profiles along the taper, shown in Fig. 5.5c, indicate that the fundamental TE mode is not strongly perturbed by the Si waveguide until the latter becomes wider than 210 nm. This indicates that any reflections introduced by this taper will be minimal.

5.4 Heterogeneous integration of III-V semiconductor optical amplifiers & electrical contacting

The heterogeneous integration process described in section 2.6 can be applied on this sample as well. The same amplifier coupons are used in this part, with a central length of 900 µm. The printing process is schematically shown in Fig. 5.6 A solution of 3 parts mesitylene per part BCB 3022-35 is spincoated on the target to apply a thin adhesive layer (Fig. 5.6a). III-V coupons with a central length of 900 µm and a total length of 1315 µm are picked from the source (Fig. 5.6b) and printed on the c-Si coupons (Fig. 5.6c). Afterwards, the photoresist encapsulation is stripped with O_2-plasma in the RIE etcher, and the sample is baked for several hours at 280°C to cure the adhesive BCB layer. Finally a thick BCB layer is spincoated on the sample and cured at 280°C as well (Fig. 5.6d). A transfer printed coupon before the encapsulation removal is shown in Fig. 5.6e.
After the planarization with BCB, successive etching steps are carried out to open up the electrical contacts on the sample, as shown in Fig. 5.7. First, the BCB layer is etched back until the P-contacts of all III-V coupons are exposed (Fig. 5.7a). Next, the modulator contacts are opened up (Fig. 5.7b), followed by the N-contacts of the III-V coupon (Fig. 5.7c). The vias towards these contacts are several microns deep. To ensure a good step coverage of the metal, the positive photoresist (AZ 10XT, 6.3 µm thick) is reflowed by baking the sample at 120°C after the development. This creates a slanted sidewall in the resist, which is transfered in the BCB and silicon oxide claddings. Finally, a layer of 1 µm gold is deposited on the sample for the probing pads (Fig. 5.7d). The vias towards the amplifier's N-contact are designed to be as large as they can be in the recess and etched all the way down to the lithium niobate layer. This improves the heat spreading and the thermal

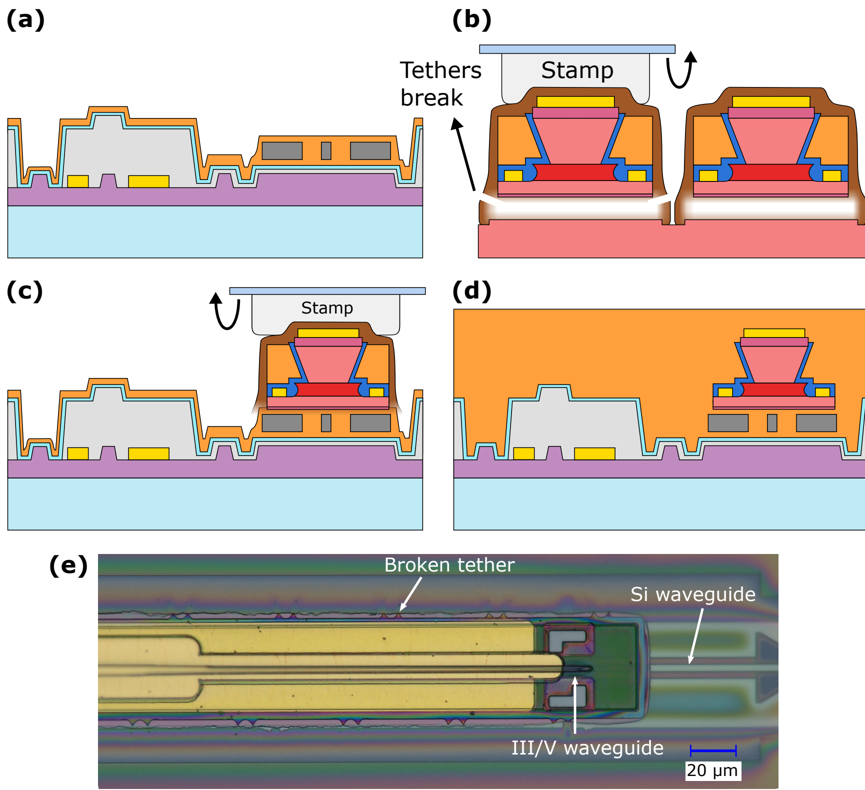


Figure 5.6: Heterogeneous integration of the SOAs on the c-Si coupon. (a) Spincoating a new layer of BCB for adhesion of the coupon. (b) Coupon picked from the source wafer. (c) Coupon printed on the target. (d) Strip encapsulation in O_2-plasma and planarize sample with thick BCB cladding layer. (e) Transfer printed SOA on the Si coupon.

resistance to the sapphire substrate, since there is no thermally insulating layer below the LN, as in the stack from Chapter 2. Also the P-contact is thermally connected to the LN layer using the final metallization layer and the slanted sidewalls of the N-contact vias.

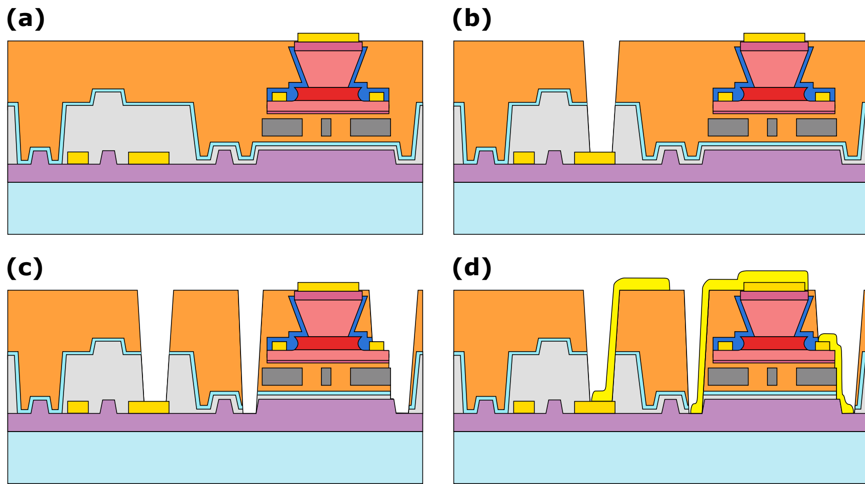


Figure 5.7: Electrical contacting of the SOA coupons and the electro-optic phase shifters. (a) Etching back the BCB to expose the SOA's P-contact. (b) Etching a via down to the phase shifter contacts. (c) Etching vias to open the SOA's N-contacts and expose the LN slab for a good thermal contact to the substrate. (d) Final metallization.

6
Heterogeneously integrated III/V-on-$LiNbO_3$ lasers

When God said "Let there be light" he surely must have meant perfectly coherent light.
Charles H. Townes

6.1 Introduction

In this chapter, the results from the integration of III-V amplifiers on a lithium niobate platform are discussed. Similar to chapter 4, the results of a standalone amplifier, a multimode ring laser, and a single-mode laser will be discussed. The fabrication steps for these devices have been previously described in Chapter 5. Since the lithium niobate platform was not developed by us but by our collaborators are Stanford university, there will be no detailed analysis of the passive components. Only a few key measurement results will be reported. Parts of this chapter have been previously published in [171].

6.2 Passive components and thermal resistance

The grating couplers are designed to have very low reflections. They are probed using standard single-mode fibers angled at 25°. The response of the reference grating coupler for the measurement of the amplifiers is shown in Fig. 6.1a. Lateral misalignment of the fiber can lead to the excitation of the second order mode in the LN waveguide. This manifests itself as a ripple in the transmission spectrum. The period of the ripple (7.5 nm±0.3 nm) is consistent with the length of the waveguide (2047 µm) and the simulated difference in group index between the fundamental and the second order mode (Δn_g = 0.165). A longitudinal misalignment shifts the peak wavelength due to the chirp in the grating period. These effects are obvious when measuring the reference waveguide, but can be difficult to spot when measuring e.g. the amplifier's response.

The losses of the LN-Si transition were measured with test structures containing one, two, three and four pairs of transitions. The losses extracted from this measurement are shown in Fig. 6.1b. Below 1540 nm, the excess losses of going to the Si coupon and back are around 1.5 dB.

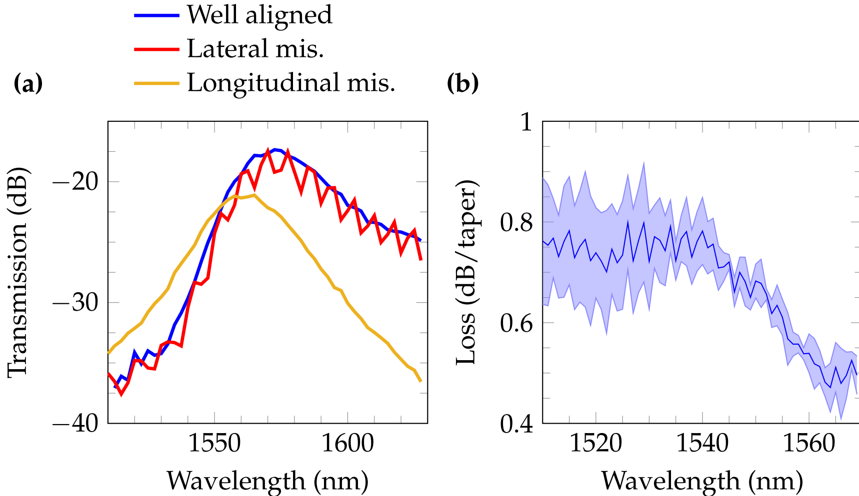


Figure 6.1: Measurement of passive components on the $LiNbO_3$ platform. (a) Grating coupler response and effects of misaligning the fiber. (b) LN-Si taper losses. The shaded area indicates the confidence interval.

The thermal resistance to the substrate was also simulated for this platform.

The two new elements in this simulation are the new materials (LN and sapphire) and their thermal conductivities (resp. 5.6 W/m·K and 35 W/m·K). All other simulation parameters are kept the same as in Section 3.7. As a heat source, again an electrical power dissipation of 200 mW is taken, assuming a device length of 1 mm. The same amplifier stack is used. The BCB bonding layer thickness, both for the amplifier and the c-Si coupon, are 20 nm. The resulting temperature profiles are shown in Fig. 6.2, together with an overlay of the material stacks. Both temperature profiles are plotted on the same scale. The maximal temperature elevation is 12.7°C, corresponding to a thermal impedance of 63.5 K/W. This is only about half of the a-Si:H-on-Si_3N_4 platform and about a third lower than the 400 nm SOI platform. The thermal conductivity of sapphire is 4 times lower than that of silicon, but the absence of the intermediate silicon oxide layer improves the thermal heat sinking capabilities significantly.

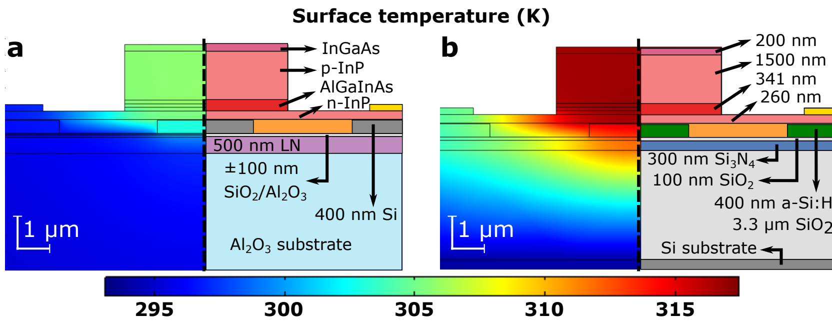


Figure 6.2: Comparison of the thermal behaviour of integrated amplifiers on (a) our c-Si-on-LN platform and (b) our a-Si:H-on-Si_3N_4 platform. The BCB bonding layers are 20 nm thick in both simulations (including the LN-Si bonding layer).

6.3 III/V-on-$LiNbO_3$ amplifier

The III/V-on-$LiNbO_3$ amplifiers are characterized by adding grating couplers on each side for transmission measurements. The processed sample is placed on a temperature-controlled chuck, which is set to a temperature of 20°C. Each device under test (DUT) is accompanied by a nearby reference $LiNbO_3$ waveguide to calibrate the grating coupler efficiency. A schematic layout of the amplifier test structure is shown in Fig. 6.3a. The potential spurious cavities are also indicated.

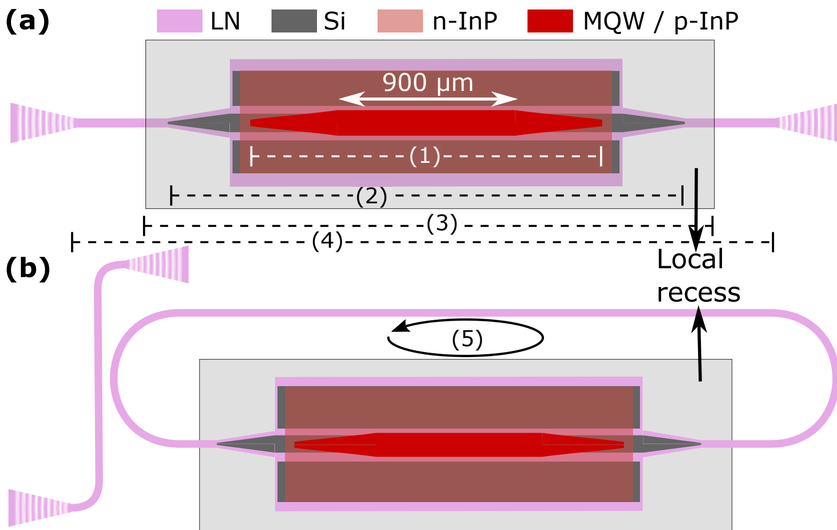


Figure 6.3: Schematic layout of the III/V-on-LiNbO$_3$ amplifier (a) and multimode ring laser (b). The same SOA length is used in both devices. The dashed lines indicate possible spurious cavities of which the FSR is calculated in Table 6.2.

The same characterization as for the amplifiers on Si_3N_4 is done. Figure 6.4 shows a measurement of the saturation of the on-chip gain at 1540 nm with increasing input powers. The response at the two highest bias currents was fitted to the model of Eq. (4.1). The results are shown in the table inset. The highest recorded gain is 10.6 dB. This is lower than the gain recorded in the amplifiers on Si_3N_4, despite using longer coupons. The higher refractive index of c-Si compared to a-Si:H should result in a lower confinement per quantum well and hence a lower gain per unit length, although the lower confinement should be accompanied with a higher saturation power. This is not the case. Losses in the transitions will contribute to this lower performance, although more fabrication runs and experiments are needed to draw conclusions for further optimization.

Figures 6.5a and 6.5b respectively show the wavelength dependence of the gain, and the saturation of the gain at 1540 nm as a function of bias current. The fact that the gain peak is around 1540 nm (instead of at 1570 nm for the amplifiers on Si_3N_4) is a clear proof that the thermal heat sinking is significantly better on the sapphire substrate compared to the Si_3N_4 layer stack. No saturation can be noted at high bias currents, although the effect

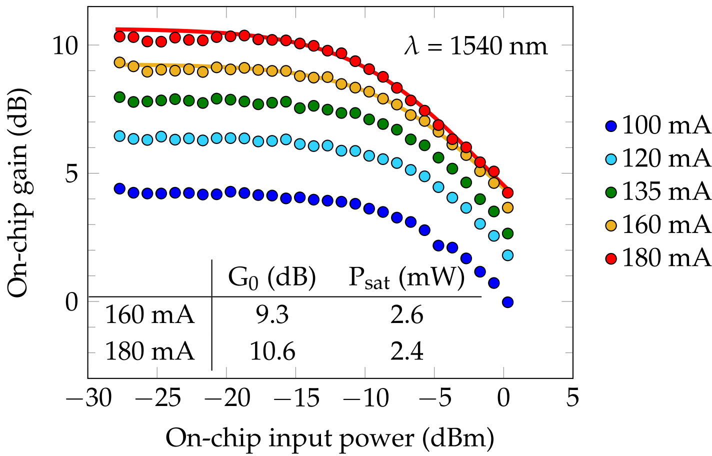


Figure 6.4: On-chip gain of the III-V-on-$LiNbO_3$ amplifier at 1540 nm as a function of on-chip optical input power for different bias currents. The onset of gain compression is visible. The solid lines represent the fit to the gain compression model.

of self-heating starts causing a red-shift of the gain above 120 mA. The bandwidth of the gain is significantly higher than in the measurements on Si_3N_4. The dip in the gain around 1540 nm is not fully understood. It could be due to a systematic misalignment of the fibers (which would skew the whole gain measurement), or due to a spurious cavity.

6.3.1 Spurious reflection analysis

The amplified spontaneous emission was recorded with an optical spectrum analyzer (Anritsu MS9740A) and decomposed with Fourier analysis to investigate the different sources of reflections and to verify the presence of a dip in the gain around 1540 nm. Following the theory from Hakki-Paoli [169], regions in the ASE with strong oscillations either have a high gain, or they suffer from strong feedback (high reflection). Figure 6.6a shows the ASE spectrum of the amplifier at a driving current of 140 mA. Parasitic reflections are causing a strong ripple on the spectrum around 1540-1550 nm. If the gain would suddenly drop by 3-4 dB at 1540 nm, as indicated in Fig. 6.5a, a clear drop in the amplitude of the ripple would be expected centered at 1540 nm (the misalignment between the laser the spectrum analyzer is less than 1 nm). This is not the case, which could indicate that the measured gain is incorrectly estimated.

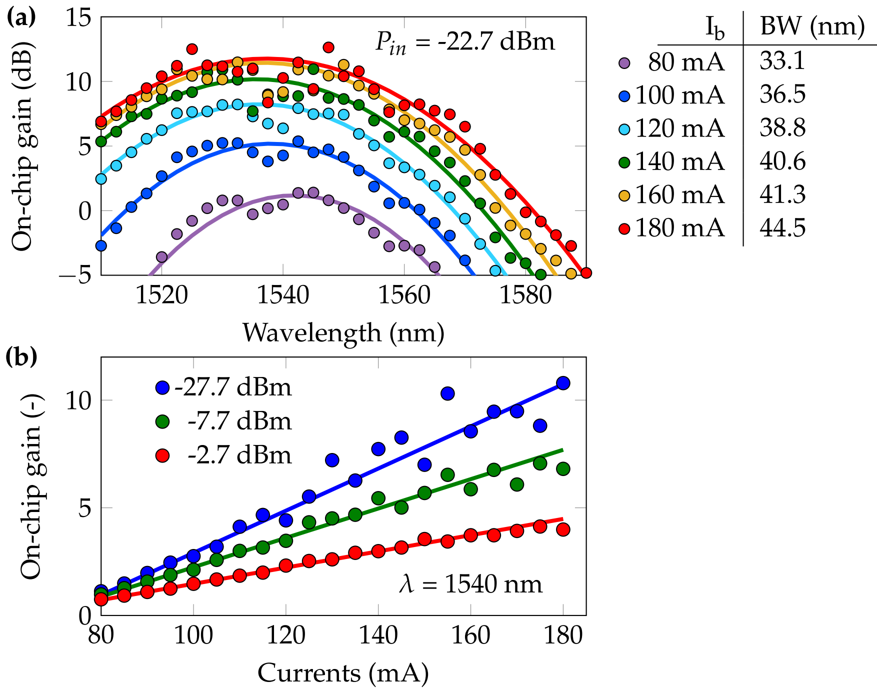


Figure 6.5: (a) Wavelength dependence of the gain of the III-V-on-LiNbO$_3$ amplifier at different bias currents for an optical input power of -22.7 dBm. The legend includes the gain bandwidth, extracted from the fits. (b) On-chip gain of the III-V-on-LiNbO$_3$ amplifier at 1540 nm as a function of bias current for different optical input powers.

The group indices and physical lengths of the different parts of the cavities are listed in Table 6.1. The FSR of the spurious cavities as shown in Fig. 6.3a are listed in Table 6.2. Spectral decomposition of the ASE spectrum (Fig. 6.6b) shows distinct peaks at the estimated FSRs. The FSR of the recess boundaries occurs in the spectrum, but this could also be a combination of reflections on the grating couplers and the c-Si. The standard single-mode width for the lithium niobate waveguides in the components is 1.2 µm. Upon entering the recess, the effective index of the fundamental mode changes from 1.9463 to 1.9517. This would prompt a reflection of only -57 dB based on Snell's law. The overlap between the mode in the recess and the oxide-clad mode is 99.90%. For this reason, no detrimental effects are expected from the recess boundary. The strongest spurious reflection appears to originate from the grating coupler after all.

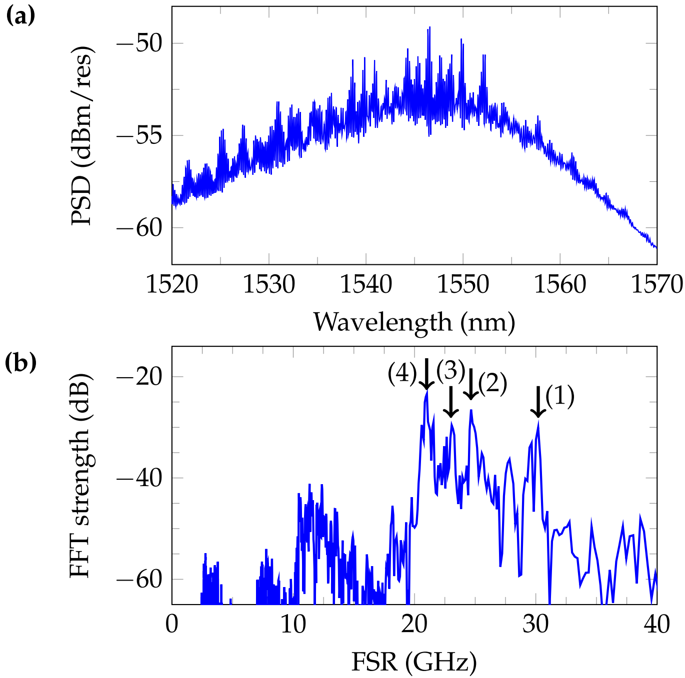


Figure 6.6: Analysis of the amplified spontaneous emission from the amplifier at 20°C. (a) ASE spectrum at a driving current of 140 mA. (b) Spectral distribution of the gain ripple. The arrows indicate the spurious Fabry-Pérot cavities calculated in Table 6.2.

Layer	n_g	Length (µm)
III-V amplifier	3.56	1315
c-Si	3.78	324
$LiNbO_3$ (recess)	2.3	260
$LiNbO_3$ (amp.)	2.3	404
$LiNbO_3$ (las.)	2.3	3965

Table 6.1: Waveguide lengths and group indices in each layer.

Number	L_{opt} (mm)	FSR (GHz)
(1)	4.681	32.0
(2)	5.925	25.3
(3)	6.523	23.0
(4)	6.854	21.9
(5)	15.045	19.9

Table 6.2: Optical length and FSR estimation of the cavities in Fig. 6.3.

6.4 III/V-on-$LiNbO_3$ multimode laser

A more indirect way of characterizing an amplifier is to purposefully provide it with strong feedback and create a simple ring laser by connecting the two outputs. A directional coupler in the LN waveguide layer extracts a portion of the light each roundtrip. The gap in the directional coupler is 550 nm. When the amplifier's gain overcomes the propagation losses, the excess loss from the different layer transitions and the loss from the light extracted by the directional coupler, it will start lasing. In Fig. 6.7, a few lasing spectra are shown at different bias currents at 20°C. A modest red-shift in the lasing wavelength (and hence gain peak) can be observed at higher bias currents. The fact that the lasing starts at 1540 nm is another indicator that the measured dip in the gain of the amplifier is an artefact of the measurement, and not a property of the amplifier itself.

The operation of the laser at higher wavelengths was also tested to assess the temperature dependence of the gain in the amplifier. The results are shown in Fig. 6.8a. The threshold increases from 85 mA at 20°C to 165 mA at 60°C. The measured output power reaches 0.42 mW on chip. Figure 6.8b compares the CW and the CCW output of the laser. The modes appear coupled, most likely by the reflectors indicated in Fig. 6.3. At some current levels, a switch of the lasing direction can be observed.

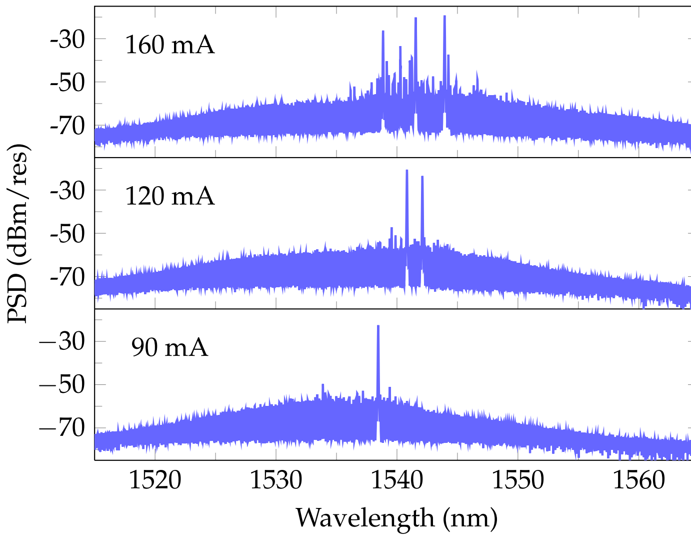


Figure 6.7: Lasing spectra of the multimode laser at 20°C, showing a redshift of the lasing wavelength at higher bias currents.

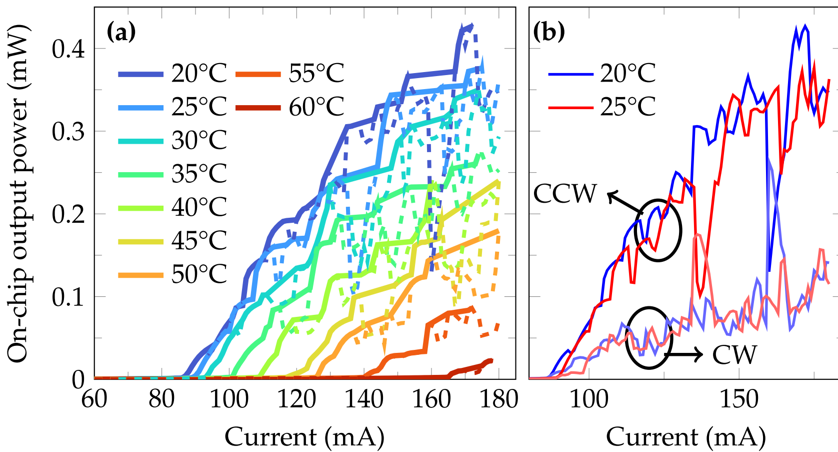


Figure 6.8: (a) Temperature dependence of the ring laser's CCW output. The dashed lines represent the actual data. For clarity, the monotonously increasing envelope is highlighted by full lines. (b) Comparison of CW and CCW output. Clear mode coupling and switching of the dominant mode can be observed.

6.5 III/V-on-LiNbO$_3$ single-mode laser

Having lasers with a lithium niobate cavity offers the unique possibility of wavelength tuning using the quasi-instantaneous electro-optic effect. Wavelength tuning in external cavities on silicon nitride is almost exclusively done using heaters, which have time constants of the order of tens of microseconds and are very power consuming due to the material's low thermo-optic coefficient. Moving to a thicker silicon nitride layer with stronger confinement allows to bring the heater elements closer to the waveguide and boost the efficiency and speed a bit, but switching times between non-adjacent wavelengths are still over 50 µs [172]. The electro-optic effect on the other hand consumes no static power and the tuning speed is limited by the electronic signal rather than the physical effect. On silicon, fast (nanosecond-scale) carrier-based tuning of ring resonators is possible, but this is always accompanied by increasing losses in the resonator. Nevertheless, a widely tunable laser based on this principle has been demonstrated [173]. For some applications, only discrete wavelength switching is necessary. If the wavelength switching should not happen in real-time and the wavelength sequence is known in advance, tricks can be played where the laser cavity is switched from one mirror to another using carrier-based variable optical attenuators [174]. The back-up cavity can then be pre-tuned to the desired wavelength using slow heaters. For achieving a pure phase shift, III-V semiconductors [175] or electro-optic materials [99] can be employed, but the required heterogeneous integration technology is not widely available.

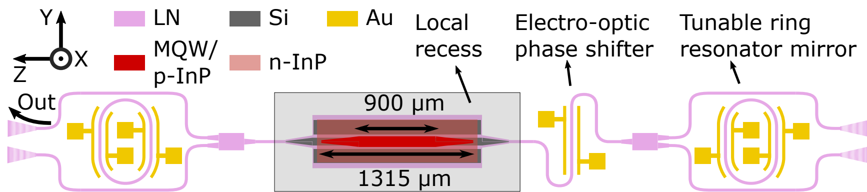


Figure 6.9: Schematic layout of the III/V-on-LiNbO$_3$ tunable laser. The amplifier in the recess has a ring resonator mirror on each side. A phase tuning section allows to finetune the longitudinal modes to overlap with the ring resonator resonances. The LN crystal orientations are indicated in the upper left corner. The output was collected from the upper left grating coupler, unless mentioned otherwise.

6.5.1 Coarse wavelength tuning

The single-mode laser was designed by adding tunable ring resonator mirrors on each side of the amplifier, as shown in Fig. 6.9. The resonance frequencies of the mirrors can be adjusted electro-optically. An extra electro-optic phase shifter is added in the cavity for fine-tuning the roundtrip phase. The original intention was to design the rings as a Vernier mirror. However, due to a design error the path length in both rings is identical and only the gaps between the rings and their feeding waveguides are slightly different. Within the wavelength range that we work in, the FSRs of both rings are quasi-identical. Despite this design flaw, a sweep of the amplifier's bias current in Fig. 6.10 shows an abrupt increase of the output power, a clear sign of lasing. The fiber-coupled output power reaches -9.8 dBm. This value cannot easily be translated into an on-chip power level, but given the measured grating coupler efficiency around 1540 nm (the gain peak), it is most likely > 1 mW. The oscillating behaviour in the blue curve is caused by longitudinal mode-hopping. However, the left and right outputs don't show similar lasing peaks. In this sweep, no bias voltage was applied to the tunable ring resonator mirrors, and hence it is unlikely that their resonances are aligned. This asymmetric output indicates that the feedback for lasing comes from the mirror on the right, and at least one spurious reflection on the left side of the cavity.

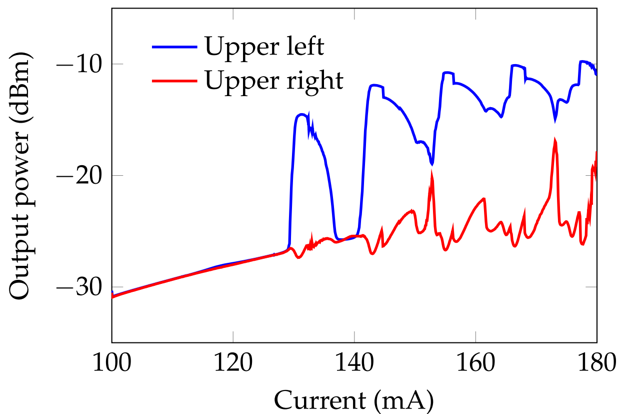


Figure 6.10: Fiber-coupled output power versus amplifier bias current, with no applied voltage bias on the ring resonator mirrors. The output power was measured at the upper left and right grating couplers of the device.

A detail of two lasing spectra with different biasing conditions is shown in Fig. 6.11a. This output was collected from the upper left grating coupler in

the design. Peaks and dips can be seen in the ASE floor. These correspond to the resonances of respectively the right and left ring resonators. The reflection from the right resonator gets amplified, whereas the resonance frequencies of the left ring are suppressed at the measured port, except at the lasing wavelength. In the blue curve, the lasing peak around 1547 nm coincides with the resonance of the right ring mirror, although the resonance of the left mirror lies 200 pm higher. Around 1540 nm, the expected dip from the left mirror is absent, instead, another peak can be seen. This might indicate the presence of another lasing mode in the cavity which reflects on the left mirror. A detailed view of this is shown in the inset. In the red curve, the electro-optic effect has been used to shift the resonances of the right mirror (the peaks in the blue curve) to the resonances of the left mirror. It can be seen that the amplified reflection from the right mirror is suppressed at all but one wavelength, where a lasing mode appears. This mode uses the feedback from both mirrors to achieve lasing. The background ASE is also 4 dB more suppressed in this mode.

By tuning the amplifier's bias current and the voltage over the mirrors, single-mode lasing with more than 30 dB side-mode extinction could be obtained over a range of 21 nm, as shown in Fig. 6.11b. Also in this measurement, the output was collected from the upper left grating coupler.

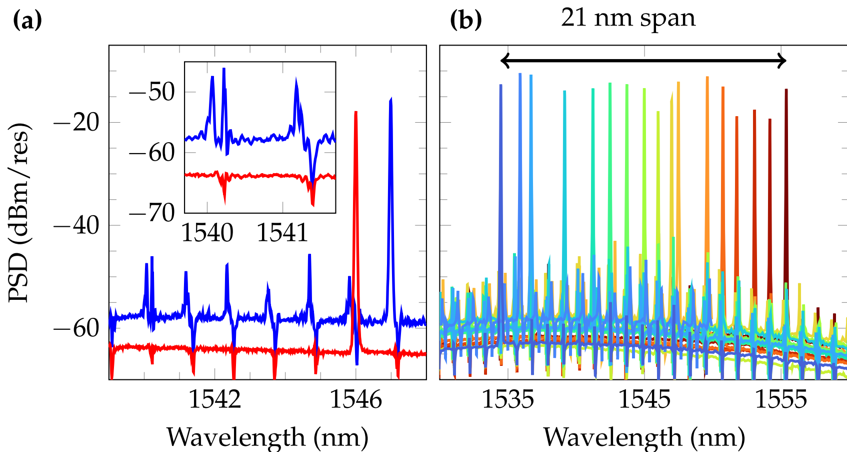


Figure 6.11: (a) Detail of two lasing spectra, showing lasing both with aligned (red) and misaligned (blue) resonances. (b) Lasing spectra of the tunable laser at different settings of the bias current and mirror voltage.

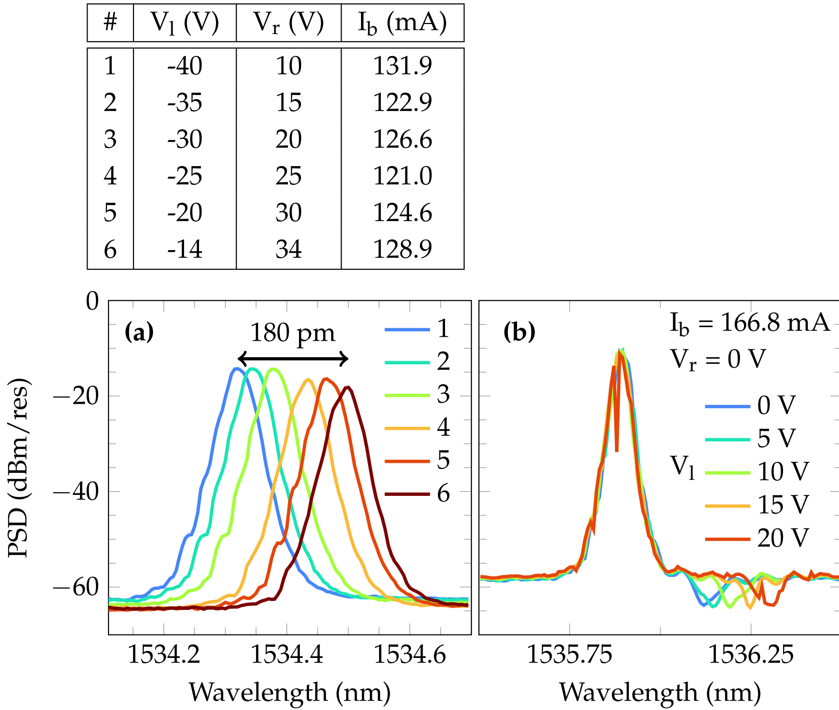
6.5.2 Fine wavelength tuning

Proof that the laser can work using both rings as mirrors is obtained by tuning both rings simultaneously and shift the lasing wavelength. The roundtrip phase is adjusted by changing the bias current instead of using the electro-optic phase tuning section to limit the number of probes on the setup. Changing the bias current has an impact on the effective index of the mode in the amplifier through the plasma dispersion effect and the thermo-optic effect. The measurement in Fig. 6.10 indicated that one longitudinal mode hop could be achieved by changing the bias current (resp. dissipated electrical power) by 11-12 mA (resp. 34-36 mW). The result of the fine tuning measurement is shown in Fig. 6.12a. The lasing wavelength shifts 180 pm upon a 26 V change of the voltage over the ring mirrors. The FSR of the rings is 1.14 nm. A 180 pm shift is then equivalent to a phase shift of 0.32π in the rings. The two phase sections in the rings are each 321 µm long. From these data, the V_{π} L of the phase shifters is calculated to be 5.2 V·cm. Figure 6.12b shows a detailed view of the other type of lasing observed on this device. Lasing starts already without applying any voltage to the ring mirrors. The lasing peak coincides with the resonance of the right ring mirror, as mentioned before. Applying an increasing voltage on the left mirror to shift its resonance away from the lasing peak has no influence on it. This proves that this lasing mode is reflecting on another point in the cavity.

6.5.3 Phase noise measurement

In order to determine the phase noise of the tunable laser, a delayed self-heterodyning (DSH) measurement [176] was done using the setup shown in Fig. 6.13a. The output of the Vernier laser is split into two branches. One branch is delayed in time using 500 m of optical fiber, the other is shifted in frequency using an accousto-optic modulator (AOM). The two branches are then recombined and collected in a photodiode, of which the electrical output is sent to an electrical spectrum analyzer (ESA). The time delay decorrelates the portion of the phase noise that is of interest. The frequency shift upconverts the signal from direct-current (DC) to 200 MHz and separates it from the common-mode noise at DC in the photodiode. In principle, the AOM can be omitted (as it has a relatively high insertion loss of around 8 dB), but then the upconversion should be done in the electrical domain [177].

Typically, the phase noise in semiconductor lasers gives rise to spectral shape that can be well approximated by a Voigt profile [178]. A Voigt profile is the convolution of a Gaussian and a Lorentzian. The Lorentzian shape



#	V_l (V)	V_r (V)	I_b (mA)
1	-40	10	131.9
2	-35	15	122.9
3	-30	20	126.6
4	-25	25	121.0
5	-20	30	124.6
6	-14	34	128.9

Figure 6.12: (a) Fine tuning of the lasing wavelength by simultaneous adjustment of the voltage on both rings and the bias current. The laser's settings for each spectrum are listed in the table above. (b) Proof that lasing can occur without reflecting on the left mirror. The lasing mode remains unchanged as the resonance of the left mirror is shifted.

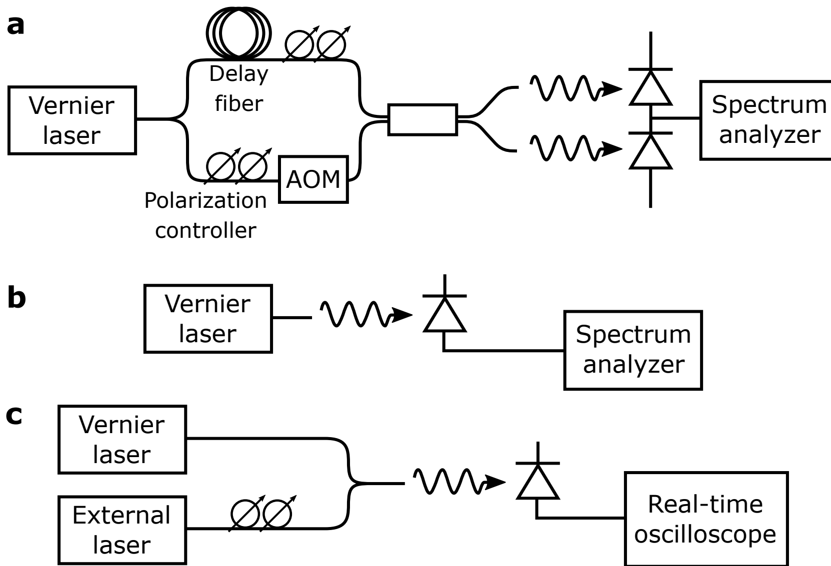


Figure 6.13: (a) Delayed self-heterodyne setup. (b) Intensity noise measurement setup. (c) Setup for the phase noise estimation of the beat note of the Vernier laser with an external tunable laser (Santec TSL–770).

arises from the fundamental ASE noise in the amplifier [179,180], which has a white frequency distribution. In semiconductors, a low-frequency noise component with a 1/f frequency distribution is also present. It arises from random generation-recombination events with a large spread in lifetimes [181]. A part of these events occur in the active region, causing a partial correlation between the electrical and optical noise [182]. This low-frequency contribution will distort the Lorentzian lineshape close to the spectral peak. It is often well approximated by a Gaussian lineshape near the center. The total spectral lineshape *caused solely by phase noise* can hence be approximated by a Voigt profile.

The captured signal from the DSH measurement is shown in blue on a linear and logarithmic scale in Figs. 6.14a-6.14b. This signal does not represent the spectrum of the original laser, but the beat note of the two branches. Ideally, these two can be considered to be uncorrelated. In that case, the beat note's spectrum is the result of twice the frequency noise of the original Vernier laser. This spectrum can still be fitted to a Voigt profile. The fit matches the profile in Fig. 6.14a well, however it does not correctly estimate the far-out frequency noise, as shown on the logarithmic scale in Fig. 6.14b. This indicates that the Voigt model is inadequate for this spectral shape.

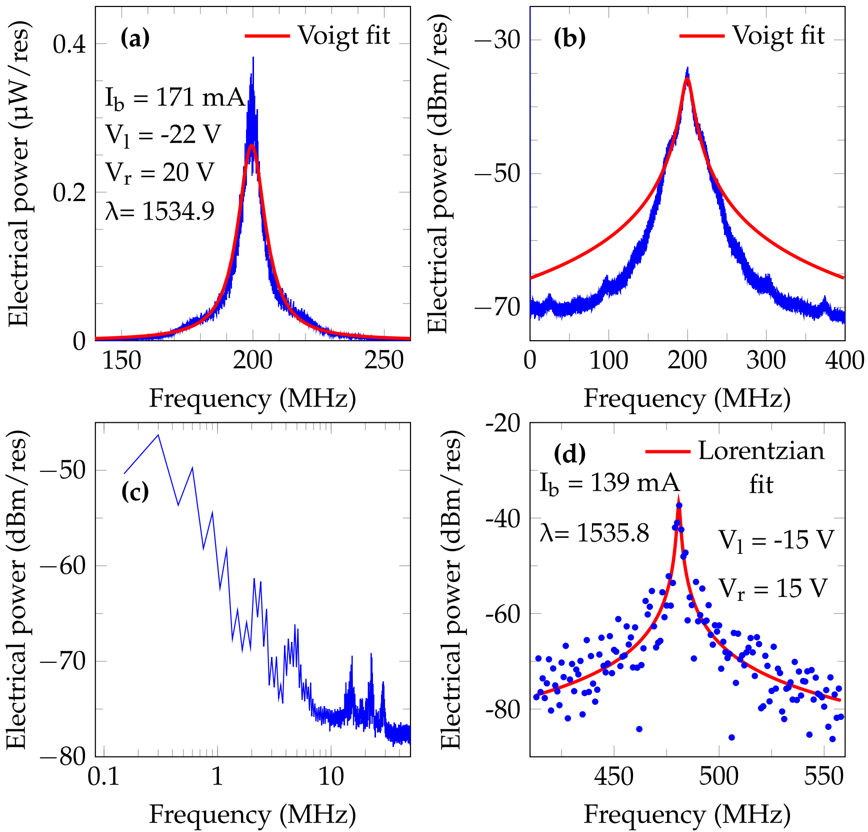


Figure 6.14: Phase noise measurement results. (a)-(b) Electrical spectrum of the beat note in a self-heterodyne measurement, in linear and logarithmic scale. A fiber length of 500 m was used. The spectra were recorded with a video bandwidth of 100 Hz and a resolution of 100 kHz. A Voigt model was used to fit the linear data, however the fit is unsatisfactory in the logarithmic scale. (c) Intensity noise measurement. Several peaks can be seen. (d) Spectrum of the beat note of the Vernier laser with an external tunable laser (Santec TSL-770). The data were recorded using a real-time oscilloscope with a sampling rate of 2.5 GSa/s. The shown spectrum is calculated from 1 µs of data.

A possible reason is that the laser suffers from non-negligible amounts of intensity noise. Small, but discernable satellite peaks are present in the DSH spectrum at 100 MHz and 175 MHz from the central frequency. A measurement of the intensity noise was done to verify this. The output of the laser is immediately sent to the photodiode and the spectral decomposition of the laser's power was shown on the ESA (see Fig. 6.13b). The results are shown in Fig. 6.14c. Ideally, this spectrum should only contain a peak at DC, with higher frequencies disappearing in the noise floor. Several peaks are however present, at 2.2 MHz, 4.5 MHz, 15.0 MHz, 22.5 MHz and 29.0 MHz. Intensity noise distorts the spectral shape and hampers the extraction of information using a Voigt-model or even a Lorentzian model. A second measurement was done to attempt to estimate the white frequency noise component. The setup is shown in Fig. 6.13c. The output of the Vernier laser was combined with the output of an external tunable laser (Santec TSL-770) with a known white noise component. It's Lorentzian linewidth is less than 60 kHz according to the manufacturer. The wavelength of the external laser is tuned close to the emission wavelength of the Vernier laser to obtain a beat note of a few hundreds of MHz. This beat note was collected by the photodiode and recorded on a real-time oscilloscope, sampling at 2.5 GSa/s. This sampling rate is sufficient to reliably reconstruct the spectrum of the data. Using a Fourier transformation, the spectrum of 1 μs of recorded data is used to reconstruct a spectrum. This timespan is not too short to have insufficient resolution, and not too long to avoid spectral distortion by low-frequency frequency noise and intensity noise. The spectrum is shown in Fig. 6.14d, together with a Lorentzian fit to the data. The tail of the spectrum allows for a good fit to the Lorentzian model, despite the limited resolution near the peak. The estimated linewidth is 1.35 MHz, which is the sum of the linewidths of the Vernier laser and the Santec. The estimated fundamental linewidth for our Vernier laser is hence 1.30 MHz.

6.6 Conclusion

The design of the single-mode laser cavity has a lot of room for optimization. A design such as the single-mode tunable laser on Si_3N_4 could be tried. A more thorough analysis of the origin of the off-resonance lasing should shed some light on ways to reduce potential scattering points in the cavity. Using a lower etch depth in the silicon layer could help minimizing the scattering at the taper tip of the III-V mesa. The fundamental linewidth of the laser should improve by increasing the cavity length in the low-loss LN waveguide layer.

7

Conclusion and Perspectives

"Begin at the beginning," the King said gravely,
"and go on till you come to the end: then stop."
Lee Caroll, Alice in Wonderland

7.1 Overview

The main goal of this work was to demonstrate the heterogeneous integration of III/V semiconductor based light sources onto silicon nitride photonic integrated circuits operating at telecom wavelengths. Adding active functionality on silicon nitride, in itself a purely passive platform (apart from thermal phase shifters), has been the goal of many studies and is still an active research domain. The integration of III-V components started with hybrid integration techniques based on edge-coupling and chip assembly techniques [79, 183, 184]. A few years later, almost simultaneously several demonstrations using heterogeneous integration techniques started appearing [102,103,106], with a clear trend towards multi-layered platforms. Bridging the gap between silicon nitride and III-V platforms will allow the design of more complex circuits on a single chip, and individual devices reaching higher performance.

In the first part of this work, a process was developed to add an intermediate layer of a-Si:H to the passive silicon nitride platform with a minimal amount of extra processing steps. This intermediate layer served to bridge the gap in effective index between the fundamental modes in the silicon nitride and III-V waveguides. A design study was done to choose the optimal thickness of the a-Si:H layer and to optimize the interlayer taper. The influence of these extra processing steps on the quality of the silicon nitride circuit was verified by comparing the response of ring resonators on both platforms. The process was found to have only a weak impact. Semiconductor optical amplifiers were integrated onto these multilayer circuits with the micro-transfer printing method. A standalone integrated optical amplifier was demonstrated, as well as a multimode and a single-mode laser. During the attempted fabrication of a widely tunable, single-mode laser, the limitations of using DVS-BCB as a cladding material became apparent. The addition of heaters for thermo-optic phase shifting proved troublesome. An on-chip optical gain of 13.7 dB and a gain saturation power of 8 mW were measured for an amplifier with a central section of 700 µm. This gain includes the losses of the transition to and from the silicon nitride waveguide. The trade-off between gain per unit length and saturation power can be further optimized by changing the a-Si:H waveguide geometry. The output power of the single-mode laser reaches 730 µW. The estimated steady-state power coming out of the amplifier is around 3.5 mW.

In the second part of this work, the process was adjusted to a back-end module on a patterned and oxide-clad sample of thin-film lithium niobate on sapphire. To access the waveguide near the transfer printing site, a local recess was etched to expose the waveguide layer, leaving only a thin layer of SiO_2 on top. The deposition of a-Si:H was replaced by a micro-transfer printing step of crystalline silicon coupons into the recess, followed by the printing of the III/V amplifiers. Also on this platform, a standalone amplifier and multimode laser were demonstrated, as well as a tunable single-mode laser. The measured on-chip gain and gain saturation power of an amplifier with a central section of 900 µm reach 10.6 dB and 2.6 mW, despite the longer device and better thermal heat sinking properties. The grating couplers used to characterize the amplifier add uncertainty to the results, and the transition losses between the $LiNbO_3$ and the silicon waveguide adds >1 dB more loss as compared to the transition on silicon nitride. Despite a design flaw in the single-mode laser, its on-chip output power likely exceeds 1 mW (the uncertainty originating in the grating coupler response). Coarse and fine tuning of its output wavelength using lithium niobate's electro-optic effect, respectively over a range of 21 nm and

180 pm, has been demonstrated. The work done in this thesis comprised the first demonstrations of heterogeneous integration of III-V based light sources on lithium niobate and the first fully integrated laser with electro-optic wavelength tuning capabilities. Also in this topic, not much time elapsed before other demonstrations using micro-transfer printing [185] or flip-chip bonding [186].

7.2 Future perspectives

The micro-transfer printing method reduces the number of processing steps of the heterogeneous integration process compared to a wafer bonding approach. Furthermore, the integration of exotic materials (III/V, lithium niobate, gold ...) can be moved to the back-end of the process. For the case of silicon or silicon nitride wafers that are processed in CMOS fabs, this limits the needed number of extra dedicated tools and hence reduces the hurdles for foundries to adopt this technology. A variety of different materials/components can be added on silicon nitride using the micro-transfer printing technique, e.g. optical amplifiers (this work), photodiodes [187,188] and electro-optic modulators [92]. This closes the gap between active and passive platforms and has the potential to enable PICs with more complex functionalities, or exceptional performance, with scalability to high volumes. Another feature that distinguishes micro-transfer printing from (die-to-) wafer bonding is the possibility to integrate different materials, e.g. III-V stacks with different emission wavelengths, very closely together. A disadvantage that needs to be addressed is the need for an adhesive polymer layer to ease the surface requirements, as such a layer increases the thermal resistance between the active device and the substrate. For low chip volumes, the micro-transfer printing technique could already be used to offer some extra functionalities in a modular approach, e.g. amplifiers and simple photodiodes with the same material stack. The silicon intermediate layer for III/V integration can be replaced by another material, such as silicon-rich silicon nitride [107] or i-InP.

In general the trend towards multi-layer platforms combining silicon and silicon nitride, and often including some III-V functionality, is moving to the foundry level [106,110,189]. Even though in the integrated photonics world, there is not one single layer stack that can serve everybody's purpose, this evolution may make multi-layered Si/Si_3N_4 circuits accessible and more affordable in the future.

Cleanroom process details

In this Appendix, some details from the cleanroom processes are listed.

RIE etch recipes

Use case	Pressure mTorr	RF power W	CF_4 sccm	SF_6 sccm	H_2 sccm	O_2 sccm
a-Si:H/SiO_2 (iso.)	60	150	0	50	0	3
a-Si:H/SiO_2 (aniso.)	20	210	80	3	7	0
c-Si (aniso.)						
Si_3N_4 (aniso.)	20	210	80	0	3	0
DVS-BCB	40	150	0	5	0	50
resist (aniso.)	20	-275*	0	0	0	25
resist (iso.)	100	75	0	0	0	50

Table A.1: Used etch recipes in RIE. Abbreviations: aniso. = anisotropic; iso. = isotropic. (*) In this recipe, the DC bias (in Volt) is fixed, instead of the RF power.

PECVD deposition recipes

Use case	Pressure mTorr	RF power W	Temp. °C	N_2O sccm	SiH_4 sccm	Ar sccm	N_2 sccm
a-Si:H	650	50	180	0	45	470	0
SiO_x	700	30	270	1425	10	0	393

Table A.2: Used deposition recipes in PECVD.

AR-P 6200 spincoating curves

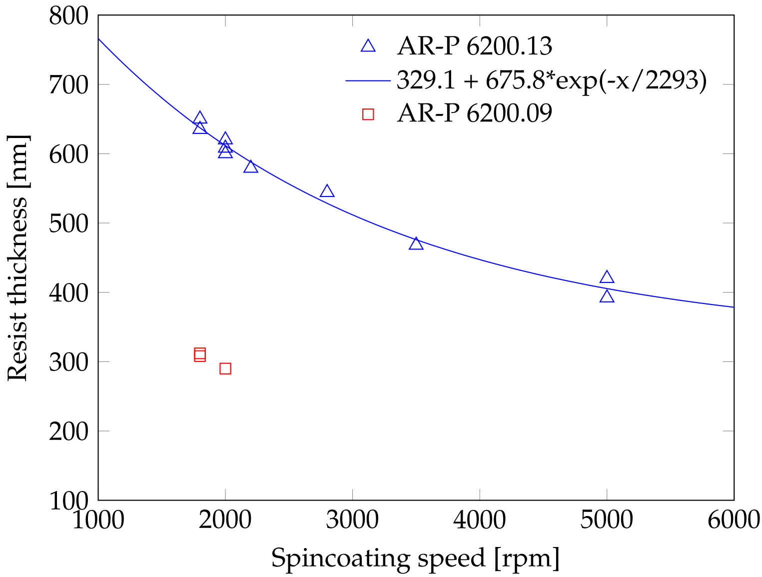


Figure A.1: Spincoating curves of the AR-P 6200 positive E-beam resist. Measured using a white light interferometer on samples of around 25 x 25 mm^2.

B
Effective length of an add-drop ring resonator

The effective length of an add-drop ring for light coupled out at the drop port is

$$L_{eff} = L_{ring} \cdot \frac{\partial \varphi_d}{\partial \phi}, \tag{B.1}$$

where φ_d is the effective phase delay of the ring at the drop port and ϕ is the accumulated phase over one roundtrip in the ring. Given the amplitude transmission to the drop port t_d:

$$t_d = -\frac{k_1 k_2 \sqrt{a} e^{j\frac{\phi}{2}}}{1 - a r_1 r_2 e^{j\phi}}, \tag{B.2}$$

we can find an expression for the effective phase shift of the light at the drop port:

$$\begin{aligned}
\varphi_d &= \arg(-k_1 k_2 \sqrt{a}) + \arg\left(e^{j\frac{\phi}{2}}\right) + \arg\left(\frac{1}{1 - a r_1 r_2 e^{j\phi}}\right) && \text{(B.3)} \\
&= \pi + \frac{\phi}{2} + \arg\left(\frac{1 - a r_1 r_2 \cos\phi + j \cdot a r_1 r_2 \sin\phi}{1 + a^2 r_1^2 r_2^2 - 2 a r_1 r_2 \cos\phi}\right) && \text{(B.4)} \\
&= \pi + \frac{\phi}{2} + \operatorname{atan}\left(\frac{a r_1 r_2 \sin\phi}{1 - a r_1 r_2 \cos\phi}\right). && \text{(B.5)}
\end{aligned}$$

With this expression of φ, we can calculate the factor $\frac{\partial \varphi_d}{\partial \phi}$. To ease the readability of the derivation, we substitute ar_1r_2 with A.

$$\frac{\partial \varphi_d}{\partial \phi} = 0 + \frac{1}{2} + \frac{1}{1+x^2} \cdot \frac{\partial x}{\partial \phi} \text{ with } x = \frac{A \sin \phi}{1 - A \cos \phi} \tag{B.6}$$

$$= \frac{1}{2} + \frac{(1 - A\cos\phi)^2}{(1 - A\cos\phi)^2 + (A\sin\phi)^2} \cdot \frac{A\cos\phi - A^2}{(1 - A\cos\phi)^2} \tag{B.7}$$

$$= \frac{1}{2} + \frac{A\cos\phi - A^2}{(1 - A\cos\phi)^2 + (A\sin\phi)^2} \tag{B.8}$$

$$= \frac{1}{2} + \frac{A\cos\phi - A^2}{1 - 2A\cos\phi + A^2\cos^2\phi + A^2\sin^2\phi} \tag{B.9}$$

$$= \frac{1}{2} + \frac{A\cos\phi - A^2}{1 - 2A\cos\phi + A^2} \tag{B.10}$$

$$= \frac{1 - 2A\cos\phi + A^2 + 2A\cos\phi - 2A^2}{2(1 - 2A\cos\phi + A^2)} \tag{B.11}$$

$$= \frac{1 - A^2}{2(1 - 2A\cos\phi + A^2)} \tag{B.12}$$

$$\Rightarrow \frac{\partial \varphi_d}{\partial \phi} = \frac{1 - (ar_1r_2)^2}{2(1 - 2ar_1r_2\cos\phi + (ar_1r_2)^2)} \tag{B.13}$$

This function is maximal at resonance, when $\phi = 2\pi$:

$$\left.\frac{\partial \varphi_d}{\partial \phi}\right|_{\phi=2\pi} = \frac{1 - (ar_1r_2)^2}{2(1 - ar_1r_2)^2} \tag{B.14}$$

$$= \frac{1 + ar_1r_2}{2(1 - ar_1r_2)} \tag{B.15}$$

$$\approx \frac{1}{1 - ar_1r_2} \tag{B.16}$$

The approximation in the last step is valid for low losses and weakly coupled rings.

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