Hybrid III-V/Si DFB Lasers Based on Polymer Bonding Technology

Hybride III-V/Si-DFB-lasers gebaseerd op polymeerbondingtechnologie

Stevan Stanković

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List of Acronyms

A

ARC	Anti-Reflection Coatings

B

BCB	Benzocyclobutene
BOX	Buried Oxide

C

CAMFR	Cavity Modeling Framework
CB	Carrier Blocking
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical-Mechanical Polishing
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapour Deposition
CW	Continuous Wave

D

DBR	Distributed Bragg Reflector

DEMUX	Demultiplexer
DFB	Distributed Feedback
DI	Deionized
DVS-BCB	Divinylsiloxane-bis-benzocyclobutene

E

EAM	Electro-absorption Modulator
ELOG	Epitaxial Lateral Overgrowth
EMI	Electro Magnetic Interference

F

FIB	Focused Ion Beam
FLOP	Floating Point Operation
FTTH	Fiber To The Home
FWHM	Full Widht at Half Maximum

H

HPC	High Performance Computing

I

IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IPA	Isopropyl alcohol, Isopropanol
ITO	Indium-Tin-Oxide
ITRS	International Roadmap for Semiconductors

L

LAN	Local-Area Network
LD	Laser Diode
LED	Light Emitting Diode

M

MAN	Metropolitan-Area Network
MBE	Molecular Beam Epitaxy
MCE	Microchannel Epitaxy
MCM	Multi-Chip Module
MECSL	Monolithic Evanescently Coupled Silicon Laser
MEMS	Micro-Electro-Mechanical Systems
MIT	Massachusetts Institute of Technology
MOEMS	Micro-Opto-Electro-Mechanical Systems
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MOVPE	Metal Organic Vapour Phase Epitaxy
MQW	Multiple Quantum Wells
MSM	Metal-Semiconductor-Metal
MUX	Multiplexer

O

OSA	Optical Spectrum Analyzer

P

PAB	Plasma-Assisted Bonding
PCB	Printed Circuit Board
PD	Photodiode
PECVD	Plasma Enhanced Chemical Vapour Deposition

PI	Polyimide
PIC	Photonic Integrated Circuit
PL	Photoluminescence
PMMA	Polymethylmethacrylate
PRBS	Pseudo Random Binary Sequence

Q

QD	Quantum Dot
QW	Quantum Well
QWI	Quantum Well Intermixing

R

RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing

S

SCH	Separated Confinement Heterostructure
SEM	Scanning Electron Microscope
SiP	System-in-Package
SLID	Solid-Liquid Interdiffusion
SMSR	Side-Mode Suppression Ratio
SoC	System-on-Chip
SOG	Spin-On-Glass
SOI	Silicon-On-Insulator
SRIM	Stopping and Range of Ions in Matter

T

TEM	Transmission Electron Microscope

TRIM	Transport of Ions in Matter
TSV	Through-Silicon-Via

U

UBM	Under Bump Metallization
UCSB	University of California, Santa Barbara
UT-BOX	Ultra-thin Buried Oxide
UV	Ultraviolet

V

VCSEL	Vertical Cavity Surface Emitting Laser
VLSI	Very-Large-Scale Integration
VOC	Vertical Outgassing Channel

Nederlandse samenvatting –Summary in Dutch–

Introductie

De exponentiële vooruitgang in de prestaties van microprocessor chips, vaak geformuleerd als de wet van Moore, wordt geconfronteerd met ernstige uitdagingen in de nabije toekomst door beperkingen in elektrische verbindingen. Die zijn immers niet in staat om de toekomstige uitdagingen voor bandbreedte, integratiedichtheid en laag vermogen verbruik te realiseren. De meest beloftevolle oplossing is de ontwikkeling van optische verbindingen geschikt voor chip-naar-chip en intra-chip communicatie. In deze context biedt silicium fotonica de meeste mogelijkheden voor de productie van zulke verbindingen. Deze tak van de fotonica die zich snel ontwikkelt, is gebaseerd op een materiaal platform van silicium op isolator (SOI) en dit platform gebruikt dezelfde fabricageprocessen en toestellen als in de micro-elektronica industrie. Op deze manier maakt het enerzijds een goedkope fabricage mogelijk van geïntegreerde optische circuits en anderzijds de integratie van zowel optische als elektronische componenten op een enkele chip.

Het maken van een efficiënte lichtbron in silicium blijft echter een ernstige uitdaging, omwille van de indirecte bandkloof in dit materiaal. De laatste jaren werd er in silicium fotonica verwoed gewerkt aan de realisatie van een elektrisch aangedreven laser. Verschillende benaderingen worden geprobeerd, maar de meest bemoedigende resultaten werden bereikt met de heterogene integratie van III-V halfgeleiders (als efficiënte lichtbron) op een SOI platform. Dit is ook de aanpak van Intel die een gedeelte van het werk in deze thesis ondersteund hebben. Bij de aanvang van deze thesis, waren de meest veelbelovende componenten hybride III-V/Si lasers gebaseerd op een evanescente koppeling en een directe (moleculaire) bonding technologie, waarbij een III-V chip en een SOI chip als het ware aan elkaar gekleefd worden. Deze bonding techniek vereist uiterst vlakke en egale oppervlakken, vrij van enige vorm van contaminatie, en deze strikte voorwaarden zouden wel eens een probleem kunnen zijn voor de

fabricage op industriële schaal.

Om dit probleem te omzeilen, hebben we in deze thesis gefocust op een alternatieve, minder strikte bonding technologie, gebaseerd op klevende polymeren. Als bonding materiaal gebruiken we divynilsiloxaan bis-benzocyclobuteen (DVS-BCB), een polymeer welbekend in de micro-elektronica industrie. De streefdoelen van dit werk waren om in de eerste plaats een DVS-BCB bonding proces te ontwikkelen dat niet manueel maar met een machine gebeurt en die bonding diktes zou opleveren die voldoende dun zijn om de fabricage van hybride III-V/Si lasers gebaseerd op evanescente koppeling mogelijk te maken. Uiteindelijk moest dit proces gebruikt worden om zowel Fabry-Perot als gedistribueerde feedback (DFB) lasers te maken die een continue output leveren en dat bij een golflengte van 1310 nm.

Ontwerp van hybride III-V/Si lasers gebaseerd op DVS-BCB bonding

Voor de actieve laag van onze hybride III-V/Si laser kozen we voor een epitaxiaal gegroeide structuur met acht kwantumputten (QWs) gebaseerd op InAlGaAs, terwijl het gekozen SOI platform gebaseerd was op rib golfgeleiders. Het doel van het ontwerp was om alle parameters te optimaliseren voor een hybride III-V/Si golfgeleider die een fundamentele optische mode moet ondersteunen met een stabiele vermogen verdeling over de actieve lagen en de silicium rib golfgeleider en dit voor een dikte van de DVS-BCB bonding laag variërend tussen 20 en 120 nm. Zulke parameters hebben we gevonden en ze zorgen voor een fundamentele optische mode met een opsluitingsfactor in de silicium golfgeleider (Γ_{Si}) en de verschillende kwantumputten (Γ_{MQW}), respectievelijk boven de 70% en 3%. Om de thermische weerstand te verminderen werd een redelijk brede (16.8 μm) III-V mesa gekozen, en deze breedte was een compromis tussen de tegenstrijdige vereisten om tegelijk een lage elektrische en een lage thermische weerstand te hebben. Een combinatie van proton implantatie in de laterale secties van de III-V mesa en een laterale onderets van de InAlGaAs lagen werd gebruikt om de geïnjecteerde ladingdragers te beperken tot de centrale regio van de III-V mesa en om lekstroom te minimaliseren.

Behalve Fabry-Perot lasers, werden ook hybride III-V/Si lasers ontworpen die bij ëën enkele golflengte werken. Deze zijn gebaseerd op eerste-orde en tweede-orde roosters, met rooster periodes van 200 en 400 nm en een vulfactor met een streefwaarde van respectievelijk 50% en 75%. Twee types van dit soort hybride III-V/Si laser werden ontworpen: 1) een conventionele DFB laser met een geïntegreerde fotodetector en 2) een zogenaamde fase-verschoven DFB laser met Bragg spiegels aan beide uiteinden en met een centrale regio zonder

rooster.

Simulatieresultaten gaven aan dat de dikte van de DVS-BCB bonding laag zo klein en zo uniform mogelijk moeten worden gehouden. Relatief dikke bonding lagen (~ 100 nm) verhogen niet enkel de thermische weerstand, maar maken de component ook gevoeliger aan variaties die bij de fabricage van de silicium rib golfgeleiders kunnen optreden en ze vernauwen ook het reflectiespectrum van de roosters. Bovendien bleken de tweede-orde roosters veel gevoeliger dan de eerste-orde roosters aan een slechte uniformiteit van de bondinglaag.

Ontwikkeling van het DVS-BCB bonding proces

Het grootste deel van het werk in deze thesis was gewijd aan het ontwikkelen van het machinale DVS-BCB bonding proces voor de heterogene integratie van een III-V chip bovenop een SOI chip met optische golfgeleiders. Dit is de eerste stap in het maken van hybride III-V/Si lasers met evanescente koppeling. De beste manier om voldoende dunne bonding lagen te bekomen, bleek het gebruik te zijn van sterk verdunde DVS-BCB in mesityleen. Een serie van tests is uitgevoerd en problemen die optraden tijdens de ontwikkeling van de bonding procedure werden opgelost door specifieke stappen in de pre-bonding voorbereiding en het bonding proces zelf aan te passen.

In de uiteindelijke versie van de ontwikkelde bonding procedure, bekwamen we DVS-BCB lagen met een dikte van minder dan 100nm (vaak ~ 50 nm). Dit is voldoende dun voor een efficiënte evanescente koppeling tussen de III-V halfgeleider lagen en de silicium golfgeleiders en dus voor de fabricage van hybride III-V/Si lasers, versterkers en detectoren. Het rendement van dit proces was hoog en de sterkte van de bonding groot. Anderzijds bleek het moeilijk om de uniformiteit van de bonding laag en dikte te controleren. Hoe meer structuren er in het SOI aanwezig zijn met 220 nm diepe gleuven, hoe groter de negatieve impact was op de uniformiteit van de bonding laag. De beste resultaten werden dan ook bekomen met SOI chips die eerst geëffend werden. Hierbij wordt SiO_2 gebruikt om de gleuven rond de silicium rib golfgeleider op te vullen.

Fabricage en karakterisering van de hybride lasers

De fabricage van de hybride III-V/Si lasers, zowel bonding als alle III-V verwerking, werd uitgevoerd in de cleanroom van de Photonics Research Group van Universiteit Gent. De proton implantatie was de enige stap die uitgevoerd werd door een externe partij. De stappen in de fabricage procedure die gepresenteerd zijn in deze thesis, evolueerden waarbij individuele stappen geoptimaliseerd

werden. Zowel het aanbrengen van de metaalcontacten (n-type en p-type) als de snelle legering stap, moesten uitgevoerd worden voor de proton implantatie.

Karakterisering van de Fabry-Perot lasers en de lasers die bij ëën enkele golflengte werken, gefabriceerd in twee aparte cyclussen, toonde aan dat de prestaties van beide types over het algemeen vergelijkbaar is met gelijkaardige hybride III-V/Si lasers gerapporteerd door andere onderzoeksgroepen. De elektrische eigenschappen van zowel de Fabry-Perot als de DFB hybride lasers waren zeer gelijkaardig, maar er waren wel duidelijk merkbare verschillen in de thermische weerstand en bijgevolg hun optische output.

Zowel Fabry-Perot als DFB lasers met eerste-orde roosters werkten in continu en in gepulst regime en bereikten daarbij optische uitgangsvermogens van verscheidene milliwatts. De thermische weerstand van beide types was relatief hoog: gewoonlijk rond de 100 K/W voor de Fabry-Perot en de 350 μm lange DFB lasers en met een minimum gemeten waarde van 64 K/W voor een 600 μm lange fase-verschoven DFB laser. Terwijl de specifieke thermische weerstand R'_{th} van de Fabry-Perot lasers onverwacht hoog was ~ 60 K·mm/W), lag het voor DFB en fase-verschoven DFB lasers wel in de lijn van zowel de gesimuleerde waarden als die gerapporteerd voor hybride III-V/Si lasers gemaakt met directe bonding (36 - 38 K·mm/W). Hierdoor kon er bij de Fabry-Perot lasers in continu regime een duidelijke zogenaamde thermische overslag waargenomen worden in de $L-I$ grafieken en was er geen laserlicht meetbaar voor een temperatuur van 30 °C en hoger. De hybride lasers die bij ëën golflengte werken presteerden daarentegen veel beter en laserlicht was waarneembaar tot een temperatuur van 55 °C.

Gekliefde facetten leidden tot de vorming van parasitaire caviteiten binnenin de hybride III-V/Si DFB lasers en deze zorgden voor onverwachte vormen van de $L-I$ grafieken in een continu regime. Dit probleem kan echter overwonnen worden op verschillende manieren. Enerzijds door het aanbrengen van anti-reflectie coatings (ARC) en anderzijds door het gebruik van adiabatische spits toelopende structuren, die de hybride mode omvormen tot een zuivere silicium rib golfgeleider mode, aan het einde van het gebied met III-V.

Conclusies

Het onderwerp van deze thesis was het ontwikkelen van hybride III-V/Si lasers gebaseerd op een bonding technologie met DVS-BCB polymeer om deze lasers te gebruiken voor optische verbindingen. We hebben het ontwerp, de fabricage en de karakterisering van evanescent gekoppelde hybride III-V/Si Fabry-Perot en DFB type lasers gepresenteerd die licht uitstralen bij 1310 nm. De machinale bonding procedure die bonding lagen met een dikte van minder dan 100 nm opleverde en daardoor geschikt is voor evanescente koppeling, werd speci-

aal hiervoor ontwikkeld. De karakterisering van de verschillende gefabriceerde hybride III-V/Si lasers toonde aan dat hun prestaties over het algemeen vergelijkbaar zijn met die van hybride lasers gemaakt met directe bonding technologie. De resultaten van dit werk openen dan ook perspectieven voor verdere ontwikkeling en verbetering, zowel in de modellering als het ontwerp. De belangrijkste objectieven voor de toekomst zijn enerzijds het bonding proces ontwikkelen om meerdere kleine III-V chips tegelijk te hechten aan een silicium chip, en anderzijds om de thermische weerstand van de hybride III-V/Si lasers te verminderen.

English summary

Introduction

The exponential improvement in performance of microprocessor chips, famously expressed as Moore's Law, is facing serious challenges in the near future due to limitations of electrical interconnects, which are incapable of meeting future demands for bandwidth, integration density and low power dissipation. The most promising solution for this problem is development of high-performance optical interconnects suitable for chip-to-chip and intra-chip communication. Within this context, silicon photonics offers the most promising technology for fabrication of such interconnects. This rapidly-developing branch of photonics is based on the silicon-on-insulator (SOI) material platform and shares the same fabrication processes and tools used in microelectronics. Thus, it enables a cost-effective fabrication of high-performance photonic integrated circuits (PICs) and co-integration of photonic and electronic devices on a single chip.

However, fabrication of efficient light sources in silicon photonics remains a serious challenge, due to the indirect bandgap of silicon. In recent years, intensive research efforts have been focused on realization of electrically-pumped lasers in silicon photonics. Among various approaches to solve this problem, the most promising results have been demonstrated using heterogeneous integration of III-V semiconductor materials (as efficient light emitters) on the SOI photonic platform. This approach is also pursued by Intel Corporation, who partly supported the work on this PhD thesis. At the start of this work, the most promising devices were hybrid III-V/Si lasers based on evanescent-coupling and direct (molecular) bonding technology. However, this bonding technique requires very clean, smooth and contamination-free surfaces. Such strict requirements could raise challenges to an industrial-scale fabrication of these lasers.

To overcome this problem, in this PhD thesis, we focus on an alternative bonding technology - an adhesive, polymer-based, bonding which should offer more relaxed bonding requirements. As the bonding agent, we use divynilsilox-

ane bis-benzocyclobutene (DVS-BCB) polymer, which is a well-known dielectric material used in microelectronics. The goals of this work were to develop a machine-based, DVS-BCB bonding process yielding sufficiently thin bonding layers suitable for fabrication of evanescently-coupled, hybrid III-V/Si lasers, and eventually fabricate and demonstrate such lasers, both Fabry-Perot and distributed feedback (DFB) lasers, emitting in continuous wave (CW) regime at the wavelength of 1310 nm.

Design of hybrid III-V/Si lasers based on DVS-BCB bonding

As the active medium for our hybrid III-V/Si lasers, an epitaxially grown structure with eight, compressively strained, quantum wells (QWs) based on InAlGaAs was chosen. The selected SOI photonic platform was based on silicon rib waveguides. The design goal was to optimize all parameters in order to create a hybrid III-V/Si waveguide supporting a fundamental optical mode that also has a stable power distribution over the active layers and the silicon rib waveguide, for the thickness of the DVS-BCB bonding layer varying between 20 nm and 120 nm. Such parameters were found, allowing the fundamental optical mode to reach confinement factors in the silicon waveguide (Γ_{Si}) and the multiple quantum wells (Γ_{MQW}), above 70% and 3%, respectively. To lower the thermal resistance of the device, a relatively wide (16.8 μm) III-V mesa was chosen, as a compromise between conflicting requirements for achieving both lower electrical and thermal resistances. Combination of proton implantation in the lateral sections of the III-V mesa and the lateral undercut etching of the InAlGaAs layers was used to confine the injected carriers into the central region of the III-V mesa and minimize the leakage current.

Apart from Fabry-Perot lasers, single wavelength hybrid III-V/Si lasers were also designed, based on first-order and second-order gratings, with grating periods of 200 nm and 400 nm and targeted duty cycles of 50% and 75%, respectively. Two types of single wavelength hybrid III-V/Si lasers were proposed: 1) a conventional DFB device with an integrated photodetector and 2) a phase-shifted DFB device with Bragg-mirrors at both ends and a central gain section without corrugations.

Simulation results showed that the thickness of the DVS-BCB bonding layer should be kept as small as possible and as uniform as possible. Relatively thick bonding layers (~ 100 nm) not only increase the thermal resistance of the device, but also make the device more sensitive to fabrication-related variations of the Si rib waveguide dimensions and narrow the reflectance spectrum of the gratings. In addition to this, the second-order gratings turned out to be more

sensitive to a bad bonding layer uniformity compared to the first-order gratings.

Development of the DVS-BCB bonding process

The major part of the work on this thesis was devoted to development of a machine-based, die-to-die DVS-BCB bonding procedure, suitable for heterogeneous integration of III-V dies on top of SOI photonic waveguides and fabrication of evanescently-coupled photonic devices. The use of very diluted DVS-BCB solutions in mesitylene proved to be the best way to achieve sufficiently thin bonding layers. A series of bonding tests was carried out and the problems that occurred during development of the bonding procedure were solved by modifying specific steps in the pre-bonding die preparation and the bonding recipe itself.

In its final version, the developed die-to-die bonding procedure yielded less than 100nm-thick DVS-BCB bonding layers (~ 50 nm, usually), which are sufficiently thin for efficient evanescent coupling between III-V semiconductor layers and silicon waveguides and fabrication of hybrid III-V/Si lasers, optical amplifiers and photodetectors. The bonding process showed good bonding yield and solid bonding strength. However, the bonding layer uniformity and thickness proved to be the most difficult parameters to control. Relatively rich SOI die topography (with 220nm-deep trenches) had an adverse impact on the bonding layer uniformity, while the best results were achieved using pre-planarized SOI dies, where plasma-enhanced chemical vapour deposition (PECVD) of SiO_2 was used to fill the trenches surrounding the Si rib waveguides.

Fabrication and characterization of the hybrid lasers

Fabrication of the hybrid III-V/Si lasers, including the bonding step and the subsequent III-V material processing was carried out in the Photonics Research Group cleanroom facilities of Ghent University. The proton implantation was the only processing step carried out by an external vendor. The process flow, presented in this thesis, evolved over a period of time during which the individual processing steps were optimized. Both n-type and p-type metallization, as well as the high-temperature fast alloying step, had to be performed before the proton implantation step.

Characterization of the Fabry-Perot and single-wavelength hybrid III-V/Si lasers, fabricated in two different processing runs, showed that the performance of both types of lasers is, in general, comparable to the similar hybrid III-V/Si lasers reported by other research groups. The electrical properties of

both Fabry-Perot and DFB hybrid lasers were similar, but some noticeable differences were observed in the specific thermal resistance of the devices and, consequently, their optical output.

Lasing in both pulsed and CW regimes, with optical output levels of up to several milliwatts, was demonstrated for both Fabry-Perot and DFB hybrid lasers based on first-order gratings. Thermal resistance of both types of demonstrated hybrid lasers was relatively high, usually around 100 K/W for the Fabry-Perot lasers and the 350 μm-long DFB lasers, with a minimum measured value of 64 K/W for a 600 μm-long phase-shifted DFB laser. While the specific thermal resistance R'_{th} of the Fabry-Perot lasers was unexpectedly high (~ 60 K·mm/W), in both DFB and phase-shifted DFB lasers it was in a good agreement with the simulated values and the values reported for direct-bonded hybrid III-V/Si lasers (36 - 38 K·mm/W). Consequently, during characterization of the Fabry-Perot lasers in CW regime, strong thermal rollovers were observed in the $L-I$ curves and no lasing occurred at 30 °C or higher temperatures. On the other hand, single-wavelength hybrid lasers performed much better and lasing in CW regime was observed up to 55 °C.

Cleaved facets led to formation of parasitic cavities in hybrid III-V/Si DFB lasers which resulted in unexpected shapes of the $L-I$ curves observed while testing these devices in CW regime. However, this problem can be overcome in several ways, including deposition of anti-reflection coatings (ARC) or the use of adiabatic tapers to terminate the III-V active region and convert the hybrid mode to a Si rib waveguide mode.

Conclusions

The subject of this thesis was hybrid III-V/Si lasers, based on polymer DVS-BCB bonding technology and suitable for optical interconnects. We presented the design, fabrication and characterization of evanescently-coupled, hybrid III-V/Si Fabry-Perot and distributed-feedback (DFB) type lasers, emitting at 1310 nm. A machine-based DVS-BCB bonding procedure, yielding less than 100nm-thick bonding layers and suitable for evanescent-coupling, was specially developed for this purpose and presented in this thesis. In depth characterization showed that the performance of the fabricated hybrid III-V/Si lasers, in general, is comparable to similar hybrid lasers based on direct bonding technology. Results of this work open new possibilities for further development and improvements, both in the DVS-BCB bonding technology and the hybrid III-V/Si laser design. Scaling-up of the developed bonding process to a multiple die-to-wafer bonding procedure and reducing the thermal resistance of the hybrid III-V/Si lasers are the most important objectives for future work.

1
Introduction

1.1 The Silicon Age

In the last couple of decades we have witnessed an unprecedented development of electronics that has revolutionized the way people communicate, work and, in general - the way people live. An average person living in a developed country, possessing a personal computer, access to Internet, a laser printer, a digital camera, and other electronic devices that are affordable to the millions of users around the world, has at his disposal the computing power, information-gathering and design capabilities that were unimaginable even to the best-equipped professional users before the development of the first semiconductor transistor in 1947 at Bell Labs. Modern electronics is primarily based on silicon as the principal semiconductor material and the impact of the silicon-based semiconductor fabrication technology on our lives has been so profound that we can speak of the Silicon Age, mimicking the terms like "The Bronze Age" or "The Iron Age" that historians use to classify various periods of ancient history.

At the core of this progress was the capability of the semiconductor device fabrication technology to continuously scale-down the dimensions of electrical components, primarily the basic building-blocks of electronics - the transistors. This development was famously predicted in 1965 by Gordon Moore, co-founder of Intel Corporation, where he stated that "the complexity for minimum component costs has increased at a rate of roughly a factor of two per

Figure 1.1: Illustration of Moore's Law in 2011. Evolution of number of transistors in microprocessors over time. Taken from [3]

year" [1]. Later, this statement was simplified, claiming that the number of components per integrated circuit (IC) doubles every 18-24 months. This "prophecy", illustrated in Figure 1.1, became known as Moore's Law and it has been valid for more than 45 years, much longer than the 10 years that G. Moore himself initially expected for this trend to continue [1]. However, as the miniaturization continues with complementary metal-oxide semiconductor (CMOS) transistor gates fabricated in the 22 nm technology node [2] and silicon wafers dimensions are expected to increase from 300 mm to 450 mm diameter, driving down the cost-per-die, we are reaching some serious limitations to further development along the exponential path defined by Moore's Law.

1.1.1 Challenges along Moore's path: power dissipation and interconnect bottleneck

As the integration density in state-of-the art microprocessors (like Intel's Ivy Bridge, fabricated in a 22 nm technology) is reaching almost one billion transistors per square centimeter, excessive power dissipation and heat build-up becomes a serious problem in the drive to further improve chip performance fol-

lowing Moore's Law. With the power dissipation proportional to clock frequency and continuously-shrinking dimensions of electrical components, the power dissipation density in modern microprocessors has reached levels of hundreds of W/cm^2 which is comparable to power density levels in nuclear reactors, as illustrated in Figure 1.2. To alleviate heat generation problems while improving the chip performance, in the last years the focus was shifted from further increase in clock frequency, to developing multi-core processors featuring several (usually, 2 to 8) interconnected CPU cores within a single package. In this way, parallel computing took the lead in improving microprocessor performances, while the clock frequencies were kept roughly in the 2-4 GHz range. In order to fully exploit the effect of the multiple cores, there is a growing demand for very fast on-chip interconnects that can provide efficient communication among them.

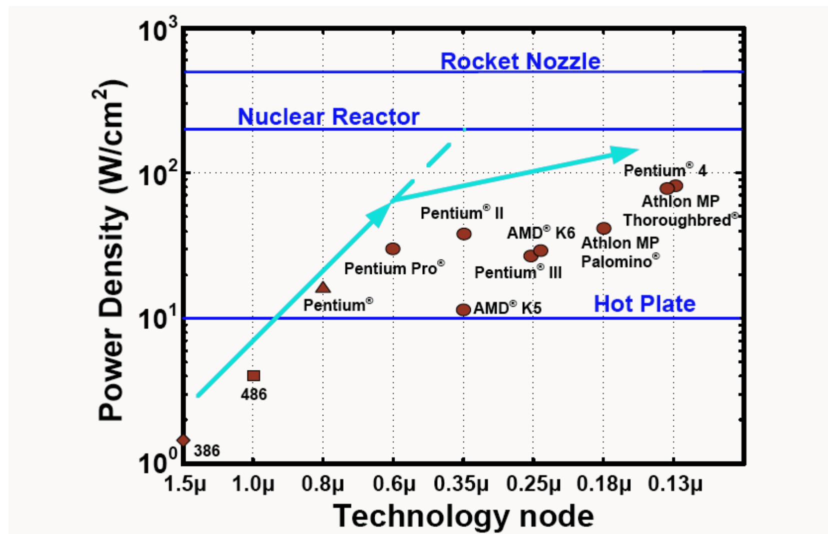

Figure 1.2: Increase in CPU's power dissipation density with the evolution of technology nodes.

Also, the current trends indicate that electrical interconnects used for chip-to-chip communication cannot keep up with chip's processing capabilities. Based on metallic wires (aluminum and copper), electrical interconnects suffer from the drawbacks like loss (due to finite resistance), signal delay (due to RC constant) which limits the bandwidth and cross-talk. These limitations are now becoming evident even at very short distances of several hundreds of microns that are characteristic for chip-to-chip ('inter-chip') and on-chip ('intra-chip') interconnects. The major reason for this lays in the fact that the electrical interconnects within a chip don't scale-down in size at the same rate as transistors,

which results in a limited range of the fast interconnects [4]. Although, off-chip electrical interconnects with 20 Gb/s over 18 cm distance have been demonstrated, it is expected that achieving comparable bit rates over 25 cm distance or above, would be extremely challenging, primarily due to the complexity of the equalization circuitry required for higher data rates [5, 6]. These performance limits become obvious when the future requirements are considered. The system architecture for the next generation of high performance integrated circuits (expected in 2022) would require input/output (I/O) data rates between 82 Tb/s [7] and 780 Tb/s per chip [8].

The bandwidth of electrical interconnects is not the only limiting factor. As the chip dimensions shrink, there is less space available at its physical boundaries to integrate interconnects that can support the required data rates. It is already shown that electrical interconnects cannot provide ~ 100 Tb/s capacity because they cannot achieve the required level of integration density. Simply, a bus of electrical interconnects that could support such data transfer rate cannot fit into the circumference of a chip [8].

The number of bytes (of communication to memory) per floating point operation (FLOP) is a common performance indicator in the computer architecture. It is desired to achieve the value of 1 Byte/FLOP of access to distant memory (not, local, cache memory). However, it is becoming increasingly difficult to maintain this ratio with the current electrical interconnects and this leads to the so-called 'Byte/FLOP gap' [8]. This phenomenon that relatively slow electrical interconnects are now imposing limits on the overall performance of integrated circuits is known as the *interconnect bottleneck* and is emerging as a major obstacle in continuing along Moore's Law path in high-performance computer systems.

Another, perhaps even more important aspect of this problem is the energy consumption. With the ever-increasing demand for on-line traffic and data storage capacity, the data centers located around the world have become a significant consumer of electrical energy. It is estimated that they consume around 2% of the total electrical power worldwide, with about 15%-30% of this consumption spent on interconnects [8, 9]. Another estimation claims that the annual costs of power-supplying and cooling high-performance switches in the data centers has reached the annual costs of purchasing new ones [10]. To solve one part of this problem, more energy-efficient interconnects are needed. The drive for less power-hungry interconnects comes also from the need to keep heat generation in microchips under control. As the miniaturization in semiconductor technology continues, switching interconnects becomes the main source of power consumption in ICs. This can be illustrated by the fact that at the 1.0 μm technological node, the switching energy needed for a single switching operation of a Metal-Oxide-Semiconductor Field Effect Transistor (MOS-

FET) was ~ 300 fJ, while it took ~ 400 fJ to switch a 1 mm-long electrical interconnect [11]. For 100 nm wide MOSFET gates, these energies shrank to ~ 2 fJ and ~ 10 fJ, respectively [11]. Today, individual switching chips consume about 20-40 pJ per switched bit, of which the switching circuits themselves can consume less than 1 pJ per switched bit (for a simple crosspoint switch), with the rest of the energy consumed by electrical I/Os of the chips [10].

The problem becomes even more critical if we take into account energy-per-bit requirements for the future chip-to-chip interconnects. Following the International Roadmap for Semiconductors (ITRS) predictions, chip power dissipation will stay around ~ 200 W, while the off-chip bandwidth in 2015 should be 82 Tb/s, which allows only ~ 490 fJ of energy per bit. Predicting off-chip bandwidth of 230 Tb/s in 2022, implies only ~ 170 fJ per bit [8].

Considering all these requirements, it becomes evident that electrical interconnects cannot support further growth in IC performance along Moore's Law and new technological solutions must be pursued.

1.2 Photonics and the Optical Interconnects

In parallel with the progress in semiconductor fabrication technology and microelectronics, a series of other inventions led to the development of modern optical components that eventually revolutionized global communication. The demonstration of the first laser in 1960, followed by the first semiconductor laser in 1962, along with the technological advances in the fabrication of low-loss optical fibers, in the early 1970's, laid the foundation of modern optical communications. Also, these developments gave birth to a new field of science dealing with generation, transmission, modulation, amplification and detection of light. In analogy to electronics, based on manipulating electrons in semiconductor devices, this science was given the name of photonics, after the fact that it was dealing with the quanta of electromagnetic radiation - the photons.

Although photonics is, by no means, exclusively focused on telecommunications, these applications were the main driving force for the research effort and development of photonics in its first decades. High-performance semiconductor lasers, low-loss optical fibers and erbium-doped fiber amplifiers revolutionized optical telecommunications and enabled the development of the communication society as we know it today, with the Internet at its core.

Advantages of optical fibers over metallic wires quickly became evident, especially in long-haul communications. Featuring low-loss, immunity to electromagnetic interference (EMI) and cross-talk, as well as a much wider bandwidth allowing multiplexing channels in frequency domain (i.e. over different wavelengths), the optical fibers replaced the metallic, coaxial cables for the

	MAN/WAN	Cables–long	Cables–short	Card-to-card	Intra-card	Intra-module	Intra-chip
Length	Multi-km	10–300 m	1–10 m	0.3–1 m	0.1–0.3 m	5–100 mm	0–20 mm
No. of lines per link	One	One to tens	One to tens	One to hundreds	One to hundreds	One to hundreds	One to hundreds
No. of lines per system	Tens	Tens to thousands	Tens to thousands	Tens to thousands	Thousands	Approximately ten thousand	Hundreds of thousands
Standards	Internet Protocol, SONET, ATM	LAN/SAN (Ethernet, InfiniBand, Fibre Channel)	Design-specific, LAN/SAN (Ethernet, InfiniBand)	Design-specific and standards (PCI, backplane InfiniBand and Ethernet)	Design-specific, generally	Design-specific	Design-specific
Use of optics	Since the 1980s	Since the 1990s	~2010	Present time	Near future	Probably after 2015	Later

Figure 1.3: Hierarchy of interconnects and the introduction of optical technologies in the course of time. Adapted from [12].

long-haul, wide-area and metropolitan-area networks (MAN) during the last two decades of the 20th century. This trend of bringing the optical links to ever shorter distances continues today, presently embodied through the Fiber-to-the-home (FTTH) network architecture. Figure 1.3, taken from [12] presents the interconnect hierarchy according to distance and illustrates the evolution in replacement of metallic interconnects with optics, with the predictions for the future.

This technology transition from electrical to optical links occurred when the energy consumption per bit per unit distance in optical interconnects became lower than in their electrical counterparts. Historically, this cross-over occurred when the optical links achieved the total bandwidth-distance product exceeding $\sim$ 100 Mb/s-km. [10]. Today, the optical fibers are already present in short-distance (1-10 m), rack-to-rack, interconnects. This is especially obvious in the case of supercomputers that rely on high-speed optical links between the individual racks. For example, IBM Roadrunner employs over 92 km of multi-mode optical fibers [13]. Such a massive amount of optical cables becomes both cumbersome and expensive to purchase and install.

On the other hand, there is a trend, and also a strong need, to switch from electrical to optical links at even shorter distances, and employ them for board-to-board, chip-to-chip and intra-chip interconnects. As this trend continues, the question arises which kind of technology is the most suitable to integrate optical and electrical components at the board or chip level.

Miniaturization in electronics led to a switch from discrete electrical components to development of monolithically integrated electronic circuits which

eventually evolved into the very-large-scale integration (VLSI) chips we have today. Following a similar pattern, miniaturization trends in photonics resulted in gradual replacement of discrete optical components with photonic integrated circuits (PICs) employing multiple optical functionalities within a single package. However, unlike electronics, which is based on a single material - Silicon, photonics employs several different material systems for fabrication of PICs. The most common of these are:

1. **Silica-on-silicon**: based on using doped silica (as a core) and undoped silica (as cladding layers) on a Silicon substrate. This is a very mature and robust technology, but due to a very low refractive index contrast, the bend radii of waveguides are large resulting in very large device foot prints. Consequently, this translates into very low integration density, rendering this technology unsuitable for on-board or on-chip interconnects. Moreover, only passive devices can be realized on this platform.

2. **Silicon-on-insulator (SOI)**: employing a high index contrast between the top silicon waveguide layer and the underlying buried oxide (BOX) layer (acting as a cladding), mounted on a silicon substrate. Based on CMOS-compatible fabrication processes and offering very high density integration, due to small bend radii of devices, this technology represents the foundation of Silicon Photonics which, as we shall later see, has a very promising perspective for the realization of on-chip optical interconnects. The phrase CMOS-compatible that is used here, refers to the fact that the SOI wafers can be processed using the standard CMOS-processing tools and recipes. As the top layer in the SOI platform is silicon, the same CMOS fabrication processes used for patterning silicon in microelectronics (like dry etching and deposition), can be employed in SOI wafers as well. In addition to this, the SOI wafers don't contain organic molecules (like polymers), alkali or alkaline earth metals or any other metal (like gold) that could act as an impurity and contaminate other silicon wafers that are subsequently (or simultaneously) processed using the same equipment.

3. **III-V Semiconductor materials**: primarily GaAs and InP-based materials (binary, ternary and quaternary alloys). Due to the direct bandgap, as well as the good optical and electrical properties, these materials have been used for decades for fabrication of semiconductor lasers. Also, the whole set of active and passive optical functions can be realized in these materials. The drawback is they are more expensive than silicon, produced in smaller diameter wafers (usually, 50 - 75mm), with more expensive, lower-yield processing technology than cannot compete with CMOS-based technology on a cost-per-chip basis. Traditionally, it is a

technology of choice for high-performance, stand-alone components (mostly lasers for long-haul optical communication networks). Recently, also some highly integrated photonic devices have been demonstrated using technological platforms based on these materials [14, 15].

4. **Lithium Niobate ($LiNbO_3$)**: a nonlinear, piezoelectric crystal that has a variety of applications in photonics, mostly in electro-optical modulators, acousto-optic devices and non-linear optics. Although a very popular material for some niche applications, lithium niobate offers little perspective as a material platform for integration due its complex processing requirements which make it economically ill-suited to large-scale photonic integration and also the fact that it cannot be used for realization of lasers and detectors.

5. **Polymers**: representing a variety of relatively cheap materials with cost-effective manufacturing. Although very attractive for some low-cost applications, these materials usually suffer from a large thermo-optic effect, low index contrast and very often long-term reliability issues. Despite having a certain potential for some niche applications, these materials are not suitable for large-scale on-chip or on-board integration with other photonic and electronic components.

This brief overview of the most important material platforms in PICs, clearly suggests that only SOI and III-V semiconductors offer the prospect of high-level co-integration with standard CMOS-based electronics. Not surprisingly, the development of CMOS-compatible, optical interconnects suitable to resolve the problem of the electrical interconnect bottleneck has been the subject of intensive research efforts in the past decade.

Many researchers focused on a hybrid architecture utilizing discrete optical components integrated with CMOS in a multi-chip module (MCM) package. Due to the lack of efficient light emitters in silicon, the preferred approach was to use discrete lasers realized in III-V materials. Very often, the use of vertical cavity surface emitting lasers (VCSELs) was suggested in these solutions. This was not surprising given the fact that VCSELs are widely used today in optical interconnects for local area networks (LAN) and short range links in data centers and high-performance computing systems. In one solution, a transceiver module based on 90 nm CMOS technology and a 1 x 12 array of VCSELs and detectors is proposed, allowing 10 Gb/s per channel (120 Gb/s, in total), with a potential for achieving 18 Gb/s per channel data rates [6], while in a different approach, an array of 256 VCSELs is bonded on a CMOS VLSI chip, in order to provide a total data rate of 320 Gb/s (256 x 1.25 Gb/s) [10].

Despite these solutions, based on hybrid integration, an even higher level of integration between optical and electrical components will be required for

the optical interconnects expected to meet the requirements of the future high-performance computing systems. Therefore, solutions based on monolithic integration, bringing the optical and electrical components within the same chip, are actively pursued. The need for such integration, clearly points to the CMOS-compatible, SOI material platform as the technology of choice for further development of such optical interconnects. This brings us to the branch of photonics that is of most interest to us.

1.3 Silicon Photonics

Based on Silicon as the primary material and a CMOS-compatible fabrication processes, Silicon Photonics evolved over the course of more than two decades from the modest beginnings in the late 1980's to one of the most dynamic and most promising branches of photonics today. The rationale for using silicon as the basic material for photonic components is based on several facts. Silicon is transparent at traditional telecommunication wavelengths around 1.3 μm and 1.55 μm. Silicon wafers have the lowest cost per unit area and the highest crystal quality of any semiconductor material. Even 300 mm diameter SOI wafers used in silicon photonics today are cheaper, per unit area, than commercial 150 mm diameter GaAs or 100 mm diameter InP wafers. Compatibility with traditional silicon manufacturing processes used in electronics is probably the most important argument in favour of Silicon Photonics. Exploiting the existing manufacturing infrastructure and processing technology of the silicon semiconductor industry bring enormous economical benefits and advantage over other photonic platforms, such as III-V materials. High quality silicon-on-insulator (SOI) wafers, provide strong optical confinement due to the high index contrast at 1.55 μm between silicon (n = 3.45) and SiO_2 (n = 1.45). This enables scaling of the photonic devices to the level of hundreds of nanometers. Additionally, this implies high optical intensity of the light confined within the silicon waveguides, making it possible to observe nonlinear optical interactions, such as Raman and Kerr effects, within chip-size devices [16].

After the development of low-loss waveguides [17] and passive components on the SOI platform during the 1990s [18, 19], the beginning of the third millennium brought significant achievements in Silicon Photonics, with the demonstration of high performance active components like high-speed modulators [20–22] and photodetectors [23, 24]. However, due to its indirect bandgap, silicon was considered unsuitable for light emission devices and for many years the demonstration of silicon optical amplifiers and lasers has been "the Holy Grail of silicon photonics" [16], both because of its physical and technological challenges and huge benefits for potential applications. Efforts in this field came to fruition when an optically-pumped silicon laser based on stimulated Raman

scattering (SRS), operating in pulsed regime was demonstrated in 2004 [25], followed a year later by the demonstration of continuous-wave (CW) lasing [26]. Despite this important success, it is unlikely that a Raman silicon laser will play any role in optical interconnects, because it is optically-pumped [16]. Therefore, realization of an effective, electrically-pumped laser on silicon remains a serious challenge and a stumbling block on the path of further on-chip integration of photonics components. This is especially obvious in the case of optical interconnects, where the integration of the light sources remains a critical issue [11].

Most of the latest solutions for optoelectronic transceivers are based on the use of co-packaged III-V lasers directly mounted on a silicon die. For example, in a 40Gb/s optoelectronic transceiver demonstrated by Luxtera, a single III-V continuous-wavelength (CW) laser enclosed in an optical micro-package (including a lens) is flip-chipped onto the underlying silicon die and optically coupled to the photonic chip via grating couplers [27, 28]. The underlying silicon photonic platform provides all other optical functionalities, including external modulation for four individual optical channels and integrated germanium photodetectors [28]. Further evolution of this device led to the demonstration of the first single chip 100 Gb/s optical transceiver, targeted for the next generation cloud computing data centers and high performance computing (HPC) systems [29].

Co-packaging high-performance III-V lasers with high level integration PICs realized in silicon photonics presented a logical step in developing high-speed optical interconnects, but future bandwidth and energy consumption requirements would require further progress into bringing the light source onto the very same die where the integrated photonic components are located.

1.4 Intel's vision for the optical interconnects

Efforts to develop high-performance and energy-efficient optical interconnects suitable for rack-to-rack, board-to-board and chip-to-chip data communication are not restricted only to university research groups around the world. Some leading companies in electronic industry, like Intel Corporation, IBM and HP are actively involved in this research. A couple of year ago, researches from Photonics Technology Lab of Intel Corporation presented their vision for optical interconnects suitable to meet the future demands [30, 31]. The main idea was to design an optical transceiver chip (module) capable of providing a 1Tb/s data link for chip-to-chip communication. The transceiver module would comprise both the transmitter and the receiver optical chips and would be integrated on a computer board, as illustrated in Figure 1.4. The transmitter optical chip in its turn would comprise an array of 25 single-wavelength lasers made in III-V

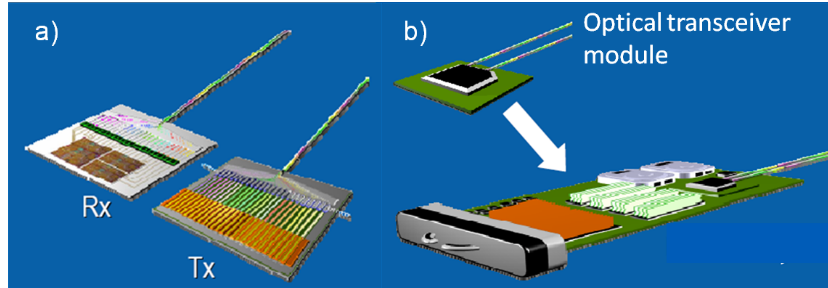

Figure 1.4: (a)Intel's vision of the optical transciever module comprising both the receiver (Rx) and transmitter (Tx) optical chips; (b) Integration of such a optical module on a computer board that can further be integrated in a Tera-scale computing system. Reproduced from [32].

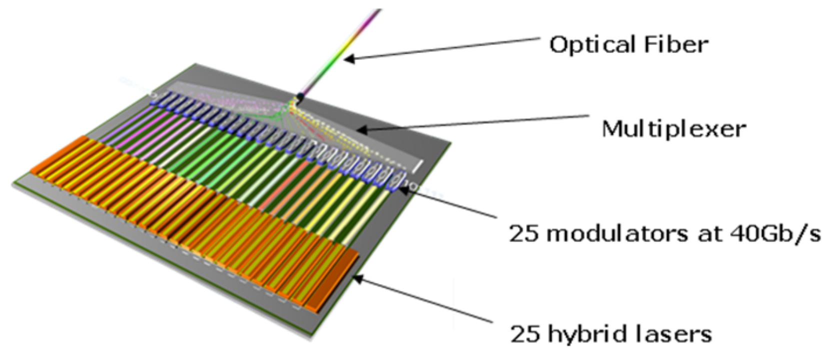

Figure 1.5: Intel's vision of the transmitter optical chip for 1 Tb/s data rate. Reproduced from [32].

materials integrated on to an SOI silicon photonic platform. More specifically, it was envisioned that these would be hybrid III-V/Si distributed-feedback (DFB) lasers. Each of these lasers would be optically connected to a 40 Gb/s modulator realized on a SOI platform. Outputs of these 25 modulators would be further connected to the multiplexer (MUX), also realized in the same SOI platform. Eventually, the MUX output would be coupled to optical fiber for transmitting outgoing signals (see Figure 1.5). Similarly, a receiver chip would comprise an adequate demultiplexer (DEMUX) and an array of integrated photodetectors for each of the optical channels transmitted through the incoming optical fiber. In this way, a 1 Tb/s data rate is achieved as a product of 40 Gb/s rate in each of 25 optical channels.

Optical modulators, multiplexers and photodetectors suitable for this concept have already been demonstrated on an SOI platform. The greatest chal-

lenge in this vision of a transceiver optical module is integration of the efficient DFB laser on an SOI platform and its cost-effective wafer-scale fabrication. Intel's vision calls for heterogeneous integration of III-V materials as well-proven and efficient light emitters to be used as gain medium for the hybrid lasers. In theory, mounting a prefabricated laser made in III-V materials on a SOI platform and optically coupling it to the underlying PIC is possible. However, the main idea is to allow wafer-scale integration of these lasers on an SOI photonic platform. Taking into account that 200 mm diameter wafer comprises, on average, 90 dies, and assuming 25 lasers on each die (as envisioned by Intel), this means that 90 x 25 = 2250 lasers would need to be integrated in a wafer-scale process. Mounting the prefabricated III-V lasers requires strict alignment and is, consequently, both time consuming and costly and, therefore, completely unsuitable for wafer-scale integration. Obviously, a different approach is needed that would allow such a wafer-scale integration. The proposed solution is a hybrid integration of III-V materials, comprising multiple-quantum wells (MQWs) providing a gain medium, onto an SOI wafer, followed by post-processing which would result in fabrication of hybrid lasers exactly where they are needed on every individual die within a wafer. In this way, no optical alignment is needed - laser positions are lithographically defined and aligned to the underlying optical structures in the SOI platform.

Due to well-know difficulties in growing III-V materials on silicon (due to lattice-mismatch), bonding is currently viewed as the only viable alternative. In practice, full wafer-to-wafer bonding is the most commonly used procedure. However, in this case, due to peculiarities of III-V materials, this approach is not seen as a cost-effective solution from the point of view of industrial scale fabrication. Namely, wafers of epitaxially-grown III-V materials are usually 50 mm (2-inch) to 75 mm (3-inch) in diameter, which is much smaller than standard 200 mm diameter SOI wafers (expected to move to 300 mm diameter in the near future). Due to this wafer size mismatch, bonding a single III-V wafer on a SOI wafer is not effective, as large areas of SOI would remain uncovered. Bonding several III-V wafers on a single SOI wafer is possible, but this approach still results in underutilization, as most of the III-V material is removed in the subsequent laser fabrication. This is because the footprint of the lasers on a SOI die containing all other optical components within a PIC (modulators, MUX, waveguides, etc.) is still very small, covering perhaps just a few percents of the total die area. Therefore, according to Intel's vision the only cost-effective integration approach is multiple die-to-wafer bonding, i.e. simultaneous bonding of the multitude of small III-V dies on a single SOI wafer. In this technique, III-V dies are arranged in such a manner to be bonded only at the specific location within the SOI die where they are needed (i.e. where the lasers would be fabricated) (see Figure 1.6). Consequently, III-V material would be much more

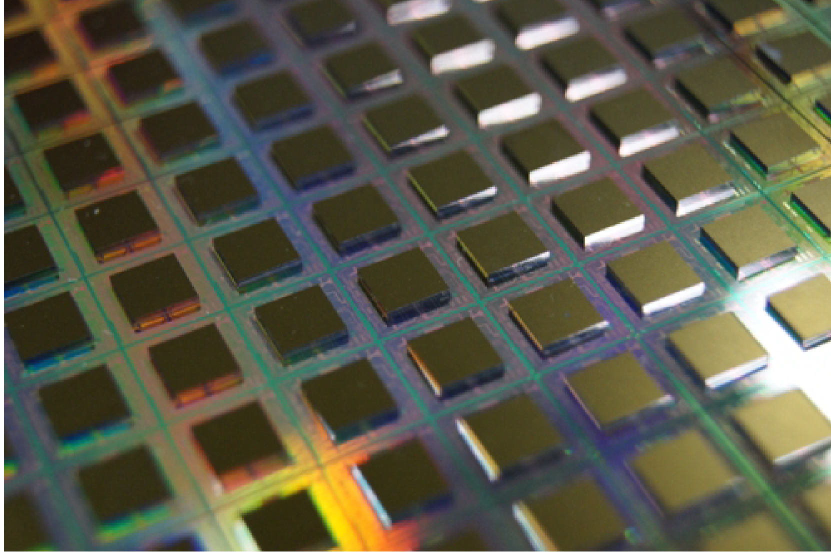

Figure 1.6: Multiple die-to-wafer bonding approach for wafer-scale integration: multitude of individual dies bonded onto a single wafer. Taken from [33].

efficiently used. Additionally, the bonding alignment requirements in this case are not too strict - in the order of hundreds of micrometers - since the devices are defined by photolithography in the post-bonding processing.

Looking beyond the bonding technology used to bring III-V materials onto an SOI photonic platform, the choices should be made regarding the design of the DFB lasers that were to be used in this optical transceiver module. In a more conventional approach, the laser cavity and the grating providing the distributed feedback can be completely realized in the III-V material. In this way, the optical confinement within the gain region can be maximized, resulting in a relatively short cavity, consequently reducing both the amount of III-V material used and the device footprint. However, as the emitted light eventually needs to get into the underlying waveguides on an SOI chip, an elaborate coupling scheme needs to be implemented in this case in order to bring the light from the III-V layers on top of the structure, down to the SOI waveguides. In theory, the use of grating couplers or narrow-tip adiabatic tapers can solve this problem, but the fabrication of these structures using standard photolithographic techniques might be too difficult for implementation. The use of wafer-scale processing techniques for laser fabrication is necessary in order to bring all the advantages of the economy of scale. High resolution, but time-consuming electron-beam (e-beam) lithography is, therefore, not considered as

a suitable fabrication technology. With these limitations in mind, it was preferable to adopt a laser design in which the silicon waveguide itself represents the part of the laser cavity, allowing the bulk of the optical power to be confined within the silicon, not the III-V gain material.

Adopting this approach, the Optoelectronics Research Group from University of California, Santa Barbara (UCSB), co-funded by Intel Corporation, demonstrated evanescently-coupled, hybrid III-V/Silicon lasers that would be suitable for this kind of integration [31, 34, 35]. Critical technology that allowed fabrication of these devices was low-temperature direct (molecular) bonding between III-V and SOI wafers [36]. With a sufficiently thin intermediate layer of SiO_2, it was possible to achieve evanescent coupling between the optical modes within the III-V material and the SOI waveguide and formation of a hybrid optical mode in which the bulk of the optical power was confined within the silicon rib waveguide itself. Within several years, using this technology and the concept of evanescent-coupling, several components were demonstrated including DBR and DFB lasers emitting at 1550nm [35, 37, 38], a mode-locked laser [39], a Fabry-Perot laser at 1310 nm [40] as well as amplifiers and photodetectors [41].

This progress represents a successful proof of concept of evanescently-coupled lasers and amplifiers on an SOI platform. However, the road from a successful demonstration of a device prototype in the lab to the industrial scale fabrication is a very long one. Requirements for the latter are very strict and rigorous testing and overall assessment is required to bring the product to a large-scale production, requiring high yield fabrication processes and device reliability. Following the initial success of evanescent, hybrid III-V/Si lasers based on molecular bonding, Intel was willing to make another assessment of the integration technology in order to make sure that the best bonding technology would be chosen for this purpose.

1.5 Rationale for this work

Following Intel's vision of integration of III-V material on an SOI photonic platform, it is obvious that the choice of the adequate bonding technology for the multiple die-to-wafer bonding is essential. The low-temperature, direct bonding process developed by the research group at UCSB and used for fabrication of evanescent hybrid III-V/Si lasers, requires very clean, smooth and contamination-free bonding surfaces. Molecules on both bonding surfaces need to get into intimate contact so that covalent bonds between them can be created. This implies an elaborate wafer cleaning procedure before the bonding and practically no tolerance to any particle contamination which would create a large unbonded area at the interface between two wafers. Such strict requirements raise questions whether this technology can provide sufficiently

high bonding yield in an industrial fab environment.

Among other bonding techniques, which will be presented in more detail in Chapter 2, the adhesive bonding based on thermosetting polymers looked as an attractive alternative to direct bonding. The greatest potential advantage was seen in the fact that the polymer is applied to the wafer surface in a liquid form, filling the voids and compensating for the surface roughness and the presence of small particles that could be enveloped within the polymer and therefore not compromise the bonding quality. Subsequent curing at elevated temperature causes polymerization and solidification of the bonding layer creating a permanent bond between the wafers.

The most promising thermosetting polymer for this purpose, is divynilsiloxane bis-benzocyclobutene (DVS-BCB) which was developed in the late 1980s by Dow company and gained a variety of commercial applications during 1990s in microelectronic packaging as a dielectric suitable for physical protection and insulation of fabricated devices [42]. Thanks to its good properties and the fact that its polymerization gives no byproducts (thus, no out-gassing), DVS-BCB (or BCB, for short) also became popular as a material for adhesive wafer bonding [43–46]. Not surprisingly, it was recognized as an attractive material for heterogeneous integration in photonics as well.

During the first decade of this century, the Photonics Research Group at Ghent University in Belgium has reported a BCB bonding process [47] and it has demonstrated photodetectors [48, 49], hybrid III-V/Si lasers with adiabatic polymer-overlayed inverted tapers [50] and several other photonics devices [51] based on BCB bonding. Following this development, it was interesting to study the possibility of using BCB bonding technique as a technological alternative to direct bonding. The challenge was in the fact that evanescent-coupling devices required relatively uniform bonding layers usually thinner than 100 nm which had not yet been demonstrated using BCB bonding. Additionally, all the previously reported photonic devices were based on a manual BCB bonding process, suitable for research and development, but not for an industrial cleanroom environment. Developing a machine-based process, utilizing commercial wafer-bonding tools was a prerequisite for consideration of the industrial application of this bonding technique.

Consequently, the rationale for this work came from the idea to explore the possibility of using DVS-BCB bonding for a demonstration of evanescently-coupled hybrid III-V/Silicon lasers, emitting at 1310 nm. To achieve this objective, a joint research project between the Photonics Research Group of Ghent University and Intel's Photonic Technology Lab was agreed. The work on this PhD thesis was carried out within that project.

The goal of this work was to demonstrate that adhesive bonding based on the use of DVS-BCB polymer is a viable technology for integration of III-V ma-

terials on an SOI platform and that evanescently-coupled, hybrid III-V/Silicon lasers can be effectively fabricated using this technology.

As no evanescently-coupled lasers had been previously demonstrated using DVS-BCB bonding technology, the innovative aspect of this work comprises the following elements:

1. development of a special, machine-based, DVS-BCB bonding process producing sufficiently thin bonding layers and therefore suitable for the fabrication of evanescent, hybrid III-V/Si lasers;
2. design of robust evanescently-coupled hybrid III-V/Si lasers which can tolerate variations in the DVS-BCB bonding layer thickness (20 - 120 nm);
3. optimizing the fabrication process for hybrid III-V/Si lasers based on DVS-BCB bonding; and finally
4. demonstration of both Fabry-Perot and DFB hybrid III-V/Si lasers based on DVS-BCB bonding, emitting at 1310 nm in a continuous-wave (CW) regime.

1.6 Outline of the thesis

Following this chapter, which presented the short introduction and the motivation for this work, the rest of this thesis is divided into six additional chapters. In Chapter 2, a more elaborate review of competing bonding technologies, suitable for heterogeneous integration of lasers on an SOI platform will be presented. In addition to this, an overview of the state-of-the-art lasers fabricated on an SOI platform will be given, mentioning the advantages and the drawbacks of each design. After this chapter, which to some extent supplements the introduction, the focus will finally shift to the research that was carried out during the work on this thesis. Design of heterogeneously-integrated III-V/Si lasers based on adhesive bonding will be presented in Chapter 3. Both Fabry-Perot and single wavelength laser designs will be discussed in detail. In Chapter 4, development of the DVS-BCB bonding process suitable for evanescent coupling will be presented. Chapter 5 focuses on the device fabrication process that also needed a lot of optimization effort in order to produce sufficiently good results. All of the work on development of the DVS-BCB bonding procedure, and most of the work on the laser fabrication was carried out in the cleanroom facilities of Ghent University. As we shall see in these two chapters, success in this work was critical for the eventual demonstration of the lasing devices. Characterization of the fabricated lasers is presented in Chapter 6. In the final, seventh chapter of this

thesis, concluding remarks on this work will be given along with the prospects and suggestions for future work.

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2

Heterogeneous Integration on SOI platform: Technologies and Devices

This chapter will focus on the heterogeneous integration of III-V materials on an SOI photonic platform, providing a short review of state-of-the-art technologies employed for such integration and demonstrated lasers that were fabricated using these technologies. In the beginning of the chapter, the most important technologies for heterogeneous integration will be presented. Special attention will be given to the bonding techniques which, at this moment, offer the most promising solutions for the fabrication of effective, electrically-pumped lasers on an SOI photonic platform. Following this, a short review of the most important lasers based on heterogeneous integration on an SOI platform will be presented. After this review of state-of-the-art in the field of heterogeneously integrated lasers, the chapter will be concluded with the motivation for the work on adhesively-bonded, evanescently-coupled hybrid III-V/Silicon lasers.

2.1 Technologies for heterogeneous integration - introduction

Continuous efforts to improve performance of integrated circuits in order to follow the predictions of Moore's Law were presented in the previous chapter. Ac-

cording to the terminology adopted by the International Technology Roadmap for Semiconductors (ITRS), this continuous scaling (more precisely, shrinking) of physical dimensions of components providing digital functionalities, resulting in increase in integration density and device performance (higher speed, lower energy consumption), is known as "More Moore". This phrase intuitively suggests the main goal of this effort: to continue along Moore's Law path in improving overall performance of digital integrated circuits.

However, in parallel with this, the progress in integration technologies gives a possibility to incorporate some non-digital functionalities onto a single chip or a single package. These non-digital functionalities (like sensors, actuators, analog and RF circuits, photonic components, biochips, etc.), don't necessarily scale according to Moore's Law, but when incorporated together with digital functionalities, they provide an additional value to them and allow fabrication of more complex, fully functional systems. In the recent years, we are witnessing strong efforts to incorporate these additional functionalities into a single package or even a single chip. Consequently, this leads to transition from fabrication of systems on a board level to lower levels of integration, namely System-in-Package (SiP) and System-on-Chip (SoC). To describe this approach leading towards functional diversification within a chip, ITRS adopted a phrase "More than Moore", clearly suggesting the main direction of this effort: to bring non-digital functionalities into a single package (or a chip) in order to provide additional value (more than just scaling and improved performance) and a system-level functionality. The relation between "More Moore" and "More than Moore" approaches is illustrated in Figure 2.1.

Many of these non-digital functionalities are realized in materials other than silicon, implying that in order to continue along the "More than Moore" direction, it is necessary to integrate these different materials onto a single substrate. Heterogeneous integration is the technology enabling this kind of integration. Among these non-digital functionalities, the photonic functionalities are especially suitable for integration with digital electronics, due to a relatively straightforward signal conversion from optical to electrical domain and vice versa. Adding a layer comprising integrated photonic devices (realized, for example, in some non-silicon material) onto a CMOS substrate containing standard digital electronic circuits is a typical example of heterogeneous integration. The vision of on-chip optical interconnects enabling fast communication between multiple processor cores, as mentioned in Chapter 1, can also be viewed within this context. Beside this heterogeneous integration of a digital electronics layer with a non-digital functionality layer, we can speak of heterogeneous integration within the photonics itself. Various materials providing different photonic functionalities can be employed together to form a specific photonic component, giving it a new quality that would be very difficult to re-

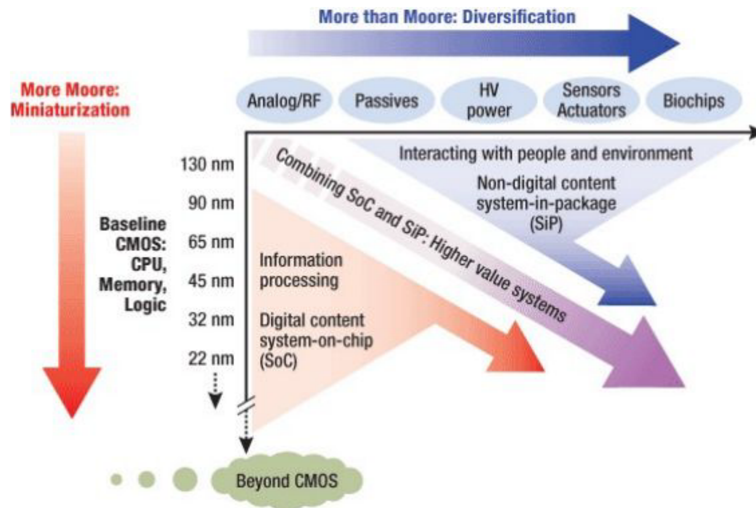


Figure 2.1: Trends in integration technologies: More Moore and More than Moore directons. Taken from [1]

alize on a single material platform. From the perspective of the subject of this thesis, we are interested in heterogeneous integration technologies that allow the realization of active optical functions (based on III-V material) on a passive SOI photonic platform.

From the technological point of view, we can classify three different approaches in this kind of integration: (i) hybrid integration (flip-chip bonding), (ii) monolithic integration (based on hetero-epitaxial growth) and (iii) wafer bonding techniques.

2.2 Hybrid Integration (Flip-Chip Bonding)

Hybrid integration assumes mounting and bonding of individual, pre-fabricated, optimized components (e.g. lasers or light-emitting diodes) on a common substrate containing the circuitry that connects individual components into a functional system. This is a very well-known technology with broad applications, mostly in electronics where fabricated electrical or optoelectronic components are mounted on printed circuit boards (PCBs). This integration method is called flip-chip bonding. Typically, gold or gold-tin (AuSn) alloy solder bumps are used to attach the components (chips) to the substrate in a process also known as controllable collapse chip connection (C4).

The usual processing sequence comprises creation of contact pads, known as under bump metallization (UBM) on both surfaces. This metallization en-

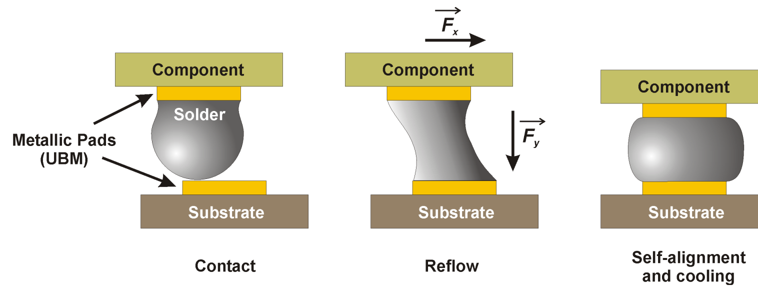


Figure 2.2: Flip-chip bonding: self-aligning of the component and the substrate during reflow

sures not only a good electrical contact, but also an easily wettable surface for a molten solder alloy. Following this, solder bumps are applied to the contact pads on top of the chip and the chip is then flipped over (hence the term "flip-chip") and positioned precisely above the substrate so that the solder bumps are facing the corresponding contact pads on the substrate. The chip is then mounted on top of the substrate, solder balls are re-melted and soldered to the UBM pads on the substrate. At this stage, the surface tension of molten solder bumps is used to self-align chip to the substrate, as illustrated in Figure 2.2. In the final step, the gap between the mounted chip and the substrate is filled with an electrically-insulating adhesive, providing additional mechanical strength and protecting the solder bumps from moisture and chemicals. An additional, very important, role of the underfilling adhesive is to compensate for differences in the coefficients of thermal expansion (CTE) of the chip and the substrate.

Beside flip-chip bonding based on soldering, there are other flip-chip techniques employing different materials and bonding principles. In a thermocompression flip-chip bonding, metal bumps (usually, gold bumps) are heated and exposed to pressure in order to achieve diffusion bonding. In a thermosonic flip-chip bonding, ultrasonic vibrations are used in combination with heat to soften the metal and achieve bonding at lower temperatures compared to standard thermocompression flip-chip bonding. Recently, flip-chip bonding techniques based on adhesives became popular. Typically, conductive adhesives are used. They represent polymer resins which are filled with conducting particles. In case of isotropic conductive adhesives, these particles provide conductivity in all directions. Usually, these are silver particles suspended in epoxy. In the case of anisotropically conductive adhesives, the metal particles or metal-coated polymer spheres within the adhesive assure electrical insulation in all directions before the bonding. However, after the bonding, metallic particles come into contact at the bonding pads and become electrically conductive in

the vertical direction.

From the perspective of heterogeneous integration for photonic applications, flip-chip bonding has certain advantages, being a well-known, established and robust technology. Solder flip-chip bonding has been used for integration of vertical cavity surface emitting lasers (VCSELs) on CMOS circuits for more than a decade [2]. However, some of its aspects make it unsuitable for high-density integration and wafer-level processing. Namely, a very accurate alignment (with a sub-micron tolerance) is needed for flip-chip bonding. Also, it is performed sequentially, on a die-per-die basis, drastically increasing the processing time. This is a serious drawback when a fast, wafer-level integration process is required. Additionally, in the case of photonic circuits, a gap between the substrate and the chip, which is usually several microns wide, makes the optical coupling between the bonded elements difficult and less efficient. In the end, the integration density of the components is limited by the pitch and size of the bumps, making this technology impractical for high-density integration applications.

2.3 Monolithic Integration (Hetero-Epitaxial Growth Techniques)

Unlike flip-chip or wafer bonding techniques, which are based on bonding two separately grown and processed semiconductor materials, monolithic integration in silicon photonics assumes growth of mostly III-V materials on silicon or SOI substrates. This approach is appealing, because, in perspective, it could allow selective growth of the desired, high-quality III-V layer stack on a wafer-scale without any need for complex bonding techniques. Additionally, no precision alignment, characteristic for flip-chip bonding would be required, as the photonic devices would be grown and fabricated in a post-growth processing. Despite the obvious allure of this integration approach, there are many challenges in its practical implementation.

2.3.1 Direct Growth on Silicon

Direct growth of III-V materials on Silicon (001) substrates is difficult due to a mismatch in lattice constants between most of III-V materials and silicon and a difference in thermal expansion coefficients. This leads to threading, misfit dislocations and anti-phase boundaries (APBs), which severely degrade the quality of the grown layers. The lattice constants of III-V materials, silicon and germanium are illustrated in Figure 2.3. The lattice mismatch of Si(001) and GaAs (4%) and Si(001) and InP (8%) is sufficiently large to prevent direct growth

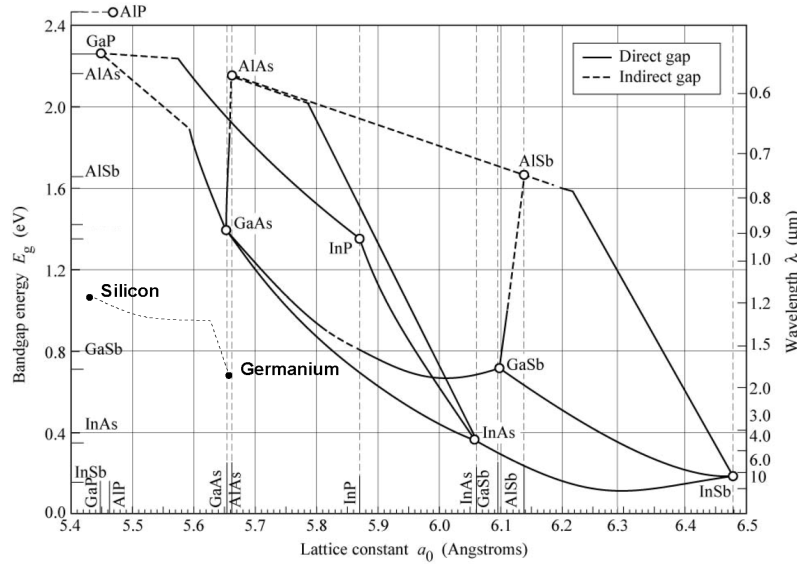


Figure 2.3: Lattice constants and bandgaps of the most important III-V semiconductors, silicon and germanium. Reproduced from [4].

of thin, high-quality GaAs or InP layers on silicon. Usually, there is a need for a buffer layer to suppress APBs. In one early work on fabrication of InP-based lasers emitting at 1.55 μm on Si(001) substrate, a 13 μm thick InP buffer layer was deposited on silicon for this purpose [3]. A popular technique to suppress formation of APBs is misorientation of a Si(001) substrate, usually by 4° towards the [110] direction in order to form diatomic steps on the silicon surface. However, since exactly oriented Si(001) substrates are used in the standard processing in the silicon industry, the prospects of use of misoriented Si substrates on industrial scale is still uncertain. It remains to be seen if the CMOS industry will tolerate a few degrees off-oriented Si(001) substrates for silicon photonics.

Due to the fact that GaP has a lattice constant very close to Si (lattice mismatch of only 0.36%), a group of researchers focused on growth of GaP on Si [5], using this technique to demonstrate electrically pumped GaNAsP/GaP quantum well lasers, emitting at ~ 980 nm [6]. Despite using an exactly oriented Si(001) substrate, an advanced annealing procedure was developed to generate diatomic steps in order to restrict the APB domains in the grown GaP to only 50 nm (~ 180 monolayers) above the Si substrate. The laser demonstration confirms the high quality of the quantum wells grown above only a 50nm-thick buffer layer of GaP on Si. However, the wavelength of 980 nm is not of interest in telecommunications and current research efforts are focused on achieving las-

ing at longer wavelengths, using Ga(NAsP) layers. The latest tested structures showed photoluminescence (PL) emission at 1.2 μm wavelength [7].

Antimony-based, III-Sb compounds represent another material system interesting for silicon photonics. Recently, there have been some promising results using GaSb-based system grown on a Si(001) substrate misoriented by 5° towards the [110] direction. Lasing in a pulsed regime at room temperature was reported at 2.25 μm [8] and 1.55 μm [9]. Using the same technique, a laser emitting in a continuous wave (CW) regime, at 2 μm and operating up to 35 °C has been demonstrated [10]. These successes make monolithic integration of III-Sb materials on silicon very attractive since the antimonide system can be exploited to fabricate several building blocks necessary for silicon photonics [7].

In another effort, focused on nitride-based compounds, researchers have recently demonstrated direct growth of InN nanowires on a Si(111) substrate. The grown nanowires exhibit almost no structural defects and good optical properties [11]. Additionally, InN/InGaAs core-shell nanowire heterostructures have been demonstrated [12]. The growth temperature of InN is in the range of ~400–500 °C, which is within the CMOS fabrication thermal budget.

2.3.2 Growth on silicon using buffer layers

Another strategy for growing III-V materials on a silicon substrate is based on the use of buffer layers, which are grown directly on silicon and used to filter out and accommodate all the structural defects. This approach is popular in efforts to grow III-V quantum dots on silicon. Using a 2μm-thick buffer layer of GaAs grown on a Si(001) substrate, oriented 4° towards the [111] direction, researchers have demonstrated $In_{0.5}Ga_{0.5}As$/GaAs quantum dot (QD) lasers, emitting at ~ 1 μm in pulsed regime and operating up to 85 °C [13]. InAs and InGaAs-based quantum dots were grown on top of the buffer layer to act as dislocation filters. In continuation of this work, the same research group has recently demonstrated lasers, emitting at 1.05 μm, that are monolithically integrated with a silicon waveguide [14]. In another work, a QD laser at 1.3 μm wavelength, operating up to 42 °C in a pulsed regime was demonstrated by growing GaAs-based quantum dot in a well (DWELL) structure on a Si(001) substrate oriented 4° towards the [110] direction [15]. In this case, InGaAs/GaAs and GaAs/AlGaAs superlattices were used as dislocation filters.

Another material system which is very interesting for potential applications in silicon photonics is germanium-silicon-tin ($Ge_{1-x-y}Si_xSn_y$) grown on silicon substrate. Some of its advantages lay in the facts that: (i) it can be deposited on Si(001) at low temperatures in a CMOS-compatible process, (ii) it can be grown selectively on silicon without nucleation on silicon dioxide, (iii) it can act as a buffer layer for the further growth of SiGeSn-based quantum wells at telecom

wavelengths and beyond, and (iv) its lattice constant can be tuned from 5.4 to 6.5 Å, so that several other III-V semiconductors can be grown on it. Feasibility of fabricating a GeSn/SiGeSn-based light source, modulator and photodetector, all monolithically integrated on a silicon platform and suitable for optical interconnects has been presented [16].

Aside from growing III-V materials on a silicon platform, a lot of effort has been put in the development of photonic components in the Ge-on-Si material system. Pioneering work in this field was carried out by a research group from Massachusetts Institute of Technology (MIT), led by professor Kimerling. Their approach is based on the epitaxial growth of a tensile-strained, n-type germanium on a silicon substrate, with the basic idea to achieve a direct bandgap light emission in germanium [17], which is, similar to silicon an indirect bandgap semiconductor. Tensile strain reduces the difference between the direct bandgap (located at Γ-valley) and the indirect bandgap (located at L-valley) in Ge to ~100 meV [18], while the n-type doping helps filling the L-valley with thermally generated extrinsic electrons [17], making such a modified germanium layers to start acting as a direct bandgap semiconductor. Following the initial demonstration of photoluminescence using such a tensile-strained, n-type germanium grown on a silicon substrate [19], both light emitting diodes [20] and electrically pumped lasers [21] have been demonstrated. However, the lasing is achieved at 15 °C with a very high threshold current density of 280 kA/cm^2 and only in a pulsed regime [21]. This raises question whether this integration approach can provide lasers with sufficiently low power consumption and superior characteristics. Beside these devices, detectors [22] and modulators [23], based on monolithic integration of Ge on Si have also been reported.

2.3.3 Epitaxial lateral overgrowth techniques

The use of thick buffer layers is not an ideal solution for heterogeneous integration of III-V materials and silicon waveguides, especially when evanescent-coupling needs to be achieved which requires a distance between the III-V active layers and silicon waveguides in the order of hundreds of nanometers. Epitaxial lateral overgrowth (ELOG), also known as microchannel epitaxy (MCE), is another attractive method to grow lattice mismatched III-V materials on a silicon substrate. In this approach, a III-V seed layer is deposited directly on a planar silicon wafer, either by Metal Organic Vapour Phase Epitaxy (MOVPE) or Molecular Beam Epitaxy (MBE). This seed layer normally contains a very large dislocation density ($\sim 10^9$ cm^{-2}). After this initial growth, a mask with the openings is deposited on the grown layer, as illustrated in Figure 2.4. After this, a

material, lattice-matched to the seed layer, is epitaxially grown. However, it is essential that the growth occurs only in the mask openings and that there is no nucleation on the mask itself that could initiate a growth process. In this way, when the growing material reaches the rim of the mask window, the growth continues laterally and along the mask surface (see Figure 2.4). Hence the term epitaxial lateral overgrowth comes to describe this kind of growth along the mask. To prevent threading dislocations to penetrate to the grown ELOG layer, it is essential that the width of the opening is smaller than the mask thickness, leading to the, so called, "necking effect" [24]. Using this simple geometrical feature, the dislocations are contained within the mask opening and the ELOG layer grown above the masks exhibits no defects.

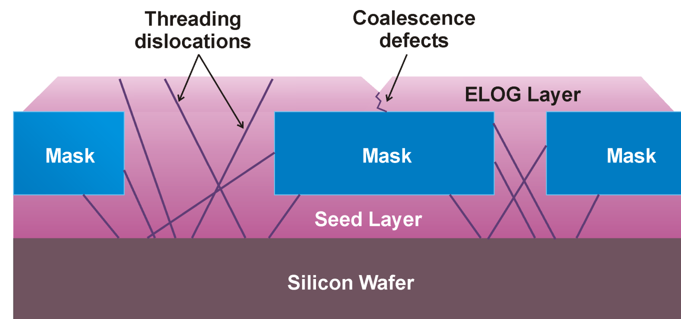


Figure 2.4: Schematic description of epitaxial lateral overgrowth (ELOG). Illustration of the *necking effect* used to prevent threading dislocations into an ELOG layer. Coalescence defects may occur at the interface of two adjacent ELOG layers.

This approach in monolithic integration has recently gained popularity and several research groups are actively pursuing it for applications in silicon photonics. Epitaxial lateral overgrowth of InP on Si shows that the room temperature photoluminescence intensity of ELOG InP layers is ~30% of that of homoepitaxial InP [25]. Recently, an integration scheme has been proposed for fabrication of a monolithic evanescently coupled silicon laser (MECSL) by combining an ELOG of InP on Si/SiO_2 waveguide, which also acts as the defect filtering mask [26]. This MECSL structure is illustrated in Figure 2.5. Growth of InGaAs/InP on SOI substrate by ELOG has already been demonstrated [27].

Another attractive approach is based on using Ge growth in SiO_2 trenches on a Si(001) silicon substrate to monolithically integrate InP. Growth of high quality InP in the shallow SiO_2 trenches on Si(001) substrates, using germanium seeds has been demonstrated [28–30]. The use of Ge as a seed reduces the lattice mismatch to InP to 4% (down from 8% between InP and Si). Additionally, Ge is deposited inside the trench with aspect ratio (height to width) larger than 2, which

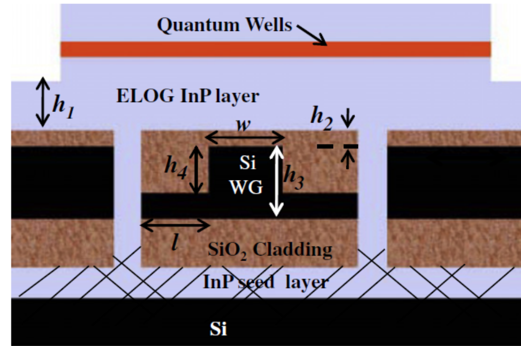


Figure 2.5: Proposed scheme of a monolithic evanescently coupled silicon laser (MECSL) realized by epitaxial lateral overgroth. Geometrical parameters can be optimised to achieve appropriate confinement both in silicon waveguide and in the quantum wells [26].

exploits the "necking effect" [24] to contain threading dislocations within the trench and allow the growth of defect-free InP at the top of the SiO_2 surface.

Obvious advantages of the ELOG technique, such as selective growth and very economical usage of generally expensive III-V materials, make it a very attractive candidate technology for large-scale, low-cost integration of nanophotonic components on silicon. However, to fully exploit the ELOG technique, the following issues have to be addressed: (i) the ELOG layer should be free of threading dislocations and coalescence defects; (ii) the thickness of the ELOG layer should be optimal to allow for effective coupling of light from the quantum wells grown on it into the waveguide beneath, which demands good control of thickness and defect elimination; (iii) the surface morphology of the ELOG layer should be smooth enough to allow further growth of quantum well (QW) structures such as lasers, detectors or modulators [7]. Also, instead of e-beam patterning, lithographic techniques should be utilized to allow large volume fabrication.

In conclusion, monolithic integration of III-V materials on silicon, as well as on the SOI platform, has gained a lot of attention recently and a steady progress is made. However, certain challenges lay ahead and it remains to be seen how they are going to be addressed. We already mentioned the use of misoriented Si(001) substrates in heteroepitaxy, as one potential problem. Procedures for successful growth on Si(001) substrates are yet to be developed. Realization of direct bandgaps in the GeSiSn material systems instead of a quasi-direct bandgap achieved through n-type doping also needs to be addressed.

This brings us to the wafer bonding techniques which have, so far, showed

the greatest potential for heterogeneous integration in silicon photonics.

2.4 Wafer Bonding Techniques

The term "wafer bonding" designates a variety of bonding techniques that are employed for permanent or temporary wafer to wafer bonding, although in some cases the same techniques can be used for die to wafer bonding, as well. During the last decade, wafer bonding has emerged as an important process technology in fabrication of SOI wafers (for both electronic and photonic applications), Micro-Electro-Mechanical Systems (MEMS), Micro-Opto-Electro-Mechanical Systems (MOEMS), photonic systems and 3D integration and packaging. However, this term comprises several different bonding techniques, based on different physical principles and it is useful to provide a classification of all the relevant bonding techniques. One possible classification is illustrated in Figure 2.6. In general, we can distinguish the bonding techniques without intermediate layers, the bonding techniques with intermediate layers and the hybrid bonding techniques which utilize the combination of two bonding techniques of which one is without intermediate layers, and the other is with such a layer.

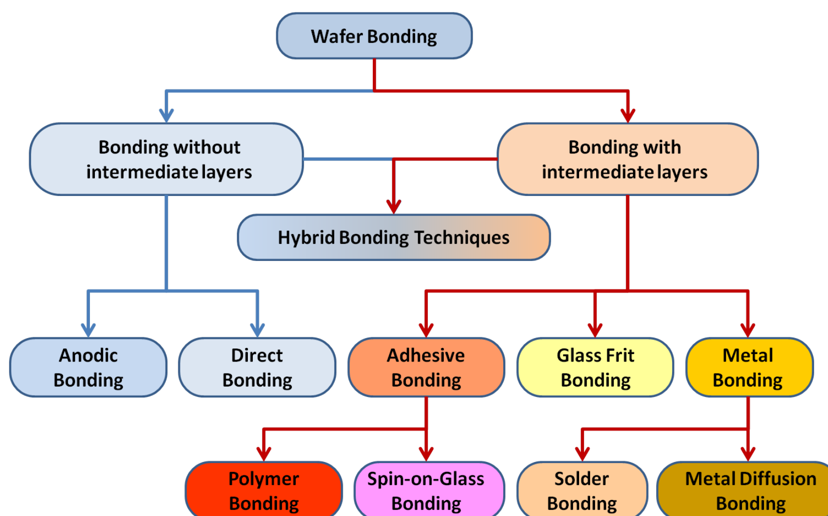


Figure 2.6: Classification of the bonding techniques

In the case of the bonding techniques without the intermediate layer, two wafers or surfaces are bonded together directly, without any additional material (acting as a glue) placed between the bonding surfaces. In the bonding techniques with the intermediate layer, some other material is placed between the

wafers in order to provide a bond between them. Usually, at the moment of bonding, this intermediate layer is in a liquid form; it comes into intimate contact with the bonding surfaces and fills the voids between them. As the bonding process continues, this layer undergoes a physical change and solidifies creating a permanent bond between the wafers.

Two bonding techniques that don't require an intermediate layer will be first presented: anodic wafer bonding and direct (or molecular) bonding. Following this, an overview will be given of the bonding techniques that employ an intermediate layer.

2.4.1 Anodic Wafer Bonding

Anodic bonding, also known as "field-assisted sealing" or "electro-static bonding" and first described in 1968 [31], is a bonding technique that is used for bonding a semiconductor wafer to an alkali element-containing glass wafer. In theory, a number of materials can be employed for this bonding, but in practice, by far the most common bonding pair combination is silicon and Pyrex glass. Si/Pyrex glass anodic bonding is a well-established industrial technique, specifically used for MEMS packaging applications [32].

In principle, anodic bonding is an electrochemical process based on polarization of alkali-containing glasses. The wafers are brought into contact and heated to 300 – 450 °C, so that glass becomes sufficiently conductive. Still, these temperatures are well below glass transition temperature (~ 600 °C), so there are no macroscopic deformations of the glass during bonding. A high DC voltage (400 - 1000 V) is applied across the wafer stack, such that the glass is on a negative potential with respect to the silicon wafer, as indicated in Figure 2.7. At such high temperature and DC electric field, alkali cations (for most of the glasses, these are primarily Na^+ and to small extent K^+) are displaced towards the cathode, leaving an cation-depleted region behind. It is important that the anode acts as a 'blocking' electrode, i.e. that it doesn't provide nor accept mobile ions from the glass. Unlike the anode, the cathode must be a non-blocking electrode allowing alkali ions to leave the glass.

The voltage drop is mostly over the cation-depleted layer (due to the fact that the glass becomes conductive), and the electric field in this region is in the order of several MV/cm. Negatively-charged oxygen ions in this layer attract the silicon wafer, eventually creating silicon-oxygen bonds at the interface.

The bonding temperature and the applied voltage are correlated in such way that at a higher temperature, a lower DC voltage is required. During the bonding, the current through the cathode is monitored as well as the total charge which is used as an indicator of the bonding process - once a certain amount of charge is reached, the bonding is considered to be completed. Re-

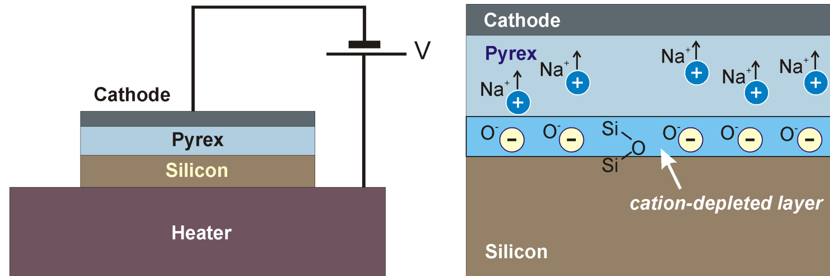


Figure 2.7: Anodic wafer bonding: mechanism of silicon-glass bonding at the wafer interface.

portedly, better bonding results are obtained with hydrophilic silicon surfaces than hydrophobic ones, and also a p-type silicon provides better bonding than an n-type [32]. The two most often used types of glass in anodic bonding are Pyrex (Corning 7740) and Schott Borofloat. Both glass types have sufficiently high sodium content and their coefficients of thermal expansions (CTE) are very close to that of silicon. In theory, anodic bonding of two silicon wafers is possible, but only using an adequate intermediate glass layer which is deposited (by sputtering or evaporation) to one of the silicon wafers prior to bonding. In this case, the bonding process is virtually the same, with the negative voltage applied to the glass-coated wafer.

The main advantages of this bonding technique lay in the fact that it can provide a hermetic seal and that it is more tolerant to surface roughness and contamination than direct, molecular bonding. On the other hand, the bonding process requires relatively high temperatures (> 300 °C) and high DC voltages. This is a serious drawback if the silicon wafer already contains fabricated microelectronic devices which are sensitive to high electric fields or if it contains components (or solder bumps) which can't tolerate such high bonding temperatures. In conclusion, this bonding technique is not very interesting for photonic integration where we usually need to bring III-V materials onto patterned SOI photonic wafers.

2.4.2 Direct Wafer Bonding

Direct semiconductor wafer bonding or 'molecular bonding', as it is also known, is a bonding technique in which two mirror-polish semiconductor wafers, with flat, smooth and ultimately clean surfaces are joined and bonded together without any intermediate layer (acting as a glue) or application of external mechanical forces or electrical field. The initial bonding step usually takes place at room temperature, but the subsequent annealing is performed at much higher tem-

peratures. Direct bonding of silicon wafers was first reported in mid-1980's [33] when two oxidized silicon wafer surfaces were bonded to eventually form a silicon-on-insulator (SOI) substrate.

Today, direct semiconductor wafer bonding, sometimes also called "fusion bonding" is an important technological process used in mass production of SOI substrates (used both in electronics and photonics), and 3-D microelectromechanical systems (MEMS).

The physics of direct wafer bonding is based on the forces that are acting at the interface between two flat wafer surfaces which are brought into an intimate contact (~ 1 nm). The most important forces involved in the initial attraction of the bonding wafers are: capillary forces, electrostatic forces (due to charged particles or contact potential between surfaces with different work functions), Van der Waals forces (between atoms and molecules acting as electrical dipoles) and hydrogen bonds between hydroxyl groups (-OH) present at both surfaces [32]. The total adhesion energy W of two planar, parallel surfaces, separated by a distance d is given by [34]:

$$W = \frac{A_{123}}{12\pi d_0^2}\left(1 - \frac{d_0^2}{d^2}\right) \tag{2.1}$$

where d_0 is interatomic distance and A_{123} is the Hamaker constant for surface 1 interacting with surface 2 via medium 3. Usually, this constant is on the order of 10^{20} J and, for example, in the case of two amorphous silica surfaces with water molecules in between, its value was measured as $A_{123} = 1.69 \times 10^{20}$ J at 20 °C [35]. Obviously, when the separation between the wafers reaches interatomic distance $d = d_0$, the surfaces are in intimate contact and the adhesion energy reaches its lowest value - zero, providing a stable state when the surfaces are bonded.

In practice, the bonding surfaces don't spontaneously reach this state, as the surface roughness, wafer warp and waviness and local presence of particles prevent such an intimate contact between them. Usually, during the direct wafer bonding, after the wafers are placed one on top of the other (at room temperature), a pressure is applied in the centre (or at the side) of the wafer to bring the surfaces there into an intimate contact and achieve local bonding. Once the bonding is achieved at this point, due to attractive forces between the wafers acting locally near the bonded centre point, the wafer surfaces get into an intimate contact and the bond wave spreads out from the centre towards the wafers periphery. This propagation of the bond wave, which takes place within just a few seconds, is illustrated in the Figure 2.8.

Surface chemistry is essential in direct wafer bonding and presence of various chemical groups affects the bonding. With respect to this, there are two

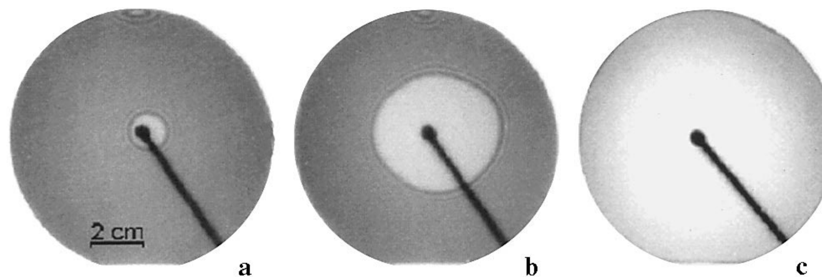


Figure 2.8: Direct wafer bonding: infrared microscope images of the bond wave propagation [36]. (a) Formation of a locally bonded area at the point of external pressure. Propagation of the bond wave: (b) after 3 seconds and (c) after 5 seconds.

direct wafer bonding techniques: *hydrophilic* and *hydrophobic* bonding.

Hydrophilic direct wafer bonding is the most commonly used technique. In this case, a layer of silicon oxide is present on both bonding surfaces (which can also be a native oxide present on the silicon wafer surface). At room temperature, water molecules adhere to this surface, bonding via hydrogen bonds to Si-OH groups present at the silica surface. These hydrogen bonds are relatively weak and in order to achieve stable, permanent bonds, formation of covalent bonds between the silicon atoms at the bonding interface is needed. Therefore, the initial bonding step is followed by annealing during which the adsorbed water is removed and strong siloxane (Si-O-Si) covalent bonds are created. In a typical process, a complete bonding via oxide is achieved for annealing temperatures of > 800 °C. This is schematically illustrated in Figure 2.9a.

Hydrophobic direct wafer bonding is performed between silicon surfaces on which the oxide was removed (usually, by HF treatment). Unlike hydrophilic surfaces, characterized by presence of silanol groups (-Si-OH), hydrophobic silicon surfaces are in general characterized by presence of Si-H groups and Si-F groups, which are formed due to exposure to HF. In this case, the initial bonding between the wafers is also achieved at the room temperature due to hydrogen bonds between Si-H groups at the bonding interface, as illustrated in Figure 2.9b. After this initial bonding step, similar to hydrophilic bonding, a high-temperature annealing step is performed (typically at > 800 °C). This eventually, leads to formation of covalent bonds between silicon atoms from the different wafers.

Direct wafer bonding has seen significant increase in applications during the last two decades. Probably, the most important application of this bonding technique is fabrication of SOI wafers by means of the SmartCut® proce-

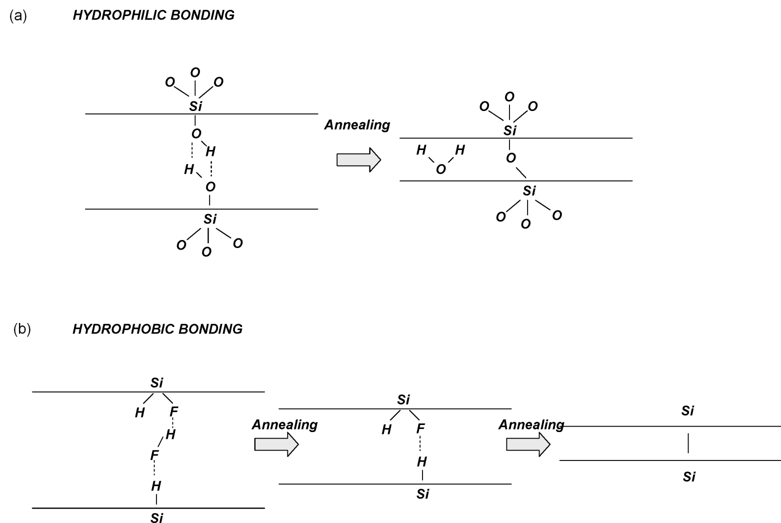


Figure 2.9: Mechanisms of direct wafer bonding in the case of: (a) hydrophilic bonding and (b) hydrophobic bonding. Reproduced from [37].

dure [38]. In this process, illustrated in Figure 2.10, a wafer is exposed to high-dose (5×10^{16} cm^{-2}) hydrogen ion implantation (or sometimes He ions) which creates micro-defects within a wafer, near the implantation depth. This implantation depth can be set at a desired value, by controlling the ion energy. After the implantation, a direct wafer bonding is used to bond this wafer to a host substrate wafer. Following this, the bonded wafers are heated to 400 – 500 °C, causing release of hydrogen into these induced micro-cavities, build-up of the gas pressure inside them and eventual cracking of the wafer at this plane. The split wafer with the buried oxide layer (where the initial direct bonding interface was located) is polished using chemical-mechanical polishing (CMP) and etching techniques to obtain a flat, high-quality SOI wafer. As another advantage of this process, the remaining Si wafer is also polished and used as a host wafer for subsequent bondings. Both 200 mm and 300 mm diameter SOI wafers are commercially available. Thickness of the buried oxide (BOX) layer may vary depending on the purpose of the SOI wafer. In the photonic SOI platform this thickness is usually 1 or 2 μm, while in some state-of-the-art electrical applications ultra-thin buried oxide (UT-BOX) layers between 20 to 150 nm are used [39].

The requirement for a high temperature annealing step (> 800 °C) is a significant drawback in employing a typical direct bonding process for wafer-level integration, as fully processed semiconductor wafers require temperatures be-

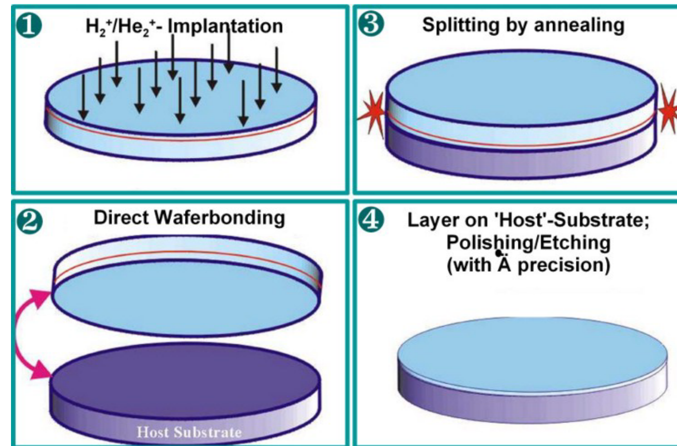


Figure 2.10: Process flow of the Smart-Cut® process: 1) Implantation of hydrogen (or He) ions below the wafer surface; 2) Direct wafer bonding to the host wafer; 3) Annealing of the implanted wafer leading to splitting parallel to the wafer surface; 4) Planarizing of the split wafer surface by polishing or etching. [40].

low 450 °C. Also, this creates problems in the case of direct bonding of different materials (e.g. heterogeneous integration of a III-V material on the SOI platform), due to thermal expansion coefficient (CTE) mismatch. Strain induced due to such temperature excursion and CTE mismatch would eventually lead to wafer cracking.

To cope with this problem, a number of low temperature wafer-bonding techniques have been developed – especially for hydrophilic surfaces. The main idea in these techniques is to modify the wafer surface in order to make chemical bonds stable at lower temperatures. Plasma treatment of the wafer surfaces prior to bonding is a popular way to achieve this. Treatments with oxygen plasma are the most often used for this purpose, but also, other non-oxygen (Ar, N_2, Cl_2) plasma treatments were reported [41].

2.4.2.1 Plasma-activated direct wafer bonding

Plasma-activated direct wafer bonding techniques are used mostly for bonding hydrophilic wafer surfaces. Several effects of plasma treatment of the silicon wafers are thought to be the reasons for the surface activation [42]:

- removal of contaminants on the wafer surface (and formation of dangling bonds);
- increase in the number of silanol (Si-OH) groups, which are pre-cursors

for subsequent formation of strong siloxane covalent bonds;

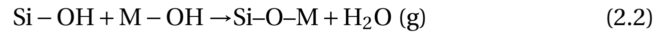
- increasing oxide thickness, combined with the increase in porosity of the amorphous layer at the bonding interface which leads to increased diffusion and faster evacuation of water and other gasses trapped at the interface;

- accelerated transformation of silanol to siloxane bonds.

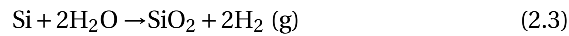
Plasma treatments are usually performed under a very low-pressure, using standard reactive ion etching (RIE) or inductively-coupled plasma reactive ion etching (ICP-RIE) processes, though atmospheric plasma-assisted bonding (PAB) can also be performed [32].

PAB direct wafer bonding techniques found commercial application in fabrication of pressure sensors, image sensors, MEMS packaging, etc. According to studies by Sanz-Velasco *et al.* [43], oxygen plasma treatment in ICP-RIE can be used for CMOS applications.

From the perspective of heterogeneous integration for active photonic devices, bonding of III-V materials on a SOI wafer is the most important targeted application for plasma-activated direct bonding. The process of forming strong covalent bonds at the interface of such wafers is described in the following equations [44]:



$$\mathrm{Si-OH + M-OH \rightarrow Si–O–M + H_2O\ (g)} \tag{2.2}$$



$$\mathrm{Si + 2H_2O \rightarrow SiO_2 + 2H_2\ (g)} \tag{2.3}$$

where M designates an atom with relatively high electronegativity (such as group III or group V elements). Similar to silicon-silicon wafer bonding, water and hydrogen gases formed during the annealing step need to be evacuated and not trapped between the bonding surfaces.

In a process, reported by Liang *et al.* [45], an oxygen plasma treatment is used to assist direct bonding between a layer of thermal SiO_2 grown on a SOI wafer, and a plasma-enhanced chemical vapor deposited (PECVD) SiO_2 layer, on the surface of a InP wafer. PECVD of SiO_2 on a InP wafer was used because the InP native oxide is not of sufficiently high quality for direct bonding [46]. In this particular case, the SiO_2 layers on both wafers were 30 nm thick, resulting in the 60 nm thick SiO_2 layer at the bonding interface, which is sufficiently thin for evanescent-coupling photonic devices [45]. Plasma-activation of the SiO_2 surfaces of both the SOI and InP wafers was performed using an RIE process with

an oxygen plasma at relatively low power (39 W), for 45 s, at 15 mTorr pressure. Annealing was carried out at 300 °C with application of 1.5 MPa pressure. This bonding procedure, developed by researchers from the University of California - Santa Barbara (UCSB) was used for fabrication of hybrid III-V/Si lasers [47–53], photodetectors [54] and hybrid silicon modulators [55].

Even before this development at UCSB, back in 2005, researchers from CEA-LETI in France demonstrated bonding of InP dies on a CMOS processed silicon wafer, using a 1 μm-thick layer of thermally grown SiO_2 on a silicon wafer and a 10-15 nm thick layer of SiO_2, deposited on a III-V epitaxial structure [56]. Plasma-activated, low temperature bonding of different materials for photonic applications has been an area of intensive research, and other authors have also reported devices fabricated using this type of bonding [57], usually with annealing temperatures of 300 °C and in some cases as low as 200 °C [56, 58] or even 150 °C [59].

In general, plasma-activated direct bonding is a CMOS-compatible technology suitable for wafer bonding and offering the advantages of standard direct bonding techniques, with the benefit of significantly reduced annealing temperatures. However, direct bonding, whether it is plasma-activated or not, also has some serious drawbacks that present a challenge in using these technologies in an industrial scale heterogeneous integration for photonic applications. These bonding technologies require ultimately flat, clean, contamination-free bonding surfaces. This implies extensive cleaning procedures and surface preparations. Also, increased surface roughness or particle contamination can create large unbonded areas and significantly reduce bond strength or lead to a complete bonding failure. An incompressible particle of radius r_p, located at the interface between two wafers of identical thickness t, produces an unbonded area of radius R [36]:

$$R = \left(\frac{2}{3}\frac{E' t^3}{\gamma}\right)^{\frac{1}{4}} \sqrt{r_p} \tag{2.4}$$

where γ is the bonding energy and E' is the biaxial Young's modulus defined as $E' = E/(1-\nu^2)$, where E is Young's modulus and ν is Poisson's ratio for the wafer material. In the case of standard 200 mm silicon wafers, with 725 μm thickness, this bonding defect radius R can be 10^4 times larger than the radius of the contaminating particle.

This example illustrate how critical the surface cleanliness is in the case of direct bonding. Also, outgassing of water and hydrogen during the bonding needs to be addressed. In case of bonding III-V material on an SOI wafer, one effective method for solving this problem is fabrication of vertical outgassing

channels (VOCs) on the SOI wafer prior to bonding [60]. This array of holes, few micrometers in diameter, connects the bonding surface to the buried oxide (BOX), allowing flow of the gaseous byproducts from the bonding surface to the porous BOX layer, where they easily diffuse and are eventually absorbed.

2.4.3 Adhesive Wafer Bonding

Adhesive wafer bonding refers to a variety of bonding techniques in which an intermediate layer of a specific adhesive material is used to establish a bond between two wafers. The basic principle in this type of bonding is that an adhesive (or, in less technical terms, a glue) fills the voids at the bonding interface between two wafers and establishes an intimate contact on a molecular level with both bonding surfaces - in a process called wetting. In order to have a good wetting of the surface, the surface energy of the wafers must be higher than the surface energy of an adhesive. In addition to this, molecules of an adhesive material establish chemical bonds with the molecules at the wafer surface. To achieve such a good contact with the bonding wafers, an adhesive is usually applied to one or both wafer surfaces in a liquid or viscoelastic state, which allows flow of the adhesive molecules along the bonding interface. To establish a permanent bond between the wafers, following this initial step, the adhesive undergoes a chemical transformation in which its molecules cross-link among each other, leading to solidification of the adhesive, which is known as *curing*.

Adhesive wafer bonding techniques (sometimes called *glue bonding*) in general offer several comparative advantages over direct wafer bonding, which makes them particularly attractive for some applications, where the strict requirements of the direct molecular bonding are difficult to meet. The most important advantages are:

- **tolerance to surface roughness, defects and rich topography:** unlike direct bonding which requires flat, parallel bonding surfaces, adhesive bonding is much more tolerant to surface topography and roughness; the adhesive usually easily fills all the voids and gaps at the bonding interface, making the bonding of patterned wafers (like SOI photonic wafers) easier;
- **tolerance to small particle contamination:** as the adhesive fills the space between the two bonding surfaces, particles that remain at the bonding interface can be enveloped by the adhesive and incorporated in the bonding layer after curing, provided that the particle diameter is smaller than the bonding layer thickness;
- **low processing temperature** compared to standard molecular bonding (usually, < 300 °C);

- **relatively simple process flow**, with less stringent surface cleaning requirements compared to direct (fusion) bonding;
- **ability to join practically any type of wafer material**, provided the good wetting of the wafer surfaces and that stress due to CTE mismatch of the wafer materials is not too large (which is usually the case due to low bonding temperatures).

On the other hand, adhesive bonding has some disadvantages as well. Some adhesives have a relatively limited temperature range within which they can be employed (like thermoplastic polymers). Typically, the adhesives used for the bonding have a relatively low thermal conductivity, which can significantly increase thermal impedance of the devices fabricated using adhesive bonding techniques. Shrinkage upon curing or outgassing of the curing byproducts, which occurs in case of some adhesives, is also a serious drawback. Providing a hermetic sealing can also be problematic with many adhesives.

Various materials can be used as adhesives, but by far the most commonly used are polymers. Therefore, polymer wafer bonding techniques will be discussed in more detail.

2.4.3.1 Polymer Wafer Bonding

Polymers encompass a large variety of compounds featuring very large molecules (macromolecules) made of a multitude of identical, single-type molecules, linked together to form long molecular chains that eventually give certain physical properties to a given polymer. The process of chemical transformation in which these single-type molecules (monomers), used as individual building-blocks, are connected together to form such a large molecular chain is called polymerization. The basic idea of polymer adhesive bonding is to apply a polymer (or a solution containing monomers) in a liquid or viscoelastic form onto a wafer surface and bring the wafers into a contact. After the wetting of the bonding surfaces is completed, polymer hardening (i.e. solidification) is initiated, eventually leading to formation of a solid polymer bonding layer between the two wafers.

In a broad sense, polymers can be classified into the following types:

1. **thermoplastic polymers** which melt at an elevated temperature and solidify upon cooling; in these polymers, this transformation is reversible and they can be re-melted again (and consequently, re-shaped) if they are heated back to the melting temperature;
2. **thermosetting polymers** which polymerize at elevated temperatures, going through an irreversible transformation, after which they can't be re-melted or re-shaped again;

3. **elastomers** (often referred to as rubbers) which can undergo large physical deformations (stretching 5 to 10 times longer than in a non-deformed state) and recover back to their original state;

4. **hybrid polymers** which are mixtures of polymers from the three previous types, forming new materials with distinctive properties, different from the original polymers.

In principle, polymers from all of these types can be used in adhesive wafer bonding. Transformation of the polymers from a liquid or viscoelastic phase into a solid phase is critical for the adhesive bonding. This hardening can occur due to:

1. **evaporation of the solvent** in which the polymer is dissolved; polymer adhesives based on this principle are called *physical drying polymer adhesives*;

2. **phase change**, in the case of thermoplastic polymers which melt when heated and solidify when cooled below their melting point; such polymer adhesives are called *hot-melts*;

3. **polymerization** (i.e. curing) of the polymer precursors, which can be initiated by different mechanisms, such as:

   - mixing of two or more components (e.g. in two-component epoxies)
   - heating (e.g. in thermosetting polymers and epoxies)
   - light illumination (e.g. ultraviolet (UV) light in UV-curing polymers)
   - presence of moisture (e.g. in some polyurethanes)
   - absence of oxygen (e.g. in anaerobic adhesives).

At room temperature, polymers are in general hard and brittle (so called, glassy-state), but at higher temperatures, they transform to a rubber-like state. The temperature at which this occurs is called the transition temperature (T_g). High bond strength is usually retained as long as the adhesive polymer layer is in a glassy-state. Therefore, application of thermoplastic polymers is limited not only by their melting temperature (T_M), but also by their glass-transition temperature, which is, of course, lower than T_M. In practice, a useful temperature range for thermoplastic polymers is up to 200 – 300 °C. They have good peel resistance, but poor creep resistance, meaning that under long-term pressure they tend to deform. Thermosetting polymers can operate up to 300 – 450 °C and they are more rigid than thermoplastics, offering generally better chemical resistance. Typically, they exhibit good creep resistance, but only fair peeling

resistance. Elastomers can operate over a broad range of temperatures, usually up to about 260 °C. They have high peel strength, low overall strength and high flexibility.

Not all of the polymers are suitable for semiconductor wafer bonding. As the semiconductor wafers are typically neither porous nor permeable to liquids and gases, the use of polymers that create gaseous byproducts during curing is not suitable, as these may get trapped at the bonding interface creating large unbonded areas. Polymers that harden due to solvent evaporation are also not suitable for adhesive wafer bonding for the same reason. On the other hand, polymers are typically several orders of magnitude more permeable to gasses and moisture than glass and metals. Molecules of water are of sufficiently small dimensions (slightly more than 0.1 nm) to allow them to diffuse into a free space between the molecular chains of polymers. This leads to one of the general shortcomings of the adhesive polymer bonding - it cannot provide hermetically sealed bonds or cavities.

The most important parameters in adhesive polymer bonding are: choice of the polymer used as the adhesive, bonding pressure, bonding temperature, temperature ramp profile and chamber pressure.

The bonding pressure helps in bringing the wafers and adhesive bonding layer into an intimate contact, and compensate for the wafer bow and topography which can sometimes prevent the adhesive filling all the voids and gaps between the wafers. Usually, the bonding pressure is important in preventing void formations, provided that there is no outgassing and that a sufficiently thick bonding layer is applied. In order to equalize the bonding pressure, deformable sheets (e.g. graphite sheets) can be inserted between the rigid bond chucks and the wafer stack. Pressure distribution between the bonding chucks can be verified using pressure sensitive papers.

The bonding temperature and the temperature profile are also very important and need to be optimized for a particular polymer used. For thermosetting polymers, the final curing temperature and the curing time must provide sufficient cross-linking, i.e. sufficient degree of polymerization. Also, after the application of the bonding pressure, polymer re-flow needs to be allowed at a sufficiently low temperature, such that the cross-linking still doesn't occur. On the other hand, in the case of thermoplastic polymers, the bonding temperature needs to be sufficiently high to allow the polymer reflow and redistribution between the wafers. Generally, very fast temperature ramps should be avoided, allowing enough time to reach a uniform temperature distribution across the bonding surface. Slow temperature changes are also very important in the case of bonding two wafers with very different CTEs in order to minimize stress.

Chamber pressure during the bonding should usually be held in vacuum, in order to prevent trapping any gas at the bonding interface. In many cases,

though, it is possible to pump out the gasses trapped at the bonding interface, before the polymer solidifies. Consequently, vacuum can be established after making the contact between the wafers, but before curing of the polymer starts.

Choice of the polymer that is going to be used for bonding is critical and depends on the specific application and requirements. Polymers which are especially popular for adhesive wafer bonding applications are: divinylsiloxane-bis-benzocyclobutene (DVS-BCB) which is a thermosetting, thermally-cured polymer, SU8 (a UV-cured polymer) and thermoplastic polymers like polymethyl-methacrylate (PMMA) and polyimides (PI). Thermosetting polymers are usually supplied in the form of a liquid polymer precursor which is initially cross-linked to a certain degree and optionally dissolved in a solvent.

For heterogeneous integration in photonic applications, a suitable adhesive polymer would have to provide a sufficiently low bonding temperature (due to the CTE mismatch between III-V materials and the SOI wafer), but also a sufficiently high thermal budget and resistance to aggressive chemicals in order to allow the bonded III-V die to survive the complete device fabrication process after the bonding. These requirements practically exclude the use of thermoplastic polymers which is not compatible with some high temperature steps in the post-bonding device fabrication (e.g. PECVD deposition of a SiO_2 layer at around 300 °C or fast-alloying of metal contacts at ~ 420 °C).

DVS-BCB as a polymer for adhesive bonding

Divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or just BCB, for short) is one of the most popular polymer materials used for adhesive wafer bonding. It was developed in the late 1980's by Dow Chemical Company as a low dielectric constant (low-k) polymer intended to replace silica as a dielectric in on-chip interconnects [61]. Today, under the commercial name Cyclotene®, it is a well-known material with a variety of applications in microelectronic packaging and interconnects applications.

Chemically, DVS-BCB is a monomer molecule that polymerizes to create a low-k dielectric material with some advantageous properties. Its full IUPAC[1] name is 1,3-divinyl-1,1,3,3-tetramethyldisyloxane-bisbenzocyclobutene and its chemical structure, illustrated in Figure 2.11, shows that this is a symmetrical molecule with a siloxane backbone, terminated at both ends with benzocyclobutene rings linked to the siloxane core via vinyl groups. During the process of polymerization, illustrated in Figure 2.12, benzocyclobutene rings open due to an increased temperature to form very reactive o-quinodimethane groups [61]. This group reacts with the vinyl group of an adjacent monomer molecule in a so called Diels-Alder reaction. This reaction can continue, eventually forming

[1] IUPAC – International Union of Pure and Applied Chemistry

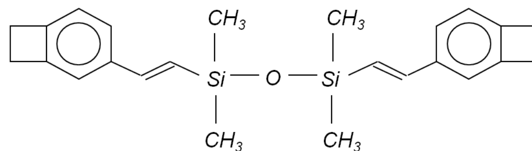


Figure 2.11: Structure of a DVS-BCB molecule: two vinyl groups connected via a siloxane core and terminated with benzocyclobutene rings.

a fully-cured polymer, featuring a three-dimensional, highly-branched molecular network structure. Crucial characteristic of this polymerization chemical reaction is that there are no byproducts that would outgass during the curing, which could result in formation of gas-filled voids at the bonding interface, weakening the overall bonding strength. For commercial applications, the monomer is usually B-staged, i.e. only partially-cured, to form an oligomer that is dissolved in mesitylene. These oligomer mesitylene solutions are commercially available under the name Cyclotene® and are used as polymer precursors. Solutions with various oligomer content (i.e. resin content) are available, like Cyclotene 3022-35 (with a 35% resin content), or Cyclotene 3022-46 (with a 46% resin content).

To improve adhesion of the polymer precursor solutions to wafer surfaces, various adhesion promoter solutions were developed. These promoters are applied to the wafer surface before spin-coating the polymer precursor solution. Adhesion promoter molecules intended for silicon wafers have the general chemical formula: G-Si$(OR)_3$ [62], where R can be hydrogen, methyl, ethyl or other more complex groups. The resulting silanol group reacts with free hydroxyl groups on an oxidized silicon wafer surface. The G-group consists of a moiety which interacts with the polymer [37]. In this way, an adhesion promoter creates a bridge between the silicon wafer and the DVS-BCB resin.

In a typical polymer wafer bonding process, the polymer precursor solutions are applied by spin-coating to one of the wafers, after which they are soft-baked in order to let mesitylene solvent to evaporate. After the solvent evaporation is completed, two wafers are brought into contact, exposed to pressure and thermally cured. The dynamics of the curing process highly depends on the curing temperature and consequently, degree of polymerization depends both on the temperature and the curing time at that temperature. This dependence is illustrated in the time-temperature-transformation isothermal cure diagram, shown in Figure 2.13. As expected, the higher the temperature is, the faster polymerization occurs. On the other hand, at sufficiently low temperatures (< 150 °C), the polymerization rate is so slow, that precursors can stay for several days without transforming into a solid phase. In practical applications, the most common

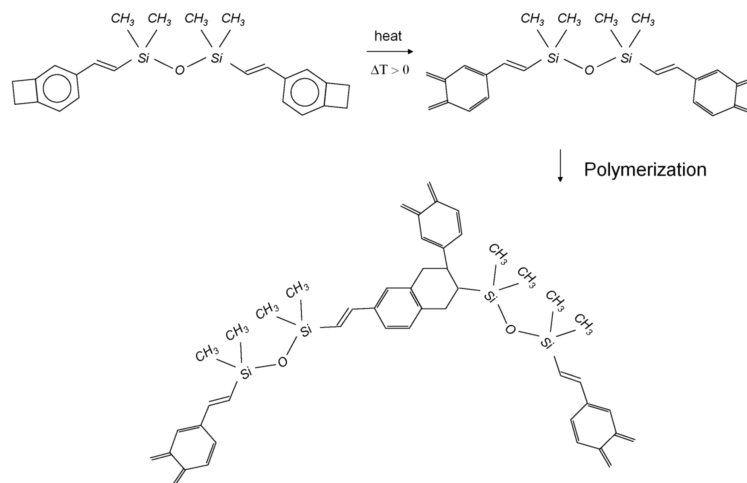


Figure 2.12: Polymerization reaction of DVS-BCB. At elevated temperatures, cyclobutene rings open and react with vinyl groups of adjacent molecules, without any out-gassing byproduct. Reproduced from [37].

curing temperature is 250 °C. Exposed to sufficiently high curing temperature, DVS-BCB transforms from a liquid phase into a sol/gel rubber (in a gelation process), finally transforming into a glass phase, in a vitrification process when the glass transition temperature T_g (which increases with the increasing degree of polymerization), reaches the curing temperature.

A typical curing temperature profile, illustrated in Figure 2.14, comprises two temperature ramps and two temperature levels (or plateau's). Initially, a wafer with the spin-coated DVS-BCB on top of it, is heated to 150 °C (the first plateau) with a moderately fast temperature ramp (5 - 30 min/°C). Baking at this temperature allows all the remnants of the solvent to evaporate, which is important in the bonding process as no outgassing should occur once the wafers are brought into contact. After around 20 minutes at this temperature, the polymer is heated to 250 °C, with a slow 1.6 min/°C ramp. Eventually, the curing is performed at the second temperature plateau of 250 °C for 60 minutes. To avoid oxidation of DVS-BCB, which would lead to increased brittleness and cracking, curing is performed in a virtually oxygen-free atmosphere (< 100 ppm O_2) [61], which is practically achieved via nitrogen purge of the processing chamber. After curing, the wafers are slowly cooled down to room temperature.

For many practical applications it is important to perform patterning of fully-cured DVS-BCB films (or BCB resins). Dow Company has developed two commercial product series: Cyclotene 3022, also known as dry-etch BCB resins

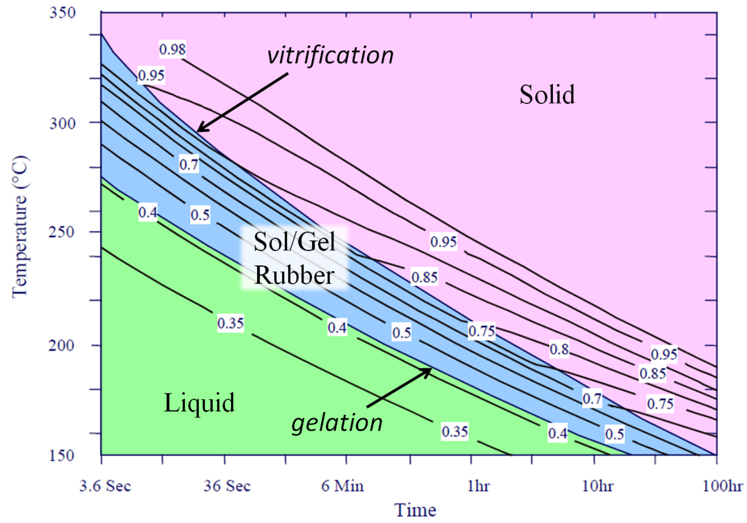


Figure 2.13: Degree of DVS-BCB polymerization and phase diagram, depending on curing time and temperature. Adapted from [63].

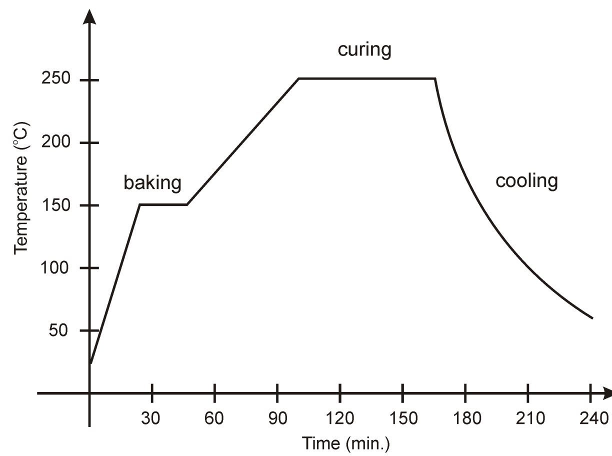


Figure 2.14: Temperature profile of a typical DVS-BCB curing process.

and Cyclotene 4000 series which represents a series of photo-sensitive BCB resins. In the case of dry-etch resins, patterning is performed via a combination of making a soft- or hard-mask on top of the BCB resin and a subsequent plasma etching process in an atmosphere of oxygen and fluorine-containing gas. Most usually, these are sulfur hexafluoride (SF_6), tetrafluoromethane (CF_4) and fluoroform (CHF_3). Photosensitive BCB resins act as negative photoresists, allowing the use of photolithography for patterning the films before curing. In a standard Cyclotene 4000 series processing sequence, after spin-coating a precursor solution and soft-baking for solvent evaporation, a photolithography is performed (using 365 nm wavelength, I-line UV lamp) and the BCB-resin is developed, removing the film from the unexposed areas. After developing, the remaining, patterned BCB film is baked (to stabilize the sidewalls at the etched openings) and finally cured [61].

The final thickness of the fully-cured BCB film depends on the initial content of a BCB oligomer in the used polymer precursor and the spin-coating revolution speed which was used for its application on a wafer. Typical cured film thicknesses for Cyclotene 3022 series resins are presented in Table 2.1. It is worth noticing that the minimum film thickness is around 1 μm, which is an order of magnitude thicker than distances that are required for efficient evanescent coupling in III-V/hybrid lasers [50, 64]

Spin Speed (RPM)	CYCLOTENE 3022-35	CYCLOTENE 3022-46	CYCLOTENE 3022-57	CYCLOTENE 3022-63
1000	2.26	5.46	13.8	26.2
1500	1.84	4.39	10.7	19.9
2000	1.59	3.76	9.04	16.5
2500	1.43	3.35	7.97	14.4
3000	1.30	3.05	7.21	12.9
3500	1.21	2.82	6.65	11.8
4000	1.13	2.63	6.20	10.9
4500	1.07	2.48	5.84	10.2
5000	1.01	2.35	5.55	9.64

Table 2.1: Thickness of Cyclotene® 3000 series films after curing (in μm) versus spin speed [63]

Electrical, mechanical and thermal properties of Cyclotene 3000 series resins are summarized in Table 2.2. The important advantages of DVS-BCB are: (i) low optical loss at telecommunication wavelengths around 1310 nm and 1550 nm, (ii) sufficiently low shrinkage upon curing, (iii) high glass transition temperature (T_g) which allows relatively large post-bonding thermal budget and (iv) very good planarization properties. On the other hand, the very low

thermal conductivity of around 0.3 W/mK and lacking the ability to provide hermetic sealing, are regarded as major drawbacks.

Property	**Measured Value**
Refractive index	1.543 at 1.55 μm
Optical loss	< 0.1 dB/cm at 1.55 μm
Dielectric constant	2.65 - 2.50 at 1-20 GHz
Dissipation Factor	0.0008 - 0.002 at 1-20 GHz
Breakdown Voltage	5.3×10^6 V/cm
Leakage Current	6.8×10^{-10} A/cm^2 at 1.0 MV/cm^2
Volume Resistivity	1×10^{19} Ω-cm
Thermal Conductivity	0.29 W/m·K at 24 °C
CTE	42 ppm/°C at RT
Tensile Strength	87 ± 7 MPa
Tensile Modulus	2.9 ± 0.2 GPa
Elongation	8 ± 2.5 %
Poisson's Ratio	0.34
Residual Stress	28 ± 2 MPa at RT
T_g	> 350 °C
Moisture Absorption	< 0.2%

Table 2.2: Thermal, electrical and mechanical properties of CYCLOTENE® 3000 series resins [44, 63].

2.4.3.2 Spin-on-Glass Wafer Bonding

Beside polymers, other materials can be used for adhesive wafer bonding and spin-on-glass (SOG) materials are one of the commercially available adhesives that can be used for this purpose. These materials were originally developed and used as interlevel dielectrics for microelectronic applications. Typical spin-on-glass materials are silicates that after curing form a molecular network, based on strong silicon-oxygen bonds (Si-O). SOG materials are deposited on a wafer using spin coating or spray coating, followed by drying (solvent removal) and finally, a thermal curing step [32]. In general, spin-coating provides better layer uniformity than spray-coating. During the drying or baking step, the applied film loses more than 50% of weight and volume due to solvent evaporation [65]. Drying temperatures may vary, with some authors reporting temperatures from 180 °C [32] to 250 °C [65]. After drying, SOG converts to a microporous oxide and has the form of a tacky gel [37]. During a thermal curing, this gel first transforms into a hard gel and eventually creates a silicate SOG with a molecular network based on silicon-oxygen bonds, as illustrated in

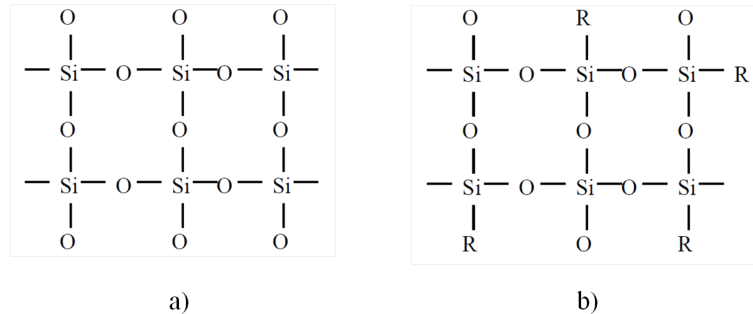


Figure 2.15: Molecular structure of: a) silicate spin-on-glass; b) siloxane spin-on-glass

Figure 2.15a. Typical curing temperatures are around 800 °C to 900 °C.

A fully cured film, contains -OH moieties, but exhibits a large shrinkage upon curing, causing a high tensile stress (~ 500 MPa) which may lead to film cracking problems [65]. Planarization properties of such fully-cured films are also not very good and normally, multiple spin-coating processes are required to achieve a good planarity. If the curing temperature is lowered to 450 °C, which is required for CMOS-compatible processes, such a cured SOG film will still contain a significant amount of silanol groups (Si-OH) and absorbed water.

Silicate-based SOG can be doped with phosphorus, which modifies the Si-O network, reducing the film stress to ~ 200 MPa [65] and helping alleviate the cracking problem [37]. Another way to lower the film stress is incorporation of organic components (usually methyl or ethyl groups) into an SOG structure. Structure of such a organosilicon compound SOG (also called siloxane SOG) is illustrated in Figure 2.15b. Cured films based on these compounds are thicker and have better planarization properties. To avoid thermal decomposition of the organic groups, curing temperatures must be kept bellow 400 °C [65]. Increase in the organic content further reduces the film stress and improves the crack resistance and planarity, but it was found that the mechanical strength of these materials is low [65].

Use of SOG was reported for wafer bonding processes [46]. However, planarization properties of spin-on glass (SOG) films are not always sufficiently good for wafer bonding, even when applied on flat surfaces. In some tests, waviness of a SOG layer, spin-coated on a flat GaAs wafer and dried at 180 °C was quite high: thickness variation of up to 80 nm was found in a SOG layer of 500 nm average thickness [32].

The need for a low-temperature wafer bonding process (< 400 °C), which doesn't allow removal of siloxane bonds and adsorbed water in SOG molecular network makes application of SOG materials challenging, especially when very

thin bonding layers (~ 100 nm) are required on a patterned SOI wafer surface, as in the case of evanescent-coupling hybrid photonic devices.

2.4.4 Glass Frit Wafer Bonding

Glass frit bonding is widely used in industrial applications for bonding fully processed wafers. Typically, this is an end-of-process-line bonding technique and it meets some very strict requirements needed for such a process: (i) the process temperature must be limited to 450 °C, (ii) no aggressive chemical cleaning can be used (otherwise, it would cause corrosion of metallic contacts), (iii) very high process yield is needed (as the fully processed wafers are involved whose fabrication is expensive and time-consuming), (iv) tolerance to wafer topography, (v) good mechanical strength, (vi) providing a hermetic seal and (vii) high reliability. In addition to this, the glass frit bonding technique allows bonding of almost any material used in microelectronics and microsystem technologies [32].

The basic principle is simple: a special glass with a low temperature melting point is used as an intermediate bonding layer between two wafers. When the wafers (and the glass between them) are heated, the glass becomes soft and liquid enough to wet the wafer surface and fill all the voids at the interface. After cooling, the glass re-solidifies providing a hermetically sealed and mechanically strong bond. Low melting point glasses that are used in this bonding technique can reflow at temperatures of 400 – 450 °C. However, they have an unstable glass matrix and can't be deposited using standard techniques (such as sputtering, CVD, etc.). Instead, they are grinded into small particles (15 μm diameter), and this powder is than mixed with an organic binder to form a paste. Solvents are also added to this paste in order to reduce viscosity as well as filler particles to reduce the coefficient of thermal expansion (CTE) of the mixture (since CTE of the glasses is usually much higher than CTE of the wafers). This slurry of finely pulverized glass particles in a liquid carrier (comprising binder, solvent, filler) is called a *glass frit*.

Typical low-melting point glasses used for glass frit are lead zinc silicate and lead borate glasses. A typical filler (for CTE reduction) is barium silicate glass ceramic [32]. The most commonly used glass frit paste is Ferro FX-11-036.

Glass frit is applied on a wafer using a screen printing techniques which allow *in situ* deposition and patterning. Thickness of the bonding layer is usually > 5 μm [32]. This means that glass frit bonding is, unfortunately, not suitable for evanescently-coupling hybrid photonic devices, usually requiring bonding layers around 100 nm or less. Additionally, planarization capabilities of this bonding technique are limited.

Glass frit bonding is a thermocompressive process, meaning that it is based on combination of temperature and application of a mechanical pressure to

complete the bonding process (similar to adhesive bonding based on thermosetting polymers). Usually, the bonding is conducted at temperatures in the range of 440 – 450 °C and the mechanical pressure is also applied when the glass starts flowing.

Major advantages of glass frit bonding are: hermetic sealing, high process yield, low mechanical stress at the bonding interface, high bonding strength and reliability. However, as mentioned before, due to the very thick bonding layers, this technique is not suitable for heterogeneous integration of III-V materials on a SOI photonic platform based on evanescent coupling. The main application of glass frit bonding is encapsulation of micromachined sensors, like gyroscopes and accelerometers [32].

2.4.5 Metal Wafer Bonding Techniques

There are several wafer bonding techniques that involve the use of metals as an intermediate bonding layer between the wafers. Classification of these bonding techniques is usually based on the physical principles of the bonding. The two most important groups among these techniques are solder bonding and diffusion bonding. In general, the use of metal bonding techniques for heterogeneous integration of III-V materials on the SOI photonic platform is limited by the fact that metals strongly absorb light. This means that the path of an optical signal and the metallic bonding layer must not cross each other. Consequently, the metallic bonding layer is usually patterned, i.e. selectively applied at the bonding interface only in those areas where it will not interfere with the optical signal. This limitation, of course, brings additional processing complexity and is especially difficult to implement in heterogeneous integration for evanescently-coupled photonic devices, where the optical signal is transmitted along the bonding interface. Therefore, metal bonding techniques are not quite the best candidates for the hybrid integration that we are interested in. Nevertheless, for the sake of having a complete overview of all the available bonding techniques, a brief summary of the metal bonding techniques will be given.

2.4.5.1 Solder Bonding Techniques

Solder bonding techniques are based on using a temporarily melted metal (or much more often a metallic alloy) as an intermediate bonding layer. Once the wafers (or dies) are brought into contact, a bonding metal layer is melted, filling the voids at the contacting interface. Metal solidifies upon cooling, forming a strong bond between the wafers. By far, the most commonly used materials are eutectic metal alloys, i.e. alloys which have composition that provides the lowest melting point for a given combination of metals. An eutectic alloy transforms from a solid into a liquid phase and vice versa at this specific single

temperature, without having a two-phase equilibrium system that comprises both liquid and solid phases. Therefore, eutectic soldering allows melting of the metals at the lowest possible temperature and only locally, where the metals have been deposited in a ratio insuring eutectic composition. Classical soldering processes involve the use of flux - a chemical cleaning agent that removes oxides from the metal surfaces and prevents solder joint oxidation.

Eutectic solders are well-known material systems with a long-established use in board assembly, die attachment and flip-chip bonding. For these applications, mainly, tin-rich alloys are used as they provide low melting points and their maximum operating temperature is limited to 150 °C (or lower). However, in the case of wafer (or die) bonding for heterogeneous integration, such low melting temperatures result in a low-temperature budget for the post-bonding processing, which is a serious disadvantage. Higher melting temperatures are characteristic for, gold-rich solders, like $Au_{80}Sn_{20}$, $Au_{97}Sn_3$, $Au_{88}Ge_{12}$, $Au_{72}In_{28}$ [32]. On the other hand, for bonding materials with different CTE it is good to have a lower bonding temperature to avoid high thermo-mechanical stress. Therefore, a compromise must be found when choosing an appropriate eutectic alloy between a low post-processing thermal budget (as a consequence of a low melting point temperature) and high induced stress, due to the very high eutectic temperature at which the bonding is performed.

Gold-tin (Au/Sn) alloys are very popular soldering materials and have been used in photonics, for fluxless processes which are needed to avoid contamination of optical surfaces. In general, Au/Sn solder provides hermetic sealing, high thermal conductivity of the bond and resistance to corrosives [32]. By far the most popular alloy is $Au_{80}Sn_{20}$, containing 20% by weight of tin. This eutectic alloy, with a melting temperature of 278 °C is very reliable and not prone to cracking due to formation of brittle intermetallic compounds. Another eutectic alloy that has been tested for wafer-scale bonding is $Au_{98}In_2$ [32]. However, its melting temperature of 156 °C gives an insufficiently small thermal budget for post-bonding processing of III-V materials.

Deposition of the metals for soldering can be performed by evaporation, sputtering or electroplating techniques. Patterning of the metal layers can also be carried out using lift-off techniques. Usually, gold is deposited first, followed by tin. The solder alloy is than formed in a post-processing step: by bump reflow at the wafer level or, in the case of flip-chip bonding, after the die placement, during reflow bonding [32]. In case of reflow soldering, no force is applied during the bonding, unlike the thermode soldering where the bonding force or the solder height are controlled.

The basic advantage of eutectic soldering is that it can accommodate much higher surface topography and non-planarity compared to other bonding techniques. In case of reflow soldering, requiring no application of force, bonding of

very sensitive components (like fragile thin membranes) is possible. Additionally, Au/Sn soldering exhibits excellent wetting behavior, a well-balanced soldering temperature (278 °C), it allows fluxless bonding, and provides excellent corrosion resistance.

2.4.5.2 Metal Diffusion Bonding Techniques

These bonding techniques are based on inter-diffusion of metals at the bonding interface, which after the process ends, create stable, solid metal layers so that the original bonding interface between the two initial metal surfaces cannot be recognized anymore. There are several metal diffusion bonding techniques, but the most common are *thermocompression bonding* in which the inter-metallic diffusion occurs in the solid phase and *solid-liquid interdiffusion bonding* (SLID) in which two metals in different phases (one as a liquid, the other as solid) inter-diffuse to eventually create a solid intermetallic compound.

Thermocompression bonding is based on interdiffusion of two solid metal surfaces, exposed to high pressure and high temperature. The most common technique is Cu-Cu thermocompression in which two copper bonding surfaces (that are, for example, deposited on two wafers that need to be bonded) are brought into contact and exposed to high temperature (usually > 300 °C) and mechanical pressure. This initiates interdiffusion of Cu atoms from the opposing metallic surface. Once this diffusion process saturates, the bonding process is finished and the original interface between the copper surfaces cannot be recognized anymore [32]. Typically, thermocompression bonding starts with the cleaning of the copper surfaces (usually by HCl treatment to remove native oxide and surface contamination). Due to diffusion process, the surface cleanliness requirements are not very strict and some contamination can be tolerated. The bonding is performed in vacuum, typically at temperatures around 400 °C and at the bonding pressure of around 4000 mbar, which is applied for at least 30 minutes. This is followed by annealing in nitrogen atmosphere at 400 °C for 30 to 60 minutes. Thermocompression copper bonding is one of the most promising technologies for wafer-level 3-D integration.

Such a high bonding and annealing temperature is a drawback (especially for bonding wafers with highly different CTE values) and research efforts are focused on realizing low-temperature metal diffusion bonding. One of the most promising strategies for achieving this is surface-activated copper bonding in which plasma treatment is used to remove oxide and contaminants from the copper surfaces. Subsequently, the bonding is performed at room temperature, in the vacuum and with the application of pressure. Another way to lower the bonding temperature is solid-liquid interdiffusion bonding.

Solid-Liquid interdiffusion bonding (SLID) is based on use of two metals: one with a high melting point T_H and the one with a low melting point T_L. The metals are deposited in such a way that there is a surplus of a high melting-point metal. The bonding is performed at a temperature slightly higher than T_L, so that a low-melting point metal melts and the metals interdiffuse at the points of contact. After this, the solid metal diffuses into the liquid, creating an intermetallic compound which solidifies at this temperature. Usually, SLID bonding consumes all of the low-melting point metal, leaving only high-temperature stable intermetallic compound and a high-melting point metal [32].

Materials suitable as high-melting point metals are Cu, Au, Ag, Co and Ni, while Sn and In are good candidates for low-melting point materials. For most of the systems the bonding temperatures are in range of: 250 °C - 350 °C. Compared to eutectic soldering, SLID bonding provides stronger, but more brittle bonds. Cu-Sn SLID bonding has been demonstrated for wafer-level bonding with through-silicon-vias (TSVs), together with hermetic sealing and packaging at the wafer level [32].

2.4.5.3 Hybrid Organic/Metal Bonding Techniques

Recently, researchers have focused on developing hybrid bonding techniques that combine metal bonding with adhesive bonding techniques. Metals are selectively applied (patterned) at the bonding interface, usually only to provide electrical contacts, good thermal conductance and initial bond between the wafers. After the metal bonding step, the gap at the bonding interface is filled with the organic adhesive, for example a thermally-cured polymer. The wafer stack is heated to cure the polymer and complete the bonding process. In this way, both mechanically strong and electrically (and thermally) conductive connection between the two wafers is made. An example of such hybrid organic/metal bonding method is a combination of InAu eutectic metal bonding and epoxy adhesive bonding, where epoxy is injected into the gap between the wafers after they were pre-bonded wafer by eutectic soldering [32]. This kind of hybrid polymer/metal bonding can be very interesting for photonics applications, especially in the case of integration of III-V materials on an SOI substrate. It offers the advantage of a good thermal conductivity and electrical contacts to the SOI substrate, via the metallic contact/bonding pads, giving the underlying silicon layer a role in both the carrier injection and effective heat removal.

Despite obvious advantages, these techniques give additional complexity to the bonding process and the problems due to usually large CTE mismatch between organic adhesive and metals need to be addressed too.

2.4.6 Bonding Techniques Based on Self-Assembled Monolayers

One special type of the bonding techniques employing intermediate layers is based on the use of self-assembled monolayers. The basic principle of these techniques is application of a monolayer of special organic molecules on one or both bonding surfaces. These organic molecules at both ends of their molecular chains terminate with special functional groups that chemically react with the bonding surfaces (or the molecules applied to the surface of the other wafer). After deposition of these layers on the bonding surface (or both surfaces), the bonding wafers (or dies) are brought into contact, heated and pressed, initiating chemical reactions. Organic molecules in the intermediate monolayer self-assemble to the reactive functional groups of the molecules at the bonding surfaces and eventually create strong chemical bonds. In this way, a permanent bond between the wafers (or dies) is established.

A big advantage of these bonding techniques lays in the fact that they can be used for bonding various materials (semiconductors, metals, dielectrics), as long as there are suitable organic molecules with functional groups that can chemically react with the given substrates. Artel *et al.* reported procedures for bonding InP to silicon and $LiNbO_3$ to silicon [66, 67], using the organic molecules with trichlorosilane ($SiCl_3$) and thioacetate functional groups. The reported bonding temperature is 120 °C [67], which significantly reduces the thermal stress due to the CTE mismatch. Such a low bonding temperature and the intermediate layers that are less than 6 nm thick [67] make this bonding technology attractive for the fabrication of hybrid evanescently-coupled photonic devices.

Since this is still a relatively novel technique from the perspective of applications in silicon photonics, we can expect to see more efforts in this field in the near future.

2.5 Comparison of Heterogeneous Integration Techniques

To summarize this review of heterogeneous integration technologies, we can compare them in several categories important from the aspect of fabrication of hybrid III-V/Silicon lasers on an SOI platform. Overview of this comparison is presented in Table 2.3. Although flip-chip bonding is a very mature technology that is already in use for integration of VCSELs on CMOS circuits [2], we have already pointed out in Section 2.2 that it is not suitable for high-density integration or wafer-scale processing. Monolithic integration techniques have recently come into in a focus of many research groups. In perspective, they offer

high integration density, wafer-scale processing, very economical and selective use of relatively expensive III-V materials and a good thermal budget. However, growth techniques still impose some limitations, either due to high temperature (e.g. ~ 600 °C in case of ELOG) which is not compatible with CMOS processing or due to a specific silicon wafer orientation required in other growth techniques. For the moment, it is difficult to say whether we can expect a breakthrough in this area, but there is no doubt that we will see considerable research efforts in this field, especially ELOG techniques.

Property	Flip-chip	ELOG	Anodic	Direct (plasma-act.)	Adhesive (DVS-BCB)	Glass-frit	Solder
Bonding/ /Growth Temp. (°C)	150 - 360	~ 600	300 - 450	200 - 300	~ 250	~ 450	60 - 400
Thermal Budget (°C)	< bond. temper.	limited by CTE mism.	> 400	limited by CTE mism.	> 350	< 400	< bond. temper.
Sensitivity to particle contamin.	low	medium	medium	high	medium	low	medium
Sensitivity to surface roughness	low	medium	low	high	low	low	low
Planarization capability	no	no	no	no	yes	yes	yes
Distance between the wafers	several μm	none	none	~ 1 nm to ~ 100 nm	10's nm to 10's μm	5-20 μm	~ 100 nm to few μm
Hermeticity	no	yes	yes	yes	no	yes	yes
Thermal conductivity	high	high	high	high	low	low	high
Optical Transparency	no	yes	yes	yes	yes	yes	no
Technology Maturity	in use for decades	new	in use for decades	> 10 years	several years	> 10 years	years
Cost	high	high	low	medium	low	low	low

Table 2.3: Comparison of the heterogeneous integration techniques.

As mentioned before, at this moment, the bonding techniques present the most promising approach for heterogeneous integration of III-V materials on the SOI platform. Although being very mature techniques, neither glass-frit nor anodic bonding techniques are suitable for the heterogeneous integration we are interested in. Thick bonding layers (> 5μm) in the case of glass-frit bonding prevent evanescent optical coupling, and impose some challenges for implementation of other coupling techniques. Also, the bonding temperature of ~450 °C is very high given the CTE difference between InP and Si (4.6×10^{-6} K^{-1}, 2.6×10^{-6} K^{-1}, respectively) On the other hand, anodic bonding requires presence of an alkali-rich glass, making it inadequate for bonding III-V materials on silicon. Various metal bonding techniques can be employed, but only by bond-

ing in selected areas, outside of the optical path, as metals are excellent light absorbers. Additionally, the thermal budget of the solder bonding techniques is usually not very high.

In practice, direct bonding and adhesive bonding techniques remain as the most serious candidates. Direct bonding has already been demonstrated as a viable technology for fabrication of evanescent hybrid III-V/Si device [68–70]. However, direct wafer bonding is very sensitive to surface roughness, particle contamination and organic contamination of the bonding surfaces. Elaborate cleaning procedures need to be implemented prior to bonding. Also, in order to lower the annealing temperature, plasma-activation of the surfaces is required. All this might lead to a process that is not robust enough to be implemented in an industrial environment, providing sufficiently high yield at an acceptable cost.

From this perspective, the use of adhesive bonding techniques looks more promising as it should offer more relaxed bonding conditions, namely a greater tolerance to particle contamination and surface roughness. Specifically, the use of DVS-BCB is appealing, as it has good optical, electrical and mechanical properties. Also, its planarization properties should enable this bonding technology ability to bond III-V material on substrates with a rich topography (e.g. a pre-fabricated CMOS wafer). This is a significant advantage over a direct bonding which would require a flat, planarized surface. Being a relatively low cost process, with a capability to bond almost any kind of material, gives DVS-BCB bonding the additional advantage. Drawbacks of this technique lay in the low thermal conductivity of DVS-BCB (0.3 W/m·K) and the polymer permeability which prevents establishing a hermetic sealing.

2.6 Hybrid lasers on an SOI platform fabricated via heterogeneous integration

In this section, a short review of the hybrid lasers fabricated on an SOI platform via bonding techniques will be presented. Two bonding technologies that were most commonly used for this purpose are plasma-activated direct bonding and polymer adhesive bonding, mostly based on DVS-BCB. The general idea of most of these concepts was to bond, unprocessed III-V wafers or dies, comprising active layers, on a host SOI substrate, with silicon waveguides and other passive components. Following the bonding, a processing of III-V layers would be performed. In this way, instead of bonding pre-fabricated components and aligning them with submicron precision, which is both time-consuming and costly, the active devices are fabricated after the bonding and their alignment to the SOI substrate is achieved via designing adequate contact masks for lithographic

processing. In this way, the device misalignment comes only as a result of a registration error in a lithographic process. Consequently, the precise alignment at the bonding of III-V material on a SOI substrate is not required, and commercial pick & place machines can be used for fast positioning of multitude of III-V dies in a multiple die-to-wafer bonding process. Bonding and subsequent processing can be performed on a wafer scale, offering a possibility for a relatively low-cost, high-volume device fabrication.

2.6.1 Heterogeneous integration via adhesive bonding - research activities at Ghent University

The Photonics Research Group from Ghent University conducted pioneering work in use of DVS-BCB for adhesive bonding of InP-based epitaxially grown active layers on other host substrates. In the early work, a DVS-BCB adhesive bonding was used to transfer active layers on a GaAs substrate. In a subsequent processing, microring resonators, light-emitting diodes (LEDs) and lasers, operating in pulsed regime were demonstrated in 2005 [71]. In the same year, InP/InGaAsP photodetectors, integrated on SOI waveguide circuits were demonstrated [72]. Since at that time relatively thick DVS-BCB bonding layers were employed, light coupling from an SOI waveguide to a bonded InP/InGaAsP photodetector was achieved via grating couplers fabricated on top of the silicon waveguide using 248 nm deep UV lithography. These early studies showed the potential benefits of reducing the bonding layer thickness, as this would both improve the device thermal characteristics and allow evanescent coupling between the III-V layers and the underlying SOI waveguides. Further improvements in the DVS-BCB bonding process were focused on optimizing curing temperature profile and diluting Cyclotene oligomer with mesitylene in order to achieve thinner bonding layers. Such an optimized bonding process yielding a DVS-BCB bonding layer thickness of less than 300 nm was reported in 2006 [73].

DVS-BCB was not the only material for adhesive bonding contemplated by the researchers from Ghent University. Parallel studies were carried out, using DVS-BCB and spin-on-glass (SOG) for adhesive bonding of unprocessed III-V dies on an SOI waveguide. Although SOG nominally allows formation of thinner layers (100 to 400 nm) than undiluted Cyclotene® 3022-35 (> 1 μm thickness), bonding using SOG on patterned SOI substrates proved to be less reproducible with inferior planarization characteristics, leading to formation of voids at the InP-SOG bonding interface [74]. Offering more reproducible results and superior planarization characteristics, DVS-BCB was selected as an adhesive of choice for further heterogeneous integration efforts.

The first electrically pumped, hybrid InP/InGaAsP laser on SOI, based on

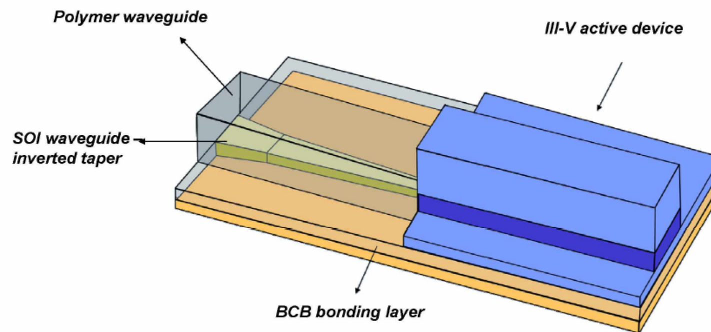


Figure 2.16: In/InGaAsP laser on SOI with an adiabatic inverted taper to couple the light into a silicon waveguide. Reproduced from [37].

DVS-BCB adhesive bonding, was demonstrated by Roelkens at al. in 2006 [75]. An adiabatic inverted taper, realized using polyimide, was used for coupling the light from a III-V material into an SOI waveguide, as illustrated in Figure 2.16. An identical structure and III-V layer stack was used for fabrication of integrated photodetectors. Lasing at 1.55 μm was observed only in a pulsed regime. The relatively high threshold current of 10.4 kA/cm^2 was the result of an inferior quality of the etched III-V layer stack facets [75]. Simultaneously, further improvements in the bonding process resulted in a reduction of the BCB bonding layer thickness down to ~100 nm, which enabled demonstration of metal-semiconductor-metal (MSM) photodetectors based on evanescent coupling [76].

Since 2008, work has intensified on other types of active photonic devices. Using the developed DVS-BCB bonding technique, the Photonics Research Group from Ghent University, in collaboration with other research groups, has demonstrated a microdisk laser [77], an optical isolator [78], a GaSb-based photodetectors for the short-wave infrared region [79, 80], an optically-pumped optical amplifier [81] and a hybrid III-V/Si laser with double adiabatic taper coupler [82].

2.6.2 Heterogeneous integration via direct bonding - research activities at UCSB

As mentioned earlier, another pioneering work in the field of evanescently-coupled lasers on SOI platform was carried out by the Optoelectronic Research Group from University of California - Santa Barbara. In their approach, they used a plasma-activated, direct bonding technique to transfer III-V epi layers

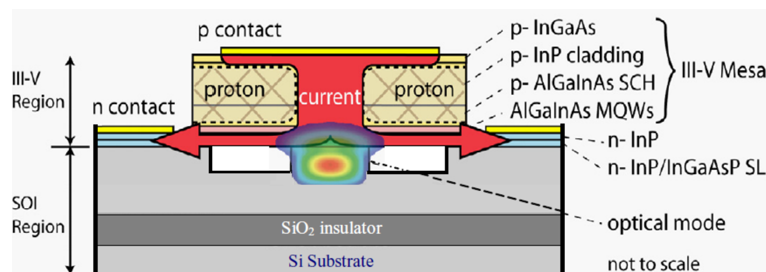


Figure 2.17: Cross-section of an electrically-pumped, evanescently-coupled, hybrid III-V/Si laser. Proton implantation of lateral mesa regions confines electrical current to the central region of the III-V mesa. Adapted from [83].

on a SOI substrate with a silicon rib waveguides [45]. Epitaxially grown III-V layers included InAlGaAs quantum wells (QWs), and InP-based top cladding, spacer and bonding interface layers. To prevent propagation of defects from the bonding interface towards the QW region, a two-period InP/InGaAsP superlattice was used [47, 49]. Initial demonstrations of optically-pumped lasers [47], operating up to 60 °C [49, 50], served as a proof of concept and paved the way for the development of electrically pumped devices.

The first electrically pumped, evanescently-coupled, hybrid InAlGaAs/Silicon laser was demonstrated in 2006 [48]. The cross-section of this device is illustrated in Figure 2.17. The basic structure of the III-V epitaxial layers was similar as before, except that the number of quantum wells was increased to eight in order to increase the fundamental optical mode confinement factor in the multiple quantum well (MQW) region. In order to confine the injected electrical current to the central region of the III-V mesa (where the bulk of the fundamental optical mode is located), a proton implantation was carried out to lower the conductivity of the lateral sections of the mesa (as illustrated in Figure 2.17). Fabricated Fabry-Perot lasers, emitting at around 1577 nm, had a threshold current of 65 mA, a maximum power of 1.8 mW and were lasing in continuous-wave (CW) regime up to 40 °C [48].

Further improvements of this design, including the reduction of the buried oxide thickness from 2 μm to 1 μm and the III-V mesa width down to 12 μm, increased the operating temperature to 45 °C and the maximum double-sided CW optical power to 24 mW at 15 °C [68]. The measured thermal impedance of 42 K/W was within 5% of the theoretically expected values [84]. Using the same direct bonding technique, the first electrically pumped, hybrid III-V/Si Fabry-Perot laser operating at 1310 nm was reported in 2007 [64]. Similar as before, eight quantum wells were based on InAlGaAs, but they also benefited

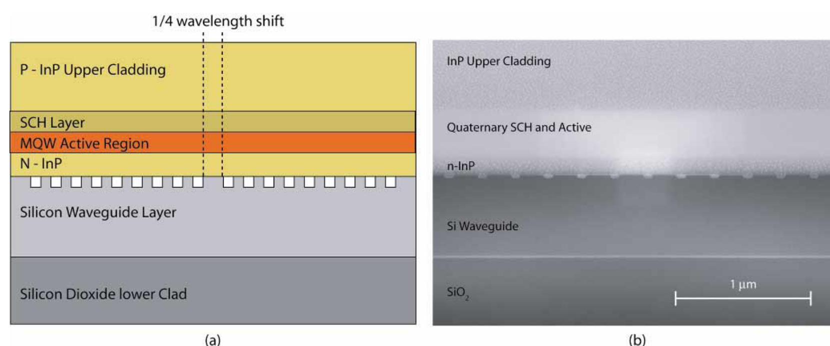


Figure 2.18: (a)Longitudinal cross-section of a distributed feedback (DFB) hybrid III-V/Si evanescent laser; (b) Scanning electron microscope (SEM) image of a DFB hybrid III-V/Si laser cross-section. Reproduced from [53].

from a larger conduction band offset and a relatively high confinement factor of 10.5%, for the second-order transverse optical mode that was, in fact, lasing. Consequently, this laser demonstrated CW operation up to 105 °C and a threshold current of 30 mA.

Following these initial results with Fabry-Perot lasers, distributed feedback (DFB) [53] and distributed Bragg-reflector (DBR) [85] hybrid III-V/Si lasers, emitting at around 1600 nm were demonstrated in 2008. In both devices, the distributed reflectors were made using a grating formed on top of the silicon rib waveguide. The longitudinal cross-section of a DFB hybrid III-V/Si laser is presented in Figure 2.18. Conceptually, it is based on a first-order grating made of ~ 25 nm deep corrugations at a period of $\Lambda = 238$ nm and 71% duty cycle. The grating is 340 μm long, with a quarter wavelength ($\lambda/4$) shift region, located in the centre, in order to break modal degeneracy. In order to minimize parasitic reflection and losses and enable a smooth transformation of the hybrid optical mode in the laser cavity into the optical mode of a silicon rib waveguide, 80 μm long adiabatic tapers made in III-V materials were fabricated at both ends of the grating [53]. Lasing in a CW regime was detected up to 50 °C, with a 25 mA threshold current and 5.4 mW maximum output power.

Similar to this, a hybrid, evanescently-coupled DBR laser was based on first-order, 75% duty cycle gratings on top of a silicon rib waveguide [85]. The layout of this laser is illustrated in Figure 2.19. It comprised a 440 μm long gain region with two 80 μm long tapers, which were also electrically pumped. The gratings were fabricated on top of the silicon rib waveguides at both ends of the device, therefore forming the front and the back mirrors. This hybrid silicon evanescent DBR laser, with a threshold current of 65 mA and maximum output power

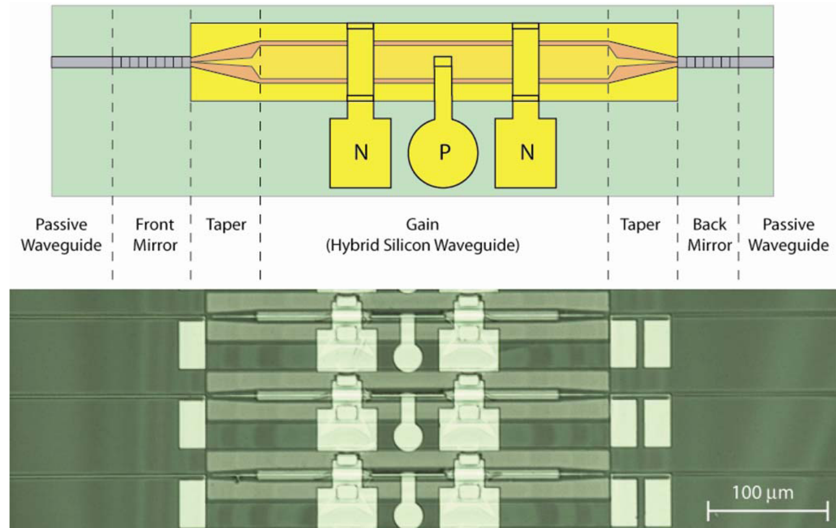


Figure 2.19: DBR laser top view structure (top) and microscope image of the fabricated devices (bottom). Reproduced from [55].

of 11 mW, demonstrated a CW operation, up to 45 °C [85]. Additionally, the laser was directly modulated using a 2^{31}-1 pseudo random binary sequence (PRBS) at 2.5 Gb/s and 4 Gb/s, resulting in eye diagrams with sufficiently high extinction ratios (8.7 dB and 5.5 dB, respectively), and characteristics comparable to commercially available lasers.

In addition to these devices, researchers at UCSB worked in parallel on the development of other active devices based on evanescent coupling, utilizing the same direct bonding process and III-V epitaxial layers with InAlGaAs-based quantum wells. An InAlGaAs/Si hybrid evanescent laser based on a racetrack resonator, emitting at 1590 nm and operating in a CW regime up to 60 °C was demonstrated in 2007 [51]. Coupling the light out of the racetrack resonator was achieved via a directional coupler which was in its turn optically connected to two integrated evanescent photodetectors, designed to detect the light propagating in both directions. A hybrid evanescent preamplifier and photodetector were demonstrated in the same year [54, 86].

Further extending the versatility of the developed integration technology, the use of a quantum-well intermixing (QWI) process was demonstrated for achieving different functionalities using the same original III-V epitaxial layer stack which would be subsequently transferred to the SOI silicon rib waveguide platform. Using the combination of a proton implantation at the selected areas of III-V layer and rapid thermal annealing (RTA), followed by selective etching, a shift in photoluminescence peak was achieved in the InGaAsP quantum

wells. This enabled the demonstration of sampled grating hybrid DBR lasers, integrated with electroabsorption modulators (EAMs) [87]. The same process was later used to demonstrate a Fabry Perot laser array comprising four lasers emitting at wavelengths within a span greater than 100 nm, from 1450 nm to 1570 nm [55]. Realization of various photonic functionalities on a single SOI substrate, utilizing a single III-V epitaxially grown layer stack via a QWI technique, showed a great potential of this heterogeneous integration concept for photonic applications requiring high-density integration.

Other evanescently-coupling, hybrid III-V/Si lasers demonstrated by researchers from UCSB included mode-locked lasers, based both on a racetrack resonator and a Fabry-Perot resonator [88], as well as a microring laser with a 50 μm diameter, with a threshold current of 5.4 mA, operating in a CW regime up to 65 °C [89, 90].

2.6.3 Hybrid III-V/Si lasers reported by other research groups

In parallel with these developments, a group of researchers from CEA-LETI institute in France, carried out a pioneering work in demonstrating direct molecular bonding as a viable technology for bonding individual InP dies on fully processed CMOS wafers. To achieve this, they deposited 10nm-thick layer of SiO_2 on a III-V die and used 1μm-thick thermally grown layer of SiO_2 on a silicon substrate to facilitate hydrophilic direct bonding. Annealing was carried out at relatively low temperature of 200 °C [56].

Not surprisingly, these results in development of hybrid III-V/Si lasers, achieved in the period between 2005 and 2008, sparked an increased interest among other researchers around the world. Since 2008, when the work on this thesis had started, there was a significant increase in number of publications on hybrid III-V/Si lasers based on bonding techniques.

An electrically pumped, evanescently-coupled, hybrid InGaAsP/Si Fabry-Perot laser based on oxygen plasma activated direct bonding was demonstrated by Sun *et al.*, from California Institute of Technology (Caltech) [91]. Conceptually, the laser was very similar to the one demonstrated by Fang *et al.* [48], featuring a superlattice for preventing threading of dislocations into the quantum well region. Operation in CW regime, up to 45 °C was reported, with a relatively low threshold current density of 1 kA/cm^2 [91]. Researchers from CEA-LETI used both hydrophilic direct bonding and BCB bonding techniques to transfer thin III-V layers on processed SOI wafers. Bonding yield of 98% was reported for direct bonding and over 80% for DVS-BCB bonding [92]. Fabry Perot lasers were fabricated only on a III-V wafer which was directly bonded to a SOI wafer. Lasing at 1571 nm was observed in a pulsed (or quasi-CW) regime of up to 60% duty cycle with a fiber-coupled output power of ~ 7mW [92].

A relatively low confinement factor (within the active III-V layers) of the lasing optical mode is typical for evanescently-coupled, hybrid III-V/Si lasers. This leads to relatively high threshold currents, which is an obvious disadvantage. To address this problem, Ben Bakir *et al.* reported the use of adiabatic mode transformers allowing the optical mode to change its profile as it propagates along the laser cavity. By varying the width of the underlying silicon rib waveguide from 700 nm to 1100 nm, the fundamental optical mode changes its shape and confinement factor within III-V material active region [93]. The silicon rib waveguide is narrow in the gain region, allowing high confinement factor within quantum wells, but as the waveguide width gradually widens to 1100 nm, the mode adiabatically transforms into one which is mostly confined within a Si waveguide. Using such adiabatic mode transformers and DBR mirrors, as well as the previously reported direct bonding technique [56], the authors have demonstrated lasing in a quasi-CW regime with a fiber-coupled output power of ~ 7mW [92]. In another work, using the same coupling and laser cavity schemes, the same authors reported a Fabry-Perot lasers at 1588 nm, operating in a CW regime up to 60 °C [94]. In the same paper, a racetrack resonator laser was demonstrated as well, employing the same adiabatic mode transformers. Another coupling scheme, based on adiabatic tapers was used by Lamponi *et al.* [82] to demonstrate heterogeneously integrated InP/SOI Fabry-Perot lasers, operating in CW regime up to 70 °C.

Several other hybrid III-V/Si lasers based on directed bonding were reported by other authors. Among several other laser designs, mostly based on thin InGaAsP/InP membranes, Arai *et al.* reported an optically pumped hybrid laser made by directly bonding InGaAsP/InP membrane on an SOI substrate, which was operating in a CW regime up to 85 °C [95]. Tanabe *et al.* demonstrated electrically pumped InAs/GaAs quantum dot lasers on a Si substrate emitting at 1.3 μm, realized by direct bonding of GaAs to silicon [57]. More specifically, the integration approach of these researchers was to create an ohmic contact between a p-type GaAs layer and a p-type silicon substrate enabling carrier injection from the silicon itself. Additional benefit of this approach is a good thermal conductivity allowing the silicon substrate to act as a heat sink. The bonding between p^+-GaAs and p^+-Si substrate was achieved at 300 °C, without any oxide deposition, which would act as an electrical insulator. Therefore, a hydrophobic direct bonding technique was applied. Lasing was demonstrated in a pulsed regime, with a threshold current density of only 205 A/cm^2 [57].

A very interesting chip-to-wafer bonding technique has been recently used by Justice *et al.* [96] and Yang *et al.* [97] for fabrication of hybrid III-V/Si lasers. In this technique, also known as 'transfer-printing', the functional III-V layers are initially grown on InP [97] or GaAs [96] substrates. Thin III-V membranes are subsequently formed by etching the mesas that are undercut from the III-V

substrate by selective etching of a sacrificial layer, which is grown just underneath the active layers comprising the mesa. These membrane chips are then picked up using a patterned elastomeric holder (a 'stamp') and then 'printed' onto the silicon surface. The chips, transferred in such a way, are attached to the silicon surface by van der Waals forces and directly bonded to it. Justice *et al.* [96] fabricated electrically-pumped AlGaAs/AlInGaAs double-quantum-well Fabry-Pérot lasers (emitting at 824 nm), with the cavity etching and deposition of the metal contacts carried out after the chip transfer. A 370 μm long laser cavity is formed in AlGaAs/GaAs layers, and silicon substrate plays no optical role in it. Continuous wave laser operation up to 100 °C is reported, with more than 25 mW optical power output per facet at room temperature [96]. Yang et al. used a similar process to demonstrate VSCEL devices based on 100-μm-diameter InGaAsP/InP disks transferred to an SOI substrate which was pre-patterned to create a photonic crystal reflector [97].

This 'print-transfer' technique offers considerable advantages in wafer-scale integration of III-V lasers on SOI substrates. At this moment, however, its application in fabrication of hybrid lasers on fully processed SOI waveguide circuits is yet to be demonstrated.

Apart from the direct bonding and adhesive bonding techniques, heterogeneous integration based on metal bonding was reported by several authors. Hong *et al.* reported an electrically-pumped, evanescently-coupled, hybrid InGaAsP/Si laser emitting at 1554 nm in a pulsed regime, up to 30 °C. Selective area metal (solder) bonding at 300 °C was used to bond pre patterned, thinned III-V layers on an SOI waveguide [98]. This is an interesting approach, as the metal bonds may also serve as excellent heat sinks and electrical contacts. Tanabe *et al.* also used full wafer, metal eutectic bonding, based on AuGeNi alloy, to demonstrate electrically pumped quantum dot InAs/GaAs lasers on a silicon substrate [99]. These lasers were not optically coupled to the underlying silicon layer, but the authors suggested the use of optical windows in the bonding layer to achieve evanescent optical coupling to the underlying SOI waveguides. In another approach, Hong *et al.* demonstrated an evanescently-coupled hybrid InGaAsP/ITO/Si laser based on the use of flip-chip bonding technique and optically transparent, yet electrically conductive, indium-tin-oxide (ITO) electrodes. At this stage, lasing at 1495 nm wavelength under cryogenic conditions (210 K) was demonstrated in a pulsed regime [100].

This short overview of hybrid III-V lasers was mostly focused on in-plane, hybrid III-V/Si lasers with a linear geometry, in which the laser cavity is parallel to the plane of an SOI substrate. Several other geometries, including vertical cavity lasers have been proposed [101, 102], but the review of these type of lasers is out of the scope of this thesis. Also, a detailed overview of the lasers

based on microdisk and microring resonators was not presented, as it is not directly related to the subject of this thesis. It is sufficent to say, that in the recent years there have been significant research efforts in development of microdisk and microring lasers and that both hybrid III-V/Si microdisk lasers based on direct [103] and DVS-BCB bonding [104, 105] have been demonstrated. Advantages of this type of lasers lay in their small footprint and power consumption, which allows very high density integration on a chip level. Major drawbacks are in its sensitivity to surface roughness (inducing scattering losses) and the fact that the precise control of the lasing wavelength strongly depends on the geometrical properties of the fabricated microdisk (or microring) resonators. Various ways to solve this problem are proposed [104, 106], but it remains an open question if these lasers are robust enough for large-scale industrial level fabrication.

2.7 Motivation for DVS-BCB bonding and evanescent-coupling

Summarizing the review presented in the previous section, it can be concluded that in 2008, at the moment when the work on this thesis started, an evanescent-coupling was viewed as the most promising coupling scheme for realization of a hybrid III-V/Si laser. Various other coupling schemes were contemplated [107], but using this type of a device layout, the research group at UCSB had already demonstrated Fabry-Perot [48], DBR [85] and DFB lasers [53]. This coupling scheme allows most of the optical power of the lasing mode within a cavity to be concentrated in the silicon waveguide. In this way, fabrication of complex coupling structures, like gratings, or employing coupling mechanisms which are not sufficiently tolerant to fabrication errors, would be avoided.

The choice of the integration technology was a relatively easy one. The Photonics Research Group of Ghent University had already been involved in the work on heterogeneous integration of III-V materials and SOI waveguide circuits, and adhesive bonding using DVS-BCB was already selected as a technology of choice. Promising results had already been achieved, including a demonstration of MSM photodetectors based on evanescent coupling [76] and featuring 100 nm thick DVS-BCB bonding layers. Further evolution of this bonding process and achieving even thinner bonding layers, suitable for evanescently-coupled photonic devices, was seen as a self-evident goal. In addition, previously demonstrated photonic devices were fabricated using a process of manual bonding of individual III-V dies on SOI substrates. In order to demonstrate feasibility of an industrial-scale DVS-BCB bonding process, there was a need to

develop a bonding procedure utilizing commercial wafer bonding tools. Additionally, machine-based bonding would provide much more uniform and reliable bonding results and improve the bonding yield.

Despite successful demonstration of hybrid III-V/Si lasers based on direct bonding, this technology requires ultra clean, smooth, particle-free and contamination-free surfaces. To achieve this, elaborate cleaning procedures are required. The robustness of this bonding procedure and suitability for large-scale fabrication in the industrial cleanroom facilities is still an open question. Therefore, the idea to use an evanescent-coupling scheme, as a proven concept, and try to fabricate hybrid lasers using DVS-BCB bonding technique was an appealing one. The expected impact of DVS-BCB bonding was that it would allow more relaxed bonding conditions, less rigorous and simpler cleaning procedure, greater tolerance to particle contamination and surface topography (due to planarization capabilities of the adhesive bonding) and more reliable, higher-yield bonding procedure.

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3

Design of a Hybrid Evanescent III-V/Silicon Laser

After choosing DVS-BCB bonding as a heterogeneous integration technique and evanescent coupling based on a hybrid III-V/Si platform, this chapter will focus on the hybrid laser design details. Initially, the general structure of the hybrid evanescent III-V/Si laser platform and the design concepts are discussed. Following this, optimization of the design parameters using optical, thermal and other physical simulations will be presented. After finalizing design parameters for Fabry-Perot lasers, the work on designing distributed feedback (DFB) and phase-shifted DFB lasers will be outlined. Although the details of the device fabrication procedure are not the subject of this chapter, some aspects of it will be considered, as they need to be taken into account while designing the devices.

3.1 General structure of the hybrid evanescent III-V/Si laser

The hybrid evanescent III-V/Si laser comprises a III-V epitaxial layer stack bonded on top of a silicon rib waveguide fabricated on a silicon-on-insulator (SOI) wafer. The general cross-section of such a laser is shown in Figure 3.1.

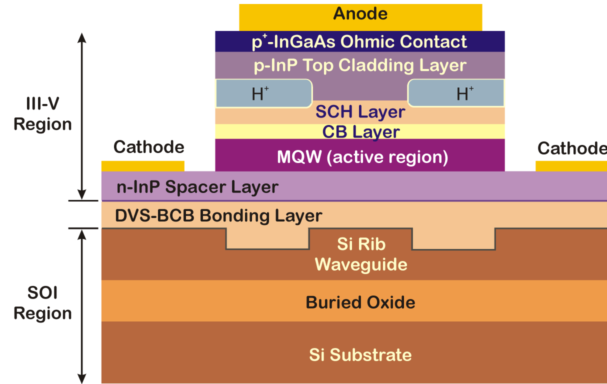


Figure 3.1: Cross-section of the hybrid III-V/Si waveguide laser

The III-V region, comprising a mesa and an n-type spacer layer is electrically pumped in order to provide population inversion in the active region of the structure, comprising multiple quantum wells (MQWs).

Top to bottom, the III-V layers comprise a highly-doped p-type ohmic contact, a p-type top cladding layer, a p-type separated confinement heterostructure (SCH) layer, a carrier blocking layer (undoped), followed by the multiple quantum well (MQW) region, made of alternating quantum wells and barriers and finally, an n-type spacer layer. Detailed composition of the epitaxial III-V layers is presented in Table 3.1. Quantum wells and barriers, SCH layer as well the carrier blocking layer are made using different $In_{1-x-y}Al_xGa_yAs$ quaternary alloys. As our goal is to fabricate a hybrid laser emitting at 1310 nm, the MQW region is designed to provide a photoluminescence peak near that wavelength. An electric p-type contact (anode) is located on the top of the mesa, while the cathodes are located on top of the spacer layer, symmetrically on both sides of the mesa. The DVS-BCB bonding layer is located between the III-V region and the SOI region, filling the trenches surrounding the silicon rib waveguide.

This whole structure, comprising the III-V region, the intermediate DVS-BCB bonding layer and the underlying silicon rib waveguide on an SOI substrate, represents a hybrid waveguide. Nominally, it is formed by two closely spaced waveguides: one within the III-V region and another one within the SOI region. In the case of the III-V waveguide, the MQW region, comprising both the quantum wells and the separating barriers, has higher refractive indices and acts as the waveguide core, while the surrounding layers, including the SCH, the top cladding and the spacer layers, act as a cladding. In the SOI region, we have a standard silicon rib waveguide made on an SOI substrate. Once the fundamental modes of these two closely-spaced, evanescently-coupled waveguides have the same effective refractive index, they are phase-matched and super-

Layer	Material	Doping (cm^{-3})	Thickness (nm)	Remarks
Ohmic contact	$In_{0.53}Ga_{0.47}As$	p-type $> 1 \times 10^{19}$	100	lattice-matched to InP
Cladding	InP	p-type 1×10^{18}	1500	
SCH	$In_{0.5305}Al_{0.4055}Ga_{0.064}As$	p-type 1×10^{17}	325*	λ_g=0.92μm lattice-matched to InP
CB layer	$In_{0.5047}Al_{0.4764}Ga_{0.0189}As$	undoped	10	λ_g=0.82μm tensile strain: -0.12%
Barrier (×9)	$In_{0.4003}Al_{0.2695}Ga_{0.3302}As$	undoped	9	λ_g=0.96μm tensile strain: -0.8%
Well (×8)	$In_{0.6986}Al_{0.178}Ga_{0.1234}As$	undoped	7	λ_{PL}=1.3μm compress. strain: +1.2%
Spacer	InP	n-type 1×10^{18}	240*	

Table 3.1: Structure of the III-V epitaxial layers. Thicknesses of the spacer layer and the separated confinement heterostructure (SCH) layer were optimization parameters and their values (marked with *) were determined after performing the optical simulations.

modes are formed. Actually, since the III-V and SOI waveguides are sufficiently close to each other, allowing evanescent coupling, they don't behave anymore as the individual waveguides, but act as a single hybrid waveguide, supporting the particular hybrid optical modes or supermodes. Basic analysis of such parallel, coupled waveguides, using the term 'supermode' was presented in 1984 [1] and later proposed for fabrication of hybrid III-V/Si lasers, amplifiers and modulators [2, 3].

By carefully designing the geometrical properties of the hybrid waveguide, the profile of the supported hybrid optical modes can be controlled [2, 3]. In this way, one can engineer how much of the optical power will be concentrated within the Si rib waveguide or the MQW active region of the III-V epitaxial layer structure. The general idea of the hybrid evanescent III-V/Si laser is to keep the bulk of the optical power of the fundamental hybrid mode within the Si rib waveguide, while providing a sufficiently high overlap of the fundamental optical mode with the multiple quantum wells to achieve the optical gain needed for lasing. Lateral confinement of the optical mode is mostly achieved using the silicon rib waveguide, while the carrier injection confinement into the III-V active region is achieved using proton (H^+) implantation into the lateral sections of the III-V mesa. More details on this will be presented in section 3.4. A typical intensity profile of the fundamental hybrid optical mode having a desired distribution of the optical power is given in Figure 3.2.

Optimization of the geometrical properties of this hybrid evanescent III-V/Si waveguide, in order to achieve the desired fundamental optical mode pro-

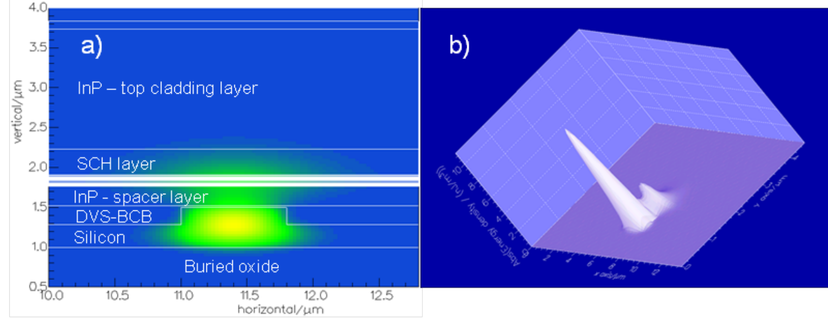


Figure 3.2: Intensity plots of the fundamental optical mode in the evanescent hybrid III-V/Si waveguide: a) 2-D plot and b) 3-D plot. The primary peak is located within the Si rib waveguide, while the secondary peak is centered around the MQW region of the III-V layer stack.

file was the first step in the design of the hybrid laser.

3.2 Optimization of the design parameters using optical simulations

3.2.1 Details of the evanescent hybrid III-V/Si waveguide

As mentioned earlier, the goal was to design an evanescent hybrid laser emitting at 1310 nm wavelength. In order to keep enough power of the fundamental optical mode within the silicon rib waveguide, the design objective was to keep the confinement factor of the fundamental optical mode in the silicon waveguide (Γ_{Si}) above 70%. On the other hand, in order to have sufficiently high overlap of the optical mode and the multiple quantum wells, another design objective was set to keep the fundamental optical mode confinement factor within the quantum wells (Γ_{MQW}) above 3%. This was in line with the calculations performed by researchers at UCSB [4].

When the lasing threshold is reached, the threshold modal gain $\langle g_{th} \rangle$ is equal to the sum of the average internal modal loss $\langle \alpha_i \rangle$ and the mirror loss α_m, which can be expressed in the following way:

$$\langle g_{th} \rangle = \Gamma_{MQW} \cdot g_{th} = \langle \alpha_i \rangle + \alpha_m \tag{3.1}$$

$$\Gamma_{MQW} \cdot g_{th} = \langle \alpha_i \rangle + \frac{1}{L} \ln(\frac{1}{R}) \tag{3.2}$$

where g_{th} is material gain at threshold, L is laser cavity length and R is mean intensity reflection coefficient of the laser facets. Taking into account that g_{th} is

of the order of several 1000's cm^{-1}, $\langle\alpha_i\rangle$ in the range of 15 to 40 cm^{-1} [4], cavity length L up to several hundreds of microns and $R \approx 0.3$ (based on the reflection at silicon/air interface), it can be shown, using Equation 3.2, that confinement factor within the quantum wells (Γ_{MQW}) should be at least 3%.

To help keep Γ_{MQW} sufficiently high, a structure with eight quantum wells, separated by 9 barriers is chosen (see Table 3.1), similar to the ones reported by researchers from UCSB [5–7]. Quantum wells are 7 nm thick, made of $In_{0.6986}Al_{0.178}Ga_{0.1234}As$, under compressive strain (+1.2%), while the 9 nm thick barriers are made of $In_{0.4003}Al_{0.2695}Ga_{0.3302}As$, under tensile strain (-0.8%). The designed photoluminescence (PL) peak of the quantum wells was set at 1275 nm and later measured to be 1277.1 nm, with a full-width at half-maximum (FWHM) of 37.2 nm. This intentional 'blue-shifting' of the PL peak is made in order to compensate for the 'red-shifting' (30 - 35 nm) of the peak lasing wavelength, experimentally observed in the initial batch of hybrid III-V/Si lasers which were fabricated using the quantum wells with a PL peak at 1310 nm.

Above the MQW region, as illustrated in Figure 3.3 there is a 10 nm thick carrier blocking (CB) layer, with a small tensile strain (-0.12%) designed to present a potential barrier for the electrons injected into the MQW region. In this way, the concentration of the injected carriers in the MQW region is increased, as well as the probability for the radiative recombination within the MQW region. Above the CB layer, there is an unstrained layer of $In_{0.5305}Al_{0.4055}Ga_{0.064}As$, lattice-matched to InP, acting as a separate confinement heterostructure. Above this, there is a 1500 nm thick top cladding layer (realized in p-type InP) and finally a 100 nm thick, heavily doped ($> 1 \times 10^{19}$ cm^{-3}) p-type ohmic contact, made of $In_{0.53}Ga_{0.47}As$, which is also lattice-matched to InP. Below the MQW region, there is an n-type InP spacer layer.

The band structure of the III-V layers is illustrated in Figure 3.4. Device simulation software ATLAS from Silvaco, Inc. was used to obtain this bandgap plot. The details of the band structure were modeled based on the Harrison's model and the data available in the literature [8–10]. The calculated bandgaps of the III-V layers are presented in Table 3.2. As seen in Figure 3.4, the carrier blocking (CB) layer acts as a barrier for the injected electrons. Similarly, the InAlGaAs barrier layer next to the InP spacer layer acts as the barrier for the injected holes. This arrangement facilitates agglomeration of the injected carriers within the MQW region where the recombination of the electron-hole pairs generates photons of the desired wavelength.

The underlying silicon rib waveguide is made on the SOI platform, with a 1 μm thick buried oxide (BOX) layer. The waveguide height is 500 nm while the rib etch depth is 220 nm. The SOI platform with these particular design parameters was selected by Intel Photonic Technology Labs. The width of the surrounding trenches is 3.5 μm. The space between the SOI region (with the Si rib waveguide

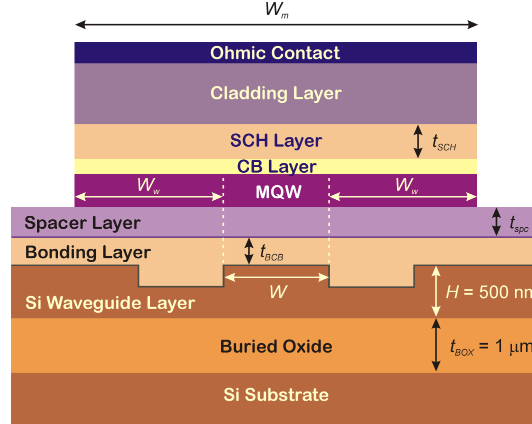


Figure 3.3: Geometrical parameters of the evanescent hybrid III-V/Si waveguide used for the optimization: the silicon rib waveguide width (W), the spacer layer thickness (t_{spc}), the SCH layer thickness (t_{SCH}), the III-V mesa wing section width (W_w) and the bonding layer thickness (t_{BCB}).

Layer	Material	Bandgap at 300 K (eV)
Ohmic contact	$In_{0.53}Ga_{0.47}As$	0.753
Cladding	InP	1.344
SCH	$In_{0.5305}Al_{0.4055}Ga_{0.064}As$	1.341
CB layer	$In_{0.5047}Al_{0.4764}Ga_{0.0189}As$	1.506
Barrier (×9)	$In_{0.4003}Al_{0.2695}Ga_{0.3302}As$	1.284
Well (×8)	$In_{0.6986}Al_{0.178}Ga_{0.1234}As$	0.718
Spacer	InP	1.344

Table 3.2: Bandgaps E_g of the III-V epitaxial layers at 300 K, calculated based on Harrison's model [8].

on the top) and the III-V region (starting from the n-type spacer layer upwards) is filled with the cured DVS-BCB bonding layer. It is assumed that the thickness of this bonding layer, measured from the top of the Si rib waveguide to the bottom of the InP spacer layer is an unknown variable, but sufficiently thin to allow the evanescent coupling between the III-V and SOI waveguides. For the purpose of simulations, it is considered to vary between 20 nm and 120 nm. The thickness of the strained layers are considered as constants, as there is no much freedom in varying them, due to the constrains in the growth of the strained layers, as expressed by the Matthews-Blakeslee formula [11]. Also, the thicknesses of the top cladding and the ohmic contact layers are fixed. In order to avoid strong light absorption in the heavily p-doped ohmic contact, the SCH and the top cladding layers are kept sufficiently thick to keep the bulk of the optical power of the fundamental mode away from the ohmic contact layer.

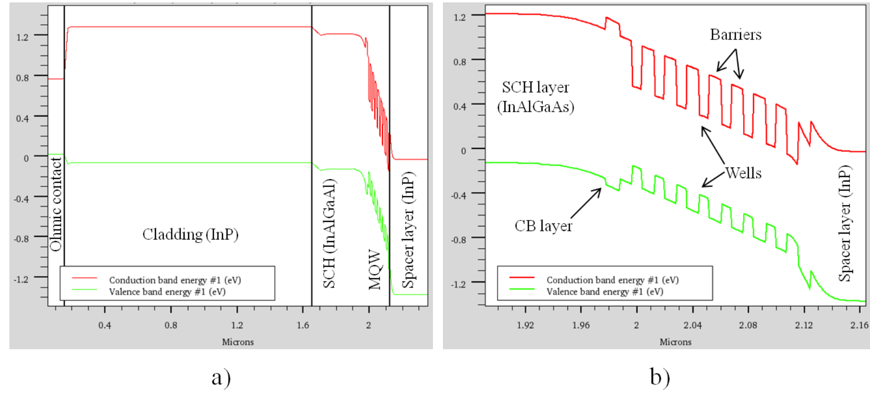


Figure 3.4: Band structure of the III-V layers when no voltage is applied: a) band structure of the all III-V layers; b) zoom-in of the multiple-quantum well (MQW) region.

3.2.2 Optimization of the hybrid waveguide geometrical parameters

After these considerations, the remaining geometrical parameters suitable for variations and optimization of the fundamental optical mode profile are the thickness of the SCH layer (t_{SCH}), the thickness of the spacer layer (t_{spc}), the width of the Si rib waveguide (W), as well as the total width of the III-V mesa (W_m). From the perspective of the simulations, it was easier to conceptually divide the mesa width into three sections: the central one, which was as wide as the Si rib waveguide (W) and two symmetrical lateral sections (or wing sections), with an adjustable width of W_w. Therefore, instead of directly varying the total III-V mesa width (W_m), we varied the wing section width (W_w). The relation between these two values, as illustrated in Figure 3.3 is: $W_m = 2W_w + W$, where W is the Si rib waveguide width. The goal of the optical design is therefore to choose the optimum values for these parameters allowing a relatively stable profile of the fundamental optical mode, for the thickness of the bonding layer (t_{BCB}) varying between 20 nm and 120 nm. In quantitative terms, this translates into a design goal that the confinement factors Γ_{Si} and Γ_{MQW} should stay above 70% and 3%, respectively, within this range of the bonding layer thickness.

The refractive indices of the layers, used in the optical simulations are given in Table 3.3. Refractive indices for the strained layers were calculated from the dielectric constants for the strained layers [12] as well as the data provided by researchers at UCSB [13]. The absorption coefficients in the doped layers were estimated based on the free-carrier absorption and the data available in the literature [14–16]. The concentration of the free carriers in these layers was as-

Layer	Material	n (at 1310 nm)	α (cm^{-1})
Ohmic contact	$In_{0.53}Ga_{0.47}As$	3.4348	8000
Cladding	InP	3.19870	80
SCH	$In_{0.5305}Al_{0.4055}Ga_{0.064}As$	3.27033	8
CB layer	$In_{0.5047}Al_{0.4764}Ga_{0.0189}As$	3.22796	0
Barrier (×9)	$In_{0.4003}Al_{0.2695}Ga_{0.3302}As$	3.45315	0
Well (×8)	$In_{0.6986}Al_{0.178}Ga_{0.1234}As$	3.59228	0
Spacer layer	InP	3.1987	1
Bonding layer	DVS-BCB	1.537	0
Rib waveguide	Si	3.49	0
Buried oxide	SiO_2	1.45	0

Table 3.3: Refractive indices and absorption coefficients of the hybrid III-V/Si waveguide layers (at wavelength λ = 1310 nm) used in the optical simulations.

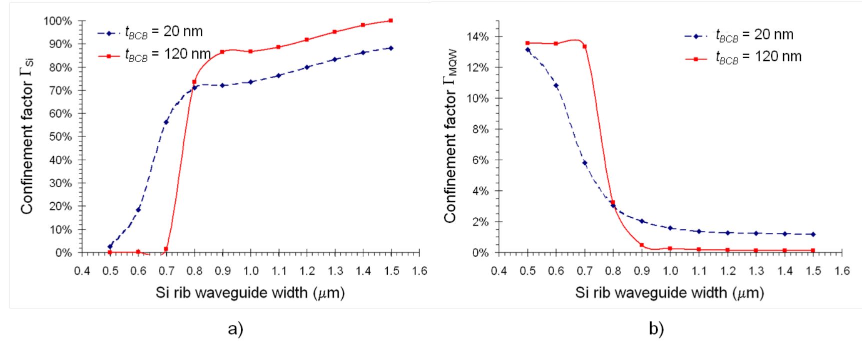


Figure 3.5: Dependence of the confinement factors: a) Γ_{Si} and b) Γ_{MQW} on the silicon rib waveguide width W.

sumed to be equal to the concentration of the dopants.

The first design step was to choose the optimum width W for the silicon rib waveguide. The simulations were made using a full-vectorial mode solver, FIMMWAVE (by Photon Design), based on the film mode matching method. For this purpose, the values of spacer layer thickness (t_{spc}), SCH layer thickness (t_{SCH}) and III-V mesa wing section width (W_w) were fixed at 240 nm, 325 nm and 8 μm, respectively. The silicon rib waveguide width was changed from 0.5 μm to 1.5 μm. Confinement factors Γ_{Si} and Γ_{MQW} of the fundamental optical modes were calculated. The results of these simulations are presented in Figure 3.5. Two extreme cases of the DVS-BCB bonding layer thickness were considered: t_{BCB} = 20 nm and t_{BCB} = 120 nm.

From these results we can conclude that a drastic change in the confinement factor values, characteristic when the phase-matching is achieved, occurs at waveguide width of W = 0.8 μm. This is especially obvious in the case of

a 120 nm thick DVS-BCB bonding layer, when the III-V waveguide and silicon rib waveguide are weakly coupled. Additional simulations with slightly different values of t_{SCH}, t_{spc} and W_w, gave similar results. For the other values of the waveguide width W, the variations in the DVS-BCB bonding layer thickness t_{BCB} significantly affect the confinement factors Γ_{Si} and Γ_{MQW} which is exactly what we want to avoid. Therefore, we fixed the value for the silicon rib waveguide at W = 800 nm and used it in the following simulations.

In the next step of design optimization, thicknesses of the spacer layer (t_{spc}) and the SCH layer (t_{SCH}) were to be selected. The impact of the mesa width, or more specifically the wing section width W_w, on the fundamental optical mode profile was relatively small. Therefore, in the following simulations, this value was fixed at $W_w = 3\ \mu$m and its optimization was left for further considerations, described in section 3.2.4. In the first round of simulations, t_{spc} was fixed at 250 nm, and the confinement factors Γ_{Si} and Γ_{MQW} were calculated for four different values of t_{SCH}: 300 nm, 325 nm, 350 nm and 375 nm. The results of these simulations are presented in Figure 3.6. Although Γ_{Si} and Γ_{MQW} showed the most stable values for the varying t_{BCB} in case of t_{SCH} = 300 nm, Γ_{MQW} didn't have sufficiently high values (> 3%), especially for thicker DVS-BCB bonding layers. Therefore, we chose the second value, t_{SCH} = 325 nm for the SCH layer, as it provided sufficiently high Γ_{MQW}. After fixing t_{SCH} at 325 nm, another round of simulations was conducted to choose the optimal thickness of the spacer layer. The confinement factors were calculated for four values of t_{spc}: 230 nm, 240 nm, 250 nm and 260 nm. The results of these simulations are shown in Figure 3.7. Obviously, for t_{spc} value of 240 nm, both confinement factors showed the least variations and sufficiently high values: $\Gamma_{MQW} > 3\%$ and $\Gamma_{Si} > 70\%$.

Therefore, the optimal thicknesses chosen for the SCH layer and the spacer layer are t_{SCH} = 325 nm and t_{spc} = 240 nm. The confinement factor values for these parameters and silicon waveguide width of 0.8 μm are shown in Figure 3.8. For the varying bonding layer thickness t_{BCB} between 20 nm and 120 nm, the confinement factors meet the following conditions: $\Gamma_{MQW} > 3.2\%$ and $\Gamma_{Si} >$ 74.5%, which are more strict than those that were originally required.

3.2.3 Impact of the III-V mesa width on the optical properties

Following selection of the optimal silicon rib waveguide width, as well as the spacer layer and the SCH layer thicknesses, it is time to focus on the impact of the III-V mesa width on the hybrid modes profile and try to find its optimum value. In the previous simulations, only the profile of the fundamental optical mode was taken into account, without considering the profiles of the higher-order modes. Simulations showed that its shape didn't change much for the III-V mesa wing section width (W_w) varying between 2 μm and 10 μm, while

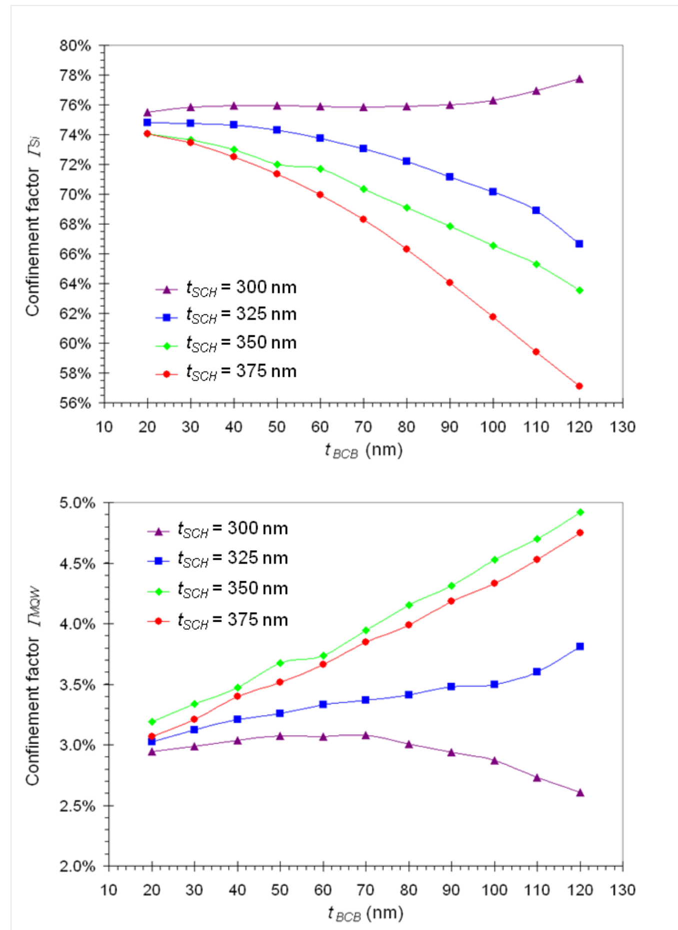


Figure 3.6: Dependence of the confinement factors Γ_{Si} and Γ_{MQW} on the DVS-BCB layer thickness (t_{BCB}) for various SCH layer thicknesses t_{SCH}. The other parameters used in simulations: W = 0.8 μm, t_{spc} = 250 nm.

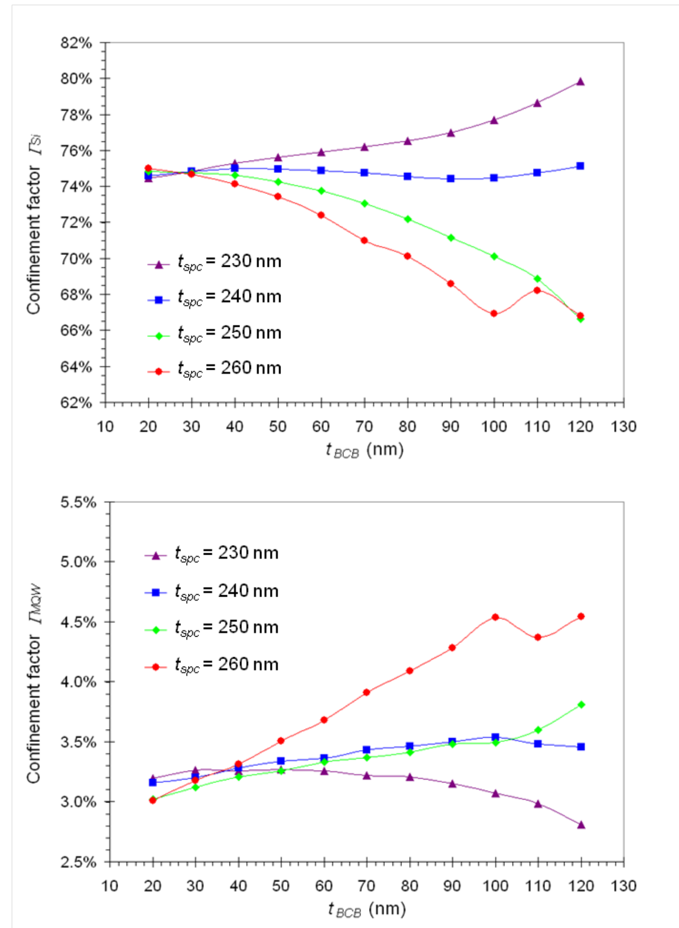


Figure 3.7: Dependence of the confinement factors Γ_{Si} and Γ_{MQW} on the DVS-BCB layer thickness (t_{BCB}) for various spacer layer thicknesses t_{spc}. The other parameters used in simulations: W = 0.8 μm, t_{SCH} = 325 nm.

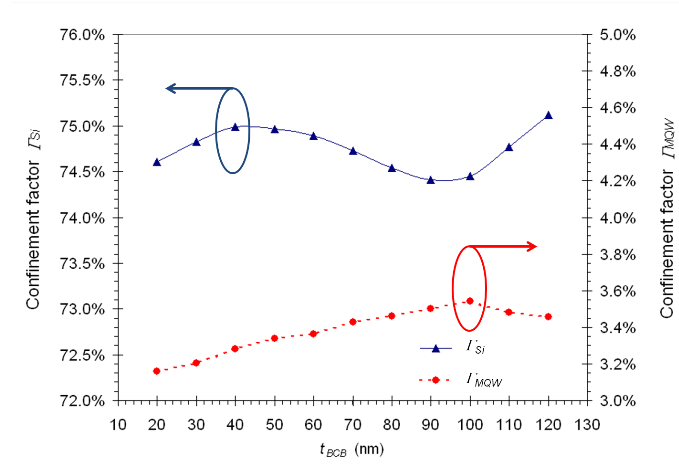


Figure 3.8: Dependence of the confinement factors Γ_{Si} and Γ_{MQW} on the DVS-BCB layer thickness (t_{BCB}) for the optimal values of SCH and spacer layer thicknesses: t_{spc} = 240 nm, t_{SCH} = 325 nm. The mesa wing section width is W_w = 3 μm.

keeping previously adopted geometrical parameters: W = 0.8 μm, t_{scp} = 240 nm, t_{SCH} = 325 nm. However, profiles of the higher-order optical modes are siginificantly affected by the total III-V mesa width. Typical intensity mode profiles for the second-order mode for two different mesa wing section widths are illustrated in Figure 3.9. In general, the second-order mode has two dominant, symmetrical intensity peaks, located within the MQW region of the III-V mesa and a third peak located witihin the Si rib waveguide, as shown in Figure 3.9a and Figure 3.9c. As the mesa width increases, the separation between two peaks in the MQW region increases as well, leaving in the central section of the mesa a region with a relatively low optical mode intensity. On the other hand, if the III-V mesa becomes too narrow ($W_w \sim 1$ μm), these two peaks will merge into a single dominant peak, as illustrated in Figure 3.9b and Figure 3.9d.

This behaviour of the second-order optical mode can be used for an efficient design of the evanescent, hybrid III-V/Si laser. The design requirement is to have only the fundamental mode lasing, not the second-order one, which conveys less optical power within the silicon rib waveguide. Also, lasing of the higher-order modes is not desired. Similar to the second-order mode, the higher order modes also have a broader distribution of the optical power within the III-V mesa. Therefore, only the fundamental optical mode has its optical intensity within the III-V mesa concentrated exclusively in the central region of the mesa, just above the rib waveguide.

Typically, the confinement factor of the second-order mode within mulit-

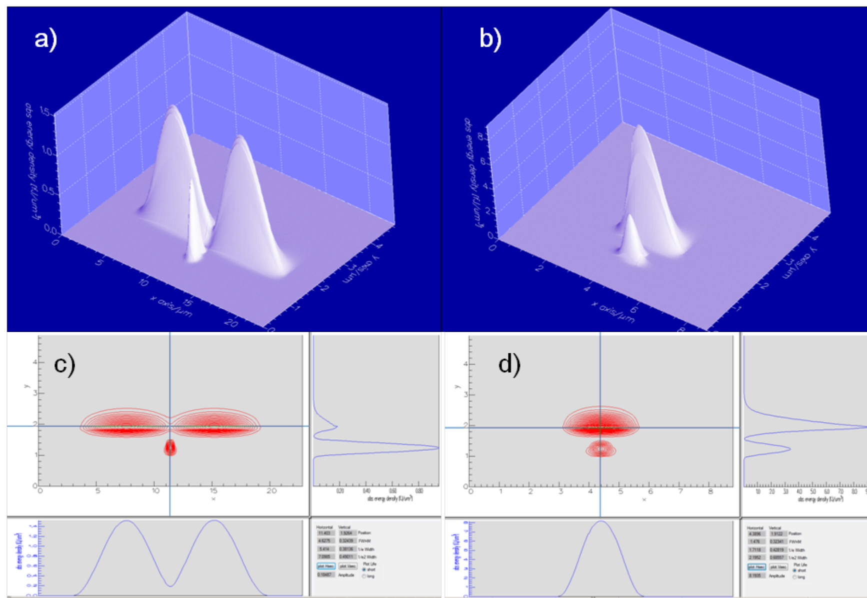


Figure 3.9: Impact of the III-V mesa width on the second-order hybrid optical mode profile. 3-D mode intensity plot for the mesa wing section width of: a) $W_w = 8\ \mu$m; b) $W_w = 1\ \mu$m. 2-D mode intensity cross-section for the mesa wing section width of: c) $W_w = 8\ \mu$m; d) $W_w = 1\ \mu$m.

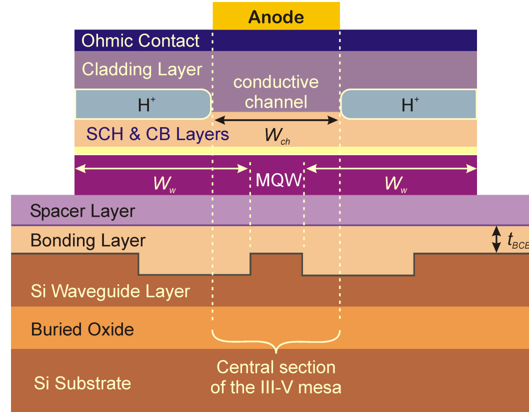


Figure 3.10: Hybrid laser cross-section with the central section of the III-V mesa defined by the width of the carrier injection channel W_{ch}. The III-V mesa wing section width W_w, used as a parameter in the simulations, is equal to the distance between the edges of the Si rib waveguide and the III-V mesa.

ple quantum wells (MQWs) is 3-4 times higher than Γ_{MQW} for the fundamental mode. Consequently, if the carriers are injected into the MQWs across the entire width of the III-V mesa, the second-order mode will be the first to start lasing. However, if the carrier injection is narrowed down only to the central section of the III-V mesa, then the confinement factor within this region for the fundamental optical mode $\Gamma^{fund}_{MQW-cen}$, can be larger than a corresponding confinement factor of the second order mode $\Gamma^{2nd}_{MQW-cen}$, provided that the separation between the second-order optical mode peaks within the III-V layers is large enough. In other words, if the III-V mesa width is large enough the following condition: $\Gamma^{fund}_{MQW-cen} > \Gamma^{2nd}_{MQW-cen}$, can be met. In this way, lasing of the fundamental mode over the second-order or any other higher order mode is assured.

Practically, this confinement of the carrier injection into the central part of the III-V mesa is achieved via proton (H^+) implantation which makes the wing sections of the mesa electrically highly resistive, leaving only the conductive channel in the middle of the mesa, as illustrated in Figure 3.10. The proton implantation will be discussed in more detail in section 3.4. Narrowing the mesa itself is not an option, as it will create a single, dominant intensity peak of the second-order mode within the MQWs, as illustrated in Figure 3.9, which would lead to initial lasing of the second-order mode, instead of the first one.

The width of the conductive channel (W_{ch}), illustrated in Figure 3.10, defines the central section of the mesa that was previously discussed, where the confinement factors of the optical modes within MQWs should be considered.

W_w (μm)	t_{BCB} = 20 nm		t_{BCB} = 70 nm		t_{BCB} = 120 nm	
	$\Gamma^{fund}_{MQW-cen}$	$\Gamma^{2nd}_{MQW-cen}$	$\Gamma^{fund}_{MQW-cen}$	$\Gamma^{2nd}_{MQW-cen}$	$\Gamma^{fund}_{MQW-cen}$	$\Gamma^{2nd}_{MQW-cen}$
2	3.21323 %	10.02749 %	3.22750 %	9.74901 %	2.72828 %	10.00217 %
3	3.22671 %	6.82068 %	3.29102 %	7.03507 %	3.07653 %	7.25818 %
4	3.22369 %	4.27632 %	3.29493 %	4.73173 %	3.15306 %	5.15549 %
5	3.30148 %	2.71785 %	3.29163 %	3.14395 %	3.16010 %	3.64461 %
6	3.28510 %	1.78850 %	3.29171 %	2.11406 %	3.17595 %	2.55922 %
7	3.29312 %	0.72322 %	3.28725 %	1.47073 %	3.15968 %	1.83005 %
8	3.27622 %	0.87777 %	3.28288 %	1.04864 %	3.16617 %	1.31500 %
9	3.28708 %	0.64660 %	3.30251 %	0.77044 %	2.92555 %	0.96341 %
10	3.28100 %	0.48696 %	3.27682 %	0.58048 %	2.90929 %	0.72381 %

Table 3.4: Dependence of the MQW confinement factors in the central section of the III-V mesa on the mesa wing section width W_w. The width of the central section is W_{ch} = 3 μm.

It should be narrow enough to satisfy the condition $\Gamma^{fund}_{MQW-cen} > \Gamma^{2nd}_{MQW-cen}$, and therefore allow the fundamental mode to be the first one to start lasing. On the other hand, W_{ch} should be wide enough to provide efficient carrier injection and reasonably low resistance of the laser diode. The same approach in narrowing the carrier injection using the proton implantation was used by UCSB researchers, where they reported a 4 μm wide channel [5, 17].

In order to minimize the chances for lasing of the second-order mode due to a wide carrier injection channel, as it was reported by Chang *et al.* [17], we have decided to narrow it down to the width of W_{ch} = 3 μm and calculate the confinement factors $\Gamma^{fund}_{MQW-cen}$ and $\Gamma^{2nd}_{MQW-cen}$ for the central mesa section of this width, as illustrated in Figure 3.10. The width of the mesa wing section (W_w) was varied between 2 μm and 10 μm and the confinement factors were calculated for three values of the bonding layer thickness: 20 nm, 70 nm and 120 nm. The results of the simulations, summarized in Table 3.4, clearly indicate that the mesa wing section width should be 6 μm or more, in order to assure that the condition $\Gamma^{fund}_{MQW-cen} > \Gamma^{2nd}_{MQW-cen}$ is fulfilled for the t_{BCB} value between 20 nm and 120 nm. For thinner DVS-BCB bonding layers (t_{BCB} = 20 nm or t_{BCB} = 70 nm), this condition is met even for W_w = 5 μm, but considering the worst-case scenario (i.e. $t_{BCB} > 70$ nm), it is safer to put the following requirement on the mesa wing section width: $W_w \geq 6$ μm.

The layout of the hybrid optical modes is not the only thing to consider in determining the optimum width of the III-V mesa. This parameter also affects the thermal and electrical properties of the hybrid laser and these impacts will be considered in sections 3.3 and 3.4, respectively. Obviously, the increase in the III-V mesa width, increases the electrical resistance of the laser as the carriers need to travel a longer distance through a relatively narrow (t_{spc} = 240 nm) InP

spacer layer. Therefore, the final choice for the width of the III-V mesa will be made following thermal and electrical simulations.

3.2.4 Impact of the Si rib waveguide dimensions on the hybrid mode layout

Before proceeding with the simulations of the thermal properties of the hybrid laser, it would be very interesting to assess the impact of variations in the Si rib waveguide dimensions on the layout of the fundamental optical mode, supported by the hybrid III-V/Si waveguide. The nominal height of the silicon waveguide is H = 500 nm, while the optimal width that is chosen is W = 800 nm. Fabrication tolerance for the waveguide height is usually within $\pm$20 nm. Also the tolerance for the waveguide width is of the similar order of magnitude. Therefore, it would be interesting to assess the robustness of the evanescent hybrid III-V/Si laser design by studying the impact of the small variations around these nominal values for H and W on the fundamental optical mode profile.

For this purpose, a series of optical simulations was carried out in order to calculate the confinement factors of the fundamental mode within the MQW region (Γ_{MQW}) and the Si rib waveguide (Γ_{Si}). The silicon rib waveguide heigth (H) was varied between 480 nm and 520 nm, while the waveguide width (W) was varied between 700 nm and 900 nm. Previously adopted values for the spacer layer and the SCH layer thicknesses, t_{spc} = 240 nm and t_{SCH} = 325 nm, were used. A III-V mesa wing section width of W_w = 8 μm was used in these simulations. The confinement factors Γ_{MQW} and Γ_{Si} were calculated for three values of the DVS-BCB bonding layer thickness: t_{BCB} = 100 nm, t_{BCB} = 50 nm, and t_{BCB} = 0 nm, which was considered as a theoretical extreme case, when the spacer layer and the top of the Si rib waveguide are in intimate contact.

The results of these simulations are presented in Figure 3.11. The colour-coded contour plots show the variations in the confinement factors Γ_{MQW} (plots on the left side of the Figure 3.11) and Γ_{Si} (plots on the right side of the Figure 3.11), depending on the variations in the Si rib waveguide width and height, presented on the horizontal and vertical axes, respectively. In general, we can conclude that as the BCB bonding layer becomes thicker, the confinement factors Γ_{MQW} and Γ_{Si} become more sensitive to variations in Si rib waveguide dimensions. As expected, an increase in either height or width of the silicon waveguide increases the value of Γ_{Si}, while simultaneously decreasing Γ_{MQW}. Therefore, the waveguide dimensions H and W, need to be keept in the right balance providing sufficiently high values for both confinement factors (Γ_{MQW} > 3 %, Γ_{Si} > 70 %). If we focus on the left plots in Figure 3.11a and Figure 3.11b, we can see how the area in which the condition 3 % $\leq \Gamma_{MQW}$ < 4 % is fulfilled, becomes narrower as t_{BCB} increases from 50 nm to 100 nm. Similarly,

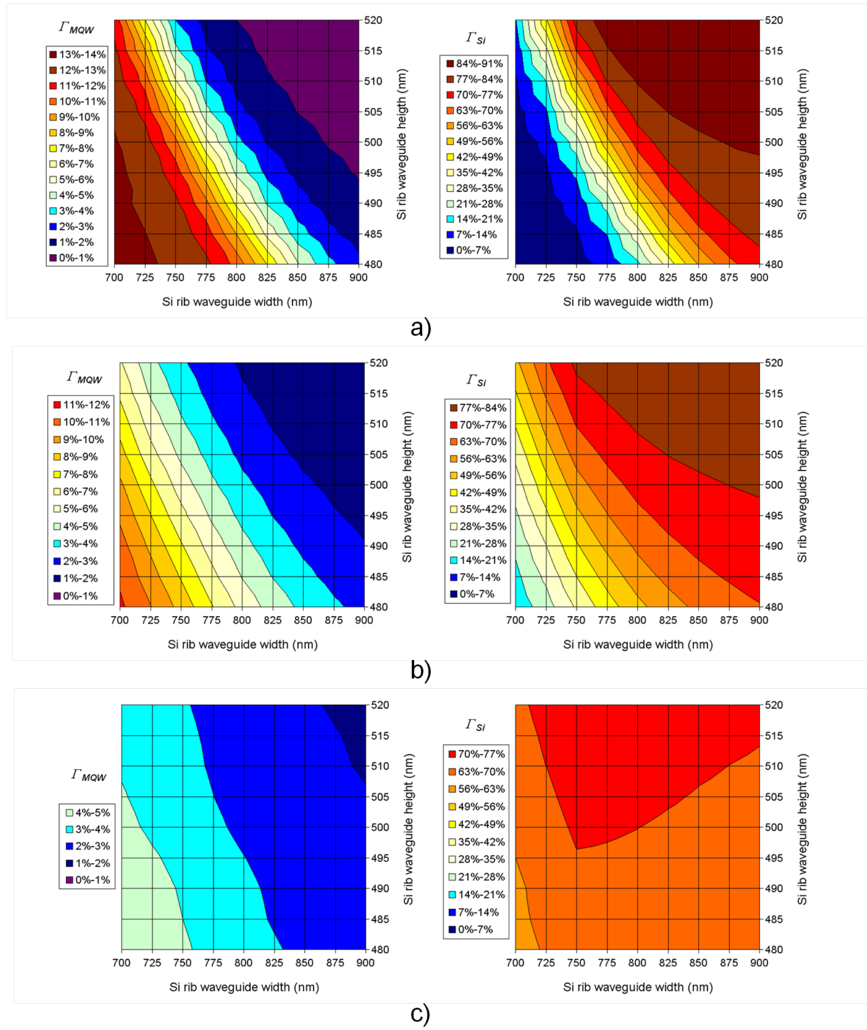


Figure 3.11: Impact of the variations in Si rib waveguide dimensions (width and height) on the confinement factors Γ_{MQW} (plots on the left side) and Γ_{Si} (plots on the right side), for three different DVS-BCB bonding layer thickness: a) t_{BCB} = 100 nm; b) t_{BCB} = 50 nm; and c) t_{BCB} = 0 nm.

as we can see on the right side plots in Figure 3.11a and Figure 3.11b, the area within which the confinement factor Γ_{Si} is between 70 % and 77 %, becomes smaller with the increase in the bonding layer thickness. On the other hand, for an idealized case of t_{BCB} = 0 nm, the variations in both Γ_{MQW} and Γ_{Si} are relatively small.

The main conclusion is that the hybrid laser robustness to variations in silicon rib waveguide dimensions increases, as the thickness of the bonding layer t_{BCB} decreases. This is one of the main arguments for having the DVS-BCB bonding layer as thin as possible.

3.2.5 Hybrid III-V/Si waveguide based on a planarized Si rib waveguide structure

Work on the development of a bonding procedure that would result in sufficiently thin DVS-BCB bonding layers is presented in Chapter 4, but here we can present another waveguide structure that was also employed for realisation of very thin bonding layers. The standard silicon rib waveguides on an SOI substrate, described in section 3.2.1, are surrounded with 220 nm deep trenches. Filling these trenches with a DVS-BCB, while simultaneously maintaining a bonding layer thickness (t_{BCB}) of only few tens of nanometers proved to be challenging. One idea to solve this problem was to planarize these waveguides during the SOI wafer fabrication, by 'filling' these trenches with silicon dioxide.

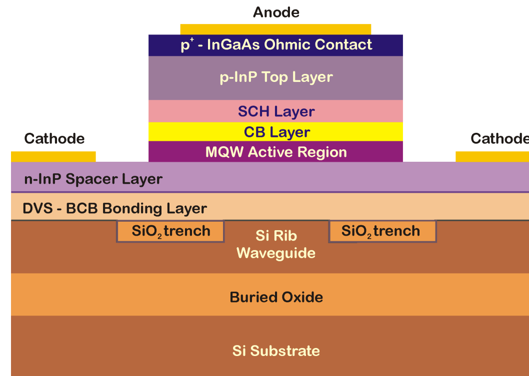


Figure 3.12: Cross-section of the hybrid III-V/Si waveguide on an ideally planarized SOI substrate with the SiO_2-filled trenches.

In practice, such waveguides are fabricated by deposition of a relatively thick layer of SiO_2 on the original SOI wafer, with 220 nm deep trenches. After SiO_2 deposition, this layer is thinned down and planarized by chemical-mechanical

polishing (CMP), leaving a layer of ~100 nm of SiO_2 on top of a Si rib waveguide. Eventually, the rest of the SiO_2 is etched away in a diluted solution of HF. In this way, the topography of such a waveguide with the 'filled-trenches' can be, in an ideal case, reduced to zero and the bonding on such an SOI substrate is equal to a bonding on a flat surface. The cross-section of a hybrid III-V/Si waveguide, made on such a planarized SOI substrate is illustrated in Figure 3.12.

The refractive index of SiO_2 at 1310 nm is 1.45, which is very close to the refractive index of DVS-BCB of 1.537. Consequently, it is expected that the optical properties of the hybrid III-V/Si waveguide, made on a planarized Si rib waveguide, will not change much compared to optical properties of the original hybrid III-V/Si waveguide, with 220 nm deep trenches. Therefore, the fundamental optical mode profiles of both hybrid waveguides should be similar, with the confinement factor values within the specified ranges: $\Gamma_{MQW} > 3$ % and $\Gamma_{Si} > 70$ %. To verify this, Γ_{MQW} and Γ_{Si} were calculated for the hybrid III-V/Si structure based on the planarized Si rib waveguide, as illustrated in Figure 3.12, and compared to the standard structure, with 220 nm deep trenches, filled with a DVS-BCB (as illustrated in Figure 3.1). The same, previously optimized, values of geometrical parameters W, t_{spc}, t_{SCH} were used for both types of waveguides. Also, a mesa wing section width of 8 μm was used in both cases. The results of the simulations are summarized in the Table 3.5.

The bonding layer thickness t_{BCB}(nm)	Γ_{MQW}		Γ_{Si}	
	the original waveguide	the planarized waveguide	the original waveguide	the planarized waveguide
20	3.18492 %	3.16849 %	75.98290 %	73.47933 %
30	3.29087 %	3.23870 %	76.12054 %	73.67326 %
40	3.34127 %	3.33093 %	76.31841 %	73.73283 %
50	3.37142 %	3.38761 %	76.47540 %	73.75239 %
60	3.39272 %	3.40189 %	76.65305 %	73.80853 %
70	3.39062 %	3.45682 %	76.85246 %	73.77518 %
80	3.37482 %	3.46487 %	77.08731 %	73.72091 %
90	3.35484 %	3.49937 %	77.32971 %	73.60805 %
100	3.33197 %	3.57578 %	77.58729 %	73.35511 %
110	3.30917 %	3.61124 %	77.78804 %	72.96054 %
120	3.31291 %	3.75022 %	77.83316 %	72.06963 %

Table 3.5: Comparison of the confinement factors Γ_{MQW} and Γ_{Si} of the fundamental optical modes in the original hybrid III-V/Si waveguide (with 220 nm deep trenches) and the hybrid III-V/Si waveguide made on a planarized Si rib waveguide (with SiO_2-'filled' trenches). The geometrical parameters for both hybrid waveguides are the same: $W_w = 8$ μm, $t_{spc} = 240$ nm, $t_{SCH} = 325$ nm.

Obviously, the difference in the fundamental optical modes of the standard

and the planarized waveguides is relatively small for variations in the BCB bonding layer thickness (t_{BCB}) between 20 nm and 120 nm. While Γ_{Si} is, on average, around 3 % less in the case of the planarized waveguide compared to the standard one, the confinement factor Γ_{MQW} is slightly higher for the planarized waveguide structure. However, the most important conclusion is that in both cases, the confinement factors show very small variations for the value of t_{BCB} changing from 20 nm to 120 nm. Therefore, the fundamental mode profiles are stable in both cases and also both confinement factors meet the targeted values: $\Gamma_{MQW} > 3$ % and $\Gamma_{Si} > 70$ %. Consequently, both waveguide structures can be used with the same optimized geometrical waveguide parameters.

3.3 Optimization of the design parameters using thermal simulations

Thermal properties of the hybrid III-V/Si lasers were studied using a two-dimensional finite element solver from COMSOL Multiphysics® engineering simulation software. In all the simulations, radiation and convection were considered negligible and conduction was treated as the only way of heat transfer. Therefore, the only equation to be solved is Fourier's law of thermal conduction:

$$\vec{q} = -k\nabla T \tag{3.3}$$

$$\nabla \cdot \vec{q} = \begin{cases} Q, & \text{within the heat source} \\ 0, & \text{outside the heat source} \end{cases} \tag{3.4}$$

where $\vec{q}$ is the local heat flux density (in W/m^2), k is the thermal conductivity of the material (W/m·K), ∇T is the temperature gradient (K/m) and Q is the local heat generation (W/m^3). In addition to this, there are boundary conditions at the heat sinks (Dirichlet condition of constant temperature, T = const) and the edges of the structure (the component of $\vec{q}$ normal to the surface is equal to zero, $q_{norm} = 0$). The cross-section of the device was defined in the simulation software, as illustrated in Figure 3.13. The heat sink was located at the bottom of the structure and set at the constant ambient temperature $T_0 = 20$ °C. No heat flow was allowed on the other outer boundaries of the structure ($q_{norm} = 0$). The simulated domain was 80 μm wide and the Si substrate was 20 μm deep (terminated with the heat sink) in order to more realistically simulate the heat flow through the structure. A too narrow domain, with the restrictive boundary conditions ($q_{norm} = 0$) would result in unrealistic temperature distribution across the device cross-section.

The most important parameter we are interested in is the thermal resistance (or thermal impedance) R_{th} of the device, which is proportional to the increase

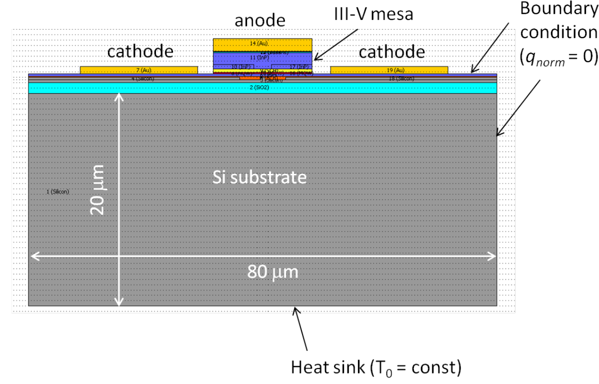


Figure 3.13: Cross-section of the hybrid III-V/Si laser defined in COMSOL® software for thermal simulations.

in the device temperature T_{dev} over the ambient temperature T_0 when a heat flux P_{heat} is generated in the device. The thermal resistance is defined as the ratio of this temperature increase and the generated heat flux P_{heat} :

$$R_{th} = \frac{T_{dev} - T_0}{P_{heat}} \quad [\mathrm{K/W}] \tag{3.5}$$

The design goal is to have the thermal resistance as low as possible. Higher values of R_{th} lead to a larger increase in the device temperature for a given dissipated power, which lowers the optical output power P_{out} and increases the threshold current I_{th} of the laser. Therefore, thermal simulations were used to estimate the thermal resistance of the hybrid III-V/Si laser and the impact of specific design parameters on its value. Two types of simulations that were performed are described in the following subsections.

3.3.1 Thermal simulations with a concentrated heat source

In the first set of simulations, we assumed that all the heat is generated within the central section of the MQW region, as illustrated in Figure 3.10. The width of this section is equal to the width of the conductive channel W_{ch} and taken to be 3 μm. Therefore, the MQW region was divided into three sections and the heat source was placed in the central section, above the Si rib waveguide, as illustrated in Figure 3.14a. This simplified model places all the generated heat in the active diode region of the device. A similar modelling approach was used by researchers from UCSB [7]. The idea was to use such a simple model to quickly assess the impact of some of the device design parameters on the thermal resistance. Most importantly, we wanted to assess the impact of the

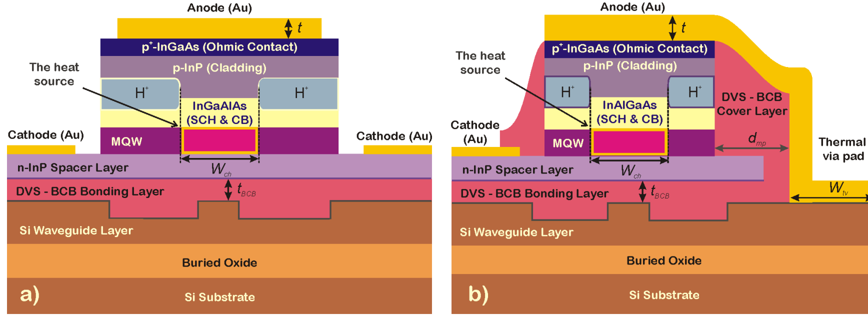


Figure 3.14: Cross-sections of the simulated hybrid III-V/Si laser structures: a) a standard structure without a thermal via; b) a structure with a thermal via on one side connecting the anode and the silicon layer.

mesa width (or equivalently, mesa wing section width W_w) and the DVS-BCB bonding layer thickness on the thermal resistance.

Anticipating a relatively high value of R_{th} due to a low thermal conductivity of the DVS-BCB, another device structure including a metallic thermal via was also modeled. The cross-section of this structure is presented in Figure 3.14b. Unlike the standard hybrid III-V/Si laser, this structure has a metallic thermal via connecting the anode on top of the III-V mesa, and a thermal via pad positioned on the silicon waveguide layer of the SOI substrate. Beside the thickness of the bonding layer t_{BCB} and the width of the mesa wing section W_w, additional design parameters in this structure, as illustrated in Figure 3.14, are thickness of the thermal via t (which is considered to be equal both at the anode and at the thermal via pad), distance between the III-V mesa and the thermal via pad d_{mp} as well as the thermal via pad width W_{tv}. In both cases of the device with and without thermal via, the other design parameters had the optimized values, as defined in Table 3.1 and in section 3.2.2.

Thermal conductivities of the materials used in the simulations are presented in Table 3.6. Thermal conductivities of the quaternary layers (InAlGaAs) were calculated using the formula for quaternary alloys [18]. Instead of modeling the individual InAlGaAs layers, the SCH and the carrier blocking layers were grouped into one layer, while the quantum wells and barriers were grouped into another layer representing the whole MQW region. The average thermal conductivities were calculated for such grouped regions and used in simulations. The heat source, located within a 3 μm wide central section of the MQW region was chosen to provide a heat flux density of q_{heat} = 10 kW/cm^2. Therefore, we defined an area-specific thermal resistance $R"_{th}$ as the ratio between the temperature increase of the device and the heat flux density q_{heat}:

Material	Thermal conductivity k (W/m·K)	Electrical conductivity σ (S/m)
Silicon	130	1×10^{-12}
SiO_2	1.24	1×10^{-14}
DVS-BCB	0.3	1×10^{-17}
InP-intrinsic	68	1.16×10^{-6}
InP (spacer layer)	68	6.72×10^{4}
InP (top cladding)	68	3.2×10^{3}
InGaAs	5	3.2×10^{4}
InAlGaAs (SCH & CB)	11.1	650
InAlGaAs (MQW)	7.2	650
Au	320	4.52×10^{7}
Ti	22	7.407×10^{5}

Table 3.6: Thermal and electrical conductivities of the materials used in the thermal simulations.

$$R"_{th} = \frac{T_{max} - T_0}{q_{heat}} \quad [\mathrm{K} \cdot \mathrm{cm}^2/\mathrm{kW}] \tag{3.6}$$

where T_{max} is the maximum device temperature and T_0 is the ambient temperature, i.e. temperature of the heat sink (T_0 = 293.15 K). Such a defined value $R"_{th}$ represents a thermal resistance of the device, normalized per unit area of the surface normal to the heat flow.

Initially, we simulated the standard, hybrid III-V/Si structure, without the thermal via, as illustrated in Figure 3.14a. The temperature distribution plot for this structure is shown in Figure 3.15a. The thickness of the BCB bonding layer t_{BCB} was varied between 40 nm and 200 nm and the thickness of the anode t was 200 nm. The anode metalization, beside the gold layer with the thickness t that was a variable parameter, also included a 40 nm thick layer of titanium, located between the ohmic contact (InGaAs) and the gold layer of the anode. The distance between the III-V mesa and the cathodes (on the both side of the mesa) was 3 μm.

The results, for three different mesa wing section widths of 3 μm, 5 μm and 8 μm are presented in Figure 3.16a. As expected, the increase in the mesa width significantly reduces the specific thermal resistance. On the other other hand, additional simulations showed that the increase in the anode thickness to 1.5 μm, reduces $R"_{th}$ by less than 5 %. Therefore, in a standard structure withouth a thermal via, the width of the III-V mesa is the most important parameter affecting the device thermal resistance.

Similar simulations were performed for the structure with the thermal via, as illustrated in the Figure 3.14b. The temperature distribution plot for this structure is shown in Figure 3.15b. In this case, we fixed the following simulation

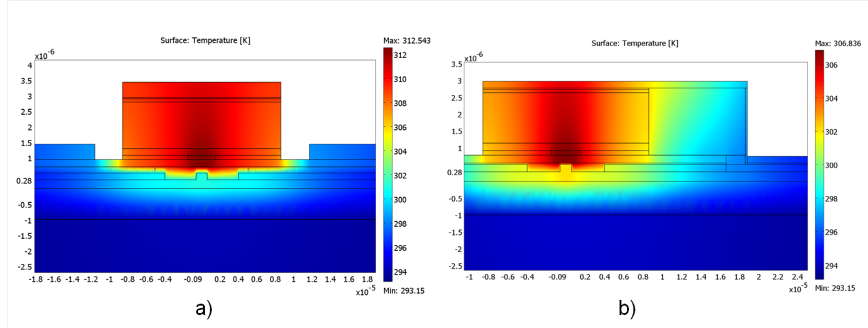


Figure 3.15: Temperature distribution in the hybrid III-V laser structures. Two simulated cases: a) the standard structure without a thermal via; b) the structure with a thermal via. In order to illustrate the temperature distribution details, only a fraction of the computational domain is presented in the plots above.

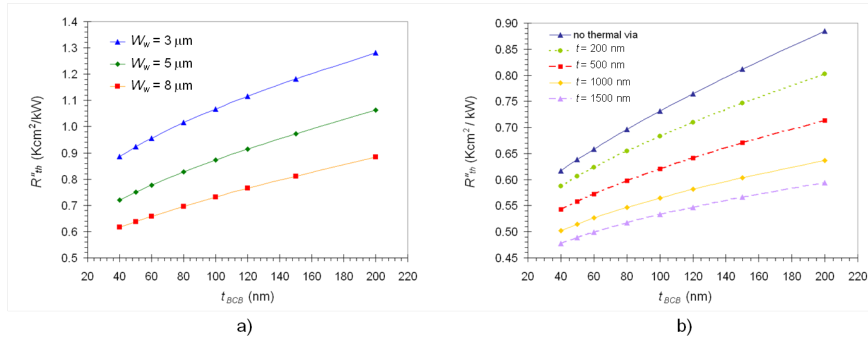


Figure 3.16: Simulated specific thermal resistance R''_{th} of the hybrid III-V/Si lasers based on: a) the standard structure without a thermal via, for three different values of the mesa wing section width W_w = 3, 5 and 8 μm; b) the structure with a thermal via, with four different thicknesses of the metallic via t = 200, 500, 1000 and 1500 nm.

parameters: W_w = 8 μm, d_{mp} = 10 μm and W_{tv} = 10 μm. The thickness of the BCB bonding layer t_{BCB} was again varied between 40 nm and 200 nm, the simulations were performed for four different thicknesses of the anode (i.e. thermal via) t = 200 nm, 500 nm, 1000 nm and 1500 nm, and compared to the results in the case when there is no thermal via. The results of these simulations are presented in Figure 3.16b.

As expected, the presence of thermal via reduces the specific thermal impedance of the device. Even a thermal via that is only 200 nm thick re-

duces $R"_{th}$ by around 10 %. In this case, however, the impact of the thermal via thickness t on $R"_{th}$ is much stronger. The increase in thermal via thickness t from 200 nm to 1.5 μm, reduces $R"_{th}$ by 20 % to 25 %. On the other hand, the additional simulations showed that the impact of the parameters d_{mp} and W_{tv} on $R"_{th}$ is much smaller. This is not surprising given the very high thermal conductivity of gold.

The thermal simulations with a concentrated heat source showed that the design parameter with the greatest impact on the thermal resistance of the device is the mesa width (W_m), in our case the mesa wing section width (W_w) which we directly varied. Also, the presence of the thermal via can significantly reduce the device thermal resistance, although it also involves additional fabrication complexity which is not discussed here.

3.3.2 Thermal simulations with a distributed heat dissipation

In the next round of thermal simulations we have adopted a more realistic model, based on Joule's heating of the device, due to the current flow. Therefore, instead of having a concentrated heat source, the heat generation was distributed throughout the whole structure, based also on its electrical properties. For these simulations, we also used COMSOL Multiphysics® simulation software with two modules: heat transfer by conduction and conductive media DC. In this approach, distribution of the DC currents within a structure is initially solved, based on the electrical conductivities and the voltage applied to the structure. Following this, the heat generation and the final temperature distribution within the structure is solved. Both the electrical and the thermal conductivities of the materials were considered as constants, not temperature dependent. Additionally, this model did not include modeling of the p-n junction and the diode-like electrical characteristic of the structure.

The cross-section of the hybrid III-V/Si laser defined in the simulation software is presented in Figure 3.17. It is similar to the one shown in Figure 3.14a, but with several differences. The thickness of the gold metalization layer in the cathodes was 700 nm, while in the anode it was 1.2 μm. These values are much closer to the real metalization layers after device fabrication. Also, the thickness of the gold layer in the anode is dictated by the conditions of a proton implantation, which will be discussed in section 3.4. The width of the cathode gold layers was 20 μm, while the width of the anode gold metalization layer was set to be equal to the III-V mesa width W_m. The distance between the III-V mesa and the cathodes was 3 μm. As in the previous simulations, a 40 nm thick layer of titanium was located between the ohmic contact layer of p^+-InGaAs and the gold contact layer of the anode. The regions with the proton implants were simulated as rectangular areas of 400 nm thickness and a sufficient width to provide

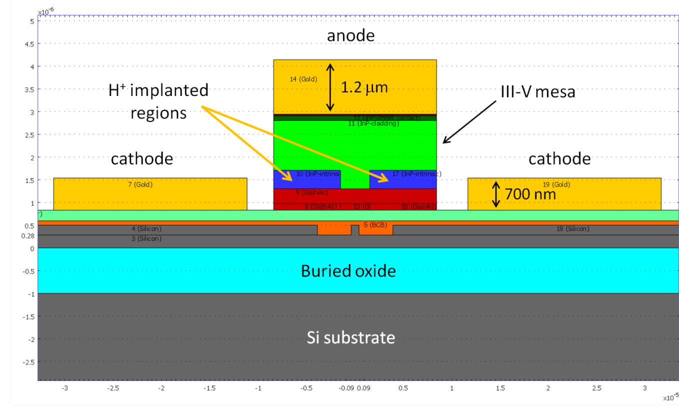


Figure 3.17: Cross-section of the hybrid III-V/Si laser defined in COMSOL® software for thermal simulations with Joule heating.

a 3 μm wide carrier injection channel in the centre of the III-V mesa. These regions were placed at the bottom of the InP cladding layer. The electrical conductivity of these regions was set to be equal to the conductivity of intrinsic InP. This very simple model of the implanted regions was based on the simulation results that will be presented in the following section. The values of the electrical and thermal conductivities of the materials used in these simulations are presented in Table 3.6. The computational window for the simulations was the same as in the previous simulations: 80 μm wide and > 20 μm high (larger than presented in Figure 3.17).

The basic goal of the thermal simulations with the Joule resistive heating, was to choose the optimal value of the III-V mesa width W_m. In order to link these results to our optical simulations presented in section 3.2, instead of directly sweeping the mesa width W_m, we have varied the mesa wing section width W_w. The relation between these two parameters is: $W_m = 2W_w + W$, where W = 800 nm is the Si rib waveguide width. The mesa wing section width W_w was varied between 4 μm and 18 μm. As in the previous simulations, the heat sink was located at the bottom of the 20 μm thick silicon substrate and its temperature was set to T_0 = 293.15 K (20 °C). The voltage between the anode and the cathodes was set at 1 V.

In this case, we calculated the total heat flux per unit length of the device P'_{heat}, flowing down from the III-V layers towards the SOI substrate. Similarly as before, in this case we defined a length-specific thermal resistance R'_{th} as the ratio of the temperature increase of the device and the heat flux per unit length P'_{heat}:

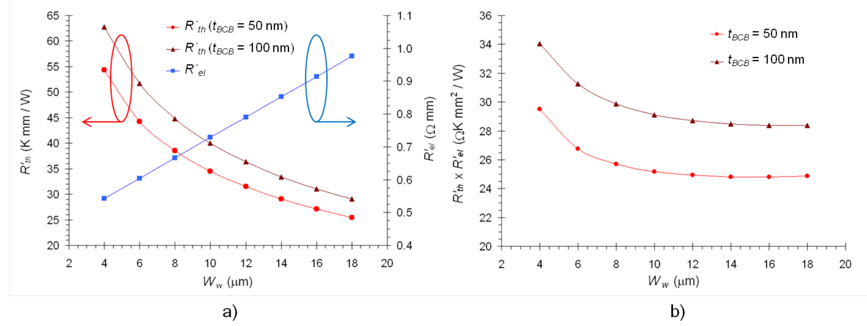


Figure 3.18: The results of the simulations based on Joule heating. The impact of mesa wing section width W_w on: a) the specific electrical resistance (R'_{el}) and the specific thermal resistance R'_{th}, for two values t_{BCB}; b) the product $R'_{th} \times R'_{el}$, for t_{BCB} = 50 nm and t_{BCB} = 100 nm.

$$R'_{th} = \frac{T_{max} - T_0}{P'_{heat}} \quad [\text{K} \cdot \text{mm/W}] \tag{3.7}$$

where T_{max} is the maximum device temperature and T_0 is temperature of the heat sink (T_0 = 293.15 K). Therefore, R'_{th} is a thermal resistance normalized per unit length of the device. In a similar way, the specific electrical resistance R'_{el} was defined as the ratio of the voltage between the anode and the cathodes V and the total electrical current per unit length I' flowing between these electrodes:

$$R'_{el} = \frac{V}{I'} \quad [\Omega\cdot\text{mm}] \tag{3.8}$$

Thermal simulations with Joule heating were carried out for two different bonding layer thicknesses t_{BCB} of 50 nm and 100 nm. Based on these simulations, the specific thermal and electrical resistances (R'_{th} and R'_{el}) were calculated, using the Equations 3.7 and 3.8. The results are presented in Figure 3.18a. As expected, thermal resistance R'_{th} decreases with the increase of W_w. However, the increase in mesa width also increases the length that carriers (mostly electrons) need to travel through a relatively thin (t_{spc} = 240 nm), n-type InP spacer layer. This increases the electrical resistance of the structure and consequently the heat dissipation. As the electrical conductance of the DVS-BCB bonding layer is negligible, the specific electrical resistances R'_{el} for the different bonding layer thickness (t_{BCB} = 50 nm or 100 nm) are practically the same.

As the increase in W_w has an opposite effect on the specific resistances R'_{th} and R'_{el}, there must be an optimum value of W_w which insures the best device performance and avoids the adverse impacts of either a very high thermal resis-

tance which occurs when the III-V mesa is too narrow or a very high electrical resistance which occurs when the III-V mesa is too wide. To find this value, we can perform a quick analysis. According to Equation 3.5, the increase in device temperature is proportional to its thermal impedance per unit length R'_{th} and the dissipated heat per unit length P'_{heat}. On the other hand, the dissipated heat P'_{heat} is proportional to electrical power dissipation per unit length of the device P'_{el}. Furthermore, using Equation 3.8 we can write:

$$P'_{el} = V \cdot I' = R'_{el} \cdot I'^2 \tag{3.9}$$

According to Equations 3.5 and 3.9, for a given device current per unit length I', an increase in device temperature is proportional to the product of the specific thermal and the specific electrical resistances: T_{dev} - T_0 = $\Delta T \sim R'_{th} \times R'_{el}$. Therefore, we have observed the dependence of this product ($R'_{th} \times R'_{el}$) on the mesa wing section width W_w. This plot is presented in Figure 3.18b.

Qualitatively, in both cases (t_{BCB} = 50 nm or t_{BCB} = 100 nm) there is a relatively steep decrease in the product $R'_{th} \times R'_{el}$, for W_w between 4 μm and 8 μm after which both curves reach a sort of a saturation region for $W_w > 12$ μm. The absolute minimum of the $R'_{th} \times R'_{el}$ product is around 14 μm in the case of 50 nm DVS-BCB layer, while in the case of t_{BCB} = 100 nm it is around 18 μm. Based on these results, and anticipating the bonding layers closer to 50 nm, than to 100 nm, we may conclude that it is best to have the mesa wing section width around 14 μm (corresponding to W_m = 28.8 μm).

However, temperature dependence of both the electrical conductivity (σ) and the thermal conductivity (k) of the materials was not taken into account. Both values decrease with the increasing temperature of the device. Also, the voltage drop and heat dissipation due to p-n junction were not taken into account. Considering this, it is safe to assume that the optimal value for W_w is less than 14 μm and most probably in the range between 8 μm and 14 μm, corresponding to the total III-V mesa width between W_m = 16.8 μm and W_m = 28.8 μm.

3.4 Optimization of the carrier injection

3.4.1 Proton implantation into the III-V mesa

The use of proton implantation to confine the injection of the carriers into the central region of III-V mesa was already mentioned in section 3.1 and the significance of this fabrication step was explained in section 3.2.4. In this section we will present more design details related to this processing step.

The use of ion implantation for the creation of highly resistive layers in III-V semiconductors is a well-know technique that has been used for more than

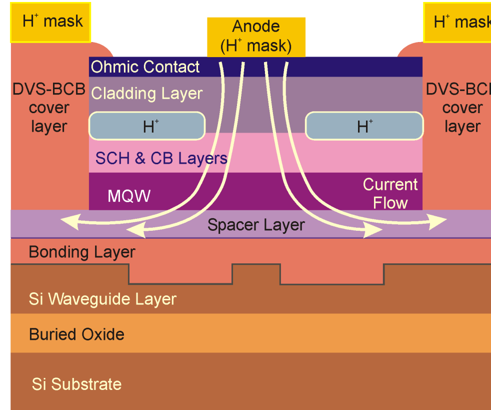


Figure 3.19: Confinement of the injected carriers via proton implantation in the lateral sections of the III-V mesa. The p-type metalization on top of the structure acts as a mask during the proton implantation.

two decades in III-V semiconductor device processing [19]. The basic principle for reducing the electric conductivity of the doped semiconductors is creation of spatially localized energy levels within the bandgap (so called, deep-level states) that efficiently trap free carriers - electrons form the conduction band or holes from the valence band. In general, this can be achieved in two ways. The first method is based on the implantation of ions which either by itself, or in combination with impurities or dopants already present in the semiconductor, create active deep-level energy states. The second method which is more commonly used, employs ion bombardment by neutral species like H, B or O to create damage-related deep levels in the targeted semiconductor. In this case, the damage to the crystal lattice is induced by the collisions of the incoming ions with the semiconductor atoms. This damage mostly comprises defects like vacancies, displaced atoms and dislocations, which eventually reduce the carrier mobility in the semiconductor and create deep-level trap centers which reduce the concentration of the free carriers. Most importantly, these deep-level centers are not thermally ionized at the device operating temperatures. However, this lattice damage can be eliminated by thermal annealing at higher temperatures and the effects of the implantation can be eliminated in this way. Therefore, in order to achieve the lasting effects of the ion implantation, it is important, in subsequent processing, not to expose the treated semiconductor to temperatures high enough to cause the annealing.

In our case, we chose proton (H^+) implantation to electrically passivate lateral regions of the III-V mesa and confine the carrier flow to the central section of the MQW region, as illustrated in Figure 3.19. The use of proton implanta-

tion in laser fabrication for the purpose of achieving carrier confinement while maintaining a relatively large III-V mesa which improves device thermal characteristics, was already reported by various authors [5, 17, 20]. Another advantage of using light ions, like H^+, is that they can penetrate deeper into the target, compared to heavy ions, like Fe^+. That means that the highly resistive region can be formed deeper into the III-V mesa, closer to the MQW region. From the practical aspect, the most important parameters in any ion implantation are the energy of the ions E, which determines how deep the implanted ions will penetrate into the III-V material and the dose or fluence of the ions Φ, which is the total number of ions implanted per unit area of the surface of the targeted material.

To determine the appropriate energy of the protons, one must consider both desired and undesired consequences of the implantation process. In the case of our hybrid III-V/Si laser structure, inducing damage to the lattice and creation of the deep-level trap centers is desirable in the cladding layer (p-type InP) and the SCH layer (InAlGaAs). On the other hand it is essential not to inflict any damage to the underlying quantum well layers as this would change their bandgap structure and consequently their desired optical and electrical properties.

After losing all of their kinetic energy in collisions with the atoms (and the bound electrons) of the semiconductor material, the protons are eventually stopped and stay implanted within the targeted material. The implanted ion profile $C(x)$, i.e. the distribution of the implanted ion concentration along the axis x, perpendicular to the surface of the targeted semiconductor material is commonly used to characterize a certain implantation process. The total ion dose Φ can be calculated by integrating the distribution $C(x)$ over the depth of the material:

$$\Phi = \int_0^{+\infty} C(x)\mathrm{d}x \tag{3.10}$$

One of the most important parameters of the implantation process is the projected range R_p of the implants, which can be calculated using the following expression:

$$R_p = \frac{1}{\Phi}\int_0^{+\infty} x \cdot C(x)\mathrm{d}x \tag{3.11}$$

It represents that average penetration depth of the implanted ion. Standard deviation of the projected range, designated as ΔR_p, and defined as:

$$\Delta R_p = \sqrt{\frac{1}{\Phi}\int_0^{+\infty} (x - R_p)^2 \cdot C(x)\mathrm{d}x} \tag{3.12}$$

is called *longitudinal straggle* (or sometimes, only straggle). Beside the projected range and the straggle, the third-order and the fourth-order moments of the distribution curve $C(x)$, known respectively as *skewness* and *kurtosis*, are also used to describe the implanted ions profile. Skewness describes the asymmetry of the distribution $C(x)$ around the coordinate of the projected range ($x = R_p$), while kurtosis characterizes the contribution of the tail sections of the distribution curve.

In order to assess distribution of the implanted ions, based on their initial energy E, we have used simulation software SRIM (Stopping and Range of Ions in Matter), version 2008.04 [21]. The core part of this software tool is a program TRIM (Transport of Ions in Matter) which uses Monte Carlo simulation methods to calculate distribution of the implanted ions into a specified target. The calculation is based on the approximation of binary collisions (the influence of the neighboring atoms is neglected). The input parameters are the type and the energy of the implanted ions E, as well as the structure of the target (thickness of the layers and their chemical composition). The most important output parameters are distribution of the implanted ions $C(x)$ and the vacancies (i.e. the profile of the lattice damage) made by knocking out the atoms of the target material out of their sites in the lattice.

Using the software, a stack of III-V layers (and their compositions), comprising the III-V mesa is defined and the implantation of protons into this structure is simulated. In practice, in order to avoid the channeling effect, the protons are launched at an angle of 7° with respect to the direction perpendicular to the III-V surface. Therefore, we used the same angle of incidence in our simulations. To assess distribution of the implanted protons with a sufficiently good resolution, simulations with 100 000 protons were run for different energy values. The simulation results showed that the optimum energy of the protons is 185 keV. Distribution of the implanted protons with an initial energy of 185 keV is shown in Figure 3.20a. The depth of the targeted material, which is in our case the distance from the top surface of the III-V mesa (InGaAs ohmic contact layer) to the layers within the mesa is presented on the x-axis. The ratio of the implanted ion concentration (in atoms/cm^3) with respect to dose Φ (in atoms/cm^2) is plotted on the y-axis. As we can see from the plot, the projected H^+ range is 1.4 μm, which is 200 nm above the boundary between the InP cladding layer and the InAlGaAs SCH layer. The calculated straggle, ΔR_p, is 178.8 nm.

As mentioned earlier, the idea is to make the lower regions of the InP cladding layer electrically insulating, while not damaging the MQW region of the mesa. Therefore, the SCH layer acts as a buffer layer where the remaining protons are stopped penetrating no further into the functional layers made of InAlGaAs. It should also be noted that from the aspect of making the semi-

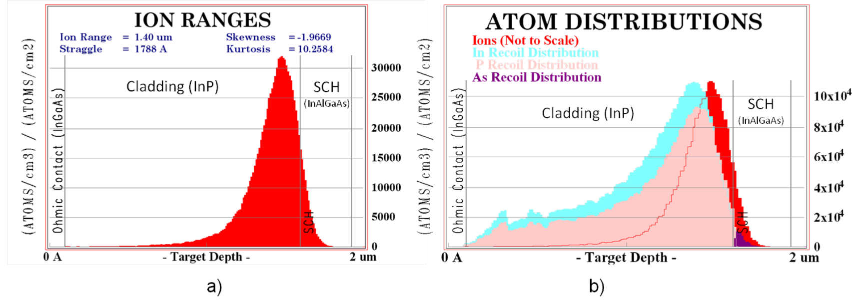


Figure 3.20: The results of SRIM simulations: a) distribution of the implanted protons (E = 185 keV) into the III-V layer stack. Projected range proton R_p of 1.4 μm is 200 nm above the boundary between the cladding and SCH layers; b) distribution of the recoiled In (cyan) and P atoms (light red) from the cladding layer and As atoms (purple) in the SCH layer, with the superimposed plot of the distribution of the implanted protons (red), with the initial energy of E = 185 keV.

conductor electrically more insulating, it is the distribution of the ion damage profile that is the most important, and not the profile of the implanted ions itself [19]. The ion damage profile is a distribution of the atoms that were knocked out of their sites in the lattice, creating vacancies. This is, the so called, recoil distribution. The peak of the damage profile generally occurs at the depth of $0.7 \cdot R_p$ to $0.8 \cdot R_p$, with a standard deviation usually around $0.75 \cdot \Delta R_p$. The distribution of the recoiled In and P atoms in the cladding layer, and the recoiled As atoms in the SCH layer, caused by the implantation of 185 keV protons (at 7° incidence angle) is shown in Figure 3.20b. The original distribution of the implanted protons (also shown in Figure 3.20a) is superimposed on this plot.

These simulation results show that virtually no damage is inflicted to the InAlGaAs layers laying below the SCH layer, which is a guarantee that the functional layers of MQW region will not be affected by the proton implantation. In addition, the damage to the SCH layer, which is also made of InAlGaAs is minimal, compared to the damage to the cladding layer. The recoil distributions of In, Al and Ga atoms in the SCH layer have even smaller peaks compared to As recoil distribution shown in Figure 3.20b. As intended, the bulk of the ion damage is concentrated in the lower section of the InP cladding layer, with the In and P recoil peaks, just within 100 nm from the peak of the proton distribution.

Determining the proper dose of the implanted protons is less straightforward. According to the tests performed by Boudinov *et al.* [22], there is a certain threshold value for the proton dose required to induce electrical insulation of p-type or n-type InP. In their tests, p-type InP samples (doped with Zn) were used, with the carrier (i.e. hole) concentration of $p = 1.9 \times 10^{17}$ cm^{-3}. The samples

were exposed to different proton implantation doses and the measurement results showed a steep increase in the sheet resistance of the samples for doses of 2.8×10^{13} cm^2 and higher [22]. Further increase in the dose, up to 10^{15} cm^2 did not result in an increase of the sample resistance. On the other hand, for the proton doses of 1×10^{13} cm^2 and lower, the sheet resistance of the samples was almost four order of magnitude lower.

In our case, concentration of the holes in the p-type InP cladding layer (which is approximately equal to the concentration of the acceptor ions) is p $\approx 1 \times 10^{18}$ cm^{-3}, which is almost five times higher than the hole concentration in the samples tested by Boudinov *et al* [22]. Therefore, it can be expected that the dose threshold value for our p-type InP layer is five times higher than the threshold value of $\Phi_{th} = 2.8 \times 10^{13}$ cm^2 reported by Boudinov *et al* [22]. According to this, the threshold dose in our case should be $\Phi_{th} = 1.4 \times 10^{14}$ cm^2. On the other hand, in the work of Getty on segmented ridge lasers [23], where proton implantation in p-type InP was used for electrical insulation, an optimum concentration of the implanted H^+ ions was reported to be in the range of 1-2 $\times 10^{18}$ cm^{-3}. In that work, this H^+ concentration was achieved using multiple proton implantations with the varying energies. However, we wanted to limit ourselves to a single exposure that would result in a sufficiently good carrier confinement. Based on the implanted proton distribution shown in Figure 3.20a, the minimum dose to achieve the H^+ concentration reported by Getty is in the range of 3.3-6.7 $\times 10^{13}$ cm^{-2}. Of course, this concentration is achieved only in the region (i.e. at the depth) around the peak value of H^+ distribution. To be sure that the concentration of the implanted H^+ ions is sufficiently high in a much broader region, a dose of 3.3×10^{14} cm^{-2} was chosen, which is an order of a magnitude higher. This chosen value is also higher than the threshold value of $\Phi_{th} = 1.4 \times 10^{14}$ cm^2, estimated based on the work of Boudinov *et al* [22]. Therefore, for electrical passivation of the lateral sections of the III-V mesa, we chose to perform a single proton implantation, with the energy of $E = 185$ keV and a dose of $\Phi = 3.3 \times 10^{14}$ cm^{-2}.

In order to prevent proton implantation in the central region of the mesa, an adequate mask had to be chosen that would absorb the incoming flux of protons during the exposure. As the p-type metalization had to be deposited onto the III-V mesa, it was a natural choice to use this metalization as a mask. Usually, the p-type metalization comprises a layer of titanium (~ 40 nm thickness) and on top of it a covering layer of gold, usually several hundreds of nanometers thick. Gold atoms, with a relative atomic mass of $A_r^{Au} = 196.97$, are much heavier than atoms of titanium ($A_r^{Ti} = 47.87$) and are therefore a better absorber of the incoming proton flux. Thus, it was decided to use gold as the mask and to choose the optimum thickness for this purpose which would be thermally

evaporated on top of the III-V mesa during the fabrication, as later described in Chapter 5. It is very important for the proton implantation mask to prevent any damage to the underlying ohmic contact layer. SRIM simulations showed that a 1.2 μm thick layer of gold can completely absorb protons of up to 200 keV energy. Consequently, this value was chosen as the thickness of the gold layer acting as a proton implantation mask.

The width of the central mask stripe that protects the central part of the III-V mesa was set at 3 μm. This is narrower than the 4 μm wide channel reported in papers of UCSB researchers [5, 17]. On the other hand, SRIM simulations showed that lateral straggle (ΔR_{pL}) for 185 keV protons is around 300 nm. From the ion implantation theory, it is known that the ion concentration in the region directly beneath the edge of a sufficiently long mask falls to 50% of the nominal ion concentration in the exposed region, far away from the mask edges. At a distance of 2.33 $\cdot\Delta R_{pL}$ from the mask edge (in the direction towards the mask), this concentration falls to 1% [19]. In our case, this range is 700 nm away from the mask edge. Therefore, if we adopt that the region with the implanted proton concentration less than 1% of the nominal value is virtually unaffected by the proton implantation, we can say that the width of the conductive channel created using a 3 μm wide mask is, at least, around 1.6 μm wide. In practice, the conductive channel is certainly wider and the current also spreads through the SCH layer before reaching the MQW region.

During the proton implantation, the entire sample is exposed to the proton flux. Therefore, the proton implantation mask needs also to protect the n-type InP spacer layer outside the III-V mesa. For that reason, the 1.2 μm thick gold layer is also deposited on both sides of the III-V mesa (as illustrated in Figure 3.19), which will be discussed in more detail in Chapter 5.

It should not be forgotten that the p-type InP layer remains electrically insulating as long it is not exposed to temperatures higher than 410 °C [23]. This temperature limit needs to be taken into account in the device fabrication, as we shall see in Chapter 5.

3.4.2 Lateral undercut etching of the III-V mesa

For an efficient injection of the carriers into the central region of the III-V mesa, another aspect of the proton implantation process needs to be taken into account. As mentioned in the previous section, the thick gold metalization used as a proton implantation mask needs to protect not only the central region of the III-V mesa, but also the n-type InP spacer layer, laying outside the III-V mesa. Ideally, the protective metalization should be deposited in such a way to expose the wing (lateral) sections of the III-V mesa and protect the InP spacer layer pro-

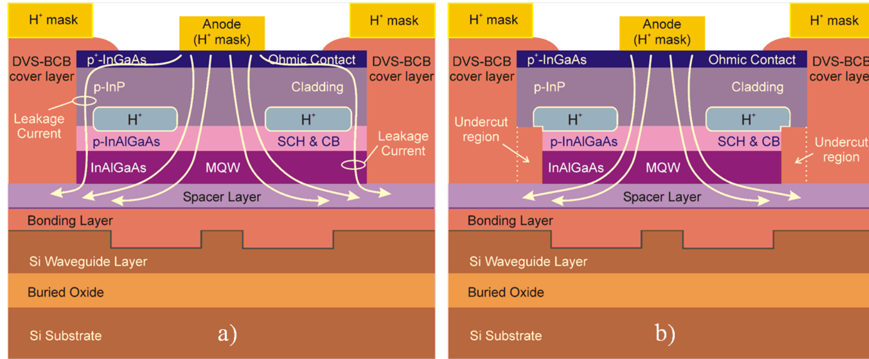


Figure 3.21: Lateral undercut etching of the III-V mesa: a) current leakage along the III-V mesa edges due to a proton implantation mask overlapping with the mesa near the edges; b) suppression of the leakage current via undercut wet etching of InAlGaAs layers of the III-V mesa.

truding outside the III-V mesa, as illustrated in Figure 3.19. However, in a real fabrication process, the III-V mesa and the p-type metalization serving as a proton implantation mask are defined in two separate lithographic processes. Consequently, if the p-type metalization mask is designed to exactly fit the width of the III-V mesa, it is quite possible that a misaligned p-type metalization (due to registration errors which are practically inevitable) partially covers one end of the III-V mesa, while exposing the InP spacer layer on the other side of the mesa.

Therefore, it is essential to design a p-type metalization mask in such a way to allow some tolerance to registration errors, which can be up to 1-2 μm in both directions. Practically, in the case of a perfect alignment, it will mean that the lateral p-type metalization is overlapping with the III-V mesa at both ends, as illustrated in the Figure 3.21a. In its turn, this means that at the both ends of the III-V mesa, there would be highly conductive regions (protected from the proton implantation), allowing a parasitic current flow, as illustrated in Figure 3.21a. This "leakage" current is not flowing through the central region of the III-V mesa and therefore, is not contributing to photon generation. To allow tolerance to registration errors, the width of these conduction channels near the edges of the mesa can be between 1 and 2 μm, which is comparable to the width of the conduction channel in the centre of the mesa. Therefore, it is essential, to somehow prevent or minimize the flow of this parasitic current.

The solution we propose is to perform controlled lateral undercut etching of the InAlGaAs-based layer at the edge of the III-V mesa. Controlled undercut etching, based on wet etching processes has already been studied in InGaAs and InGaAsP-based photonic structures [24]. Sufficiently high etch rates of InAlGaAs

layers used in our devices can be expected (order of magnitude of 1 μm/min), due to the absence of P atoms which significantly reduce the etch rates of InGaAsP layers [24]. Also, aqueous solutions of H_2SO_4 and H_2O_2 used for wet etching of these layers are very selective towards InP, which means that the InP-based layers (the spacer and the top cladding layers) would be virtually unaffected by this wet etching. By undercutting lateral sections of InAlGaAs layers in our hybrid III-V/Si laser, it is possible to effectively eliminate the conduction channels along the III-V mesa edges, as illustrated in Figure 3.21b.

3.5 Design of the distributed feedback (DFB) and phase-shifted DFB lasers

Beside designing Fabry-Perot lasers that usually exhibit several lasing longitudinal modes, it was essential to make a design for a single wavelength laser based on a distributed-feedback (DFB) provided by a Bragg grating. In principle, Bragg gratings are periodically repeating structures whose refractive indices change periodically along the direction of light propagation. While propagating along such a structure, reflection occurs at the interfaces of the regions with higher and lower effective refractive indices. Under a certain condition, called the Bragg condition, the back-reflecting waves will interfere constructively and the grating reflectance will reach its maximum value. For a grating with a period Λ and propagating light with the wavelength λ, the Bragg condition is given by the following expression:

$$2 \cdot \Lambda = m \cdot \lambda = m \frac{\lambda_0}{n_{eff}} \tag{3.13}$$

where n_{eff} is the effective refractive index of the propagating optical mode, λ_0 is the light wavelength in vacuum and m is a positive integer which represents the order of the grating. In the case of $m = 1$, we speak of a first-order grating, for $m = 2$, we have a second-order grating and so on. From the practical point of view, most of the time we deal only with first- or second-order gratings, as higher order gratings become very sensitive to variations in the duty cycle.

In the case of our hybrid evanescent III-V/Si lasers, we decided to make gratings in silicon, not the III-V materials. The reason for this is the fact that the first order grating for a 1310 nm wavelength, requires the grating period of $\Lambda \approx 200$ nm, which can be very challenging for fabrication in III-V materials. Silicon fabrication processes are more mature and stable and, working on a joint project with Intel, we had an opportunity to rely on the 193 nm UV lithography process in a commercial fab. On the other hand, in our university cleanroom we could process III-V materials using a 320 nm contact lithography.

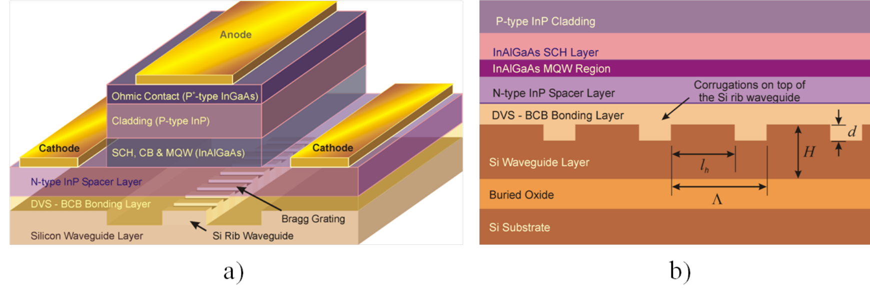


Figure 3.22: General layout of a hybrid III-V/Si laser with a Bragg grating: a) corrugations on top of the silicon rib waveguide; b) cross-section in the longitudinal plane, showing the details of the Bragg grating: the grating period Λ, the corrugation depth d, and the length of the unetched (high-refractive index) region l_h.

The easiest way for making a grating in the silicon rib waveguide is by making corrugations in it. Corrugations on the top of the grating are modulating the height of the rib waveguide, while sidewall corrugations modulate its width. Preliminary simulations showed that the most effective grating in silicon is the one with the corrugation made on top of the silicon rib waveguide, as depicted in Figure 3.22a. Such a grating is characterized by the etch depth of the corrugations made in silicon d and the duty cycle, which is defined as the ratio of the length of the unetched section l_h (with a higher effective index) of the Si rib waveguide and the grating period Λ, as illustrated in Figure 3.22b. Thickness of the silicon rib waveguide H is 500 nm, as mentioned in section 3.2.1.

The most important grating parameter is the coupling coefficient κ, which represents the optical field reflection of the grating per unit length (usually expressed in cm^{-1}). In the case of a square profile of the grating and using a small perturbation approximation, the coupling coefficient κ can be calculated using the expression:

$$\kappa = \frac{2\left(n_{eff}^{h} - n_{eff}^{l}\right)}{\lambda_0} \cdot \sin\left(m \cdot \pi \frac{l_h}{\Lambda}\right) \tag{3.14}$$

where n_{eff}^{h} and n_{eff}^{l} are effective refractive indices of the propagating optical mode in the unetched region (with a higher effective refractive index) and the etched region, respectively, while the ratio l_h/Λ represents the duty cycle of the grating. For a first-order grating, the maximum value of κ is achieved for a duty cycle of 50%, while for a second-order grating, the maxima occur for duty cycles of 25% and 75%.

The first step in designing an appropriate grating was to determine the ap-

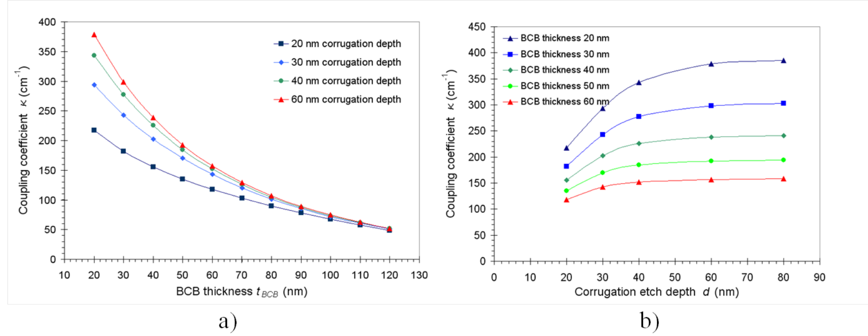


Figure 3.23: Impact of the thickness of the bonding layer t_{BCB} and corrugation depth d on the coupling coefficient κ of the first-order grating with a 50% duty cycle: a) κ vs. t_{BCB} plot; b) κ vs. d plot.

propriate corrugation depth d. Using a full-vectorial mode solver FIMMWAVE, it was possible to calculate the effective refractive indices n^h_{eff} and n^l_{eff} for the fundamental optical mode (at λ = 1310 nm) in the hybrid III-V/Si waveguide, as described in section 3.2.2. Based on these values and the previous Equation 3.14, the coupling coefficient κ was calculated for the first-order grating and 50% duty cycle, for several values of the corrugation depth d and the DVS-BCB bonding layer thickness t_{BCB} in the range between 20 nm and 120 nm. The results of these calculations are presented in Figure 3.23.

Even for a relatively shallow, 20 nm deep corrugations, the coupling coefficient is relatively high (> 150 cm^{-1}) for a bonding layer thickness t_{BCB} of 40 nm or less. Very high coupling coefficient values are not desired, as they imply relatively short grating lengths and consequently short devices in the case of distributed-feedback (DFB) lasers, which increases their thermal resistance and lowers the output optical power. Decreasing the coupling coefficient κ via increasing DVS-BCB thickness t_{BCB} is not a good option from the aspect of thermal properties of the device and its robustness with respect to fabrication tolerances, as explained in section 3.2.4. Therefore, in order to avoid very high values of κ, the best option is to keep the corrugation depth as low as possible.

However, the silicon fabrication capabilities are becoming a limiting factor in designing both the corrugation depth and the duty cycle of the first-order gratings. At the time of designing the Bragg gratings for a single wavelength laser, the minimum achievable corrugation depth in the silicon processing was limited between 20 nm and 30 nm (with the 30 nm process being a more stable one). Going below these values was not technologically feasible. Thus, we focused exclusively on these two corrugation depths of 20 nm and 30 nm.

The possibilities for variation of the duty cycle of the first-order grating were

also very limited. The fundamental hybrid optical mode at 1310 nm has an effective refractive index of $n_{eff} \approx 3.28$. The Bragg condition, given in the Equation 3.13, for the first-order grating ($m = 1$) results in a grating period of $\Lambda \approx 200$ nm. For a 50% duty cycle this translates into the width of the corrugation on top of the silicon waveguide of 100 nm (i.e. Λ - l_h = 100 nm). However, this value was at the very limit of the capabilities of the 193 nm UV lithography that was used for defining the corrugations. Control of the width of the corrugation and the duty cycle itself was not expected to be very good. Due to this constraint, we set the target value for the duty cycle of the first-order gratings to 50%.

In order to assess the length of the Bragg grating L that would provide sufficiently high reflection for the propagating optical mode, we have performed a series of 2-D simulations using CAMFR (CAvity Modeling FRamework) full-vectorial Maxwell solver tool. A layered structure, as presented in Table 3.3, was defined along the vertical (x-axis). The Bragg grating was simulated by stacking the high- and the low-refractive-index regions, alternatively, along the horizontal axis (z-axis). The high-refractive-index region had the full height of the silicon rib waveguide of $H = 500$ nm, while the low-refractive-index region had the height of $H-d$, where d is the corrugation depth. The grating length was increased by increasing the number of grating periods and the reflectance R of the fundamental mode was calculated. This value was used to estimate the product of the coupling coefficient κ and the grating length L, using the following relations:

$$R = \tanh^2(\kappa \cdot L) \quad \longrightarrow \quad \kappa \cdot L = \operatorname{artanh}(\sqrt{R}) \tag{3.15}$$

The simulations were performed for corrugation depths of $d = 20$ nm and $d = 30$ nm and grating lenghts up to 120 μm. The results are presented in Figure 3.24. As expected, the κL product is higher in the case of deeper corrugations and thinner bonding layers. In designing DFB lasers it is a common practice to keep the κL product between 1 and 3. Higher κL values lead to spatial hole burning and lower optical output. According to Equation 3.15, the values of κL product of 1, 1.5 and 3 correspond to reflectances of 58%, 82% and 99% respectively. Having this in mind, we see that even for relatively short grating lengths of less than 100 μm, the reflectances of the grating are still sufficiently high, both for 20 nm and 30 nm deep corrugations and DVS-BCB bonding layer thicknesses between 20 nm and 80 nm. For 30 nm deep corrugations, a grating length of only 40 μm provides a κL product value higher than 1, even for a bonding layer thickness of $t_{BCB} = 80$ nm. Consequently, we can conclude that the optimum grating length for the first-order 50% duty cycle Bragg gratings lays in the range between 40 μm and 100 μm.

As the fabrication of the first-order grating on top of a Si rib waveguide was challenging, we have focused more on the second-order grating. In this case,

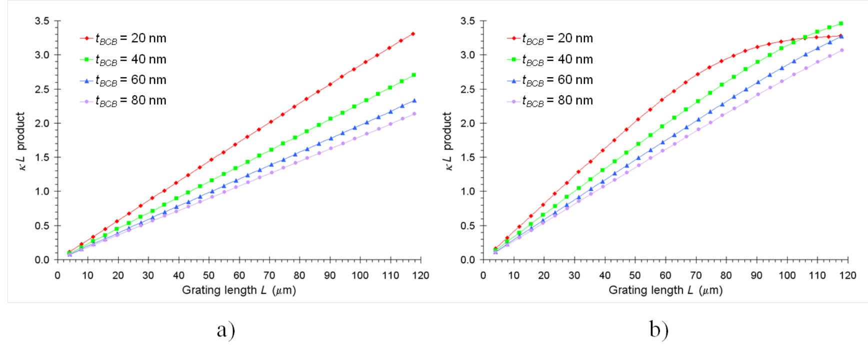
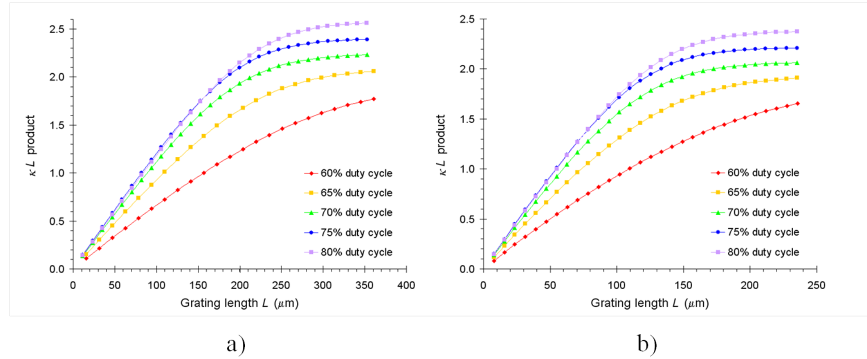


Figure 3.24: Plots of the κL product vs. grating length for the first-order grating with a 50% duty cycle and different thicknesses of the bonding layer t_{BCB} in the case of the corrugation depth of: a) d = 20 nm; b) d = 30 nm.

the grating period is doubled compared to the first-order grating, which in our case translated into Λ = 400 nm. However, since the maximum coupling coefficients are achieved for duty cycles of 25% and 75%, this means that the width of the unetched region (l_h, as shown in Figure 3.22b) in these cases should be either 100 nm or 300 nm. For l_h = 300 nm, the width of the corrugation is equal to $\Lambda - l_h$ = 100 nm, which means that for both 25% or 75% duty cycle the critical dimension of the corrugation features is 100 nm, which is still very critical from the aspect of a 193 nm UV lithography. From the fabrication point of view, the duty cycle of 75% was more favourable than the one of 25% (the tendency for overetching the corrugations was more prominent in wider corrugations). Therefore, we decided to focus on the duty cycles around 75%.

Using the CAMFR simulation tool, the product κL was calculated for the second-order gratings with duty cycles between 60% and 80%. Simulations were performed for both corrugation depths of d = 20 nm and d = 30 nm, while the BCB bonding layer thickness was fixed at t_{BCB} = 40 nm. The results are presented in Figure 3.25. As expected, the coupling coefficient κ is lower compared to the first-order gratings resulting in slightly lower κL values and longer grating lenghts required to achieve a specific κL value. In addition, for duty cycles less than 70%, radiation losses are not negligible (amounting to 10% for a duty cycle of 60%). Therefore, we have decided to set the targeted value for the duty cycle to 75%.

The simulations showed that the condition κL = 1 can be achieved with a grating length of only 80 μm for 30 nm deep corrugations. On the other hand, for the duty cycles around 75% it doesn't make much sense to have the gratings longer than 220 μm, as the κL product value is already above 2 and reaches



a) b)

Figure 3.25: Plots of the κL product vs. grating length for the second-order gratings with several different duty cycles and the the bonding layer thickness of t_{BCB} = 40 nm, in the case of the corrugation depth of: a) d = 20 nm; b) d = 30 nm.

saturation values. This κL product saturation, observed in plots in Figure 3.25 is actually a consequence of the losses in the waveguide and limitations of the coupled-mode theory which is used to derive the Equation 3.15 and which assumes relatively small refractive indices perturbation along the grating.

Additionally, 2-D CAMFR simulations were used to assess the reflection spectrum of the gratings and the impact of the DVS-BCB bonding layer thickness on it. In this case, both the first-order and the second-order gratings were defined with grating periods optimized to provide the maximum reflectance for the fundamental hybrid mode at 1310 nm, for a bonding layer thickness of t_{BCB} = 40 nm. For such a defined grating, the reflectance spectra were calculated for bonding layer thicknesses of t_{BCB} = 20 nm, 40 nm and 60 nm. The length of the gratings was fixed at 300 grating periods. The results of these simulations are summarized in Figure 3.26.

A shift in the reflectance spectrum with the change of the bonding layer thickness t_{BCB} is observed for both types of gratings. Qualitatively, thinner bonding layers result in a wider full-width at half maximum (FWHM) reflectance spectra, with a red-shift of the spectrum peak of several nanometers. On the other hand, in thicker bonding layers, blue-shifting and narrowing of FWHM is observed. However, the first-order grating provides wider FWHM values (between 7 and 8 nm) than the second-order gratings (around 4 nm). This makes them much more robust to variations in the bonding layer thickness compared to the second-order gratings. Based on the results presented in Figure 3.26, we can conclude that a second-order grating (optimized for the bonding layer thickness of t_{BCB} = 40 nm), with a bonding layer thicknesses of t_{BCB} = 20 nm and t_{BCB} = 60 nm at the opposite ends would have mismatched

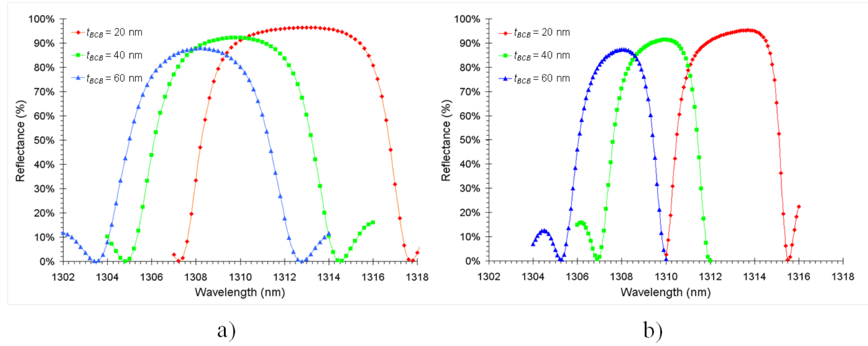


Figure 3.26: The impact of the bonding layer thickness on the reflectance spectra of the gratings: a) the first-order grating spectra; b) the second-order grating spectra. In both cases, the grating length is equal to 300 grating periods Λ.

reflectance spectra, unlike the first-order grating, which would still have a significant reflectance spectra overlap for the wavelengths between 1309 nm and 1310 nm.

From this perspective, the advantage of the first-order grating is obvious, as it can tolerate variations in the DVS-BCB bonding layer thickness of around 40 nm. On the other hand, in the case of the second-order gratings, variations in t_{BCB} should be kept within 20 nm.

Taking into account the previous considerations, two types of single wavelength hybrid III-V/Si laser designs are proposed. The first one, illustrated in Figure 3.27a is based on a standard DFB laser with an adjacent integrated photodetector, made from the same III-V epi layers as the hybrid laser itself. The laser diode and the photodetector share the same N-type spacer layer, and the functional layers made in InAlGaAs, but the highly doped cladding (InP) and ohmic contact (InGaAs) layers are etched away between the laser and the photodetector. In this way, the photodetector is electrically isolated from the laser and can be separately biased. At one end of the device, the facet is cleaved so that the emitted light can be coupled into an optical fiber or an external photodetector. On the other end, the light propagates into the photodetector, where the optical mode is absorbed, converting the optical signal into a photocurrent.

In the case of the first-order grating, a $\lambda/4$ phase-shift region is positioned in the centre of the grating in order to break the mode degeneracy and allow a single mode lasing at the Bragg wavelength, according to Equation 3.13 [25]. In the case of the second-order grating, there is no need for a $\lambda/4$ phase-shift region, as the radiation loss and the expected reflection from the cleaved (or polished)

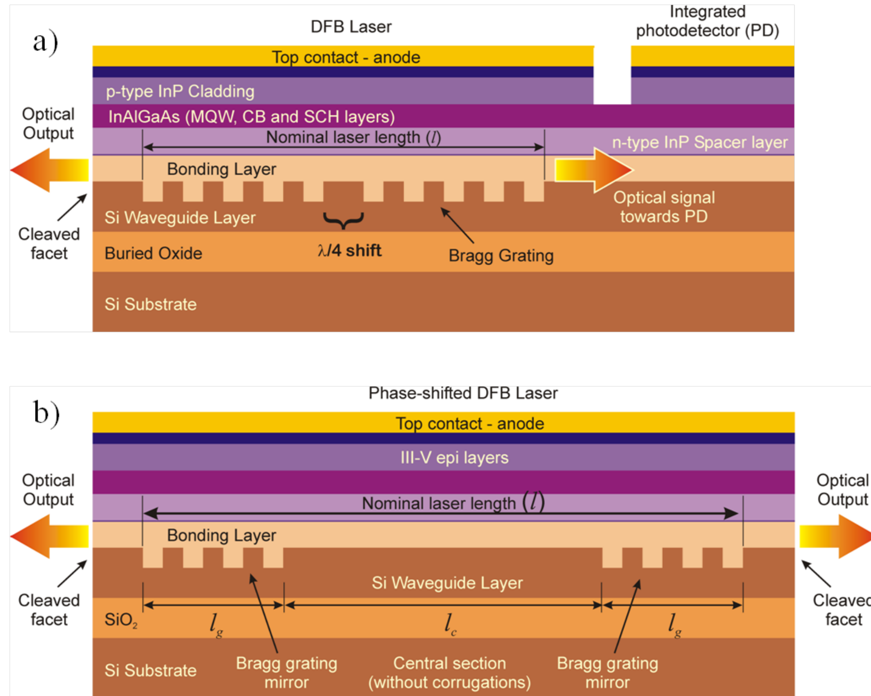


Figure 3.27: Longitudinal cross-sections of the two proposed types of hybrid III-V/Si DFB lasers: a) a standard DFB laser with a first-order grating and a $\lambda/4$ phase-shift region in the centre of the cavity, and with the adjacent integrated photodetector; b) a phase-shifted DFB laser with a central gain section without corrugations and the gratings at the both ends of the device.

facets break mode degeneracy and provide sufficient mode selectivity [26, 27]. Nominal length of the device is equal to the total length of the grating, although some optical signal amplification takes place outside of this region as the carriers are injected in the other sections of the device (e.g. between the cleaved facet and the end of the grating). This arrangement is required, as discontinuation in the metalization between the end of the grating and the cleaved (or diced and polished) facet would create a highly-absorbing region that would diminish the output optical signal.

The other type of proposed single wavelength device, illustrated in Figure 3.27b, is based on using Bragg gratings as distributed-feedback mirrors at the both ends of the device. The previously performed simulations indicate that both the first-order and the second-order gratings can provide sufficient feedback with a total grating lengths of no more than 200 μm to 250 μm. De-

vices with such a short lengths have higher thermal resistance and lower optical output. Previously reported evanescent hybrid III-V/Si lasers, had lengths of 700-800 μm for Fabry-Perot lasers [28], 600 μm for DBR lasers [29] and 340 μm in the case of DFB lasers [30]. Therefore, we propose longer devices which have Bragg gratings acting as mirrors at both ends and a central section, without corrugations, which acts as a pure gain section of the device. In this way, higher optical output and lower thermal resistance can be achieved even with a strongly reflecting grating. This type of device is acting as a phase-shifted DFB laser, and has already been described in the literature [31]. The nominal length of such a device (l) is the sum of the lengths of the grating sections (l_g) and the central gain section (l_c): $l = 2l_g + l_c$.

It is envisioned that individual hybrid lasers will be fabricated from a single III-V die bonded on the SOI chip. In this way, between 200 and 300 devices can be fabricated on a single SOI chip. These devices are organized in rows and columns. For the purpose of the characterization of the individual lasers, it is envisioned that the columns with the individual devices will be either cleaved or diced and subsequently polished. Therefore, we envision a phase-shifted DFB device with cleaved (or polished) facets at both ends, as illustrated in Figure 3.27b. Output optical signal can be detected at either facet.

In the case of DFB lasers with reflecting facets it is a better strategy to have a higher κL product (at least, $\kappa L \approx 3$) in order to achieve strong reflection within the grating and minimize the impact of the reflecting facets on the DFB laser [25]. Therefore, it was decided to make a lithographic mask for the SOI wafers with a set of the grating lengths that would achieve sufficiently high κL products even for 20 nm corrugations and thicker bonding layers.

For the standard DFB devices, the grating length was varied between 150 μm and 350 μm, for the first-order gratings and between 200 μm and 500 μm, for the second-order gratings. In the case of phase-shifted DFB devices, the grating lengths l_g were varied between 40 μm and 100 μm, for the first-order gratings, and between 80 μm and 220 μm, for the second-order gratings. The nominal length of the phase-shifted DFB lasers l (as well as the Fabry-Perot lasers), was varied between 500 μm and 900 μm.

3.6 Conclusions

Here, we will briefly summarize this chapter. An epitaxially grown structure with eight, compressively strained quantum wells based on InAlGaAs was chosen as an active medium for the 1310 nm hybrid III-V/Si laser based on evanescent coupling. To keep the fundamental optical mode confinement factors in the silicon waveguide (Γ_{Si}) and the quantum wells (Γ_{MQW}), above 70% and 3%, respectively, the optimum values were chosen for the following parameters: width

of the silicon rib waveguide W = 800 nm, thickness of the n-type InP spacer layer t_{spc} = 240 nm, thickness of the lightly p-doped (1×10^{17} cm^{-1}) InAlGaAs separate confinement heterostructure (SCH) layer t_{SCH} = 325 nm. With these design parameters, the required values of the confinement factors Γ_{Si} and Γ_{MQW} are also achieved on the SOI platform with planarized Si rib waveguides, where the trenches surrounding the rib waveguide are filled with SiO_2.

The results of the optical simulation suggest that the width of the III-V mesa W_m should be at least 12.8 μm, while the thermal simulations showed that the optimum value of W_m is between 16.8 μm and 28.8 μm. For the electric insulation of the lateral sections of the III-V mesa, a single proton implantation step is envisioned with an optimum H^+ ion energy of E = 185 keV and a dose of Φ = 3.3×10^{14} cm^{-2}. Lateral undercut etching is suggested for the suppression of the leakage current along the III-V mesa sidewalls.

Single wavelength hybrid III-V/Si laser designs are presented, based on the first-order and the second-order gratings, with grating periods of Λ^{1st} = 200 nm and Λ^{2nd} = 400 nm and targeted duty cycles of 50% and 75%, respectively. The grating designs are optimized for corrugation depths of 20 nm and 30 nm. Two types of single wavelength hybrid III-V/Si lasers are proposed: 1) an ordinary DFB device with an integrated photodetector and 2) a phase-shifted DFB device with the Bragg-mirrors at both ends and a central gain section without corrugations.

In all considerations, it turned out that the thickness of the DVS-BCB bonding layer t_{BCB} should be kept as small as possible and as uniform as possible. Beside negative impact on the thermal resistance of the device, thick bonding layers (~ 100 nm) make a device more sensitive to the fabrication tolerances of the Si rib waveguide and they also narrow the reflectance spectrum of the gratings. The second-order gratings are more sensitive to a bad bonding layer uniformity compared to the first-order gratings.

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4

DVS-BCB Bonding Procedure for Evanescently-Coupled Photonic Devices

Details of the machine-based DVS-BCB bonding procedure that yields sufficiently thin bonding layers, providing evanescent coupling between the silicon rib waveguide and the active layers made in III-V semiconductor materials will be presented in this chapter. This bonding procedure is a crucial step in the envisioned heterogeneous integration scheme and it also represents the first step in the fabrication of the hybrid III-V/Si laser.

Initially, after a general introduction to our heterogeneous integration scheme, we will focus on a die-to-die bonding procedure. Details of the bonding tool, the used materials and the experimental setup will be described. Afterwards, a typical DVS-BCB bonding procedure will be presented. Following this, we will focus on the details of the bonding experiments and the development of the bonding procedure. The results achieved in the bonding layer thickness, uniformity and the bonding strength will be presented. The observed problems will also be discussed. In the end, we will present the results of initial bonding tests with multiple die bonding, which is the first step in scaling-up the developed procedure to a multiple-die-to-wafer bonding process.

4.1 Heterogeneous integration via DVS-BCB bonding - an overview

In the first chapter we have already mentioned that the most promising, cost-effective heterogeneous integration of relatively expensive epitaxially-grown III-V semiconductor materials to SOI photonic circuits assumes bonding of individual, pre-diced III-V dies onto an SOI platform. In this way, a costly III-V material is used only at the locations within an SOI die (or a wafer) where it is really needed, avoiding unnecessary waste of material. Thus, our heterogeneous integration scheme assumes bonding of unprocessed III-V dies (with its functional layers facing down) on top of previously processed SOI waveguide circuits, as shown in Figure 4.1a. After the bonding, the III-V die is thinned down, usually by a combination of grinding (as illustrated in Figure 4.2a) and wet etching. In this way, an InP substrate (usually, around 370 μm thick) is completely removed, leaving only a thin film of functional III-V semiconductor layers bonded to the SOI substrate, as shown in Figure 4.2b.

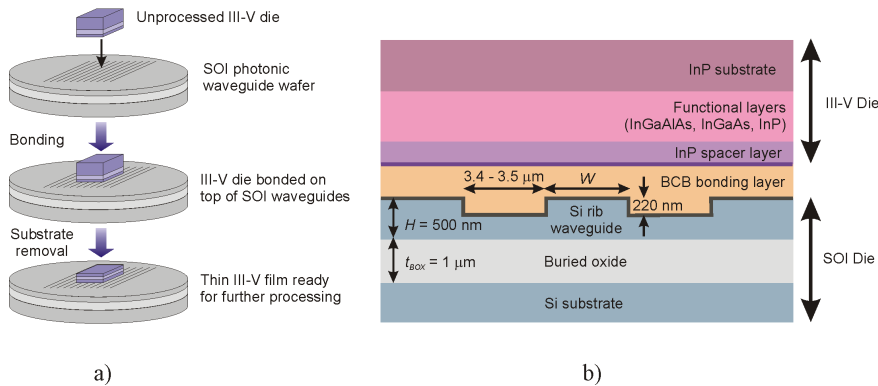

Figure 4.1: Heterogeneous integration of a III-V die on top of SOI waveguides based on adhesive bonding: a) Overall scheme of the heterogeneous integration comprising bonding and substrate removal; b) Cross-section of the silicon rib waveguide structure with a III-V die bonded on top of it.

Very precise bonding alignment is not required, as III-V films are processed after the bonding. More precisely, the hybrid III-V/Si laser is fabricated after the bonding using contact lithography in which the lithographic masks for the processing of III-V materials are aligned to the features on the SOI photonic circuit substrate. In this way, the III-V mesa and all metalization is defined exactly on top of the specified Si rib waveguide.

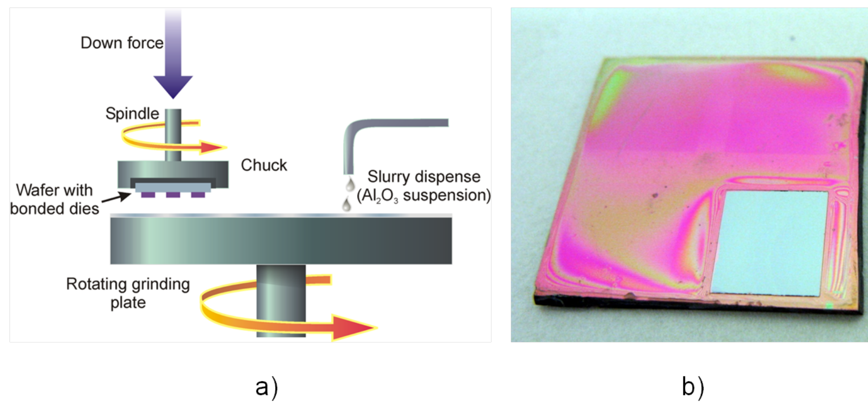

Figure 4.2: Post-bonding treatment of a III-V die: a) Mechanical grinding process used for removal of the InP substrate in the bonded III-V dies; b) After the substrate removal, a thin-film (~ 2.2 μm) comprising the III-V functional layers remains bonded to an SOI die. Interference fringes around the III-V die originate from a protective layer of photoresist film applied before the grinding.

As mentioned before, in section 2.6.1, the Photonics Research Group from Ghent University has performed pioneering work in the use of DVS-BCB as an adhesive for heterogeneous integration of III-V materials on an SOI platform. Photonic devices that were fabricated in this way included light-emitting diodes (LEDs) [1], InP/InGaAsP photodetectors [2], metal-semiconductor-metal (MSM) photodetectors based on evanescent coupling [3] and electrically pumped, hybrid InP/InGaAsP lasers on an SOI platform [4]. However, all these devices were based on a manual DVS-BCB bonding procedure, suitable for research and development, but not for an industrial cleanroom environment. Therefore, there was a need to develop a reliable and robust, machine-based DVS-BCB bonding process that would provide sufficiently thin bonding layers (< 100 nm), suitable for fabrication of evanescently-coupled photonic devices, such as hybrid III-V/Si lasers.

Due to the relatively high cost of the materials needed for the bonding, instead of performing multiple die-to-wafer bonding tests, we have initially focused on die-to-die bonding tests where a single III-V die is bonded on a single SOI die. These tests were used for the development of the DVS-BCB bonding procedure suitable for fabrication of evanescently-coupled photonic devices and will be discussed in more detail in the following section.

4.2 Die-to-die bonding - materials, tools and the experimental setup

4.2.1 Materials used in the bonding tests

In our die-to-die bonding tests, we used SOI dies with silicon rib waveguides as shown in Figure 4.1b. We had several SOI wafers with different rib waveguide layouts at our disposal. In the early bonding tests we used the design where the width of the waveguides W was 1.2 μm and the surrounding trenches were 3.4 μm wide. In the later tests, we used 0.8 μm wide Si rib waveguides, surrounded by 3.5 μm wide trenches. In both cases, the trenches were 220 nm deep, the thickness of the silicon slab layer was H = 500 nm, while the thickness of the buried oxide layer was t_{BOX} = 1 μm. Beside the SOI wafers with these Si rib waveguides, we also used dies from the planarized SOI wafers where the surrounding trenches were "filled" with a deposited SiO_2, as illustrated in Figure 3.12. As we shall later see, such a planarized surface of the SOI wafers was beneficial for achieving thin and more uniform DVS-BCB bonding layers free of voids that would compromise the optical properties of the hybrid waveguides and the bonding quality.

As for the III-V semiconductor wafers used in the bonding tests, the functional layers were epitaxially grown on a InP substrate. At the the very top of the III-V semiconductor layer stack there were two sacrificial layers of InP (at the surface of the wafer) and InGaAs (just beneath the InP layer). Each of these layers was 100 nm thick. They had a protective role and were removed by chemical wet etching before the bonding. Beneath these layers laid the sequence of the functional III-V layers, as presented in Table 3.1, but in reverse order - with the InP spacer layer at the top of the structure and the p-type ohmic contact laying at the bottom. Under it, there were two etch stop layers of InP and InGaAs (lattice-matched to InP). Similar to the sacrificial layers at the top of the structure, each of these layers was also 100 nm thick. Beneath these layers was an InP substrate with a thickness of ~ 370 μm. The role of the last InGaAs layer was to act as an etch stop layer during the removal of the InP substrate via wet chemical etching. The 100 nm thick InP layer on top of it had a protective role and was removed by chemical wet etching only before the start of the III-V processing, which will be discussed in detail in Chapter 5.

The size of III-V dies that were used in the experiments varied, but it was usually never smaller than 5 mm × 5 mm, or larger than 8 mm × 8 mm. Most often, it was 8 mm × 7 mm. The size of the SOI dies was either 20 mm × 20 mm or 10 mm × 10 mm.

The commercially available DVS-BCB resin used in the bonding tests was Cyclotene 3022-35, which nominally produces the thinnest cured DVS-BCB

films (1 μm - 2.4 μm thick) compared to other resins from the Cyclotene 3000 Series [5]. In order to obtain bonding layers much thinner than 1 μm, we diluted the original Cyclotene resin with mesitylene in different volume proportions. Mesitylene, or 1,3,5-trimethylbenzene, is an organic solvent that is generally used in DVS-BCB solutions. Diluted BCB:Mesitylene solutions were used in the bonding tests, where they were spin-coated on an SOI die, which will be described in detail in section 4.3.

4.2.2 The bonding tool

Switching from a manual to a machine-based bonding procedure was a basic prerequisite for bringing the bonding process closer to industry-compatible procedures. For this purpose, we chose to work with a Süss MicroTec ELAN CB6L wafer bonding tool (shown in Figure 4.3a). It is designated as a manual bonding tool (as compared to fully automated bonders) and is specifically designed for the needs of research and development and for the pre-production wafer bonding market. Some basic components of the wafer bonder are illustrated in Figure 4.4. The CB6L wafer bonder can handle wafers of up to 150 mm diameter. Wafers are placed on a transport fixture (shown in Figure 4.3b) and loaded into the processing chamber. The bonding process itself is specified by the user who creates the bonding recipe, which is a sequence of steps in which all the relevant process parameters and its tolerances are defined.

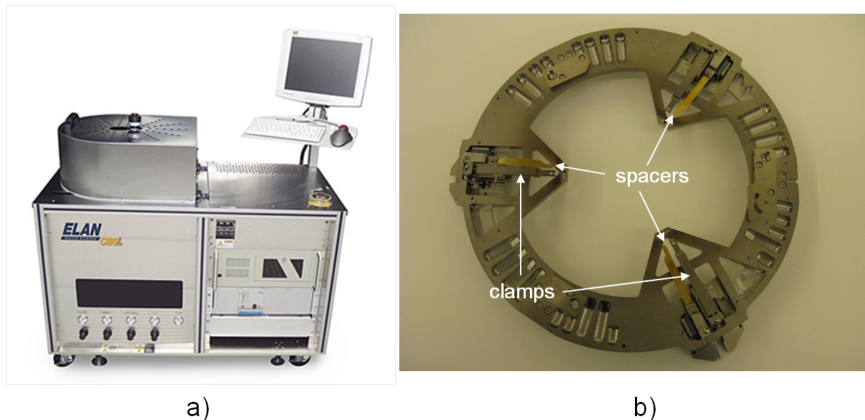

Figure 4.3: Süss Microtec ELAN CB6L wafer bonder: a) front view of the bonder with the control PC; b) transport fixture for handling 100 mm diameter wafers which was used in the bonding tests.

However, the ELAN CB6L wafer bonder is not designed for handling small dies as the ones we were using in our experiments. The standard transport fix-

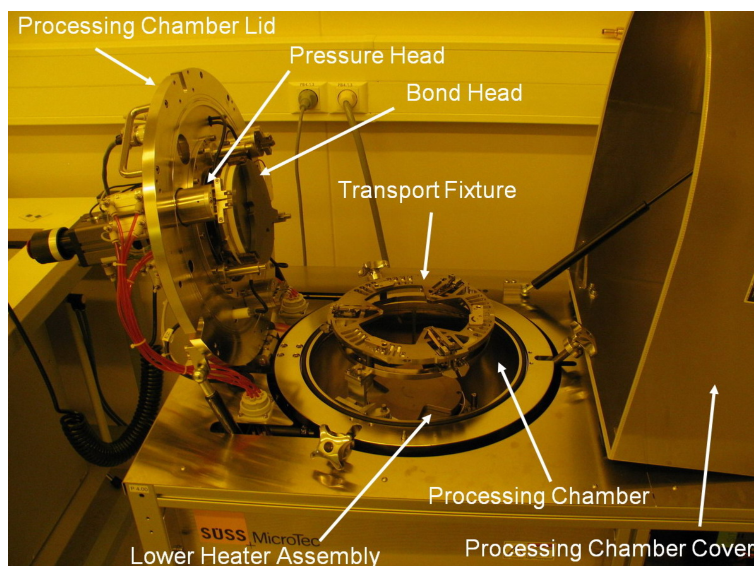

Figure 4.4: The basic components of Süss Microtec ELAN CB6L wafer bonder.

ture of this wafer bonder (shown in Figure 4.3b) can handle wafers of minimum 100 mm diameter, although with the special equipment, wafers of 50 mm diameter can be handled as well. Therefore, this problem had to be solved to enable us to handle and bond individual III-V and SOI dies.

4.2.3 Die-to-die bonding setup

Our approach was to temporarily attach both III-V and SOI dies to auxiliary wafers that acted as the die carriers. Then, we would take the auxiliary wafers, load them into into the processing chamber of the wafer bonder (with the dies attached to them), and proceed with the bonding, as in the case of bonding the full-size wafers. In this way, we were able to use a standard transport fixture of the bonding tool, designed to handle the full-size wafers, while in the end we brought only the dies into contact. The layout of this die-to-die bonding setup is given in Figure 4.5. Before bringing the dies into contact, the metallic spacers (that are the integral parts of the transport fixture) are placed between the top and the bottom carrier wafers. The thickness of the III-V dies used in tests is approximately 375 μm and the thickness of SOI dies is around 725 μm, which results in a total bonding stack thickness of roughly 1100 μm. On the other hand, the thickness of the metallic spacers is only 100 μm. To compensate for this difference, three pairs of stacked silicon dies were bonded on the bottom carrier wafer at the exact locations were the metallic spacers are positioned, as illus-

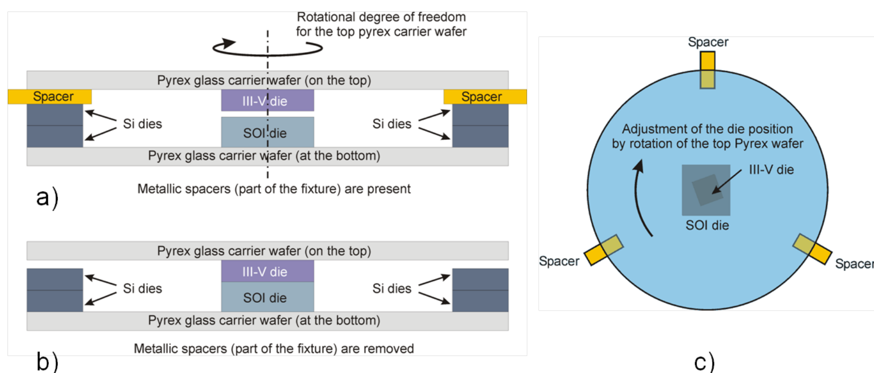

Figure 4.5: Die-to-die bonding setup: a) cross-section of the setup, prior to bonding, with the spacers put in place to provide a gap between the III-V and the SOI dies; b) cross-section of the setup after the spacers are retracted – III-V and SOI dies come into contact; c) top view of the setup – rotational degree of freedom enables an easy positioning of a III-V die.

trated in Figure 4.5. These dies act as additional spacers. In this way, the retractable metallic spacers rest on these Si dies and enable the existence of a gap between the SOI die and III-V die, prior to the bonding. When the dies had to be brought into contact, the metallic spacers are retracted and the III-V die falls on the SOI die, while the gap is now left between the Si spacer-dies on the bottom carrier wafer and the top carrier wafer, as illustrated in Figure 4.5b).

The additional advantage of this setup is that, once the metallic spacers are in place, the top carrier wafer can easily rotate around its vertical symmetry axis, as shown in Figure 4.5c. To some extent, it is also possible to have a translation movement of the top carrier wafer with respect to the bottom one. In this way, we can manually adjust the relative position of the bonding dies before placing the clamps that fix the top and the bottom carrier wafers, prior to loading the transport fixture into the processing chamber. This gives us a possibility to orient the III-V die with respect to the underlying SOI die in a desired way, as we shall discuss in more detail in Chapter 5.

We have chosen 100 mm diameter Pyrex glass wafers to act as carrier wafers. They are able to withstand the curing temperatures of DVS-BCB and provide relatively good mechanical strength, while being much less brittle than silicon wafers that were initially also considered for this role.

One of the basic problems was how to temporarily fix the dies to these glass carrier wafers prior to bonding. This attachment should be able to withstand some extreme conditions in the processing chamber (high vacuum, tempera-

tures usually up to 250 °C) and also be able to easily detach after the bonding is finished. In our first experiments, we used Apiezon® H grease, able to withstand temperatures up to 240 °C and suitable for use in a vacuum environment. Although this grease served the intended purpose, it was not convenient to work with. Applying the grease required a lot of dexterity and it was not possible to have a good control over the thickness of the grease layer between the attached die and the carrier wafer. It was not always easy to detach the samples after the bonding and it was not easy to clean them.

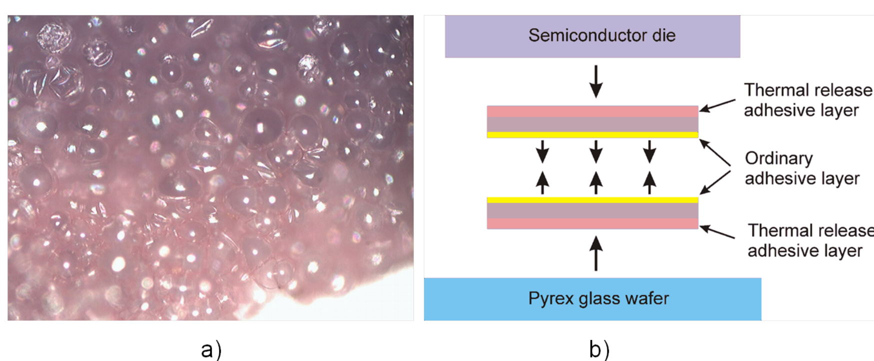

Figure 4.6: Thermal release tape Revalpha No.31950 is used for temporary attachment of the semiconductor dies: a) micro-bubbles formed in the thermal release layer after heating up to 200 °C, seen under the microscope; b) two sheets of Revalpha tape, attached back-to-back with the thermal release layers facing outwards, are used for temporary fixing of the semiconductor dies to Pyrex glass wafers.

Therefore, we started using the thermal release tape Revalpha No.31950E from Nitto Denko company. Upon reaching the nominal release temperature of the tape, the thermal adhesive layer undergoes a chemical transformation. A multitude of micro-bubbles are formed on the surface of the layer, as illustrated in Figure 4.6a and the layer practically disintegrates and looses its adhesiveness. The Revalpha tape is a double-sided adhesive tape, but the thermal release layer is located only at one side of the tape. An ordinary adhesive layer is placed on the other side. Therefore, in order to attach a semiconductor die to a Pyrex carrier wafer, we use two identical pieces of Revalpha tape that are attached to each other using the sides with the ordinary adhesive layer, as illustrated in Figure 4.6b. In this way, the thermal release layers are facing outwards and are placed in direct contact with the Pyrex wafer and the semiconductor die. Once the tape release temperature is reached, both layers loose their adhesiveness and the semiconductor die practically detaches from the Pyrex glass wafer. The thickness of a single sheet of Revalpha tape is ~ 100 μm. Therefore,

the use of thermal release tapes for temporary fixing of the dies (both the III-V and the SOI die) increases the total thickness of the stack by ~ 400 μm.

The nominal release temperature of Revalpha No.31950E tape is 200 °C, which is less than the usual curing temperature for BCB. However, we performed a series of tests and confirmed that the tape can withstand temperatures up to 240 °C, lasting for 1 hour, without substantial increase in the residual adhesive strength.

The use of this tape brought many advantages, like controllable and reproducible thickness of the bonding medium between the die and the carrier wafer, ability to easily tailor it to the shape of the dies and easy detachment of the dies from the carrier wafers after completion of the bonding process.

4.3 Description of the bonding procedure

The bonding procedure can be divided into two phases. The first one is the preparation of III-V and SOI dies, while the second one is the bonding itself. Schematically, this is illustrated in Figure 4.7. Preparation of the samples has a goal to remove any contamination from the bonding surfaces of the dies and to condition these surfaces so that DVS-BCB can be easily and effectively applied. Although the adhesive bonding is somewhat tolerant to particle contamination, since we want to achieve bonding layers of less than 100 nm thickness, it is clear that removing any residual particles from the bonding surfaces is essential. Different cleaning procedures are used for III-V dies and for SOI dies.

Cleaning the surface of the SOI dies is performed using Standard Clean 1 (SC-1) solution, comprising aqueous ammonia solution (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water in volume ratios of 1:1:5, respectively. The SOI die is exposed to SC-1 at 70 °C, for 15 minutes, after which it is rinsed with DI water, dried and placed on a spin-coater. Usually, we first spin-coat adhesion promoter AP3000 and then we spin-coat the BCB:mesitylene solution. AP3000 is an adhesion promoter that is used to improve adhesion of the BCB resins and its use is suggested by Dow Company [5]. Our usual spin-coating procedure comprises the spreading step, lasting 5 seconds at 500 rpm, followed by the spin-coating step of 40 seconds at 3000 rpm. After this, the SOI die is baked on a hot plate, usually for 5 minutes at 150 °C, to let mesitylene evaporate and the BCB film to stabilize. Finally, the SOI die is mounted on a carrier wafer and placed into the transport fixture.

In most of our experiments we have used III-V dies cleaved from the epitaxially grown InP-based wafers, comprising functional layers as described in section 4.2.1. On some occasions, as a much cheaper alternative, we used pure InP dies instead. In all of these dies, the material that was in direct contact with the bonding BCB layer was indium phosphide. However, there is no equivalent

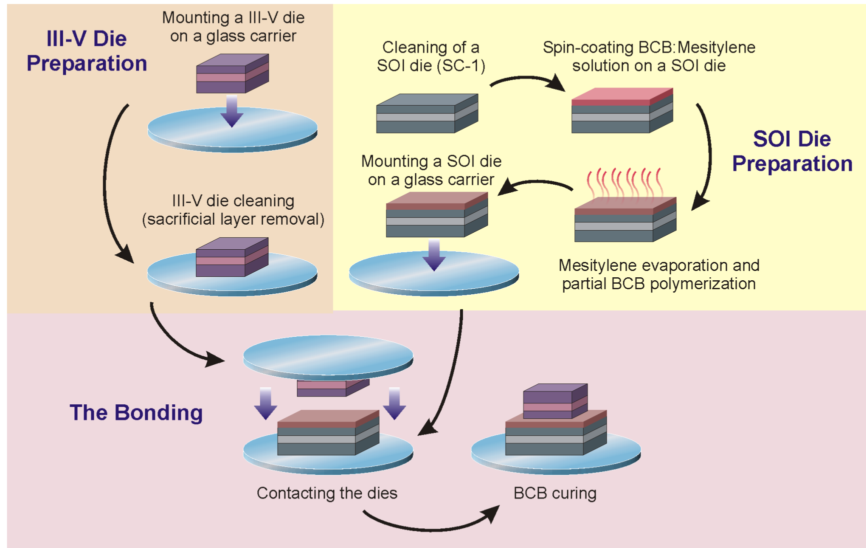

Figure 4.7: Overview of the DVS-BCB bonding procedure comprising preparation of the III-V and the SOI dies and subsequent DVS-BCB bonding and curing.

cleaning solution for III-V dies, like SC-1 used for SOI and silicon dies. To overcome this problem, two sacrificial layers are grown on the top of our epi layer stack, as described in section 4.2.1. On the wafer surface, there is a 100 nm thick InP layer, followed by a 100 nm thick InGaAs layer below. Prior to bonding, selective wet etching is used to remove these two layers, one at a time. For easier handling, the III-V die is first attached to the carrier Pyrex glass wafer using the Revalpha tape, after which the wet etching steps are performed. First, the InP layer is removed by dipping the III-V die (attached to the carrier wafer) into a 37% aqueous solution of HCl (in a chemical notation: $HCl_{(aq.\ 37\%)}$). After this, the remaining InGaAs layer is etched away using a solution comprising $H_2SO_4\ _{(aq.\ 96\%)}$, $H_2O_2\ _{(aq.\ 30\%)}$ and DI water, in a volume ratio of 1:3:1. In this way, any particles and contaminants present on the III-V die surface are removed during these two wet etching steps, exposing a clean InP layer that will come into contact with BCB during the bonding. After removing the sacrificial layers, the III-V die is rinsed with DI water, dried and mounted on the transport fixture of the wafer bonding tool.

Once both the III-V and the SOI dies, attached to their carrier wafers, are mounted on the transport fixture, the fixture itself is loaded into the processing chamber of the wafer bonder and the bonding recipe is started. A typical temperature profile of the bonding procedure is illustrated in Figure 4.8. The

bonding recipe starts with bringing the processing chamber into a vacuum and rapid heating of both the top and the bottom heaters to 150 °C. After 5 minutes in vacuum, the dies are brought into contact. Contacting of the dies in vacuum is performed in order to avoid trapping of air at the interface of the bonding surfaces. After this, the dies are kept at 150 °C for 20 minutes, while the bonding pressure is applied to them. At this temperature, DVS-BCB is still in a liquid state and can accommodate to the topography of the dies, filling the voids at the bonding interface, while the bonding pressure is being applied. Subsequently, the temperature is slowly increased up to 240 °C, with a ramp of 1.6 °C/min.

The bonding head is raised at 180 °C and no pressure is applied afterwards. This is done because the release temperature of the Revalpha tape used for temporary fixing of the dies is 200 °C. Applying the bonding pressure beyond this temperature leads to additional pressure on the bonding stack (due to creation of the micro-bubbles in the thermal release layer) which can lead to die cracking. Also, if the bonding pressure is applied beyond 200 °C, the residual adhesiveness of the Revalpha tape increases, and it becomes very difficult to remove the tape residues from the dies, after the bonding.

After reaching 240 °C, the dies are kept at this temperature for 1 hour in a nitrogen atmosphere, at 1000 mbar. Although a usual BCB curing is performed at 250 °C for 1 hour, we have lowered this to 240 °C. Initially, this modification was made to comply with the temperature limit for Apiezon® H grease and afterwards we wanted to avoid exposing the thermal tape to temperatures much higher than 200 °C, as it would increase its residual adhesiveness. According to Dow Chemicals technical notes [5], the BCB degree of polymerization in these two cases should be around 98% and 95%, respectively, which should not result in a significant difference in the bonding quality. After curing is finished, the bonded samples are cooled to room temperature and finally unloaded from the processing chamber. Afterwards, the InP substrate is grinded down to ~ 70 μm using a lapping tool (as illustrated in Figure 4.1b) and a slurry made from a suspension of aluminum oxide abrasive powder with 12.5 μm particle size. The remaining InP is subsequently removed by wet etching in $HCl_{(aq.\ 37\%)}$. In the end, a thin III-V film with the functional layers is obained, bonded to the SOI die, ready for further processing, as shown in Figure 4.2b.

4.4 Die-to-die bonding experiments

The description of the bonding procedures, given in the previous section, is a general one, and it did not give an insight into some important details that are going to be discussed in this section. Based on the simulations and analyses presented in Chapter 2 and requirements for the evanescent hybrid III-V/Si lasers, our goal was to develop a reliable DVS-BCB bonding procedure that would yield

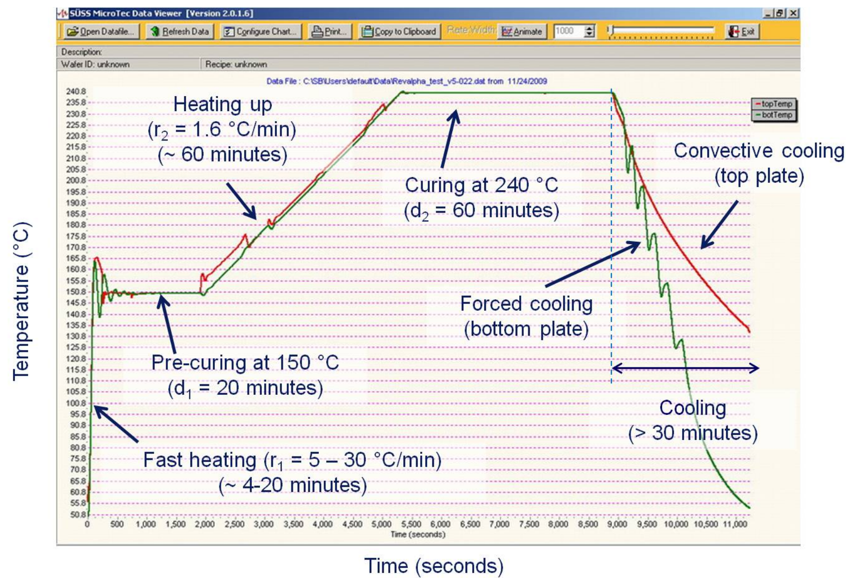

Figure 4.8: Temperature profile during the bonding process: fast heating to 150 °C, followed by 20 minutes pre-curing at 150 °C; afterwards, a slow temperature rise to 240 °C is followed by 1 hour DVS-BCB curing and eventual cooling.

less than 100 nm thick bonding layers (in fact, as thin as possible) and with a good thickness uniformity, preferably within ± 10 nm. Optimization of the bonding procedure required a large number of die-to-die bonding tests that where usually focused on optimizing one of the parameters of the processing steps. Thus, the bonding procedure evolved over a period of time and some modifications were adopted, as we shall see in section 4.4.2.

One of the first modifications of the bonding procedure was the change of the medium for temporary die attachment. After initial tests using Apiezon® H grease, we switched to thermal release tapes which provided more convenient die fixing and detachment, as well as more stable results.

4.4.1 The initial tests - achieving the adequate bonding layer thickness

Achieving the required BCB bonding layer thickness t_{BCB} was an immediate objective of the bonding tests. Parameters which were expected to have the greatest impact on t_{BCB} were: 1) the bonding pressure, 2) the BCB:mesitylene dilution used and 3) the rotation speed during the spin-coating of the dilution on an SOI die.

Setting the pressure head of the wafer bonder to the correct position was the first step in achieving the optimal pressure on the dies during the bonding. The position of the pressure head needs to be adjusted whenever the thickness of the bonding die stack changes - which was exactly the case once we started using Revalpha tape, which increased the bonding stack by ~ 400 μm. After this, an optimum value for the bonding tool pressure (p_{tool}) had to be found. The bonding tool pressure is a differential pressure between the gas in the bonding head cushion and the pressure in the processing chamber. It is entered as a parameter in the bonding recipe.

However, the bonding tool pressure (p_{tool}) is not the actual pressure exerted on the dies during the bonding. The area of the bonding head of our wafer bonder (A_{bh}) is 222 cm^2 and this is much larger than the actual bonding area between the III-V and SOI dies. In our case, this area is equal to the area of the smaller die - the III-V die (A_{die}), and it is usually around 0.5 cm^2, but in some tests it was only ~ 0.25 cm^2. The force F, exerted to the bonding stack, is equal to the product of the bonding tool pressure p_{tool} and the bonding head area A_{bh}. Therefore, the actual bonding pressure p_{die}, exerted on the dies, can be expressed as:

$$p_{die} = \frac{F}{A_{die}} = \frac{A_{bh}}{A_{die}} \cdot p_{tool} \tag{4.1}$$

In tis way, the actual bonding pressure p_{die} is scaled up by the ratio A_{bh}/A_{die} compared to the bonding tool pressure p_{tool} which is set as a parameter in the bonding recipe. In our experiments, we usually set this value at 10 mbar, which is below the nominal lower limit of our wafer bonder capabilities. The nominal operating range for the bonding pressure p_{tool} is between ~ 100 mbar and 3600 mbar. Therefore, the wafer bonder was not able to keep the bonding tool pressure p_{tool}, stable at 10 mbar, which would correspond to a bonding force F of 22.2 N. In the initial bonding tests, the actual force F applied to the bonding stack usually had a peak value between 30 N and 45 N, but its temporal profile was not constant, as shown in Figure 4.9a. In the later tests, a relatively flat temporal profile of the bonding force was achieved, but with an average value of ~ 60 N, which is illustrated in Figure 4.9b. Therefore, given the size of III-V dies used in our tests, the actual bonding pressure p_{die} was usually in the range of 8-12 bar (800-1200 kPa). These values are much higher than the bonding pressure values of 1.7 bar reported in the full-wafer DVS-BCB bonding procedure by Niklaus *et al.* [6] or 1.5 bar, reported by Choi *et al.* [7]. It was expected that such a high bonding pressures should minimize chances for void formation at the bonding interface [6].

Since the bonding pressure p_{die} was already very high and not easily reproducible, we directed our attention to varying the rotation speed during BCB spin-coating and changing the BCB volume ratio in BCB:mesitylene solutions

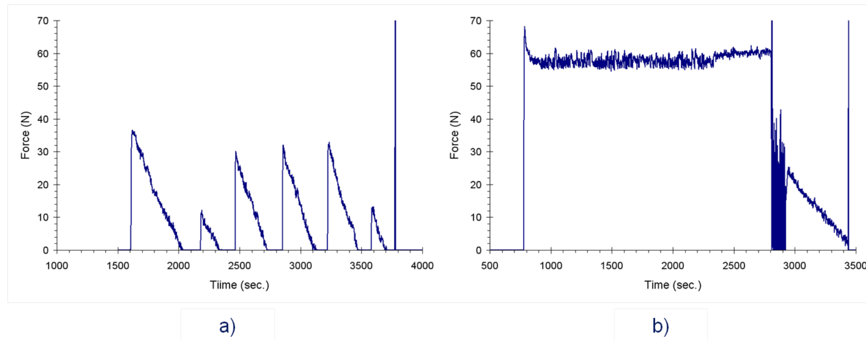

Figure 4.9: Profiles of the applied bonding force in the case of the initial bonding recipe and subsequently modified bonding recipe. a) Sawtooth-shape profile, observed in the initial bonding recipe where the bonding force was applied when the processing chamber was already pressurized; peak force values were usually between 30 N and 45 N. b) Flat-force profile achieved in the modified bonding recipe, where the bonding force was applied while the processing chamber was still in vacuum; the force amplitude was usually between 55 N and 65 N.

that were used in the tests. To assess the impact of these parameters on the BCB layer thickness we have spin-coated BCB solutions on flat, unpatterned, InP dies and subsequently cured them. Using lithography and reactive ion etching (RIE) of DVS-BCB in a plasma of oxygen and sulfur hexafluoride (SF_6), we would make "windows" in the cured DVS-BCB film on the surface of InP and measure its thickness at the edges using a contact profilometer. BCB:mesitylene solutions used in these had the component ratios of 2:3, 1:2, 1:3 and 1:7, corresponding to BCB volume ratio in solutions of 40%, 33%, 25% and 12.5% (v/v). Results of these tests are shown in Figure 4.10. We can conclude that changing BCB content in the solution has more impact on the final BCB film thickness than increasing the rotation speed. Other tests showed that spin-coating BCB on a patterned SOI die, at speeds above 5000 rpm, in some cases produced non-uniform films immediately after spin-coating. This is probably a consequence of a turbulent flow of the BCB:mesitylene solution at higher rotation speeds. To avoid this risk and further standardize our process, we fixed our spin-coating speed at 3000 rpm and used this value in all subsequent tests.

In this way, we were left with only the BCB:mesitylene solution ratio as a variable parameter that we could adjust in order to achieve the desired bonding layer thickness. According to the results shown in Figure 4.10, only the 1:7 BCB:mesitylene solution (12.5%(v/v)) provided layers less than 100 nm thick, but it was expected that the actual thickness of the bonding layers would be somewhat thinner, due to exposure to a high bonding pressure. Therefore, the

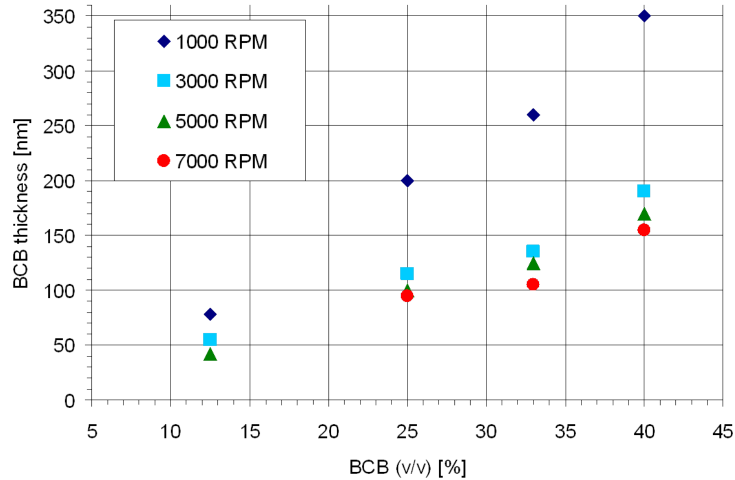

Figure 4.10: Thickness of cured DVS-BCB films, spin-coated on flat InP dies, depending on BCB volume ratio in BCB:mesitylene solution and rotation speed during spin-coating.

use of BCB:mesitylene solutions with the BCB content up to 25%(v/v) (i.e. 1:3 BCB:mesitylene ratio) was also considered for the bonding tests.

To measure the bonding layer thickness, we made a cross-section through a bonded III-V film (after the substrate removal), using a focused ion beam (FIB) tool and then made a scanning-electron microscope (SEM) image of this cross-section. In the initial tests, we focused on 1:7 BCB:mesitylene solution without the use of the adhesion promoter AP3000. We managed to achieve bonding layers above Si rib waveguide as thin as 15 nm (see Figure 4.11a). On the other hand, using 1:3 BCB:mesitylene solution, a thickness of the bonding layer of around 45 nm was demonstrated, as shown in Figure 4.11b.

However, in our post-bonding die processing, we observed peeling of the III-V film around its edges during wet etching of the InP substrate. In some cases, we also observed formation of micro-voids in the trenches around Si rib waveguides. This was especially the case when the 1:7 BCB:mesitylene solution was used. Therefore, while trying to achieve the adequate bonding layer thickness, we encountered a number of problems that eventually led to further modifications in the bonding procedure. Beside achieving sufficiently thin and uniform bonding layers, achieving a good bonding yield and a reliable process was the greatest priority.

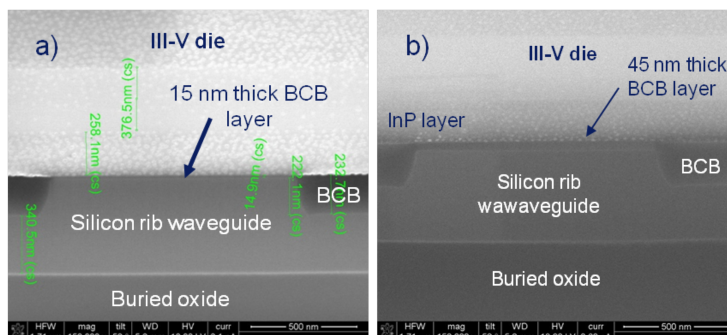

Figure 4.11: SEM images of the DVS-BCB bonding layers on top of the silicon waveguides: a) a 15nm-thick layer, obtained using 1:7 BCB:mesitylene solution; b) a 45nm-thick layer, achieved using 1:3 BCB:mesitylene solution.

4.4.2 Observed problems and evolution of the bonding procedure

The most commonly observed problems in the bonding tests were: 1) peeling or detaching of the bonded III-V film, 2) formation of micro-voids in the trenches surrounding the Si rib waveguides and 3) formation of "blisters" in the bonded III-V films, after substrate removal.

Peeling or chipping of the edges of the bonded III-V film was very often observed, especially in the early bonding tests. Peeling occurred during the wet etching in HCl, which was the last processing step in the substrate removal. In the worst cases, the entire III-V film would peel-off and detach.

Initially, to tackle this problem, we started using the adhesion promoter AP3000. It would be spin-coated on an SOI die just before spin-coating the BCB:mesitylene solution. It was expected that the BCB adhesion to the SOI die would improve and help achieving a better bond. Indeed, after this modification, the bonding yield improved and chipping was reduced, but not completely gone. On the other hand, the average thickness of the bonding layers increased as well. For example, using the "1:3" BCB:mesitylene solution, the achieved bonding layer thickness increased to 90 nm, compared to 45 nm, observed when bonding without the use of AP3000. This was probably the consequence of a better BCB adhesion to the silicon surface and increased viscosity during spin-coating. Despite this unwanted increase in the bonding layer thickness, the use of adhesion promoter AP3000 became a standard step of the bonding procedure.

Observation of the bonded III-V films after the substrate removal revealed the existence of distinctive "fault lines" near the edges of the bonded film, as

illustrated in Figure 4.12a. Measurements with both the optical and the contact profilometer showed that the area between the "fault line" and the edge of the bonded film is around 240 nm lower than the rest of the film. This height difference was equal to the thickness of the spacer layer, made of InP, suggesting that the spacer layer located near the edges of the bonded III-V die was etched by HCl during the substrate removal processing step. This hypothesis was confirmed by SEM inspection of the cross-sections (made using the FIB tool) in the various parts of the bonded III-V film. The cross-section made at the location of one of the "fault lines", clearly shows the lack of the spacer layer at one end and remnants of it on the opposite end, as illustrated in Figure 4.12b.

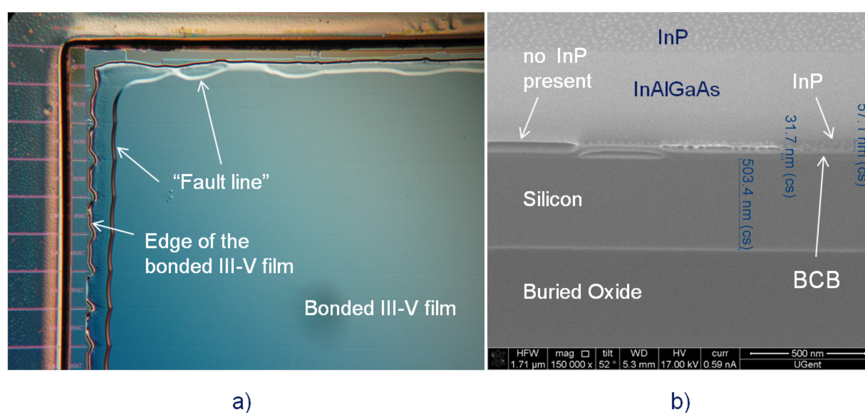

Figure 4.12: Underetching of the InP spacer layer: microscopic image (through a polarizing filter) of the bonded III-V film with the characteristic "fault line" near the edges of the film; b) SEM image of the cross-section made with an FIB tool at the location of the "fault line" - lack of InP spacer layer on the left side and the clearly visible InP remnants on the right side.

Apparently, the BCB bonding layer fails to provide a hermetic seal, allowing HCl to permeate through it and chemically attack the InP spacer layer that is in direct contact with BCB. To solve this problem, the pre-bonding III-V die preparation procedure was modified so that a protective layer of SiO_2 was deposited on the InP spacer layer, just prior to bonding. Specifically, after the removal of the sacrificial layers by wet etching, the III-V die was loaded in a plasma enhanced chemical vapour deposition (PECVD) system and a very thin (~ 10 nm) layer of SiO_2 was deposited. The subsequent bonding procedure was not changed. The role of this thin SiO_2 layer was to act as an etch-stop layer and prevent etching of the InP spacer layer by HCl, during the substrate removal.

The positive effects of this modification were immediately visible and the

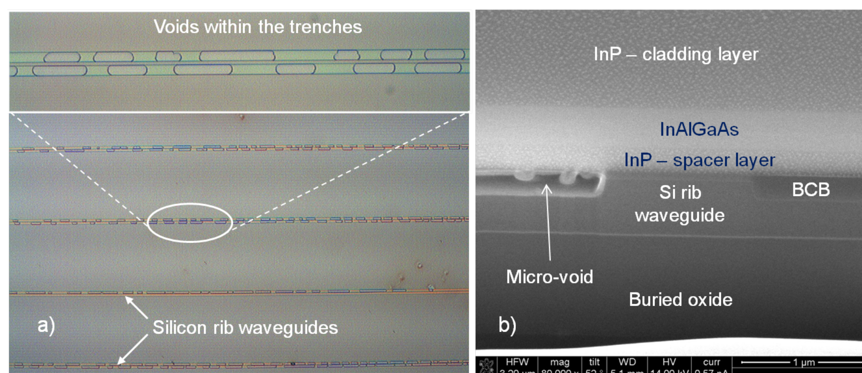

Figure 4.13: Micro-voids in the BCB bonding layer: a) microscopic image of the exposed BCB bonding layer revealing micro-voids in the trenches surrounding Si rib waveguides - a zoom-in is inserted at the top of the image; b) an SEM image showing a micro-void in at the trench left of the Si rib waveguide.

bonding yield drastically improved, while chipping and peeling was minimized. Due to similar values of the refractive indices of DVS-BCB and SiO_2 (1.54 and 1.45, respectively), the change in optical properties of the structure was minimal. Therefore, deposition of SiO_2 became a standard step in the pre-bonding III-V die preparation.

Formation of micro-voids was more often observed when very dilute BCB: mesitylene solutions were used (e.g. 1:7 BCB:mesitylene solution). These micro-voids were formed in the trenches surrounding the Si rib waveguides, as illustrated in Figure 4.13. The most adverse effect of these micro-voids was change in the refractive index of the hybrid III-V/Si waveguide which would affect the profile of the fundamental hybrid optical mode. Therefore, it was essential to avoid formation of these micro-voids.

To tackle this problem, we switched back to the use of the 1:3 BCB:mesitylene solution, instead of a more dilute, 1:7 BCB:mesitylene solution. The frequency of the micro-voids occurrence drastically decreased, but the thickness of the bonding layers increased. As a better solution, we started using planarized SOI dies, as described in section 3.2.5, in Chapter 3. The change in SOI die topography resulted in a change in the bonding layer thickness. With the planarized SOI dies and 1:3 BCB:mesitylene solution, the bonding layer thickness varied from as low as 70 nm to as high as 140 nm, observed in some samples. Therefore, we switched to 1:5 BCB:mesitylene solution and achieved bonding layer thicknesses between 40 nm and 70 nm, as illustrated in Figure 4.14a. On the other hand, the use of 1:7 BCB:mesitylene solution resulted in bonding layer

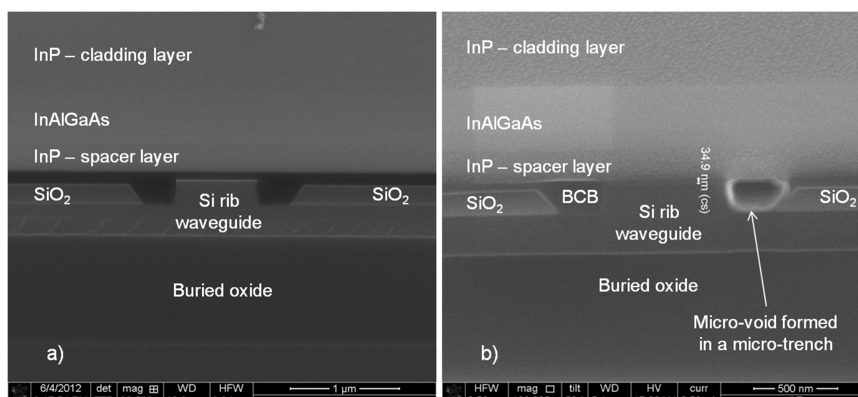

Figure 4.14: SEM images of the DVS-BCB bonding layers on top of the planarized silicon waveguides: a) a 65nm-thick layer, obtained using 1:5 BCB:mesitylene solution; b) a 35nm-thick layer, achieved using 1:7 BCB:mesitylene solution. A micro-void is formed in the micro-trench between the rib waveguide and SiO_2 deposited in the original trench.

thicknesses between 35 nm and 55 nm, but the micro-voids were again observed in the micro-trench surrounding the Si rib waveguide, as illustrated in Figure 4.14b. Consequently, we have adopted a bonding procedure consisting of using the planarized SOI dies and 1:5 BCB:mesitylene solution.

Formation of the "blisters" in the bonded III-V films was sometimes observed after substrate removal. These are illustrated in Figure 4.15a. Distinctively, it was observed that blisters grew in size when the samples were exposed to high temperatures, for example, when they were placed on a hot plate. This clearly suggested that they were caused by trapped gases that expanded once heated. SEM inspection of the cross section made through the blisters showed a gap within the DVS-BCB bonding layer, as illustrated in Figure 4.15b. However, no damage to the InP spacer layer was observed, which means that HCl did not penetrate these gaps and no gas build-up could occur due to a chemical reaction between InP and HCl. Thus, it was suspected that the only source of the gas filling the gap, could be either the remnants of mesitylene that didn't evaporate prior to die contacting, or presence of some organic contaminant on an SOI die.

To address this problem, the hot plate temperature during the 5 minute bake of the SOI die (after spin-coating a BCB:mesitylene solution), was increased to 150 °C, from 100 °C, as initially used. Also, the bonding recipe was modified in order to keep the processing chamber in vacuum as long as possible. Therefore, the bonding force was applied while the processing chamber was still in vacuum. Re-pressurization of the wafer bonder processing chamber (to 1000

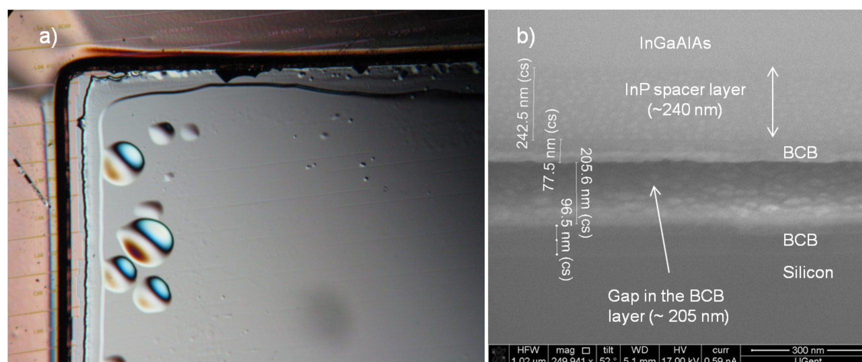

Figure 4.15: Occurrence of blisters in the bonded III-V films: a) microscopic image (through a polarizing filter) of the bonded III-V film with the blisters near the edge of the film; b) SEM image of a cross-section made through a blister: there is no damage to the InP spacer layer, but a large gap (~ 200 nm) in the DVS-BCB bonding film is visible.

mbar) was performed only after reaching 180 °C, instead of 150 °C, which was the case in the initial bonding recipe. In this way, the period during which the dies are in the vacuum was prolonged from slightly more than 5 minutes to approximately 40 minutes. It was expected that any traces of mesitylene, left in the BCB solution after the baking on a hot plate, would eventually evaporate when exposed to these temperatures, in vacuum, for such a time period. On the other hand, re-pressurization of the processing chamber is necessary to bring the bonding tool up and stop with the application of force on the bonding die stack. This bonding recipe modification - the application of the bonding force, while the processing chamber was still in vacuum, also resulted in a much more stable profile of the applied bonding force, as illustrated in Figure 4.9.

It should be mentioned here that the force "spike", visible in Figure 4.9 at the end of the force application is not actually applied to the dies. It appears due to a spike in the pressure in the bonding head cushion when the bonding head moves upwards. What is actually measured is the pressure in the bonding head cushion p_{tool}. The bonding force is then calculated as a product of the pressure p_{tool} and the area of the bonding head A_{bh}. This product is automatically set to zero only when the bonding head completely retracts to the upper most position. Therefore, while the bonding head moves upwards (which lasts for ~ 2 seconds) and the application of the force on the bonding die stack has already stopped, the bonding force F is still calculated as a product of p_{tool} and A_{bh}, and the "spike" in the value of p_{tool} is recorded as a spike in the bonding force F.

To minimize any risk of organic contamination of the SOI dies, another

modification was made to the pre-bonding SOI die preparation. Instead of only rinsing the SOI die with acetone and isopropyl alcohol (IPA), the SOI die was additionally left for 15 minutes in a Piranha solution (3:1 solution of H_2SO_4:H_2O_2 $_{(v/v)}$) at ~ 85 °C. Only after this, a treatment with SC-1 solution would follow. After applying these modifications in the bonding procedure, the occurrence of blisters disappeared.

We can now summarize all the modifications to the bonding procedure that were made compared to the general procedure described in section 4.3. Preparation of the SOI dies was changed to include a 15 minute treatment in a hot Piranha solution (~ 85 °C), followed by SC-1 solution treatment. Preparation of the III-V die was modified to include deposition of a ~ 10 nm SiO_2 layer in a PECVD tool, just after the removal of the sacrificial layers, and before loading the die into the processing chamber of the wafer bonding tool. Finally, the bonding recipe was changed so that the bonding force was applied while the processing chamber was still in vacuum, extending the time during which the dies were kept in vacuum. In the end, the bonding tests focused on using planarized SOI dies and 1:5 BCB:mesitylene solution, which proved to give the best results.

4.4.3 The bonding layer thickness and uniformity

Besides the bonding yield and reliability, achieving the adequate thickness and uniformity of the bonding DVS-BCB layers was critical for fabrication of the hybrid III-V/Si lasers. We have already mentioned how very thin bonding layers (15 nm to 45 nm) were achieved in the early bonding tests, when the adhesion promoter AP3000 was not used.

To assess uniformity of the BCB bonding layer, we have conducted several tests in which pure InP dies were bonded on top of the SOI waveguides. After the bonding, InP was etched in HCl until the III-V die was completely removed, exposing the underlying cured BCB film. Following this, a 40nm-thin layer of Au was deposited on top of the BCB film (to ensure almost total first-surface reflection) and an optical profilometer (Wyko NT3300 by Veeco Instruments Inc.) was used to obtain information about the surface uniformity. Results of one of these tests where 1:7 BCB:mesitylene solution was used, are presented in Figure 4.16. A 3-D visualization of the bonding layer topography is shown in Figure 4.16a, while Figure 4.16b shows the BCB surface profile along the direction perpendicular to the SOI waveguides. Clearly visible notches (12-14 nm deep) correspond to the locations of the Si rib waveguides, which are surrounded by 220nm-deep trenches. However, in general, there is not much variation in the bonding layer profile over a distance of 1.2 mm, which suggests a relatively good BCB layer uniformity.

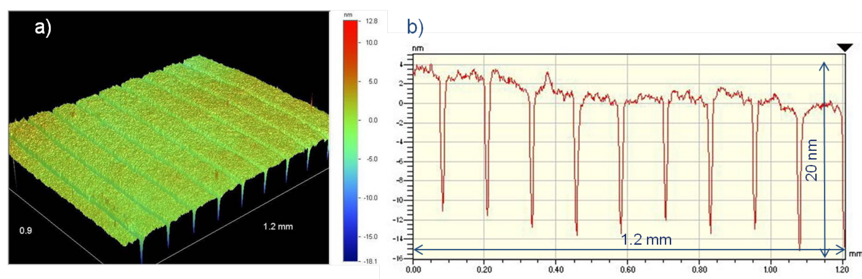

Figure 4.16: Topography of the BCB bonding layer achieved with 1:7 BCB:mesitylene solution: a) 3-D visualization of the bonding layer topography over the area of 1.2 mm × 0.9 mm; b) BCB surface profile perpendicular to SOI waveguides with the notches, at 125 μm pitch, visible at the locations of the trenches, surrounding the silicon rib waveguides.

We have already shown in section 4.4.1 and Figure 4.11 that BCB bonding layer thicknesses of 15 nm and 45 nm were demonstrated using 1:7 and 1:3 BCB:mesitylene solutions, respectively. However, as we showed in section 4.4.2, the bonding procedure had to be modified in order to achieve sufficiently high yield and reliability. Eventually, we have focused on bonding on planarized SOI dies and the use of 1:5 BCB:mesitylene solution, achieving a bonding layer thickness between 40 nm and 70 nm.

However, in all these tests with the modified bonding procedure, the bonding layer uniformity was not as good as the one achieved with 1:7 BCB:mesitylene solution and without the use of AP3000 and SiO_2 deposition. It was observed that the BCB bonding layer was always thicker in the middle of the bonding area and thinner near the edges of the III-V die. In the most extreme cases, this difference between the BCB layer thickness in the centre and at the edge of the bonding area, varied from around 80 nm (for a 1:3 BCB:mesitylene solution), to 30 nm (for a 1:5 BCB:mesitylene solution) and 20 nm (for a 1:7 BCB:mesitylene solution). This non-uniformity is illustrated in Figure 4.17a, which shows the BCB bonding layer achieved using 1:3 BCB:mesitylene solution after the III-V die peeled-off.

In several tests, the topography of the III-V dies was measured with the optical profilometer just prior to bonding. One such topographic map is shown in Figure 4.17b. The idea was to check if the III-V die topography is anyhow related to the shape of the BCB bonding layer thickness. However, despite qualitatively different surface topographies that were measured in III-V dies, with warps and bows typically of the order of several hundred nanometers, the profile of the BCB bonding layer thickness was always qualitatively the same and not corre-

lated to the pre-bonding topography of the III-V die.

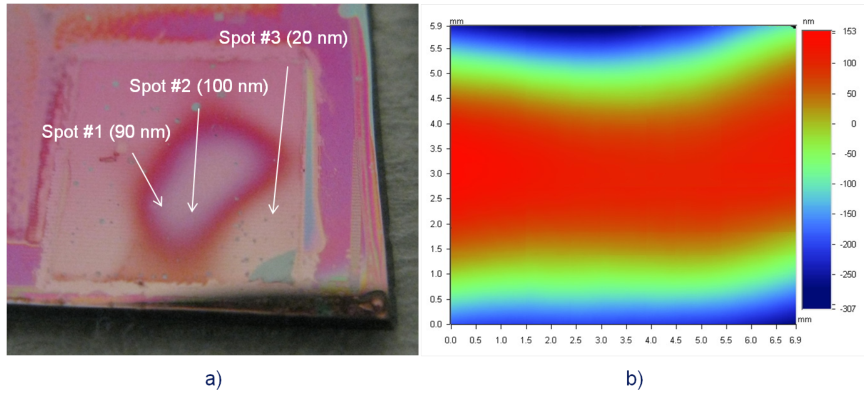

Figure 4.17: No correlation was observed between the thickness of the BCB bonding layers and pre-bonding topography of the III-V dies. a) The BCB bonding layer after the III-V die peeled-off shows a thick region in the centre of the die and thin regions around the edges. The bonding layer thickness was measured in three different spots. b) Topographic map of the III-V die surface, prior to bonding, with the red areas corresponding to high elevation and the blue ones to low elevation.

In order to improve the bonding layer uniformity, the bonding recipe was modified in such a way to achieve initial contact between the dies at 180 °C, instead of 150 °C. Compared to the original bonding recipe, the temperature profile was not changed, until reaching 180 °C. Dies were left at that temperature for 30 minutes, after which the contact was made and the bonding force applied for 10 minutes. This was inspired by work of Niklaus *et al.* [8], where it was suggested that pre-curing of DVS-BCB (for 30 minutes at 190 °C) prior to bonding, had a positive impact on the bonding layer uniformity, due to increased degree of polymerization and consequently significant reduction in DVS-BCB re-flow. However, the results of our tests carried out according to the modified recipe were bad as in both cases the III-V die detached immediately upon unloading from the wafer bonder. This could be related to the fact that Niklaus *et al.* were working with much thicker BCB bonding layers of 0.6 μm and 2.6 μm compared to the layers in our tests.

In another modification of the bonding procedure, a graphite foil was inserted between the top Pyrex wafer and the III-V die in the bonding stack in order to equalize the bonding pressure applied to the III-V die. However, this also neither improved nor qualitatively changed the BCB bonding layer uniformity. The distinctive bonding layer profile, thicker in the middle and thinner at

the edges, could be a consequence of the deformations of the top Pyrex glass carrier wafer to which III-V die is attached. As the bonding force is applied across the entire surface of the top Pyrex glass wafer, while the III-V die is attached only in the centre of the Pyrex wafer, it is possible that the Pyrex wafer deforms in such a way that it leads to the formation of such non-uniform BCB layer.

Regarding the bonding layer thickness and uniformity, the general conclusion is that better uniformity is achieved using planarized SOI dies and more diluted BCB:mesitylene solutions, with 1:5 BCB:mesitylene solution providing the optimal balance between the bonding layer thickness and uniformity, on one side, and the bonding reliability and lack of micro-voids, on the other side. The profile of the planarized samples that we used was not completely flat, as can be seen in Figure 4.14b. The SiO_2 didn't completely fill the trenches surrounding the Si rib waveguides. It had a trapezoid shape forming additional micro-trenches between the edges of SiO_2 and the rib waveguide. Better planarization of the SOI wafer would have allowed the use of more diluted solution, like 1:7 BCB:mesitylene solution, which would probably result in thinner and more uniform bonding layers.

On the other hand, the BCB bonding layer thicknesses achieved in the tests with planarized SOI dies and 1:5 BCB:mesitylene solution varied between 40 nm and 70 nm. These values were well within the range suitable for evanescent coupling. The biggest variations in the bonding layer thickness of 30 nm was observed over relatively long distances of ~ 2.5 - 3 mm. As none of the designed hybrid lasers was longer than 1 mm, the expected variation in the bonding layer thickness within one device was ~ 10 nm. This was still a satisfying result, as design of the DFB and phase-shifted DFB lasers was robust enough to tolerate such variations in the bonding layer thickness.

4.4.4 Shear stress tests

To assess the strength of the bonded dies, a batch of 11 bonded samples was prepared, using the bonding recipe without deposition of SiO_2 on the III-V die. For easier comparison, the die sizes were standardized: 5 mm × 5 mm for the III-V dies and 10 mm × 10 mm for the SOI dies. The indium phosphate substrate was not removed in the bonded III-V dies. In these tests, a 1:3 BCB:mesitylene solution was used, except in one case, where the dies were bonded using undiluted BCB, as a reference. Shear strength was measured with a die shear test method, using a Dage 4000 multipurpose bondtester. The tool speed was 700 μm/sec and the shear tool height was set to 100 μm. These measurements were carried out by an external vendor, selected by Intel's Photonics Technol-

ogy Labs, as our project partner. The measured shear stress values, at which the dies broke, ranged from 1.98 MPa to 2.02 MPa, with an average value of 2.00 MPa and a standard deviation 0.017 MPa. Additional four samples were bonded using the same bonding recipe and the thickness of the DVS-BCB bonding layer was measured in these samples using transmission electron microscopy (TEM). The bonding layer thickness in these four samples varied between 32 nm and 83 nm and was used as a reference value to assess the thickness of the bonding layer in the tested dies.

The results of the shear tests showed a very small variation (within 1%) in the shear stress, which may suggest a very good robustness of the bonding process. However, it is perhaps, more likely that in all 11 tested dies it was the III-V die itself that cracked rather than the BCB bonding layer. The average shear stress value of 2 MPa is testimony of a solid bonding strength that is achieved despite the expected variations in the bonding layer thickness. This value is higher than shear stress values between 0.2 MPa and 0.8 MPa that were previously reported for InP dies (5 mm × 10 mm) directly bonded to Si [9, 10].

4.5 Multiple die-to-die bonding tests

Upgrading a single die bonding procedure to a multiple die bonding process was one of the objectives in this work. In our multiple die-to-die bonding tests, we have exclusively focused on bonding four III-V semiconductor material dies on a single SOI die. At a later stage, it was planned to switch to bonding up to eight III-V dies on a larger piece of SOI, but this did not materialize due to the fact that a significant amount of time was devoted to development of a single die-to-die bonding procedure, leaving not much time to perform multiple die-to-die bonding tests.

Distribution of the bonding pressure was essential in multiple die-to-die bonding tests. Tests with the pressure measurement film Prescale, by Fujifilm, revealed a non-uniform pressure distribution across the bonding head of the wafer bonding tool. This was not a problem when bonding a single die, centrally-positioned with respect to the bonding head. However, it became a problem when a uniform bonding pressure had to be achieved over an area of approximately 20 × 20 mm, that was a standard size of the SOI dies used in the bonding tests.

To solve this problem, a piece of graphite foil was used between the top Pyrex carrier wafer and the III-V dies. The use of graphite foil to achieve uniform distribution of the bonding pressure was reported in literature [11]. In our initial implementation, the graphite foil was inserted between the top Pyrex wafer and the III-V dies, as illustrated in Figure 4.18a. Revalpha tape was used to attach the graphite foil to the Pyrex wafer and the III-V dies to the foil itself.

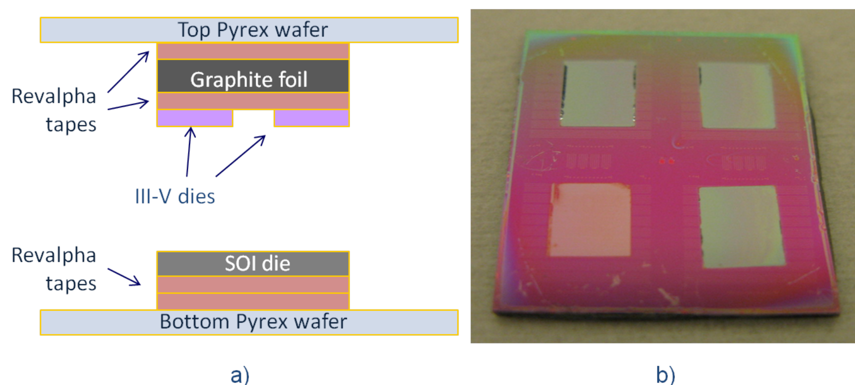

Figure 4.18: Multiple die-to-die bonding tests: a) schematics of the die attachment with the use of a graphite foil to achieve more uniform bonding force distribution; b) result of one of the initial bonding tests, where problem with the removal of photoresist residues from the III-V dies was observed: three dies remain bonded after substrate removal, but the die with the photoresist residues detached immediately.

To avoid wet-etching (needed to remove the sacrificial layers) and SiO_2 deposition while III-V dies were mounted on a graphite foil, these steps were performed before, on larger pieces of III-V epi wafers. After this, a protective layer of photoresist was spin-coated and baked. Prior to bonding, the individual dies, 5 mm × 5 mm, were cleaved and mounted on the graphite foil and Pyrex wafer, as illustrated in Figure 4.18a. The only pre-bonding processing step performed while the III-V dies were attached to the graphite foil was rinsing with acetone and IPA to remove the photoresist.

Several multiple die-to-die bonding tests were performed according to this procedure. However, we observed problems in removing the photoresist in some III-V dies. These dies would immediately detach after unloading from the wafer bonder, as shown in Figure 4.18b. Also, the bonding layer uniformity was not very good, with a distinctive thin BCB bonding layer at the edge and thick in the centre of the III-V die.

In the next series of bonding tests the III-V dies were not attached to the top Pyrex wafer. All the pre-bonding preparation of the III-V dies (including SiO_2 deposition) was carried out working with individual dies that were manually placed on a SOI die (after spin-coating BCB:mesitylene solution and baking it on a hot plate). The III-V dies were then covered by a graphite foil and the top Pyrex glass and loaded into a wafer bonding tool. Results of two tests carried out according to this procedure were successful, as illustrated in Figure 4.19a.

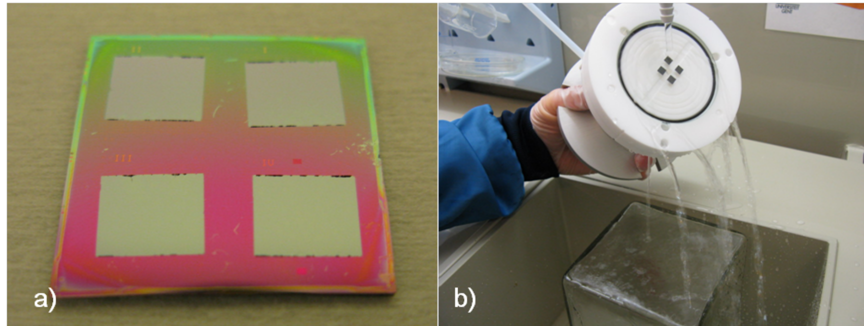

Figure 4.19: Multiple die-to-die bonding tests: a) tests with individual die handling during wet etching and SiO_2 deposition immediately prior to bonding gave good results; b) vacuum chuck for handling multiple dies allows simultaneous wet etching and rinsing of the III-V dies.

Despite excellent bonding yield achieved in these tests, the fact that the III-V dies needed to be handled individually, was a disadvantage of this method. To allow simultaneous handling of multiple dies, including the wet etching steps, a specially designed vacuum chuck was ordered from the Swiss company Idonus. As illustrated in Figure 4.19b, the chuck allows mounting of several dies (interchangeable plates for handling 4, 8, 16 or 32 dies are available). Wet etching in the aggressive acidic solutions used for the removal of sacrificial layers is also possible. An additional advantage of this vacuum chuck was the ability to turn the III-V dies upside down and detach them at a desired location on an SOI die (or wafer). The initial tests performed using this tool showed some promising results, but also revealed problems in releasing the III-V dies (due to wetting of the back side of the dies and surface tension).

Unfortunately, there was no time to continue with multiple die-to-die bonding tests and further improve the bonding process. Thus, the development of this procedure remains as a goal for future work.

4.6 Conclusions

In this chapter, we have presented a die-to-die adhesive bonding procedure, based on the use of DVS-BCB, suitable for the heterogeneous integration of III-V dies on top of SOI photonic waveguides. The demonstrated BCB bonding layers thickness is less than 100 nm, which is sufficiently thin for efficient evanescent coupling between III-V semiconductor layers and silicon waveguides. Several problems that occurred during the development of the bonding procedure were solved by modifying specific steps in the pre-bonding die preparation and the

bonding recipe itself.

In the final version of the bonding procedure, pre-bonding preparation of the SOI dies included treatment with hot Piranha and SC-1 solutions, spin-coating the adequate BCB:mesitylene solutions and baking on a hot plate. The preparation of the III-V dies comprised wet etching steps to remove InP and InGaAs sacrificial layers, with subsequent deposition of a thin (~ 10 nm) layer of SiO_2 in a PECVD tool.

The bonding process showed good bonding yield and solid bonding strength (with the dies detaching at shear stress of 2 MPa). Uniformity of the bonding layer thickness proved to be dependent not only on the concentration of DVS-BCB in the BCB:mesitylene solutions used for the bonding, but also on the topography of the SOI dies. The bonding layer uniformity and thickness proved to be the most difficult parameters to control. Rich SOI die topography (with 220nm-deep trenches) and BCB:mesitylene solutions with higher content of DVS-BCB, resulted in thicker and less uniform bonding layers. The best results were achieved using planarized SOI dies and 1:5 BCB:mesitylene solutions, with a BCB bonding layer thickness in the range between 40 nm and 70 nm.

Such bonding layers are suitable for fabrication of evanescently-coupled hybrid III-V/Si lasers, as presented in Chapter 3. Although primarily targeted for hybrid lasers and optical amplifiers, this bonding procedure can also be used for fabrication of photodetectors based on evanescent coupling.

A series of multiple die-to-die bonding tests showed the importance of uniform distribution of the bonding pressure over a larger area. Relatively good results were obtained using a graphite foil and manual handling of the individual dies. However, the critical issue in these tests proved to be the solution for simultaneous handling of a multitude of III-V dies. In order for this bonding process to have any potential for industrial-scale fabrication, the problem of simultaneous handling and preparation of III-V dies needs to be solved. The vacuum chuck developed for this purpose could be a step in the right direction, but further tests with this tool are required.

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5

Fabrication of Hybrid Evanescent III-V/Silicon Lasers

In this chapter, we will present details of the fabrication of the hybrid III-V/Si lasers. In a broader context, the bonding procedure described in the previous chapter is also a part of the hybrid laser fabrication process. However, the focus of this chapter will be on the processing steps that follow after the bonding of a III-V die on an SOI die with the silicon rib waveguides. First, a general layout of the devices will be presented. After this, the post-bonding preparation steps for further processing of III-V epi layers will be discussed. Then, a general overview of the process flow will be presented, followed by the details of each processing step. Problems that were encountered and optimization steps that were undertaken will also be outlined. The concluding remarks will be given at the end of the chapter.

5.1 General layout of the hybrid III-V/Si lasers

Details of the structure of the hybrid III-V/Si laser based on evanescent coupling have already been presented in Chapter 3. Here, we will give just a short overview of some of the design aspects that were not discussed in full detail in Chapter 3.

As we have seen in sections 3.1 and 3.5, the layout of the III-V semiconductor

functional layers is essentially the same for both Fabry-Perot and DFB lasers. Consequently, both types of hybrid lasers share the same III-V processing steps, which will be presented later in this chapter. As mentioned in section 3.5, both DFB lasers and phase-shifted DFB lasers are designed, with differences in total device length. Nominal lengths of both Fabry-Perot lasers and phase-shifted DFB lasers vary from 500 μm to 900 μm (in steps of 100 μm), while the lengths of DFB lasers vary between 150 μm and 350 μm (in steps of 50 μm) for the first-order gratings and between 200 μm and 500 μm (in steps of 100 μm) for the second-order gratings.

It was envisioned to fabricate a multitude of hybrid III-V/Si lasers from a single piece of III-V film bonded on a patterned SOI die. The individual devices were to be organized in rows and columns. Devices on a given row would be fabricated along the same Si rib waveguide on an SOI die, while devices having the same length would be placed in a single column. After the completion of device processing, the individual bars, each comprising a single column of hybrid lasers, would be either cleaved or diced and polished. This would allow testing of individual hybrid lasers and coupling its optical output via optical fiber to either optical power meter or optical spectrum analyzer (OSA).

From the point of view of III-V semiconductor processing, two types of devices were designed: stand-alone lasers and lasers with integrated photodiodes. Fabry-Perot lasers and phase-shifted DFB lasers, sharing the same nominal lengths, were designed as stand-alone lasers. DFB lasers, having shorter lengths, were designed with the adjacent integrated photodiode, as illustrated in Figure 3.27, in section 3.5.

The general layout of both of these devices is illustrated in Figures 5.1 and 5.2. Top view of the devices is given in Figure 5.1, while the schematic cross-sections of the hybrid III-V/Si lasers in planes AA' and BB' are illustrated in Figure 5.2. The width of III-V mesa in all devices is 16.8 μm and the carrier injection channel is 3 μm wide. To distinguish the metallization layers deposited before and after proton implantation, they are represented with different colours in Figure 5.2. As explained in section 3.4.1, p-type metallization which is deposited before proton implantation, acts as a mask protecting the underlying layers from the incoming protons. The total width of the p-type metallization is 52.8 μm, which is sufficiently wide to overlap 15 μm with the n-type metallization on both sides of III-V mesa, as illustrated in Figure 5.2. In this way, the n-type InP spacer layer located beneath the p-type metallization is protected from the proton implantation and can perform its function.

Metallization which is deposited after the proton implantation on both n-type and p-type contacts serves as a probing layer - a relatively thick, protective layer on which the probe needles are placed while testing the device. As shown in Figure 5.1, a single 70 μm × 70 μm contact pad is designed for the p-type met-

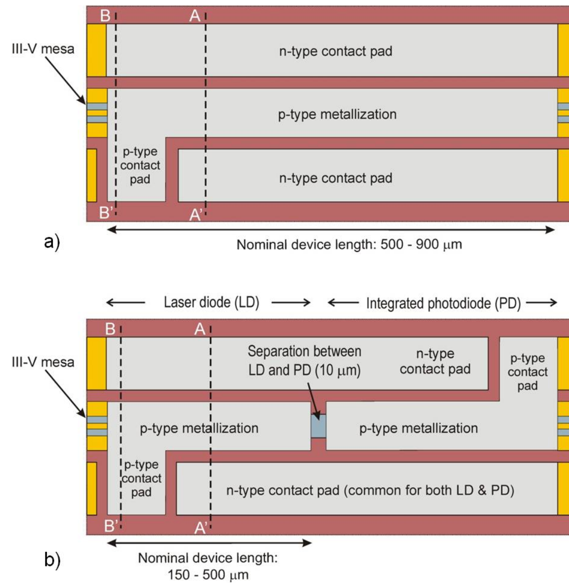

Figure 5.1: Top views of the two types of devices: a) stand-alone hybrid III-V/Si laser (Fabry-Perot or phase-shifted DFB laser); b) DFB hybrid III-V/Si laser diode (LD) with an adjacent integrated photodiode (PD).

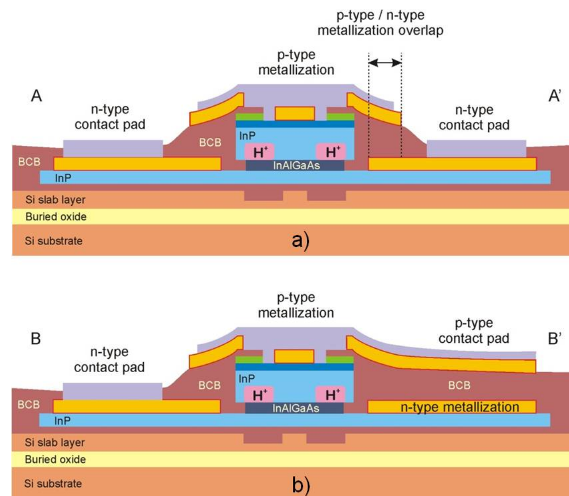

Figure 5.2: Cross-section of the hybrid III-V/Si lasers, at two distinctive perpendicular planes: a) cross-section along direction AA'; b) cross-section along direction BB', where a p-type contact pad completely overlaps the underlying n-type metallization. Metallization deposited after the proton implantation is presented in grey colour.

allization, both in the hybrid laser and the integrated photodetector. The probing layer for n-type metallization on both sides of the III-V mesa is 60 μm wide, which is sufficiently wide for placing the contact needles. The gap between the p-type metallization of the laser diode and the integrated photodiode is 10 μm.

The buffer zone between the devices in the adjacent columns is 100 μm wide. When the individual columns are cleaved at the end of the device processing, the cleaved facets would ideally lay within this buffer zone. The probing layer of metallization is not deposited here, but both the p-type and n-type metallization extend through this region in order to insure carrier injection into this zone after the device is cleaved. Alternatively, individual bars with the columns of devices can be diced and the facets can be subsequently polished.

The length of the probing metallization layer in hybrid lasers is equal to the nominal length of the devices. On the other hand, the actual length of the Fabry-Perot devices is determined by the distance between the cleaved facets, which is usually somewhat longer than the nominal device length.

5.1.1 Layout of the SOI dies used for the hybrid lasers

The SOI dies, designed for fabrication of the hybrid III-V/Si lasers had dimensions of 20 mm × 20 mm. The silicon rib waveguides were grouped into four quadrants, each containing 8 mm long rib waveguides. It was planned for a single III-V die to be bonded on a single quadrant within an SOI die and be used for subsequent processing. As both wafers with 20nm- and 30nm- deep corrugations were fabricated using the same lithographic mask, the grating lengths optimized for both corrugation depths were placed in the design. Three quadrants contained waveguides with the 2nd-order gratings, while the fourth quadrant was designed with the 1st-order gratings. The targeted duty cycles were 75% for the 2nd-order gratings and 50% for the 1st-order gratings. However, some overetching was expected during the grating fabrication process. Therefore, three sets of waveguides were designed for the 2nd-order gratings, with duty cycles of 75%, 80% and 81.25%. Also, two sets of waveguides were designed for the 1st-order gratings, having duty cycles of 55% and 62.5%.

The duty cycles that were actually achieved in the fabricated wafers were somewhat different. Among the 2nd-order gratings, only those with a designed 75% duty cycle were successfully fabricated. The actual duty cycle was around 68%. A top view SEM image of this grating is shown in Figure 5.3a. Corrugations with a nominal duty cycle of 80% were not properly fabricated, exhibiting incomplete and irregular shapes, as illustrated in Figure 5.3b. Corrugations with a 81.25% duty cycle were not fabricated at all. On the other hand, fabrication of the 1st-order gratings was more successful, as illustrated in Figure 5.4. However, instead of the designed duty cycles of 55% and 62.5%, the actually achieved duty

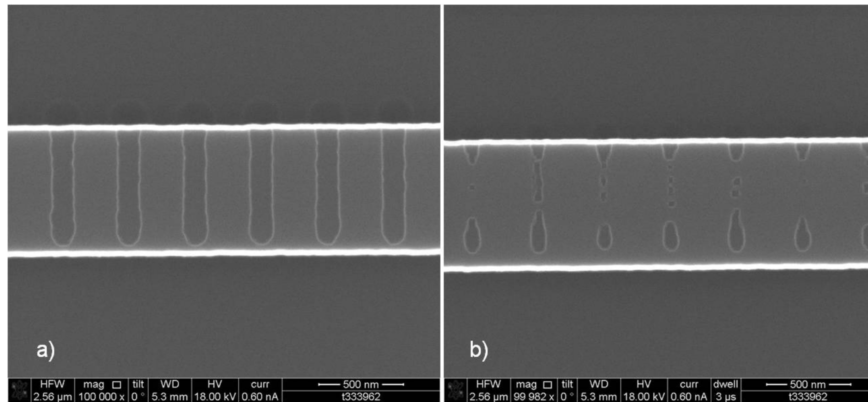

Figure 5.3: SEM of the 2nd-order gratings on top of a Si rib waveguide: a) for the designed duty cycle of 75% (the actual duty cycle is ~ 68%); b) for the designed duty cycle of 80%.

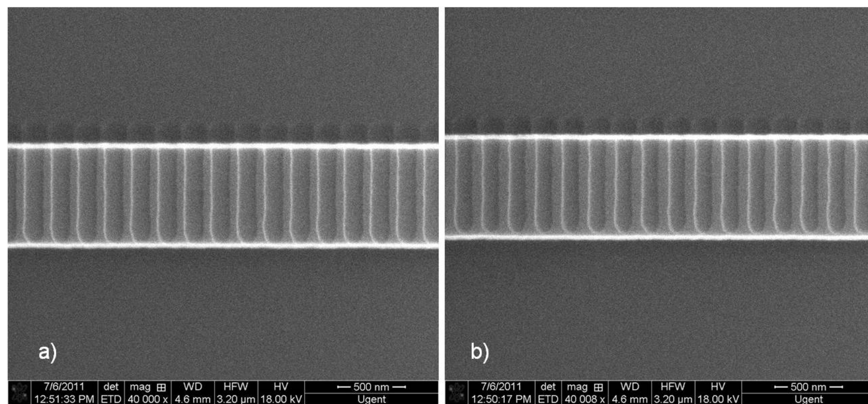

Figure 5.4: SEM of the 1st-order gratings on top of a Si rib waveguide: a) for the designed duty cycle of 55% (the actual duty cycle is ~ 34%); b) for the designed duty cycle of 62.5% (the actual duty cycle is ~ 45%).

cycles were around 34% and 45%, respectively.

5.2 Post-bonding preparation for lithographic processing

After the bonding of a III-V die to a desired quadrant of an SOI die, the InP substrate is removed via combination of grinding and wet-etching, as described in section 4.3. However, chemical wet etching of InP using an aqueous solution

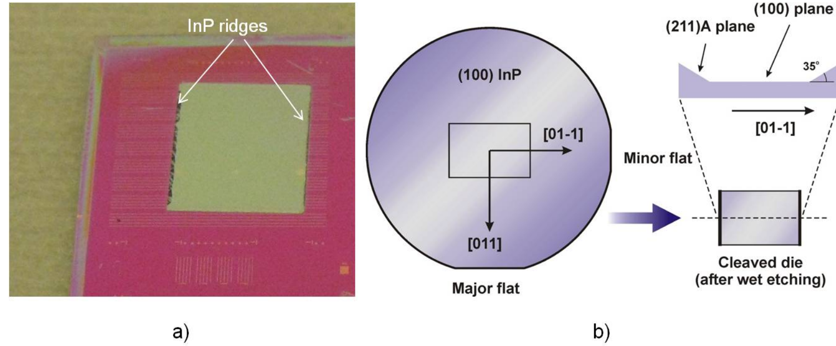

Figure 5.5: Ridges at the edge of the bonded III-V film: a) III-V film after substrate removal by wet etching in HCl; b) crystallographic directions and planes in a InP wafer and position of the ridges formed due to anisotropic etching in HCl.

of HCl is anisotropic. Consequently, unetched ridges (or ramps) are formed at two opposite edges of the bonded III-V film, as illustrated in Figure 5.5a. The slopes of the ridges are formed along the (211)A crystallographic plane, which forms an angle of ~ 35 ° with the surface of the bonded film, laying in the crystallographic plane (100) [1]. The ridges are formed because HCl doesn't etch the exposed (01-1) planes of the InP die [2]. Planes (011) and (01-1) are exposed by cleaving of the III-V dies grown on (100) InP substrate. The orientation of the (01-1) plane along which the ridges are formed is parallel to a minor flat on the original III-V wafer, as illustrated in Figure 5.5b.

These unetched ridges can be up to several tens of micrometers high and consequently prevent the intimate contact between the lithographic mask and the sample. In the contact lithography, used for III-V semiconductor processing, this prevents definition of narrow features, such as 3μm-wide p-type metallization central stripe that is used as a proton implantation mask to create a carrier injection channel. Therefore, it is essential to eliminate these ridges before starting with III-V semiconductor processing.

One way to eliminate the ridges is to perform an isotropic, but non-selective chemical wet-etching of the edges of the bonded III-V film. To protect the III-V film and expose only the ridges, we used proximity lithography and the photoresist AZ5214E, from MicroChemicals GmbH. Initially, in our experiments we used an isotropic wet-etching procedure based on 1:1 $HCl_{(37\%\ aq.)}$: $HNO_{3\ (65\%\ aq.)}$ solution, as previously reported in literature [3]. However, sometimes the results were not satisfactory, as this solution proved to be very aggressive and the photoresist could not always provide the best protection. Additionally, the solution is volatile and should be used immediately after

preparation. The etch rate in a freshly-made solution is > 15 μm/min, but this can drop to ~ 5 μm/min after 15 minutes. As an alternative, we started using an isotropic wet-etching procedure based on a solution of sodium chlorate ($NaClO_3$), hydrochloric acid (HCl), acetic acid (CH_3COOH) and H_2O, based on a recipe reported in a PhD thesis of Youcai Zhu [4]. This solution also needs to be freshly made and used, but the achieved results were more stable and the photoresist, acting as a mask, was not damaged. As a drawback, it can be noted that the observed etch rate of ~ 1μm/min is relatively low.

Another way to avoid formation of the ridges is to saw the III-V dies (instead of cleaving) in such a way not to expose the (01-1) crystallographic plane. However, this might not be the best solution in view of further III-V die processing. Namely, in the process of lateral undercut etching of the III-V mesa, it is useful to have either (01-1) or (011) crystallographic plane exposed as directions from which InAlGaAs is underetched. Based on the results for wet etching of InGaAs [5], it can be concluded that the etch rates are the same in both directions and lower than the etch rate in <100> direction, which might help achieve better control over the extent of the mesa undercut.

5.3 Process flow - a general overview

After removing InP ridges at the edges of a bonded III-V die, the processing of the III-V semiconductor layers can start. The process flow for the fabrication of III-V/Si hybrid lasers is schematically presented in Figure 5.6. The first processing step is the definition of the, so-called, III-V semiconductor islands, where the individual hybrid lasers will be fabricated. In this step, the III-V layer stack is completely etched in the designated areas in order to create the "islands" of III-V material stretching along the individual silicon rib waveguides. In this way, hybrid lasers that are fabricated on top of different silicon rib waveguides are galvanically isolated. On the other hand, the lasers fabricated along the same rib waveguide will be galvanically isolated by discontinuous p-type metallization and eventual cleaving or dicing of the bonded die.

The next processing step is definition of the III-V mesa. In this step, a deposited SiO_x layer is used as a hard mask to allow etching the III-V layer stack all the way to the n-type InP spacer layer, in order to form III-V mesas on top of the silicon rib waveguides. In the next step, n-type metallization is deposited on the InP spacer layer. After this, a relatively thick layer of DVS-BCB is spin-coated over the structures and cured to serve as a protective layer and electric insulator. In the next processing step, openings (or windows) are etched in the BCB layer on top of the III-V mesas. Also, the SiO_x layer acting as a hard mask during III-V mesa definition is etched away. In this way, the ohmic contact layer (p^+-InGaAs) is exposed and ready for p-type metallization. Because the BCB layer covering

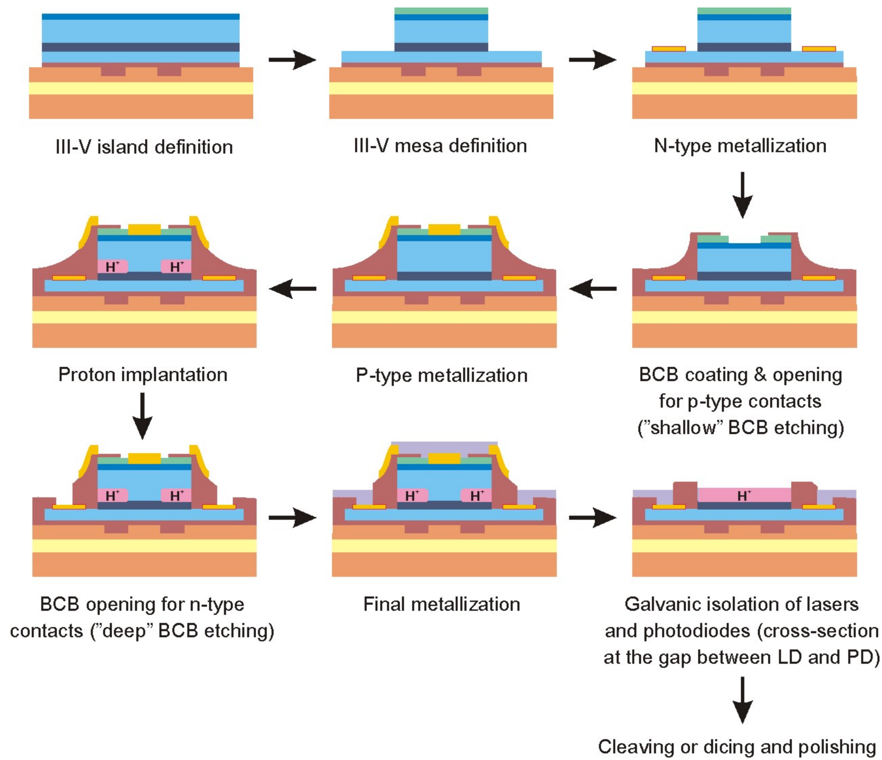

Figure 5.6: Process flow for the III-V/Si hybrid lasers fabrication showing cross-sections of the device at the various processing steps. A cross-section of the device structure at the gap between a laser diode (LD) and a monitor photodiode (PD) is presented in the step of galvanic isolation.

the III-V mesa is relatively thin (< 600 nm), compared to the layer of BCB on top of the InP spacer layer (~ 2 μm), this processing step is named "shallow" BCB etching.

Following this, a p-type metallization is deposited in the next processing step. This relatively thick metallization plays also the role of the mask for the subsequent proton implantation. After the proton implantation is completed, another BCB etching step is performed. This time, the windows are made to expose the previously deposited n-type metallization. As the etching is made through a relatively thick BCB layer, this processing step is named "deep" BCB etching. After this, the final layer of metallization (i.e. the probing layer) is deposited on both n-type and p-type contacts. In the next processing step, a galvanic separation between the hybrid lasers and the adjacent integrated photodiodes is performed by etching the highly doped ohmic contact and top cladding layers in the part of the III-V mesa between the laser diode and the photodiode. In the end, the bars containing a column of individual hybrid III-V/Si lasers, are finally cleaved or diced and polished to allow optical characterization of the individual devices.

This sequence of processing steps was imposed by the thermal budget of the proton implantation process. As mentioned in section 3.4.1, after proton implantation, the temperature of the sample should not exceed 410 °C. Otherwise, p-type InP layers will again become electrically conductive due to annealing of the crystal lattice. The fast-alloying step, in which this temperature is reached (and slightly exceeded) is necessary to form a good n-type ohmic contact. On the other hand, the p-type metallization itself serves as a mask for proton implantation. Therefore, it was necessary to perform both n-type and p-type metallization steps as well as the fast-alloying step before the proton implantation.

After presenting this general overview of the process flow, we will now focus on the details of the individual processing steps.

5.4 Process flow - details of the individual processing steps

5.4.1 III-V island definition

As previously mentioned, the first step in processing of the bonded film of III-V semiconductor layers is the definition of the III-V islands. Before any lithography is performed, two etch-stop layers of InGaAs and InP, each of them 100 nm thick, are removed by chemical wet etching techniques. The etching of the InGaAs layer (lattice matched to InP) is performed by dipping the sample for 10 seconds into a 1:3:1 H_2SO_4 $_{(95\%\ aq.)}$:H_2O_2 $_{(30\%\ aq.)}$:H_2O solution. InP etch-stop layer is removed by 15 seconds dipping into a 3:7 HCl $_{(37\%\ aq.)}$:H_3PO_4 $_{(85\%\ aq.)}$

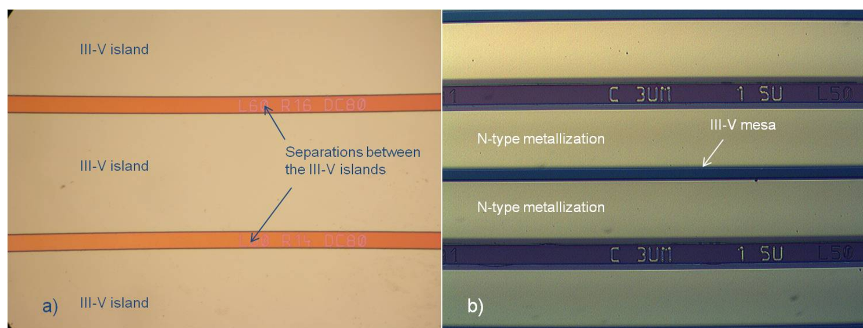

Figure 5.7: Microscopic images of the sample at various stages of the III-V processing: a) sample after III-V island definition; b) sample after completion of the n-type metallization processing step.

solution. After this, the sample is rinsed with DI water and dried. Removal of the etch-stop layers, with a combined thickness of 200 nm was confirmed using a contact profilometer Dektak 150 (from Veeco Instruments, Inc.) and by measuring profiles of the bonded III-V film before the wet etching and afterwards.

After this, the lithography is performed using photoresist AZ5214E. In general, this specific photoresist is capable of image reversal, but in this particular step, it is used as a positive photoresist. Following the lithography, the exposed III-V layers are removed by four wet etching processing steps. In the first etching step, the 100nm-thick p^+-InGaAs ohmic contact layer is removed using a 1:1:8 H_2SO_4:H_2O_2:H_2O solution. In the next step, a 1.5μm-thick InP cladding is etched in a 3:7 HCl:H_3PO_4 solution. Quaternary layers (made of InAlGaAs) are also etched in a 1:1:8 H_2SO_4:H_2O_2:H_2O solution, while the last layer - the 240nm-thick InP spacer layer is eventually etched in a 3:7 HCl:H_3PO_4 solution.

Following the wet etching steps, the photoresist is removed by rinsing with acetone, IPA and DI water. A look of the sample after this processing step is given in Figure 5.7a. The "islands" or "stripes" of the bonded III-V material stretching along the silicon rib waveguides are separated by regions where the III-V materials were completely etched away. The contact profilometer was used once again to measure the profile of the bonded III-V film and verify that all the layers of the bonded III-V thin film were etched away.

5.4.2 III-V mesa definition

The next processing step, definition of the III-V mesas, starts with the deposition of silicon oxide (SiO_x) which acts as a hard mask for subsequent etching steps. Prior to SiO_x deposition, the sample is cleaned using oxygen plasma in a reactive ion etching (RIE) tool in order to remove any remaining traces of pho-

toresist. Following this, a one minute dip into 1:10 H_3PO_4:H_2O solution is used to remove the layer of native oxide formed on the top of p^+-InGaAs ohmic contact layer. After this, the sample is rinsed with DI water and dried, leaving a clean and oxide-free surface of InGaAs layer on the top of the sample.

At this stage, the sample is loaded into a PECVD tool and a 300nm-thick layer SiO_x is deposited on top of it. The deposition is performed at 300 °C. Following this, a lithography is carried out using AZ5214E as a positive photoresist. After development, the photoresist acts as a mask for the etching of the previously deposited SiO_x in an RIE tool. This plasma etching step is performed in a mixture of O_2 and SF_6. Once the etching is completed, the remaining photoresist is removed by RIE etching using a pure oxygen plasma, leaving only the deposited silicon oxide as a hard mask.

The following step is dry etching of the exposed III-V layers. This step is preferably performed via inductively coupled plasma (ICP) reactive ion etching process, although in some cases we have used a regular RIE system. Since dry etching is not selective, it is not easy to precisely etch all the III-V semiconductor layers down to the InP spacer layer. Therefore, the goal of this step is to etch the ohmic layer (InGaAs) and most of the top cladding layer (InP), leaving just around 100 nm to 200 nm of InP in the cladding layer unetched. After this, a selective chemical wet etching is performed using 3:7 HCl:H_3PO_4 solution, just to remove the remaining InP and reach the layers made of InAlGaAs.

Removing these functional layers (SCH, CB and MQW layers) is a critical step, as we also need to undercut the III-V mesa, and suppress the flow of the leakage current, as explained in section 3.4.2 of Chapter 3. Therefore, an isotropic chemical wet etching in a 1:1:8 H_2SO_4:H_2O_2:H_2O solution is used for this purpose. A 2 minute treatment is enough to etch away the InAlGaAs layers and make lateral undercuts in a III-V mesa, that are ~ 2.3 μm wide, as illustrated in Figure 5.8a. In the previous processing runs, a more diluted solution, 1:1:18 H_2SO_4:H_2O_2:H_2O, was used. In this case, the wet etching took 3 minutes and the undercut was usually ~ 1.5 μm, as illustrated in Figure 5.8b. However, in some cases using this more diluted "1:1:18" solution, we observed problems such as very low etch rates and not very good undercut reproducibility. For this reason, we switched to a more concentrated, "1:1:8" solution. However, to achieve reproducible etch rate and lateral undercut, stability of the hydrogen peroxide is critical. Therefore, the use of stabilized 30% H_2O_2 aqueous solution during this etching step is highly recommended.

After the etching is finished, the sample is rinsed with DI water and dried. It can be noted that, in theory, it is possible to modify the process flow by swapping the sequence of the island definition and the III-V mesa definition processing steps, so that mesa definition is performed first, followed by the III-V island definition afterwards. However, the tests that were performed using this

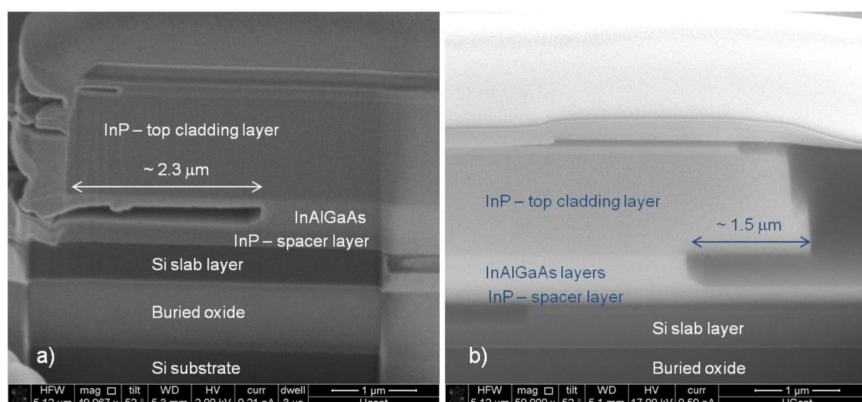

Figure 5.8: SEM image of the lateral undercut of the III-V mesa via wet etching of InAlGaAs layers: a) undercut of ~ 2.3 μm achieved after 2 minute etching in 1:1:8 H_2SO_4:H_2O_2:H_2O solution (material re-deposition around the edges is also visible); b) undercut of ~ 1.5 μm achieved after 3 minute etching in 1:1:18 H_2SO_4:H_2O_2:H_2O solution.

processing sequence pointed out to a hidden risk in this procedure. Deposition of SiO_x is performed at a relatively high temperature of 300 °C. In cases when there are traces of gases trapped at the bonding interface between the III-V film and the SOI die (indicated by the presence of 'blisters', as described in section 4.4.2), exposure to such a high temperature leads to a rapid expansion of the blisters which eventually burst, damaging large areas of the bonded III-V film. On the other hand, when the III-V islands are already formed, apparently, the outgassing of the trapped gases is easier and no bursting of the III-V film was observed when this processing sequence was followed.

5.4.3 N-type contact metallization

Similarly to the previous processing step, the n-type contact metallization begins with a one minute dip into a 1:10 H_3PO_4:H_2O solution, in order to etch away the layer of native oxide formed on top of the InP spacer layer. After rinsing with DI water and drying, the sample is ready for lithography.

The lithography is performed with a relatively thick layer (~ 2.5-3 μm) of AZ5214E used as an image reversal photoresist. The reason for this is that thicker layers of photoresist enable easier and more reliable lift-off procedure. The metallic layers are deposited in a Leybold Univex thermal evaporation and sputtering system. First, a 1nm-thick layer of nickel (Ni) is sputtered, followed by deposition of 150 nm of AuGe alloy (12% $_{(w/w)}$ Ge content), and 60 nm of Ni on top of it. Finally, another layer of ~ 150 nm of gold is deposited on the top.

The reason for deposition of the first, thin layer of nickel is to improve the adhesion of the deposited metal to the InP surface. The Scotch tape tests, that we performed with the deposition of AuGe alloy on Si and InP substrates, showed that sputtering of a very thin (~ 1 nm) layer of Ni on InP surface improves the adhesion of n-type metallization.

Following the metal deposition, a lift-off procedure is performed by dipping the sample in acetone for 15 to 30 minutes, after which the sample is rinsed and dried. Microscopic image of the sample after this processing step is illustrated in Figure 5.7b.

5.4.4 Shallow DVS-BCB etching

After the n-type metallization, the devices are covered by a protective layer of DVS-BCB which would also later provide an electric insulation between the p-type metallization on the top and the n-type electrodes located below, on the spacer layer, as illustrated in Figure 5.2. For this purpose, an undiluted Cyclotene 3022-35 resin is spin-coated (at 2000 rpm) on the sample and cured in an oven, according to a standard DVS-BCB curing procedure, as described in section 2.4.3.1 and illustrated in Figure 2.14. According to data provided by Dow Company, spin-coating at this rotation speed on a flat surface should provide an approximately 1.6μm-thick layer of the cured BCB film [6]. However, the topography of the sample is not flat, featuring the III-V mesas that are ~ 2.1 μm high, and the thickness of the cured DVS-BCB layer on top of the sample is not uniform. On top of the III-V mesas, the BCB thickness is usually ~ 300 nm, while above the n-type metallization, outside the mesas, the BCB is usually > 1μm thick.

Following the BCB curing, the lithography is performed and the sample is loaded into the plasma RIE system. Dry etching is performed in two steps, both based on using a mixture of O_2 and SF_6 gases. In the first process, the BCB is etched in an oxygen rich gas mixture (50:5 volume ratio), usually within 2 minutes. In the second process, which usually lasts 6 minutes, an SF_6 rich mixture (3:50 volume ratio) is used to etch the SiO_x layer on top of the III-V mesa. After this, the sample is rinsed with acetone, IPA and DI water and another RIE cleaning procedure in oxygen plasma is performed to remove any residues of the photoresist that could affect the quality of the p-type contact.

In this way, the ohmic contact on top of the III-V mesa is exposed again and ready for the deposition of p-type metallization. The width of this "window" in the BCB and SiO_x layers on top of the III-V mesa is 6.8 μm, leaving 5μm-wide regions at the edges of the III-V mesa with the SiO_x and BCB layers intact on top of them. In this way, the effective p-type contact is narrowed down to the central section of the III-V mesa, as another way to favour the flow of current

into this region and minimize the current leakage along the edges of the mesa.

Theoretically, the openings for the n-type metallizaton in the covering BCB layer could be made in this processing step, as well. At the first glance, this looks as a good solution which would simplify the process flow and reduce the number of lithography masks by one. However, in practice, this has not proved as the best solution. The photoresist, used as a mask for RIE etching, is also etched by the same plasma that etches BCB. In addition to this, after performing lithography, due to a non-uniform topography of the sample, a relatively thin layer of photoresist would be on top of the III-V mesa. As the thickness of the cured BCB layer on top of the III-V mesa (~ 300 nm) is much thinner than the BCB layer covering the n-type metallization (> 1 μm), the dry etching process would continue until the thick BCB layer is etched, and the window to n-type metallization is fully opened. However, by that time, the photoresist mask on top of the III-V mesa, may be etched away completely and the BCB on top of the mesa might be etched as well. As a result of this, the metallization would subsequently be deposited across the entire width of the III-V mesa, instead of only the central section of it.

5.4.5 P-type contact metallization

P-type metallization follows immediately after the shallow BCB etching. Similar to the procedure used for n-type metallization, lithography is performed with a thick layer of AZ4214E used as an image reversal photoresist. The lithography mask for this processing step contains 3μm-wide stripes that are used for defining the central electrodes which act as a proton implantation mask that defines the width of the carrier injection channel. Because of such a relatively small critical dimensions, the lithography parameters are very important, especially the first exposure of the photoresist.

After completing the lithography, the sample is loaded into Leybold Univex system for metal deposition. Initially, a 40nm-thick layer of Ti is sputtered on the sample, followed by thermal evaporative deposition of a 1.2μm-thick layer of gold. Once the deposition is completed, the sample is dipped into acetone for a lift-off procedure. Given the fact that the layer of deposited metals in this processing step is much thicker than in the case of n-type metallization, the lift-off procedure can take up to 60 minutes. As for any lift-off process, the edges of the photoresist need to have inverted slopes in order to have the good results. Also, it is essential to have sufficiently thick layer of photoresist prior to metal deposition.

After the lift-off is completed, the sample is rinsed and dried. The last processing step that is carried out prior to proton implantation is fast alloying. The goal of this processing step is to create an ohmic contact at the interface be-

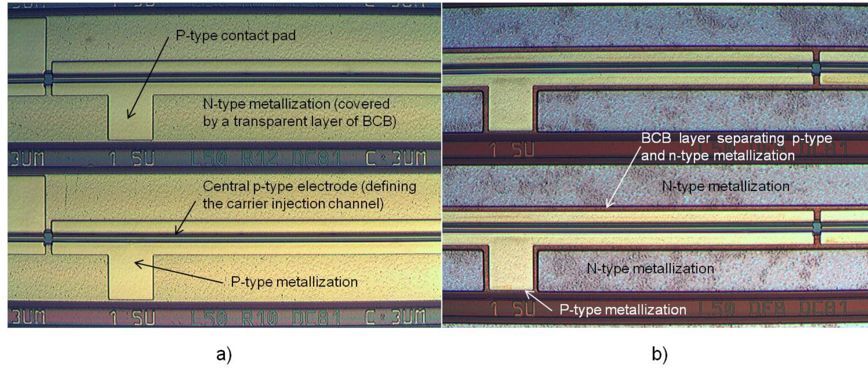

Figure 5.9: Microscopic images of the sample at various stages of the III-V processing: a) sample after p-type metallization, but prior to fast-alloying; b) sample after completion of the deep BCB etching processing step.

tween InP and n-type metallization. It is a rapid thermal alloying process, performed in a fast alloy oven, in the atmosphere of forming gas (1:10 mixture of H_2:N_2). This is a well-know process that has been reported in literature [7]. Within a minute, temperature rises up from room temperature to ~ 430 °C, after which the sample cools down to the room temperature. The forming gas is used as a reductive agent, to avoid oxidation of the metal during the heating step and to react with any traces of oxide present at the surface. During the thermal alloying, Au atoms diffuse down into InP, Ni atoms diffuse down through AuGe layer towards the InP surface, while In atoms diffuse upwards into a top Au layer [8]. As a consequence of these inter-diffusions, the colour of the n-type metallization, observed under the microscope, slightly changes after the fast-alloying step. This is illustrated in Figure 5.9 where the look of the devices prior to fast alloying and after deep BCB etching step can be compared.

5.4.6 Proton implantation

Following the fast-alloying, which is the last high-temperature processing step, the sample is ready for proton implantation. This processing step was carried out by the CuttingEdge Ions company from Orange, California. A single proton implantation step is performed at room temperature, according to parameters specified in section 3.4.1, Chapter 3, with a proton energy of E = 185 keV and a dose of $\Phi = 3.3 \times 10^{14}$ cm^{-2}. To avoid the channeling effect, the protons were implanted with an inclination angle of 7° with respect to the direction perpendicular to the sample surface. In addition, in order to avoid mask undercuting, as illustrated in Figure 5.10a, the protons were directed parallel to the SOI wave-

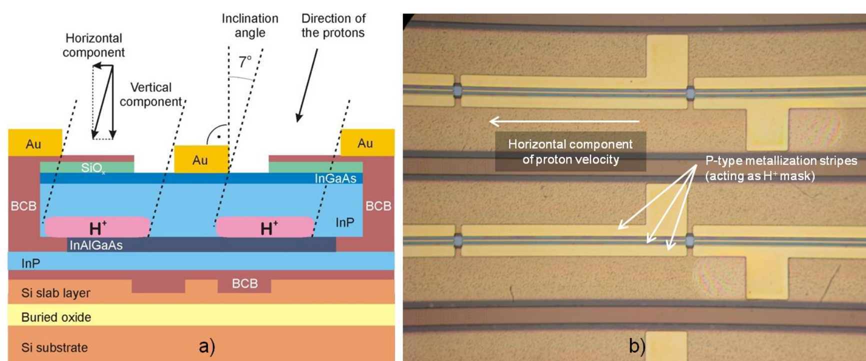

Figure 5.10: Proton implantation and proper positioning of the sample relative to the direction of the incoming protons. To avoid a "channeling" effect, protons are directed at the inclination angle of 7 °. a) If the horizontal component of the proton flux is perpendicular to the SOI waveguides and p-type metallization stripes, mask undercutting will occur, due to which the implanted regions will be shifted with respect to the position of the central p-type stripe. b) To avoid undercutting, the horizontal component of the proton flux should be directed along the SOI waveguides and p-type metallization stripes.

guides and p-type metallization stripes, as shown in Figure 5.10b.

5.4.7 Deep DVS-BCB etching

Upon finishing the proton implantation step, the processing continues with etching of the openings for n-type metallization in the covering BCB layer.

The lithography is performed with a thick layer (~ 2.5-3 μm) of photoresist and the sample is loaded into plasma RIE system. Dry etching of the BCB is performed using the same recipe as in the case of shallow BCB etching, with a 50:5 O_2:SF_6 gas mixture. Usually, the etching is completed within 7 minutes. It is important to have sufficiently long etching time in order to assure that all traces of BCB are etched away from the n-type metallization. To check if the BCB layer covering the n-type metallization has been removed, several individual hybrid lasers within a sample can be electrically probed to check if the resistance between the n-type metallization pads on the opposite sides of the III-V mesa is of the correct order of magnitude. After dry etching is completed, the remaining photoresist is removed by rinsing with acetone, IPA and DI water. Microscopic image of the devices after this processing step is given in Figure 5.9b.

5.4.8 Final contact metallization

Opening of the windows in the BCB layer for n-type metallization is followed by the final metallization step. The role of this step is to deposit the final layer (sometimes referred to as the probe layer) of metallization on both types of contacts that will be directly contacted with the probe needles. Lithography for this step is performed in a similar way as for the previous steps with metal depositon, employing a thick layer of photoresist. Deposition sequence includes sputtering a 40nm-thick layer of titanium, followed by thermal evaporation of a 500nm-thick layer of gold. As in the previous metallization steps, the lift-off procedure is performed in acetone and can take up to 60 minutes.

In the initial process flow, it was envisioned for the final metallization step to be performed via electroplating. This is much more cost-effective way of depositing relatively thick gold layers, compared to thermal evaporation, but requires one additional lithography step and a short dip into diluted aqueous HF solution. However, the initial results using this procedure were not satisfactory, as significant number of laser diodes turned out to be short-circuited after this step. Therefore, we switched to thermal evaporation which gave good results and more reliable processing.

5.4.9 Isolation of lasers and photodiodes

The final processing step involving lithography is galvanic isolation of laser diodes and adjacent, integrated photodiodes in the fabricated devices. In this step, a dry etching technique is used to etch the highly conductive p^+-InGaAs ohmic contact layer and the p-type InP cladding layer in the exposed region of the III-V mesa between the laser diode and the photodiode. The width of this etching window is 10 μm. In this way, p-type layers of the hybrid III-V/Si laser and the integrated photodiode are galvanically isolated, enabling separate biasing during device characterization. On the other hand, n-type metallization remains continuous and therefore can be used as a common electrode while testing a device.

Although, at this stage of device fabrication, metallization (or BCB) covers most of the III-V semiconductor materials, there are still exposed areas in the buffer zone, between the individual device columns, which have to be protected from the etching. Therefore, a relatively thick (~ 2.5 μm) protective layer of AZ5214E photoresist is spin-coated over the sample and image reversal lithography is performed in order to open only the etch windows at the desired locations, at both ends of the integrated photodiodes.

In our case, we have performed dry etching in an RIE plasma processing system using a two-step cycle, involving gas mixture of CH_4:H_2 in the first step and oxygen plasma in the second step. In principle, the same processing can be

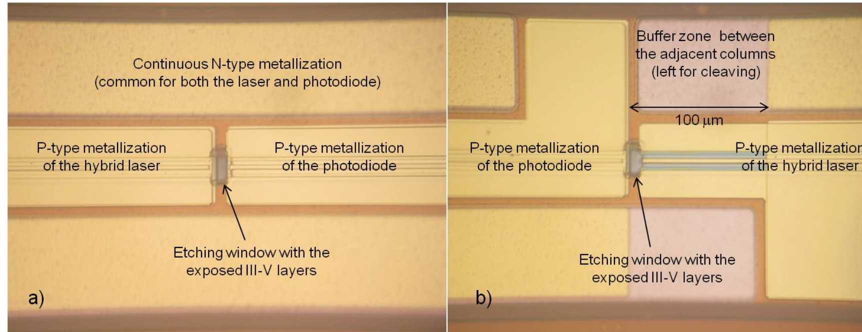

Figure 5.11: Microscopic images of the etching windows between hybrid lasers and monitor photodiodes that provide galvanic isolation for the p-type metallization: a) the gap between the hybrid laser and an adjacent monitor photodiode; b) the gap between the monitor photodiode and the hybrid laser from the adjacent column - a 100μm-wide buffer zone separates the adjacent device columns.

performed in an ICP RIE processing system.

Around 40 cycles were performed in order to etch ~ 1.5 μm of III-V semiconductor layers. In this way, only ~ 100 nm of p-InP cladding layer were left on top of quaternary InAlGaAs functional layers. According to the simulations performed using FIMMWAVE software, transmittance for the fundamental optical mode at such discontinuity in the InP cladding layer is ~ 97%. Microscopic images of the etching windows between laser diodes and adjacent photodiodes are given in Figure 5.11.

Following the etching, the sample is rinsed in acetone, IPA and DI water. In order to remove any traces of photoresist, a 10 minute ashing step in oxygen plasma is performed. Subsequent tests revealed that the electric resistance between the p-type contact pads of the laser diode and the adjacent photodiode is in general > 10 kΩ.

After this step, the individual devices can be tested on chip, before cleaving or dicing of the individual device bars.

5.4.10 Cleaving/dicing of the individual device bars

Cleaving was envisioned as the last processing step, carried out in order to isolate individual III-V/Si hybrid lasers along the same column and allow their individual testing and direct coupling of their optical output to optical fibers and photodetectors. Cleaving of the fabricated samples, which include an SOI die (~ 725 μm thick) and, on top of it, a few micrometers thick section comprising the bonded III-V film and the metallization, is not a very reproducible process.

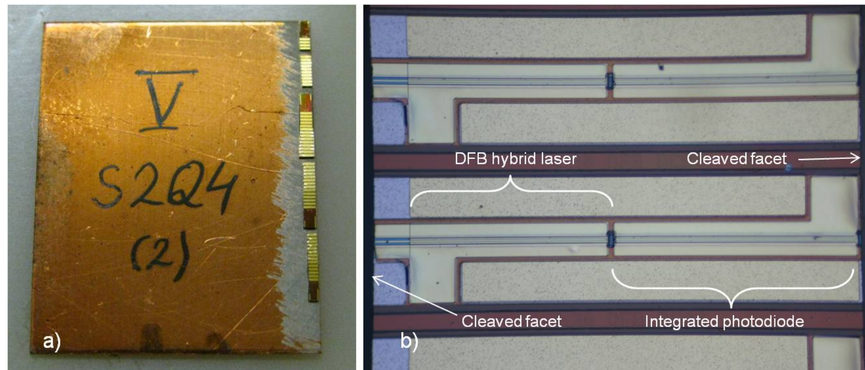

Figure 5.12: a) Cleaved device bars mounted at the right edge of a copper plate; b)Microscopic image showing individual hybrid III-V/Si lasers with integrated photodiodes on a cleaved device bar.

In order to achieve the best results and keep the cleaving lines as straight as possible, the silicon substrate of the SOI die needs to be thinned down in order to obtain a favourable aspect ratio between the width and the thickness of the cleaved bar. As the designed widths of the individual device bars varied between 600 and 1000 μm, we have thinned the fabricated samples down to ~ 150 - 180 μm, using the lapping tool and slurry with aluminum-oxide particles. Finally, the individual bars (containing the hybrid lasers) are cleaved and fixed on a copper plate using a silver epoxy resin, that is cured at 130 °C for 30 minutes. After this, the copper plate with the bonded bars is mounted on the optical setup and the individual devices are probed and characterized. One such a copper plate with the mounted device bars is illustrated in Figure 5.12a, while the microscopic image of the individual hybrid lasers on a cleaved device bar is given in Figure 5.12b.

Alternatively, the possibility of dicing the individual columns of devices from the fabricated sample was also envisioned. After dicing, the facets of the individual bars would be polished. However, both dicing and subsequent polishing steps assume substantial loss of material (several hundreds of micrometers per polished facet), and the buffer zone of 100 μm between the individual device columns (which is left for cleaving) is too narrow for these processing steps. Therefore, in the samples that were selected for dicing and polishing, only every other column of the devices was fabricated, leaving sufficiently wide areas without metallization between them. To allow this, an additional photolithography mask layer was designed which allowed protection of either odd or even columns of the devices. This mask was used in the image reversal lithography of the metal deposition steps in order to fabricate the columns without

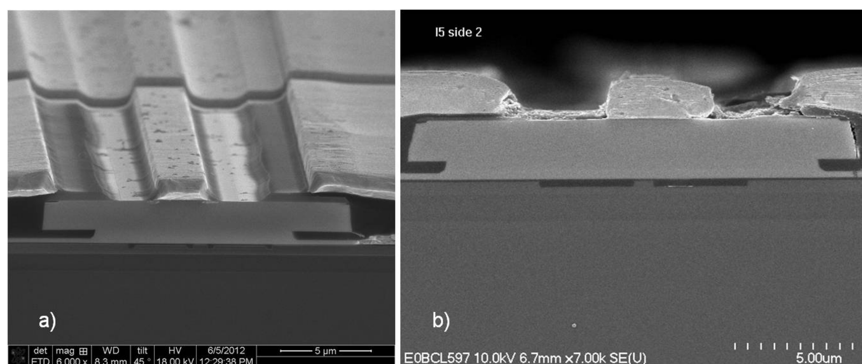

Figure 5.13: SEM images of the fabricated device facets: a) a cleaved facet; b) a diced and polished facet.

metallization, therefore allowing easier dicing and polishing in these areas.

Both dicing and polishing were performed by the external vendor, selected by Intel Coporation Photonics Technology Lab. In the initial dicing tests, problems with the metallization peeling off were observed. This led to modification of our metal deposition steps, including the initial Ni sputtering in the case of n-type metallization and use of thermal evaporation instead of electroplating, for the final metallization layer. In addition to this, chipping of the cured BCB layers was sometimes observed after dicing. To avoid this, an additional processing step was introduced to remove the cured BCB films in the buffer areas between the devices columns using plasma RIE techniques.

SEM imaging was used to inspect facets of both cleaved and diced/polished device bars. An example of one cleaved and one polished facet is illustrated in Figure 5.13. In principle, cleaving yielded more stable results, although in the best cases, dicing and polishing also yielded a relatively good-looking facets. However, occasional problems related to BCB layer chipping and cracking of III-V material were also observed in the diced and polished samples. As the details of dicing and polishing processing steps are not familiar to us, it is difficult to establish the root causes for these problems. On the other hand, neither BCB chipping nor III-V material cracking were observed at the cleaved facets.

5.5 Conclusions

The fabrication of the hybrid, evanescently-coupled III-V/Si lasers was presented in this chapter. Details of the device layout and the used SOI dies were also given, but the details of the DVS-BCB bonding step, which is the subject of the Chapter 4, were excluded. The focus of this chapter was on the post-

bonding processing of the bonded samples and eventual fabrication of the hybrid III-V/Si lasers.

The process flow that was presented evolved over a period of time and eventually yielded working hybrid lasers, as we shall see in Chapter 6. Existence of the proton implantation step, imposed a need to perform both n-type and p-type metallization, as well as the high-temperature fast alloying step, before the proton implanation. Separation of the BCB etching steps for opening the p-type and n-type contacts into two separate steps enabled much better control over the layout of the BCB and SiO_x layers on top of the III-V mesa and the actual width of the top contact between the p-type metallization and InGaAs ohmic contact layer. Also, the undercut etching of InAlGaAs layers of the III-V mesa, during the mesa definition step, proved to be a reliable, although a critical processing step, enabling an effective way to suppress carrier leakage near the III-V mesa edges.

Eventual cleaving of the fabricated devices, in principle, resulted in less problems that the approach including dicing and polishing of the facets. Occasional chipping of the cured DVS-BCB film was reported during dicing and polishing of the fabricated hybrid III-V/Si lasers. However, since these procedures were performed by an external vendor, we can't reach firm conclusions on the real causes of these problems. Obviously, optimization of the sample dicing and polishing procedures should be included in the future work.

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[8] James L. Merz. *Investigation of InP Processing Techniques for Device Applications.* Technical report, University of California, Department of Electrical and Computer Engineering, January 1990.

6 Characterization of Hybrid Evanescent III-V/Si Lasers

Following the description of the fabrication of the hybrid, evanescently-coupled III-V/Si lasers, in this chapter we will now focus on the characterization of these devices. Results of the characterization will be presented for the devices from two different processing runs (or batches). Fabry-Perot hybrid lasers have been fabricated in the first processing run and, therefore, we will first present the results for these devices. Distributed feedback (DFB) lasers have been fabricated in the second processing batch and characterization of these devices will be presented in the second part of this chapter. Beside standard measurements of the electrical and the optical properties, optical spectral measurements were used to asses the thermal resistance of both Fabry-Perot and DFB hybrid III-V/Si lasers. The obtained results are discussed and conclusions are given at the end of the chapter.

6.1 Characterization of Fabry-Perot hybrid III-V/Si lasers

After completing the fabrication, devices from this processing batch were cleaved and mounted on copper plates, as described in section 5.4.10. The

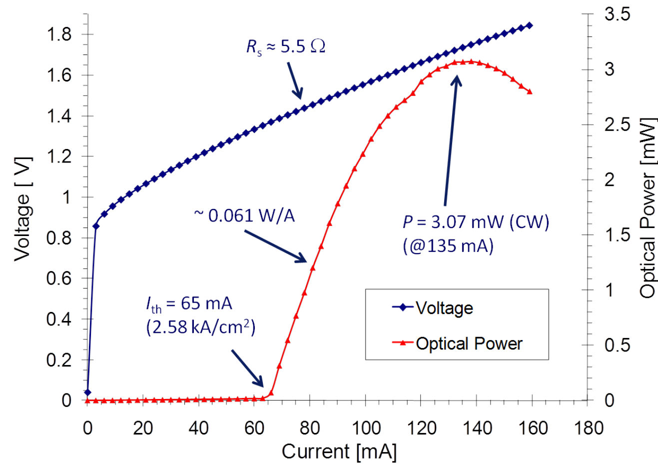


Figure 6.1: I-V and L-I plots of a Fabry-Perot hybrid III-V/Si laser in a continuous-wave (CW) regime, without temperature control setup. The actual length of the tested device is 840 μm.

cleaved devices were tested with both DC and pulsed current sources. The output power of the tested laser was measured at one facet of the device using a large-area photodetector positioned in close proximity to the facet, so that practically all the emitted optical power from that facet was detected.

In the initial tests, probing of the devices was performed at room temperature and no active temperature control scheme was used. Typical current vs. voltage (I-V) and optical power vs. current (L-I) plots are given in Figure 6.1. In this particular case, the actual length of the tested device is 840 μm (from facet to facet). The turn-on voltage is 0.9 V, the series resistance is ~ 5.5 Ω and the threshold current (I_{th}) is 65 mA. The measured series resistance is lower than values of 7.5 Ω [1] and 11.5 Ω [2], previously reported for 860μm-long, Fabry-Perot hybrid III-V lasers fabricated using direct bonding. Given the device length and assuming the width of the current injection channel to be 3 μm, the threshold current density (J_{th}) is 2.58 kA/cm^2. Maximum optical power in continuous-wave (CW) regime is 3.07 mW, while the slope efficiency (single-sided) is 0.061 W/A. For a 1310 nm wavelength, this corresponds to a differential quantum efficiency η_d of 6.4 %. However, since the light is emitted on the other facet as well, we should speak of a combined, double-sided, differential quantum efficiency of 12.8 %. In the remainder of this chapter we will express slope efficiency for a single-sided optical output (which is easy to assess from a typical L-I curve), but the differential quantum efficiency will be expressed taking into account both facets.

Ideally, if we could have identical hybrid III-V/Si lasers that only differ in the total device length, it would be possible to estimate the internal quantum efficiency of the devices (η_i) using the following relation [3]:

$$\frac{1}{\eta_d} = \frac{\alpha_i}{\eta_i \ln(1/R)} L + \frac{1}{\eta_i} \tag{6.1}$$

where α_i is the net internal optical loss and R is the mean mirror reflectivity, $R = r_1 r_2$ (where r_1 and r_2 are the amplitude reflection coefficients of the facets). From the plot of the differential quantum efficiency (η_d) versus the device length (L), one could estimate the internal quantum efficiency η_i from the intercept and the internal optical loss α_i from the slope. However, this is only possible if all the devices have identical internal optical loss, facet reflectivities and internal quantum efficiency.

Unfortunately, in the case of our Fabry-Perot devices from the first fabrication batch, it was not possible to reliably estimate these parameters using the equation 6.1. First of all, calculations of the differential quantum efficiencies of the lasing devices revealed that these varied between 8.6 % to 12.8 %, but there was no monotonously increasing dependence of the inverse differential quantum efficiency ($1/\eta_d$) versus device length. This clearly indicated that the individual lasers differed in other aspects, aside from the length. In addition to this, it turned out that most of the lasing devices had lengths of around 600 μm or 800 μm, making it relatively difficult to have a good estimation of these parametes based on virtually only two device lengths.

The optical spectrum of the devices was measured by coupling the output light into a single-mode fiber connected to an optical spectrum analyzer (OSA). Typical optical spectra of the hybrid laser at the injected currents of 100 mA and 130 mA, are presented in Figure 6.2. The longitudinal modes, characteristic of Fabry-Perot lasers, are clearly visible. The best observed side-mode suppression ratio (SMSR) was around 19.3 dB. Also, a relatively large spectral shift was observed with increasing injected current. As illustrated in Figure 6.2, with the current increase from 100 mA to 130 mA, the center wavelength shifts from 1317 nm to 1320.5 nm, which indicates a relatively strong self-heating of the device.

6.1.1 Temperature-controlled measurements

In the next round of measurements, temperature stabilization of the tested devices was achieved using a Peltier element. A copper plate, with the attached device bars was placed on a large metal pad under which a Peltier element is located. This setup is illustrated in Figure 6.3. Characterization of the devices was performed at fixed temperatures, both in CW and pulsed regime.

Typical L-I plots in CW regime, for two different devices, at temperatures of 10 °C, 15 °C, and 20 °C are given in Figure 6.4. The length of the tested de-

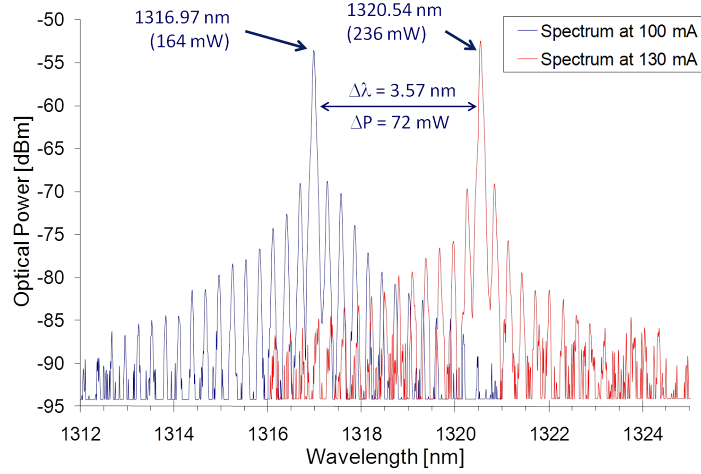


Figure 6.2: Spectra of a 900μm-long Fabry-Perot hybrid III-V/Si laser for the injected currents of 100 mA and 130 mA. The peak wavelength shift of $\Delta\ \lambda$ = 3.57 nm, for an increase in a dissipated power of ΔP = 72 mW, indicates a strong self-heating and suggest a relatively high thermal resistance of the device.

vices are 630 μm and 830 μm. For a 830 μm-long device, the threshold current at 20 °C is 92 mA (corresponding to a current density of 3.69 kA/cm^2), the maximum optical power at 20 °C is 1.71 mW, while the slope efficiency is 0.052 W/A (corresponding to η_d = 11.08%). At 10 °C, the threshold current is 68 mA (2.73 kA/cm^2), the maximum optical output power is 5.21 mW and the slope efficiency rises to 0.096 W/A (η_d = 20.34%). On the other hand, the 630-μm long laser has a threshold current of 64 mA (3.33 kA/cm^2) at 20 °C and the maximum optical power 1.09 mW. The slope efficency is 0.043 W/A (η_d = 9.04%). At 10 °C, the threshold current is 45 mA (2.38 kA/cm^2) and the maximum optical power is 2.95 mW, while the slope efficiency is 0.058 W/A (η_d = 12.32%). The fact that the differential quantum efficency η_d in a shorter device was found to be smaller than in a longer device, contradicts the relation of Equation 6.1 and indicates that the individual devices have different internal quantum efficiency η_i, internal loss α_i or mirror loss.

For comparison, differential quantum efficiencies of 12.7% and 11.8% were reported for direct-bonded Fabry-Perot lasers based on evanescent coupling [1] and adiabatic mode transformers [4], respectively.

In most of the devices, lasing in CW regime was not observed at 25 °C, indicating a strong self-heating of the devices and suggesting a relatively high thermal resistance.

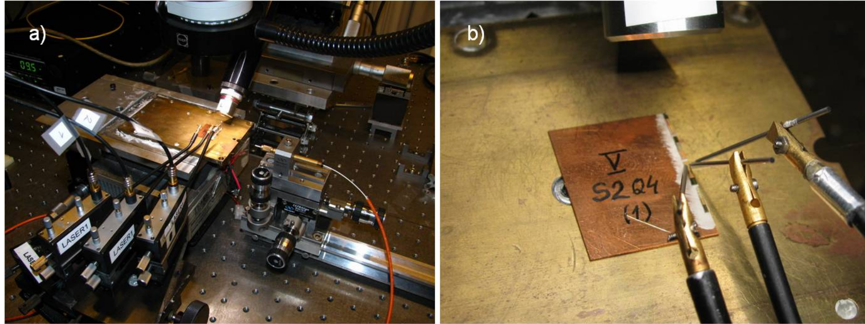


Figure 6.3: Experimental setup for temperature-controlled measurements: a) an overall layout of the setup; b) a close-up showing a copper plate with the cleaved device bars on a metal pad and the probing needles on a tested device. In this particular case, a multi-mode optical fiber was used to collect the output light from the hybrid lasers.

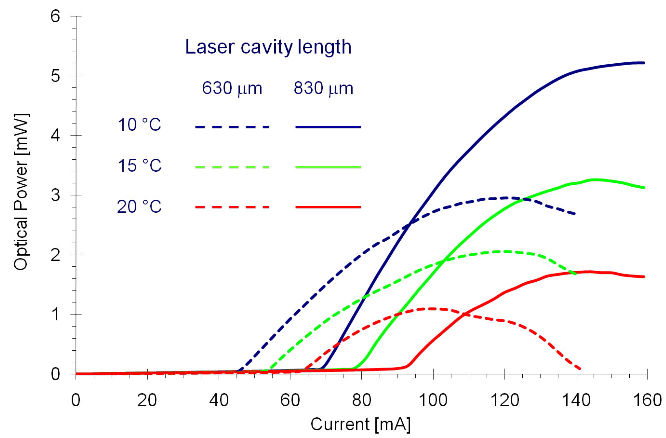


Figure 6.4: L-I plots of 630μm- and 830μm-long Fabry-Perot hybrid lasers in a CW regime obtained using a temperature controlled setup.

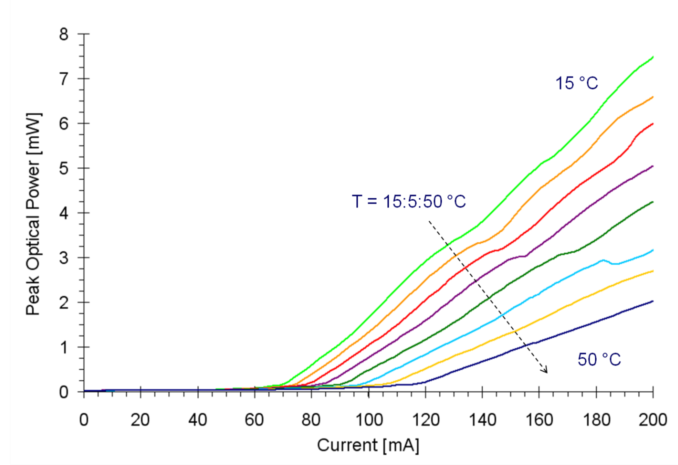


Figure 6.5: L-I plots of a 900 μm-long hybrid Fabry-Perot III-V/Si laser in a pulsed regime.

In the next step, devices were tested in pulsed regime. Typical L-I plots of a hybrid III-V/Si laser in a pulsed regime (5% duty cycle, 100 μs pulse repetition interval), in a temperature range from 15 °C to 50 °C are given in Figure 6.5. This particular Fabry-Perot laser has a 900μm-long cavity. As expected, there is no thermal rollover for injected currents up to 200 mA. Also, the lasing is observed up to 50 °C.

Based on these measurements in the pulsed regime, the temperature dependence of the threshold current I_{th} can be assessed. In general, this dependence is modeled with an exponential fit [3, 5]:

$$I_{th} = I_0 e^{T/T_0} \tag{6.2}$$

where T_0 is an overall characteristic temperature, while I_0 is another fitting parameter. Above the threshold, the current I necessary to obtain a desired optical power can also be modeled in a similar way with the following relation:

$$I - I_{th} = I_{p0} e^{T/T_1} \tag{6.3}$$

where T_1 is an above-threshold characteristic temperature, while I_{p0} is a fitting parameter.

Using the L-I curves, presented in Figure 6.5 and Equation 6.2, we can plot stage temperature versus natural logarithm of threshold current and obtain parameters T_0 and I_0 through a linear fit. The slope of the linear fit will give the characteristic temperature T_0, while I_0 can be calculated based on the intercept

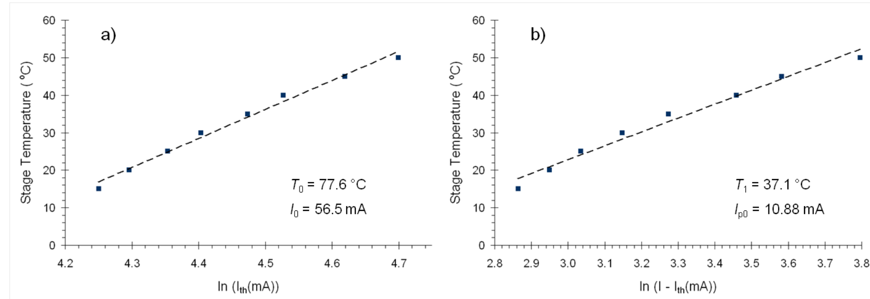


Figure 6.6: Estimation of the characteristic temperatures T_0 and T_1 for a 900 μm-long hybrid III-V/Si Fabry-Perot laser: a) natural logarithm of the threshold current I_{th} as a function of the stage temperature; b) natural logarithm of the difference between the current required to achieve 1 mW peak optical power and the threshold current as a function of the stage temperature.

and the slope. This plot is presented in Figure 6.6a, and the overall characteristic temperature obtained from it is 77.6 °C, while I_0 is 56.5 mA. These values are comparable to the values of T_0 = 51 °C and I_0 = 48 mA, reported by Sysak *et al.* for a 850μm-long InAlGaAs-based, Fabry-Perot evanescent hybrid III-V/Si laser realized by direct bonding to an SOI substrate [5]. Nominally, a higher T_0 value indicates a smaller temperature dependence of the threshold current.

In an analogue way, the data from L-I curves obtained in pulsed regime can be used in combination with Equation 6.3 to find the parameters T_1 and I_{p0}. In this case, the natural logarithm of the difference between the current required to obtain 1 mW of a peak optical power and the threshold current can be plotted against the stage temperature T. This plot is presented in Figure 6.6b. The above-threshold characteristic temperature obtained from the linear fit is 37.1 °C, while I_{p0} is 10.88 mA. In their work, Sysak *et al.* reported T_1 = 100 °C and I_{p0} = 10.65 mA [5]. In our case, it is unusual that the value of the characteristic temperature T_1 is lower than the overall characteristic temperature T_0 and much lower than the value reported by Sysak *et al.* This indicates a strong temperature dependence of the current required to obtain a given optical output power, which again suggests a relatively high thermal resistance of the device.

6.1.2 Thermal resistance measurements

To assess the thermal resistance R_{th}, using the method described by Sysak *et al.* [5], we have performed a series of optical spectral measurements in both CW and pulsed regimes, tracing the shift in the peak lasing wavelength $\Delta\lambda$. Assuming that practically all of the applied electrical power is dissipated as heat, the

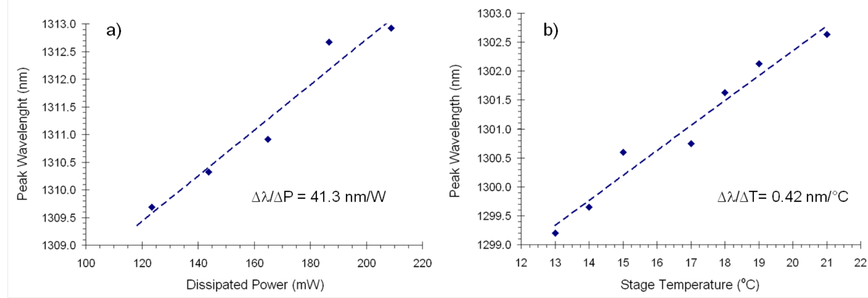


Figure 6.7: Estimation of the thermal resistance of a 630 μm-long Fabry-Perot hybrid III-V/Si laser: a) peak wavelength shift versus dissipated power (CW regime measurements); b) peak wavelength shift versus stage temperature(pulsed regime measurements).

thermal resistance R_{th} can be expressed as the following ratio:

$$R_{th} = \left(\frac{d\lambda}{dP}\right) \Big/ \left(\frac{d\lambda}{dT}\right) \tag{6.4}$$

where (dλ/dP) is the rate of shift in the lasing wavelength versus the applied electrical power, while (dλ/dT) is the rate of shift in the lasing wavelength versus the temperature of the active region (which can be changed using temperature-controlled stage).

In CW regime, we measured the shift in the peak wavelength $\Delta\lambda$ versus the dissipated power in the device, while in the pulsed regime (1% duty cycle, 100 μs pulse repetition interval) we measured the shift $\Delta\lambda$ versus the temperature of the stage (controlled using a Peltier element). In this way, self-heating of the device is minimal, and we can assume that the temperature of the active region is equal to the temperature of the stage.

Results of these measurements are presented in Figure 6.7. Using a linear fit, we measure a wavelength shift with the increase of dissipated power to be $\Delta\lambda/\Delta P$ = 41.3 nm/W. Similarly, the wavelength shift with the increase of the temperature of the stage is $\Delta\lambda/\Delta T$ = 0.42 nm/°C.

Dividing these two values, according to Equation 6.4, we obtain the thermal impedance value of 95.3 K/W. This is significantly higher than the value of 41.8 K/W that was reported for the direct wafer bonded hybrid III-V/Si laser [5]. However, for a direct comparison of these two devices we have to take into account their total lengths: 850 μm for the direct bonded hybrid laser reported in [5] and 630 μm for the BCB-bonded hybrid laser reported here. Even then, if we compare the length-specific thermal resistance of these devices R'_{th} (as defined in Equation 3.7 in Chapter 3), we can conclude that the BCB-bonded evanescent hybrid III-V/Si laser has a significantly higher specific thermal resis-

tance: 60.0 K·mm/W versus 35.5 K·mm/W. Also, this measured value of specific thermal resistance R'_{th} of 60 K·mm/W is 50% higher than the values around 40 K·mm/W, which were predicted by thermal simulations (for a mesa wing section width of 8 μm), as shown in Figure 3.18a, in section 3.3.2.

The exact cause of this discrepancy between the simulated and the calculated values of the thermal resistance remains unclear. The fact that the electrical characteristics of the devices (including series resistance) are relatively good, may lead to the hypothesis that the thermal contact between the III-V layers (containing the active layers and metallization) and the underlying BCB bonding layer was not sufficiently good, leading to a much higher thermal resistivity of the structure. During the bonding tests, SEM inspections of the cross-sections of the bonded III-V films, occasionally revealed small gaps between the cured DVS-BCB bonding layer and the InP spacer layer that should be in the intimate contact with the BCB. In a fabricated III-V/Si hybrid laser, such a gap could impede heat flow and increase the thermal resistance of the device.

6.2 Characterization of distributed feedback (DFB) hybrid III-V/Si lasers

6.2.1 On-chip testing of the hybrid lasers

In the following processing run, samples with hybrid, evanescently-coupled, III-V/Si distributed feedback (DFB) lasers were fabricated, according to the procedures described in Chapters 4 and 5. Before cleaving, on-chip testing of the devices was performed in order to check for the lasing devices. For this purpose, integrated photodetectors, adjacent to the DFB lasers were used to detect the optical power and provide information about the optical output. As there were no cleaved facets at this stage of testing, any detected lasing (observed as an abrupt rise in the photocurrent during the injected current sweep), would unambiguously come as a consequence of the reflection from the gratings fabricated on top of the silicon rib waveguides.

On-chip testing of the devices was carried out in CW regime. Only DFB devices with the integrated photodetector were tested. The results showed that lasing was observed only in those devices that were fabricated on top of the first-order gratings. Additionally, most of those lasing devices were observed in the gratings with a nominally 62.5% duty cycle, which is not surprising. As mentioned earlier, in section 5.1.1, the actual duty cycle of the fabricated first-order gratings was around 34% (for the designed 55% duty cycle) and 45% (for the designed 62.5% duty cycle).

These initial on-chip tests were used only to identify the individual lasing devices on the fabricated samples. The problem in these tests was the fact that

the tested devices were not fully galvanically isolated. For a given DFB hybrid laser, as schematically presented in Figure 5.1b, the integrated photodetector next to it was galvanically isolated as explained in section 5.4.9 of Chapter 5 in order to allow separate biasing, but the hybrid laser from the adjacent device column was not. This device in the adjacent column is a phase-shifted DFB laser, as presented in Figure 5.1a, which has no integrated photodetector. The continuous p-type metallization was intentionally left, anticipating eventual cleaving of the individual device bars. Due to uncertainties and bad reproducibility of the cleaving process, if any gap was left in the metallization between the devices from the adjacent columns, then after cleaving, in a worst-case scenario, one could get a cleaved device that has a section of III-V semiconductor material at its end, where the carriers can't be effectively injected. This section would absorb the light and diminish the optical output from such a badly cleaved facet.

Therefore, in order to perform on-chip testing of the individual hybrid III-V/Si DFB lasers, the adjacent hybrid lasers had to be galvanically isolated in order to avoid simultaneous electrical pumping of two hybrid lasers fabricated along the same silicon rib waveguide. For this purpose, we selected several candidate devices, based on the initial tests, and performed selective milling (or cutting) of the p-type metallization using a focused ion beam (FIB) system. An SEM image of one such cut is shown in Figure 6.8. The procedure was optimized in such a way to cut through the p-type metallization layer, the top InGaAs ohmic contact layer and the top several hundred nanometers of p-InP top cladding layer.

After such a galvanic isolation, the chip with the fabricated devices was mounted on a setup with a Peltier element, as shown in Figure 6.3. Photocurrent (I_{ph}) from the integrated photodetector was measured and used to assess the optical output of the laser. Typical $I_{ph} - I$ plots in CW regime, for temperatures in the range from 10 °C to 55 °C are shown in Figure 6.9. The threshold current at 20 °C is 20 mA. Since the tested DFB laser is 350μm-long and assuming a 3μm-wide injection channel, this corresponds to a threshold current density of 1.9 kA/cm^2. The optical power is assessed based on the detected photocurrents. Responsivity R of the photodetector can be calculated using the following relation:

$$R = \eta \frac{q\lambda}{hc} \tag{6.5}$$

where η is the quantum efficiency of the photodetector, λ is the wavelength of the detected light, q is the electron charge and h is Planck's constant.

At a wavelength λ = 1310 nm, the maximum responsivity of the integrated photodetectors is 1.05 A/W, assuming 100% quantum efficiency. In order to conservatively estimate the output power of the lasers, we adopt this value. In

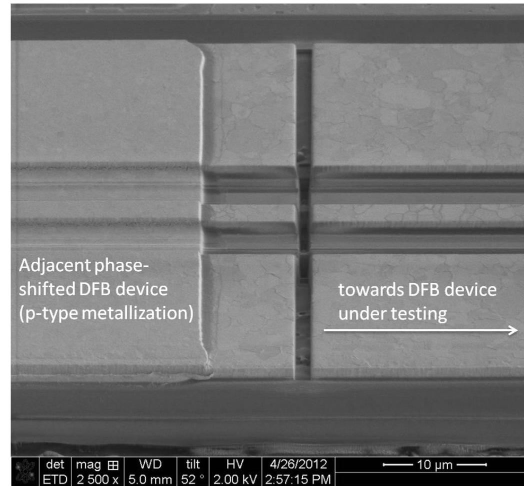


Figure 6.8: SEM image of the cut made in p-type metallization (and top III-V material layers) by FIB milling for the purpose of galvanic isolation of the adjacent hybrid lasers. P-type metallization of the adjacent phase-shifted DFB device is visible on the left side of the image, while the DFB hybrid laser that needs to be tested is to the right (outside the image).

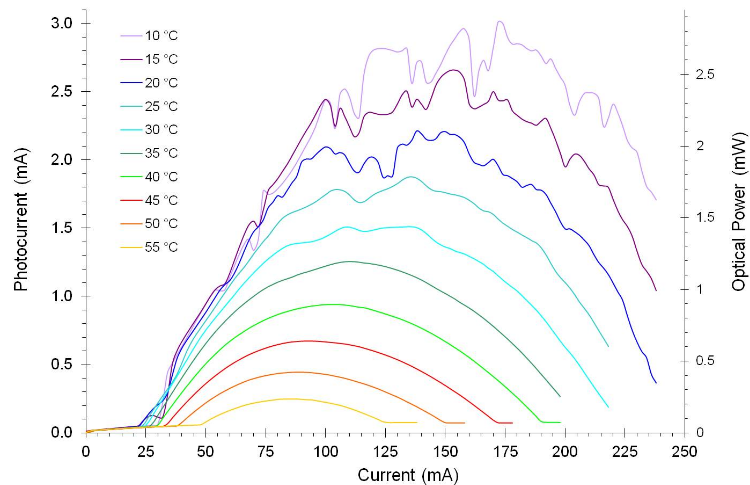


Figure 6.9: Detected photocurrent vs. injected current ($I_{ph} - I$) plots of a 350 μm-long hybrid III-V/Si DFB laser in a CW regime, during on-chip tests for stage temperatures from 10 °C to 55 °C. The right axis shows the optical power, estimated using 1.05 A/W responsivity for the integrated photodetector.

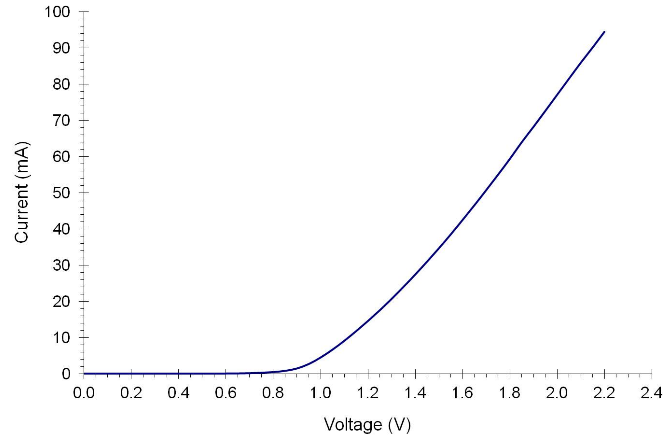


Figure 6.10: Typical $I - V$ characteristic of a 350μm-long hybrid DFB laser.

this way, we conclude that the maximum optical power at 20 °C is 2.1 mW, while the slope efficiency (for a single-side output) is ~ 0.026 W/A. At 10 °C, the maximum optical output power rises to 2.85 mW and the slope efficiency is ~ 0.03 W/A.

The kinks observed in the $I_{ph} - I$ curves at lower stage temperatures and higher output optical power levels are similar to those reported by Fang *et al.* [6] and are attributed to instabilities in the laser optical output caused by the reflections from the corrugations of the adjacent DFB lasers, which are located on the same Si rib waveguide. As the current injection increases, the device heats up and this changes the phase of the reflected light resulting in instabilities in the total optical output.

A typical I-V characteristic of a 350μm-long hybrid III-V/Si DFB laser is shown in Figure 6.10. The turn-on voltage is around 0.8 V and the series resistance of the tested DFB lasers is around 12 Ω. The measured series resistance is comparable to values of 11.5 Ω and 13 Ω, previously reported for 600μm-long DBR hybrid laser [7] and 360μm-long DFB laser [6], respectively. The specific electrical resistance R'_{el} of this laser, as defined in Equation 3.8, in section 3.3.2 of the Chapter 3, is 4.2 Ω·mm. This in a good agreement with a specific electrical resistance of 4.62 Ω·mm, calculated for a 840μm-long Fabry-Perot device, reported in section 6.1. These relatively comparable values of the specific electrical resistances show that electrical properties of both types of hybrid lasers, coming from two different fabrication batches, remain similar.

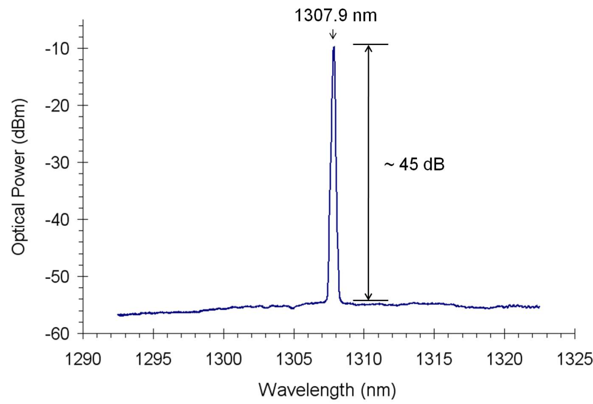
6.2.2 Testing of the cleaved hybrid lasers

In the next phase of characterization, we wanted to measure the optical spectrum of the lasing devices in order to confirm a single-mode behavior, characteristic for DFB lasers. For this purpose, the chip with the fabricated devices was cleaved into narrow bars, as described in section 5.4.10. The emitted light was collected from the cleaved facet of a DFB laser using a multi-mode optical fiber and coupled to an optical spectrum analyzer (OSA). A typical optical spectrum of a 350μm-long DFB laser in continuous wave (CW) regime, measured with a resolution of 0.1 nm, is given in Figure 6.11a. The peak wavelength is at 1307.9 nm. The side mode suppression ratio (SMSR) is about 45 dB and the fact that there are no other peaks within a wavelength span of 30 nm, clearly suggest that this device really operates as a quarter-wave shifted DFB laser.

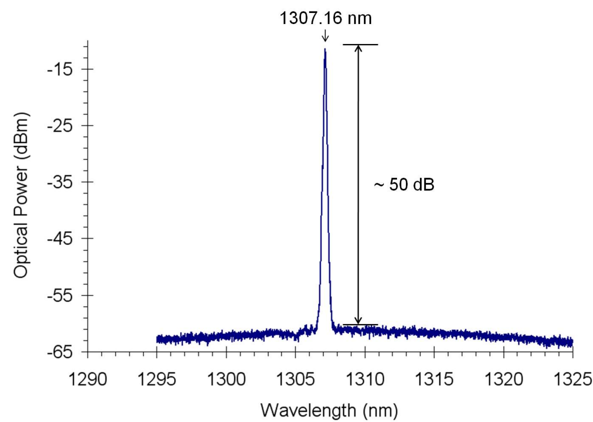
Beside measuring the spectra of the DFB lasers with the integrated photodetectors, we also measured the optical spectra of the phase-shifted DFB lasers that were not designed with integrated photodetectors. The optical spectrum of a 600μm-long phase-shifted DFB laser with 100μm-long gratings at both ends is shown in Figure 6.11b. The peak wavelength is at 1307.16 nm, with a SMSR value of ~ 50 dB. Similarly to the previous case, there are no other prominent peaks within a wavelength span of 30 nm, which confirms single-mode lasing of this phase-shifted DFB laser. The achieved SMSR value of ~ 50 dB is the same as the one reported for the hybrid III-V/Si DFB and DBR lasers based on direct bonding [6, 7].

Most of the phase-shifted DFB lasers exhibited single-mode behaviour, but in a few cases, for lasers of 800 μm and 900 μm nominal lengths, we observed more complex spectra combining one prominent peak, characteristic for single-mode lasers, and several equidistant peaks characteristic for Fabry-Perot lasers. One such example is illustrated in Figure 6.12. In this case, we have an optical spectrum of a phase-shifted DFB laser, with a 800 μm nominal length and approximately 1050 μm distance between the cleaved facets. For a relatively low injected current (100 mA), a single-mode is observed, as shown in Figure 6.12a. For a higher value of injected current (140 mA), another set of peaks, characteristic for Fabry-Perot lasers, appears along with the original peak. This is shown in Figure 6.12b. Finally, after 2 minutes of pumping the laser with 140 mA direct current, the mode competition is finished and a single peak at around 1307.3 nm remains as the only lasing mode. This spectrum is presented in Figure 6.12c. This kind of behaviour is not fully unexpected, taking into account that this particular device had a relatively long (~ 1.05 mm), parasitic Fabry-Perot cavity made after cleaving.

Following this, a series of spectral measurements in both CW and pulsed regime were performed in order to measure the thermal resistance (or thermal impedance) R_{th} of the lasing devices, using the method described in [5] and



(a)



(b)

Figure 6.11: Optical spectra of the single-wavelength hybrid III-V/Si lasers: (a) spectra of a 350 μm-long DFB hybrid laser; (b) spectra of a 600 μm-long phase-shifted DFB hybrid laser.

explained in section 6.1.2. First, we measured the optical spectrum of a 350μm-long DFB laser. In CW regime, the observed shift in the peak lasing wavelength ($\Delta\ \lambda$) was measured versus the dissipated power in the device. In the pulsed regime (1% duty cycle, 100 μs pulse repetition interval), the peak wavelenght shift $\Delta\ \lambda$ was measured versus the temperature of the stage (controlled using a Peltier element, as explained in section 6.1.2). Results of these measurements are shown in Figure 6.13.

Using a linear fit, we measure the wavelength shift with the increase of dissi-

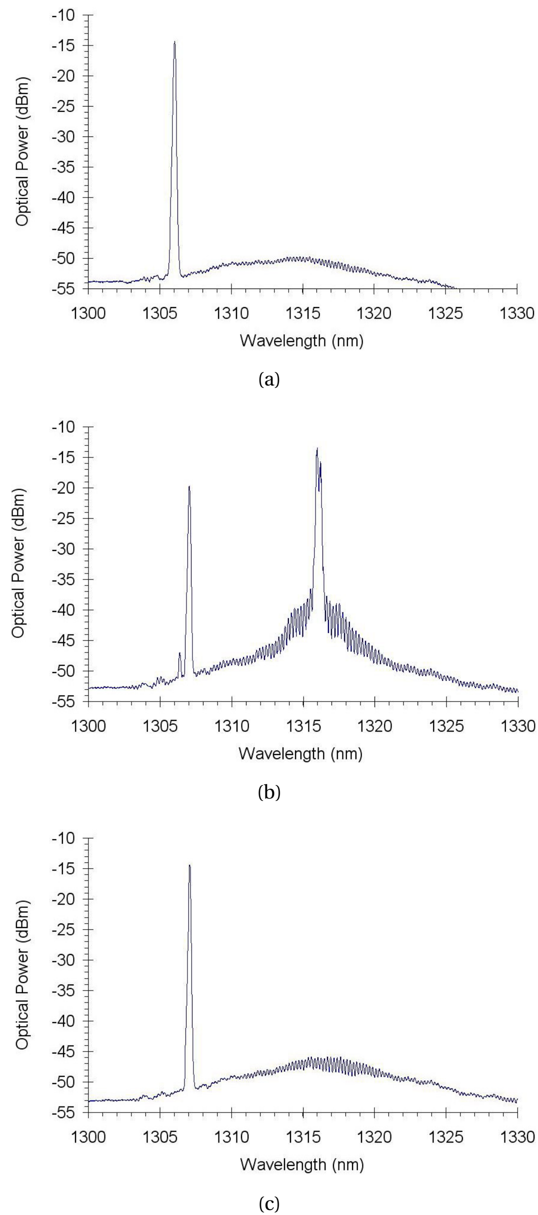


Figure 6.12: Complex optical spectra of a 800 μm-long, phase-shifted DFB laser with cleaved facets: (a) a single lasing mode observed for the injected current of I = 100 mA; (b) two additional lasing modes initially appear for the injected current of I = 140 mA; these modes occur due to the cleaved facets which form a Fabry-Perot cavity; (c) after 2 minutes at I = 140 mA, a single lasing mode is restored.

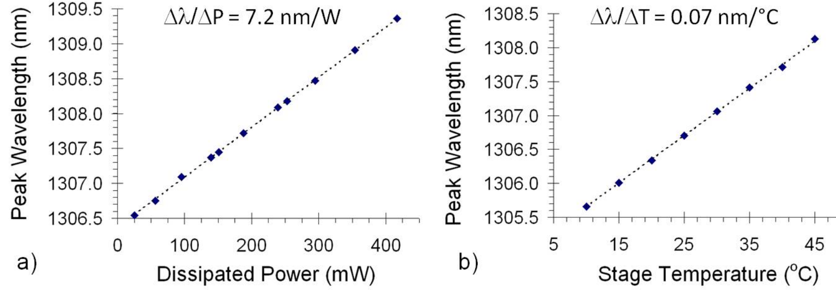


Figure 6.13: Estimation of the thermal resistance of a 350 μm-long DFB hybrid III-V/Si laser: a) peak wavelenght shift versus dissipated power (CW regime measurements); b) peak wavelenght shift versus stage temperature(pulsed regime measurements).

pated power of $\Delta\lambda/\Delta P$ = 7.2 nm/W, while the wavelength shift with the increase of the temperature of the stage is $\Delta\lambda/\Delta T$ = 0.07 nm/°C. Dividing these values yields a thermal resistance of 102.9 K/W. The same set of measurements performed for a 600μm-long phase-shifted DFB hybrid laser, provided a thermal resistance value of 64 K/W.

Given the different device lengths, it is better to compare the specific thermal resistances R'_{th} of these devices. Multiplying the calculated thermal resistances with the device lengths, we obtain values of 36 K·mm/W for a 350μm-long device and 38.4 K·mm/W for a 600μm-long phase-shifted DFB laser. These values are in a relatively good agreement with the values predicted by thermal simulations for a mesa wing section width of 8 μm, as shown in Figure 3.18a, in section 3.3.2.

On the other hand, the measured values of thermal impedance are larger than 41.8 K/W reported for a 850μm-long hybrid III-V/Si laser based on a direct wafer bonding [5]. However, the specific thermal resistance R'_{th} of this device is 35.5 K·mm/W which is almost identical to the calculated specific thermal resistances of the fabricated BCB-bonded hybrid III-V/Si DFB lasers. Similarly, a specific thermal resistance of ≈ 37 K·mm/W was reported for a 240μm-long phase-shifted DFB laser, based on InAlGaAs and fabricated using direct bonding [8]. This shows that despite the presence of a several tens of nanometers thick DVS-BCB bonding layer, the thermal performance of a hybrid evanescently-coupled III-V/Si laser, per unit length, is similar to that of the directly bonded hybrid III-V/Si laser. This is probably due a to relatively wide III-V mesa (16.8 μm, compared to 14 μm III-V mesas in directly bonded devices [6]) and thick metallization layers. Nevertheless, strategies for reducing thermal resistance of the device should be further pursued in future work.

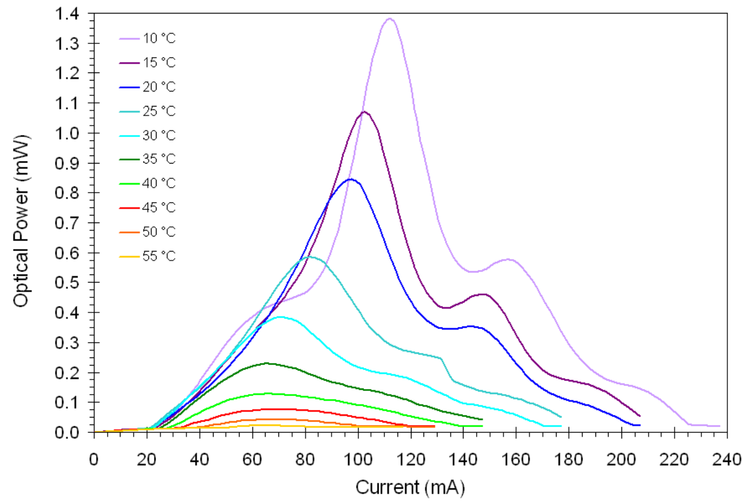


Figure 6.14: $L-I$ plots of a cleaved, 350μm-long, hybrid DFB laser in CW regime, at different stage temperatures.

After cleaving the individual device bars, we planned to directly measure the optical output power of the lasing devices and obtain $L-I$ curves at different temperatures in both CW and pulsed regime. The optical output was measured at the cleaved facet of the laser, by placing a large-area photodetector in a close proximity to the facet. Optical power versus injected current curves measured for a 350μm-long DFB laser device in a CW regime, at different stage temperatures, are shown in Figure 6.14. The tested device is the same DFB laser for which $I_{ph}-I$ curves obtained during on-chip testing were presented in Figure 6.9. No lasing was observed in CW regime above 55 °C.

The difference between these $L-I$ curves and the $I_{ph}-I$ curves measured before cleaving is obvious, both in the shape of the curves and the level of the detected optical power. At higher stage temperatures (35 °C and above), $L-I$ curves have the expected shape with the ascending slope, the thermal rollover and the descending slope. However, at lower temperatures, the shape of the curves becomes more complex, even exhibiting a second local peak at temperatures below 20 °C.

On the other hand, $L-I$ curves for the same device, measured in pulsed regime, with 1% duty cycle and 100 μs pulse repetition interval, presented in Figure 6.15, have a more expected form. Though, it also can be noted that at lower temperatures, there are more kinks in the $L-I$ curves.

To further investigate this behaviour, another series of temperature con-

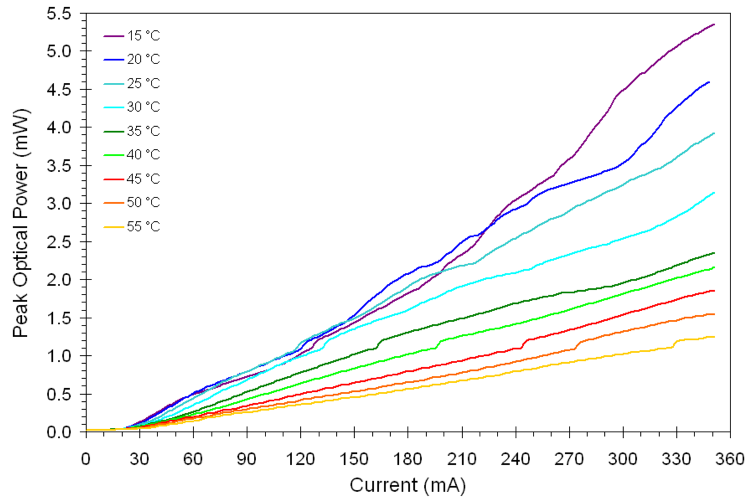


Figure 6.15: $L-I$ plots of a cleaved, 350μm-long, hybrid DFB laser in pulsed regime (1% duty cycle, 100 μs pulse repetition interval), at different stage temperatures.

trolled measurements was performed. While sweeping the DC current, the output optical power was simultaneously measured both at the cleaved facet (using an external photodetector) and with the integrated photodetector. In this way, we had information about the optical signal emitted from the DFB laser in both directions - towards the integrated photodetector and towards the cleaved facet.

In Figure 6.16a, optical powers emitted in both directions and the combined, total optical output are plotted against the injected DC current, at a stage temperature of 20 °C. The equivalent optical power, detected by the integrated photodetector is estimated in the same way as in section 6.2.1, assuming 100% quantum efficiency. The difference in the optical output from the cleaved facet and the output detected by the integrated photodetector is obvious. On the other hand, the combined optical output, which is just the sum of the two optical outputs is a curve with a smoother shape. Following this, measurements of the combined optical power of a hybrid DFB laser were performed in CW regime, for various stage temperatures, and the results are presented in Figure 6.16b. The obtained plots, in general, more resemble the expected shapes of the typical laser $L-I$ curves than the plots obtained measuring only the optical output from the cleaved facet, shown in Figure 6.15.

In addition to 350μm-long DFB hybrid lasers, the $L-I$ curves at different stage temperatures in both CW and pulsed regime (1% duty cycle and 100 μs pulse repetition interval) were measured for a 600μm-long phase shifted hybrid

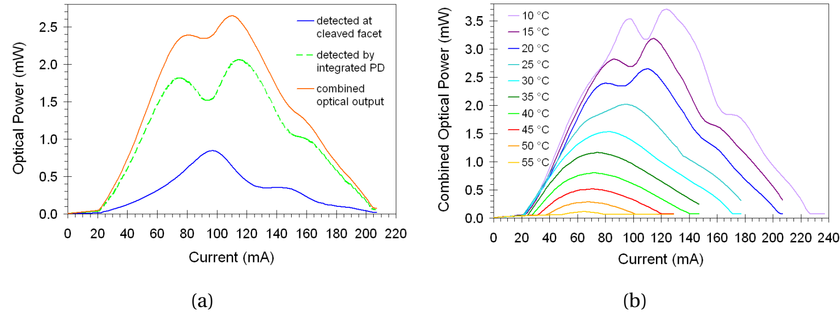
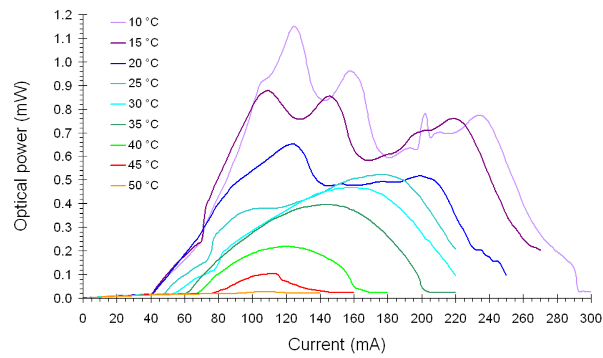


Figure 6.16: Total optical output of a cleaved, 350 μm-long hybrid DFB laser in CW regime: (a) $L-I$ plots of the individual components of the optical output and the total, i.e. combined optical output at 20 °C; (b) $L-I$ plots of the total (combined) optical output at different stage temperatures.

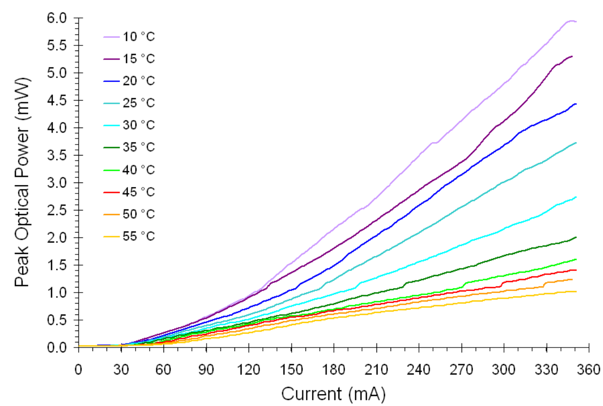
laser. The results of these measurements are presented in Figure 6.17. As we can see from Figure 6.17a, the $L-I$ curves for this device look even more complex than the $L-I$ curves of a 350μm-long DFB laser, given in Figure 6.14. Threshold current (at 20 °C) is 40 mA. Taking into account that the total lenght of the tested device (between the cleaved facets) is ~ 700 μm, this corresponds to the threshold current density of J_{th} = 1.90 kA/cm^2, which is identical to what was measured for a DFB hybrid laser. This value is lower compared to values measured in Fabry-Perot hybrid lasers, reported in section 6.1, but still a bit higher than threshold current density values of 1.4 kA/cm^2 reported for DFB hybrid lasers based on direct bonding [6]. One of the reasons for this certainly comes from the fact that the optical mode confinement factor in the quantum wells (Γ_{MQW}) in our BCB-bonded hybrid III-V/Si laser is lower than in the DFB laser based on direct bonding (3.2% compared to 5.2%).

In the case of this phase-shifted DFB hybrid laser, there is no integrated photodetector adjacent to the laser that could provide information about the optical output in the other direction. On the other hand, similar to the previous case, the $L-I$ curves in the pulsed regime have the expected shape for all the temperatures between 10 °C and 55 °C, as can be seen from Figure 6.17b.

The presented data suggest that the unusual shape of the $L-I$ curves in CW regime comes as a consequence of a parasitic cavity formed by cleaving of the devices. This is illustrated in Figure 6.18, for both a DFB device with the integrated photodetector and a phase-shifted DFB laser without the photodetector. In the first case, shown in Figure 6.18a, there is practically only one parasitic



(a)



(b)

Figure 6.17: $L-I$ plots of a cleaved, 600μm-long, hybrid, phase-shifted DFB laser, at different stage temperatures: (a) in CW regime; (b) in pulsed regime, with 1% duty cycle and 100 μs pulse repetition interval.

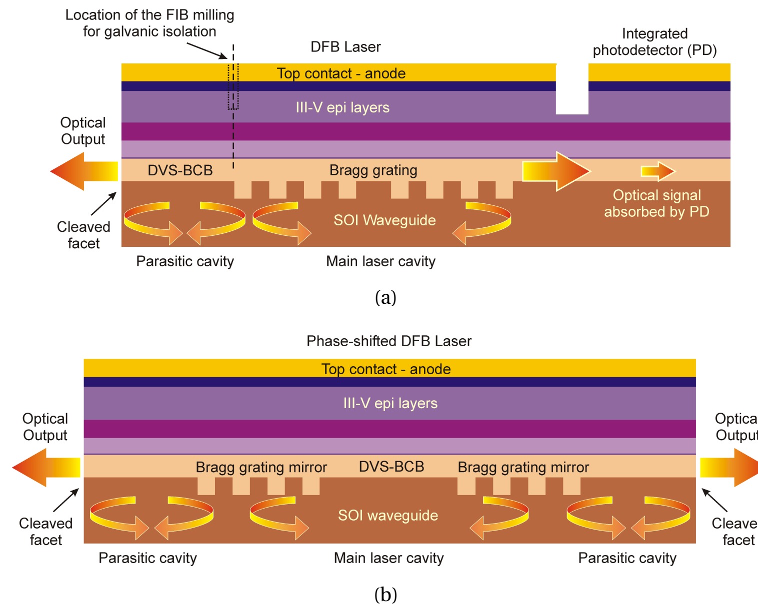


Figure 6.18: Parasitic cavities in single-wavelength hybrid III-V/Si lasers formed due to cleaved facets: (a) in DFB laser, where only one cavity is of interest, as the light emitted to the other side is absorbed by integrated photodetector; (b) in phase-shifted DFB laser, where two parasitic cavities are formed at both ends of the device, between the cleaved facets and the end of the Bragg grating mirrors.

cavity, formed by the cleaved facet from which the optical output is collected and the grating. Due to the length of the integrated photodetector (480 μm), it is assumed that practically all the light emitted in that direction is absorbed. Therefore, the cleaved facet located at the other side of the integrated photodetector plays no role in the behaviour of the hybrid laser. On the other hand, in the case of the phase-shifted DFB lasers, when there is no integrated photodetector, there are now two parasitic cavities formed at both ends of the device, between the cleaved facets and the gratings, as illustrated in Figure 6.18b.

In both cases, the electrical current is injected in the parasitic cavities (due to the continuous metallization) and both can amplify the optical signal coming from the main cavity. In practice, the lengths of these parasitic cavities are between 20 μm and 100 μm. Although this is much shorter than the lengths of the main laser cavities (350 μm and 600 μm in the previous cases), it can be sufficient to generate an additional optical signal that will constructively or destructively interfere with the optical signal coming from the main cavity. It is also indicative that the most irregular $L-I$ curves were observed in CW regime,

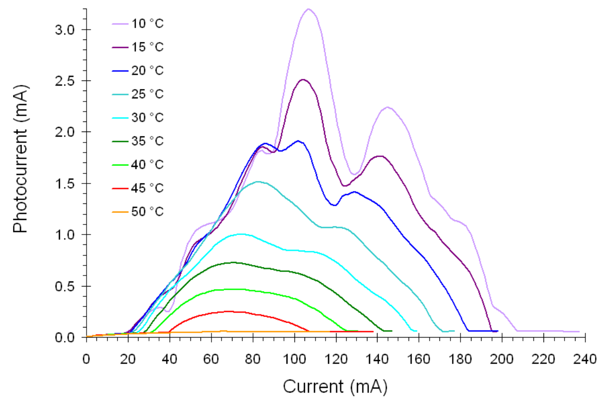
at lower temperatures (between 10 °C and 25 °C). This may indicate the importance of self-heating of the device (which is negligible in pulsed regime, but very prominent in CW regime) and subsequent temperature increase.

In order to check the impact of these parasitic cavities, we have performed a galvanic isolation of one of the parasitic cavities in a 350μm-long DFB hybrid laser. The galvanic isolation was performed in an identical way as previously described in section 6.2.1, using the FIB tool to mill the p-type metallization and the highly conductive InGaAs ohmic contact layer from the top of the III-V mesa. The milling was conducted at the end of the grating, as illustrated in Figure 6.18a. The idea was to prevent carrier injection into the parasitic cavity and therefore to impede any amplification of the optical signal in this region. After milling, the electrical resistance between two separated parts of p-type metallization (one on top of the parasitic cavity and the other on top of the DFB laser itself) was > 13 kΩ.

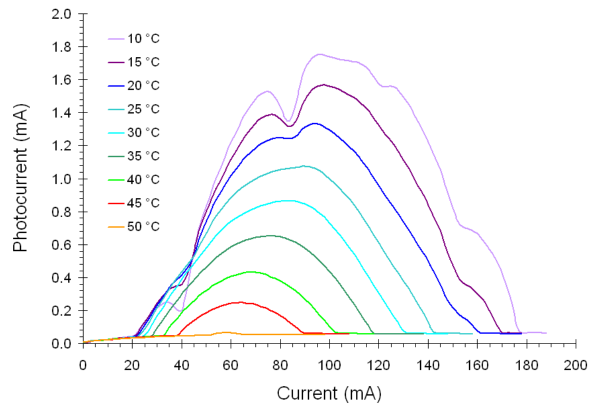
As a consequence of this galvanic isolation, the parasitic cavity now became an absorber for the light emitted from the DFB laser. Therefore, only the photocurrent from the integrated photodetector was used to quantify the optical output of the hybrid laser. Comparison of the plots of the photocurrent I_{ph} versus the injected DC current I at different stage temperatures is shown in Figure 6.19. The $I_{ph} - I$ plots before the galvanic isolation of the parasitic cavity are given in Figure 6.19a, while the $I_{ph} - I$ plots after the galvanic isolation are shown in Figure 6.19b. Although some notches in the plots are still visible at lower temperatures (10 °C to 20 °C) after the galvanic isolation, we can generally conclude that the $I_{ph} - I$ characteristics after the galvanic isolation look much smoother and closer to the plots expected for a laser in a CW regime.

Comparing the optical outputs (i.e. the detected photocurrents) in both cases, we can conclude that the biggest difference between the laser performance before and after the galvanic isolation of the parasitic cavity, occurs at the lower temperatures, between 10 °C and 20 °C. On the other hand, at the higher temperatures, starting from 40 °C and above, the $I_{ph} - I$ curves are almost identical. This might be the consequence of the temperature shift of the gain spectrum of the multiple quantum wells. Namely, at the higher temperatures, the gain peak shifts towards longer wavelengths, and consequently moves away from the lasing wavelength which is determined by the grating period. This is clearly visible in Figure 6.12b, where three lasing peaks are observed - one due to the grating period (at the shorter wavelength) and two more, due to a parasitic Fabry-Perot cavity, occurring at the longer wavelengths and corresponding to the gain peak. Therefore, at the higher temperatures, the gain of the parasitic cavity for the lasing wavelength is lower and the interference that it causes is drastically lower.

The fact that after galvanic isolation we observed much smoother $I_{ph} - I$



(a)



(b)

Figure 6.19: $I_{ph} - I$ plots of a cleaved, 350 μm-long DFB laser in a CW regime, at different stage temperatures: (a) before galvanic isolation of the parasitic cavity; (b) after galvanic isolation of the parasitic cavity.

curves even at the lower temperatures, clearly indicates that amplification of the optical signal in the parasitic cavity is the main reason for the unusual $L-I$ plots that were measured in CW regime. Cleaving of the samples was, of course, a necessary step in order to directly measure the optical spectra of the lasing devices. However, in a photonic integrated circuit (PIC) in which a hybrid III-V/Si laser would represent just one of the components, no such parasitic cavities would be formed and the problems that we observed with the cleaved facets would be avoided.

6.3 Conclusions

Characterization of the fabricated Fabry-Perot and single-wavelength (DFB) hybrid III-V/Si lasers based on adhesive DVS-BCB bonding was presented in this chapter. The performance of both types of lasers is, in general, comparable to similar hybrid III-V/Si lasers reported by other research groups [1, 4–6, 9]. As expected, the electrical properties of both Fabry-Perot and DFB hybrid lasers were similar, but some noticeable differences were observed in specific thermal resistance of the devices and, consequently, their optical output.

Lasing in both pulsed and CW regimes was demonstrated for both Fabry-Perot and DFB hybrid lasers with optical output levels of up to several milliwatts. The lower optical output observed in DFB lasers compared to Fabry-Perot devices is probably due to the relatively high $\kappa \cdot L$ product (estimated to be ~ 5.5 for a 350μm-long DFB laser) and the shorter device lengths of the single-wavelength lasers (350 μm and 600 μm) compared to Fabry-Perot lasers (≥ 630 μm). Thermal resistance of both types of demonstrated hybrid lasers was relatively high, usually around 100 K/W for Fabry-Perot and 350 μm-long DFB laser, with a minimum measured value of 64 K/W for a 600 μm-long phase-shifted DFB laser. However, a significant difference was observed in values of specific thermal resistance R'_{th}. For Fabry-Perot lasers, the value of ~ 60 K·mm/W was unexpectedly high, while the values of 36 - 38 K·mm/W measured in DFB and phase-shifted DFB lasers, were in good agreement with the simulated R'_{th} values and those reported for direct-bonded hybrid III-V/Si lasers [5, 6]. Consequently, during characterization of Fabry-Perot lasers in CW regime, strong thermal rollovers were observed in $L-I$ curves and no lasing was observed at 30 °C or higher. On the other hand, single-wavelength hybrid lasers performed much better and lasing in CW regime was observed up to 55 °C. Nevertheless, in absolute terms, thermal resistance of the devices remains relatively high and strategies for reducing it should be the focus of future work.

Unexpected shapes of $L-I$ curves observed while testing cleaved hybrid III-V/Si DFB lasers in CW regime are attributed to parasitic cavities, formed by the cleaved facets and the gratings on top of Si rib waveguides, where light-

amplification can be significant due to injected carriers. In principle, deposition of anti-reflection coatings (ARC) would minimize reflection from the cleaved facets and hopefully solve this problem. However, in the long-term perspective, the proper solution would be to use adiabatic taper sections to terminate the III-V active region and convert a hybrid mode to a Si rib waveguide mode, as reported in other works on hybrid III-V/Si lasers [4, 6, 7, 9]. This would eliminate the need for the continuous metallization and the continuous III-V mesa that was used in our work and that caused creation of parasitic cavities where the optical signal was amplified.

The problems mentioned above point out the need for further improvements in design of the evanescently-coupled, hybrid III-V/Si lasers based on DVS-BCB bonding. However, the most important conclusion, following the demonstration of both Fabry-Perot and DFB hybrid III-V/Si lasers at 1310 nm, is that the DVS-BCB bonding technology can be used for fabrication of evanescently-coupled hybrid lasers on the SOI platform with properties that are, in general, comparable to the devices fabricated using direct bonding technology.

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7 Conclusions and Perspectives for Future Work

7.1 Conclusions

Challenges that are encountered in further miniaturization of microelectronic integrated circuits and the looming interconnect bottleneck represent a major force driving the development of optical interconnects capable, in perspective, of overcoming these problems. Silicon photonics, which is a rapidly-developing technology based on the silicon-on-insulator (SOI) material platform, promises to provide cost-effective fabrication of high performance photonic integrated circuits (PICs) and their co-integration with the electronic devices on a single chip. Therefore, it is considered as the most promising technology, not only for fabrication of optical interconnects which would allow further progress along "More Moore" direction, but also for providing development of integrated electrical and photonic circuits enabling further functional diversification within "More-than-Moore" paradigm.

Despite impressive developments in silicon photonics during the last decade, fabrication of efficient, electrically-pumped, light sources in this technology still remains the most serious challenge and is considered as the "Holy Grail" of silicon photonics. In the second chapter of this thesis, we have summarized various approaches and technologies that are actively pursued to solve this

problem. Along with this, we presented our motivation to choose adhesive bonding, and more specifically DVS-BCB bonding, as a technology of choice for heterogeneous integration of III-V semiconductor materials on the SOI photonic platform. From the perspective of the device design, an evanescently-coupled, hybrid III-V/Si laser was chosen as the most promising candidate for an efficient, electrically-pumped laser. The basic idea behind these choices was to combine a very promising design approach, i.e. an evanescently-coupled hybrid III-V/Si laser, with a polymer-based bonding technology that was perceived as a more robust technique for industrial-scale fabrication of the hybrid lasers, compared to direct bonding technology that was used so far.

The subject of this thesis was the development of a DVS-BCB bonding process enabling heterogeneous integration of III-V semiconductor materials on the SOI photonic platform and demonstration of evanescently-coupled, hybrid III-V/Si lasers fabricated using such a process. The design of the hybrid lasers, based on InAlGaAs multiple quantum wells was presented in Chapter 3. Thicknesses of the functional layers in III-V semiconductor material stack were optimized to allow the III-V/Si cavity to support a fundamental hybrid optical mode that has a stable power distribution profile for a thickness of the DVS-BCB bonding layer in the range between 20 nm and 120 nm. Other designed parameters were chosen to allow efficient electrical carrier injection and sufficiently good thermal properties. Aside from Fabry-Perot hybrid lasers, we presented designs of DFB hybrid lasers with integrated photodetectors and phase-shifted DFB hybrid lasers based both on first-order and second-order gratings formed on top of Si rib waveguides. Optical and thermal simulations also demonstrated the importance of keeping the DVS-BCB bonding layer as thin as possible and as uniform as possible.

A die-to-die DVS-BCB bonding procedure, developed using a commercial wafer bonding tool and described in Chapter 4, yielded less than 100nm-thick bonding layers which are sufficiently thin for efficient evanescent coupling between III-V semiconductor layers and silicon waveguides. The developed bonding procedure is suitable for fabrication of hybrid lasers, optical amplifiers, and photodetectors based on evanescent coupling. The bonding process evolved over time and in its final form showed a good bonding yield and a solid bonding strength. However, the bonding layer uniformity and thickness proved to be the most difficult parameters to control, especially on the SOI substrates with relatively rich topographies. The best results were achieved in bonding III-V dies on pre-planarized SOI dies, where a pre-bonding SiO_x deposition was used to fill the trenches surrounding Si rib waveguides.

Fabrication of the hybrid III-V/Si lasers, described in detail in Chapter 5, comprised several critical steps including the undercut etching of InAlGaAs layers of the III-V mesa and proton implantation, both with the goal of confining

injected carriers to the central region of the III-V mesa edges and enhancing quantum efficiency of the lasers. All the processing steps in the fabrication were perfected and optimized, which eventually resulted in demonstration of both Fabry-Perot and single-wavelength hybrid III-V/Si lasers. For testing the individual devices, dicing the samples and polishing the facets was envisioned as a preferred technique. However, development of these procedures was entrusted to an external vendor who demonstrated non-consistent results. For this reason, we chose to cleave most of the samples with the fabricated devices, in order to perform their characterization, which was described in detail in Chapter 6.

Lasing in pulsed and CW regimes was demonstrated for both Fabry-Perot and DFB hybrid III/V/Si lasers with optical output levels of up to several milliwatts. Lasing was observed only in the single-wavelength lasers based on the first-order gratings. The exact reason for failure of the hybrid lasers based on the second-order gratings is not known, but it may be related to variations in the bonding layer thickness which affect the reflection spectra of the gratings within a hybrid III-V/Si waveguide. In general, electrical and optical properties of the demonstrated hybrid lasers are comparable to similar hybrid lasers based on direct bonding technology. Single-mode spectra with side-mode suppression ratios of 45-50 dB and a lasing wavelengths around 1310 nm, were demonstrated by both DFB and phase-shifted DFB hybrid lasers. Somewhat higher thermal resistance was observed in the tested hybrid lasers, especially in the Fabry-Perot devices fabricated in the earlier processing run. On the other hand, specific thermal resistances of the single-wavelength lasers were in a good agreement with the simulated values and virtually identical to those reported for hybrid lasers based on direct bonding technology. Problems observed during characterization of the cleaved DFB single-wavelength hybrid lasers were found to be due to parasitic cavities formed by cleaved facets and can be overcome using adiabatic tapers in the future designs.

7.2 Perspectives for Future Work

Successful demonstration of evanescently-coupled, hybrid III-V/Si lasers based on DVS-BCB bonding technology, presented in this work, opens new perspectives for future work and further improvements, both in the bonding process and the hybrid laser design. Here, we will summarize the most important issues and give some suggestions and general guidelines for future research.

- **Improvements in the bonding technology** - despite demonstration of the DVS-BCB bonding layers that are ≤ 100nm-thick and allow formation of the hybrid optical cavities comprising SOI waveguides and layers of III-V semiconductor materials, further improvements of the bonding pro-

cess are still required. Specifically, it is important to improve the bonding layer uniformity and continue the efforts to achieve even thinner DVS-BCB bonding layers. Bondings using very diluted BCB:mesitylene solutions on a pre-planarized SOI dies/wafers are the most promising approach in this effort. Further experiments with pre-curing of DVS-BCB before bonding, in order to increase degree of polymerization and minimize BCB re-flow should also be considered in order to improve the bonding layer uniformity. Additionally, it would be important to perform a series of tests with thermal cycling of the BCB-bonded devices to verify the robustness of this bonding technology and assess its possible performance degradation. It would be also interesting to combine these thermal cycling tests with CW lasing tests of hybrid lasers in order to assess the combined long-term effects of low temperatures and exposure to light on the DVS-BCB bonding layer.

- **Scaling-up the bonding process** - in order to achieve any commercial significance, the demonstrated die-to-die bonding process must be scaled-up to a multiple-die-to-wafer bonding process (along the vision given by Intel's Photonic Technology Lab) or to a wafer-to-wafer and even a multiple-wafer-to-wafer bonding process. The initial tests with a multiple-die-to-die bonding procedure using a vacuum chuck may be a step in the right direction. The biggest challenge in this effort is a reliable handling of multiple III-V dies (or wafers) during pre-bonding preparation steps.

- **Improvements in thermal properties of hybrid lasers** - despite exhibiting specific thermal resistance values comparable to those of the hybrid lasers fabricated using direct bonding, the absolute thermal resistances of the demonstrated hybrid III-V/Si lasers are still relatively high and need to be reduced. Fabrication of an effective, metallic thermal via is the most obvious approach that should be taken. However, other solutions should be contemplated as well, for example turning the fabricated hybrid lasers upside down and flip-chipping them to a silicon substrate (that can also be an electronic layer in a multi-layer photonic/electronic integrated circuit) so that perhaps, both types of contact metallizations can also play the role of thermal vias.

- **Improvements in the hybrid III-V/Si laser designs** - obviously, one of the first improvements that should be made in the hybrid laser design is addition of adiabatic tapers, acting as mode converters, at both ends of the laser. In order to reduce thermal resistance of the device and increase optical output, perhaps more efforts in the future work should be focused on phase-shifted hybrid DFB lasers. Also, an interesting approach would be

to design hybrid lasers with adiabatic tapers in Si waveguides that would allow conversion of the hybrid optical mode from the one with a high confinement within III-V MQW layers (suitable for the gain section of the laser) to the one with a high confinement within Si waveguides (at both ends of the lasers). In the end, design efforts should be directed towards integration of such BCB-bonded hybrid III-V lasers with other photonic components in order to build more complex photonic integrated circuits.

The results of the work presented in this thesis open new possibilities in design and fabrication of hybrid III-V/Si lasers based on DVS-BCB polymer bonding technology. As the need for efficient, electrically-pumped lasers on the SOI platform grows, it is essential to pursue these possibilities with a maximum effort. It will be interesting to see, in the coming years, which of the competing technologies will hopefully lead to the realization of this "Holy Grail" of silicon photonics. Nothing less than that, will allow silicon photonics to "come of an age" and unleash its full potential, bringing new advances and possibilities in the Silicon Age.

List of Publications

A.1 Publications in international journals

1. S. Keyvaninia, M. Muneeb, S. Stanković, R. van Veldhoven, D. Van Thourhout and G. Roelkens. *Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate.* Optical Materials Express, 3(1):35-46, January 2013.

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4. S. Stanković, R. Jones, J. Heck, M. Sysak, D. Van Thourhout and G. Roelkens,. *Die-to-Die Adhesive Bonding Procedure for Evanescently-Coupled Photonic Devices.* Electrochemical and Solid-State Letters, 14(8):H326–H329, May 2011.

A.2 Publications in international conferences

5. G. Roelkens, S. Keyvaninia, S. Stankovic, N. Hattasan, A. Gassenq, Y. De Koninck, M. Tassaert, S. Ghosh, P. Mechet, D. Vermeulen, G. Morthier, R. Baets and D. Van Thourhout. *III-V/silicon photonic integrated circuits for communication and sensing applications.* Accepted for presentation at SPIE Photonics West 2013 Conference (invited paper), San Francisco, CA, USA, February 2013.

6. R. Baets, Y. De Koninck, S. Keyvaninia, S. Stankovic, D. Van Thourhout and G. Roelkens. *In search for the ideal hybrid silicon laser.* In 2nd International Symposium on Photonics and Electronics Convergence (ISPEC 2012) (invited paper), page 5, Tokyo, Japan, December 2012.

7. Y. De Koninck, S. Keyvaninia, S. Stankovic, D. Van Thourhout, G. Roelkens and R. Baets. *Hybrid silicon lasers for optical interconnect.* In IEEE Photonics Conference 2012 (IPC12) (invited paper), page 812–813, Burlingame, CA, USA, September 2012.

8. S. Keyvaninia, M. Muneeb, S. Stankovic, G. Roelkens, D. Van Thourhout and J. M. Fedeli. *Multiple die-to-wafer adhesive bonding for heterogeneous integration.* In 16th European Conference on Integrated Optics (ECIO 2012), paper 186, Barcelona, Spain, April 2012.

9. G. Roelkens, S. Keyvaninia, S. Stankovic, M. Tassaert, N. Hattasan, A. Gassenq, P. De Heyn, Y. De Koninck, P. Mechet, R. Kumar, M. Muneeb, D. Vermeulen, G. Morthier, R. Baets and D. Van Thourhout. *III-V-on-silicon membrane photonics for near-infrared and mid-infrared applications.* In 16th European Conference on Integrated Optics (ECIO 2012) (invited paper), N-1284, Barcelona, Spain, April 2012.

10. G. Roelkens, S. Stankovic, S. Keyvaninia, P. Mechet, R. Kumar, T. Spuesens, G. Morthier, R. Baets, D. Van Thourhout, M. Lamponi, G. Duan, Y. Halioua, F. Raineri and R. Raj. *Laser sources on a heterogeneous III-V/silicon platform.* In IEEE Photonics Conference 2011 (IPC11) (invited paper), pages 395–396, Arlington, VA, USA, October 2011.

11. W. Bogaerts, S. Selvaraja, H. Yu, T. Spuesens, P. Mechet, S. Stankovic, S. Keyvaninia, J. Van Campenhout, P. Absil, G. Roelkens, D. Van Thourhout and R. Baets. *A Silicon Photonics Platform with Heterogeneous III-V Integration.* In Integrated Photonics Research, Silicon and Nano-Photonics (IPR 2011) (invited paper), p. IWC2, Toronto, Canada, June 2011.

12. S. Stanković, G. Roelkens, D. Van Thourhout, R. Jones, M. Sysak and J. Heck. *1310nm evanescent hybrid III-V/Si laser based on DVS-BCB bonding.* In Integrated Photonics Research, Silicon and Nano-Photonics (IPR 2011), p. IWC3, Toronto, Canada, June 2011.

13. G. Roelkens, S. Stankovic, S. Keyvaninia, D. Vermeulen, M. Muneeb, R. Baets and D. Van Thourhout. *III-V/silicon photonic integrated circuits for communication applications.* In 16th Opto-Electronics and Communications Conference (OECC) (invited paper), p. 8S1, Kaohsiung, Taiwan, July 2011.

14. G. Roelkens, Y. De Koninck, S. Keyvaninia, S. Stankovic, M. Tassaert, M. Lamponi, G. Duan, D. Van Thourhout and R. Baets. *Hybrid Silicon Lasers.* In SPIE Photonics West 2011 Conference (invited paper), San Francisco, USA, January 2011.

15. S. Stanković, G. Roelkens, D. Van Thourhout, R. Jones, M. Sysak and J. Heck. *Evanescently-Coupled Hybrid III-V/Silicon Laser Based on DVS-BCB Bonding.* In 15th Annual Symposium of IEEE Photonics Society Benelux Chapter, pages 77–80, Delft, Netherlands, November 2010.

16. S. Stanković, D. Van Thourhout, G. Roelkens, R. Jones, J. Heck and M. Sysak. *Die-to-die adhesive bonding for evanescently-coupled photonic devices.* In 218th ECS Meeting Transactions: Symposium on Wafer Bonding, 33(4):411–420, Las Vegas, USA, October 2010.

17. G. Roelkens, D. Vermeulen, L. Liu, T. Spuesens, R. Kumar, P. Mechet, K. Huybrechts, S. Keyvaninia, S. Stankovic, M. Tassaert, P. De Heyn, K. Komorowska, S. Selvaraja, D. Van Thourhout, G. Morthier, R. Baets and R. Halir. *III-V/silicon photonic integrated circuits for FTTH and on-chip optical interconnects.* In 5th International Conference on Broadband and Biomedical Communications (IB2COM) (invited paper), Malaga, Spain, December 2010.

18. S. Stanković, G. Roelkens, D. Van Thourhout, R. Baets, R. Jones, M. Sysak and B. Koch. *Hybrid III-V/Silicon laser based on DVS-BCB bonding.* In 13th Annual Symposium of IEEE/LEOS Benelux Chapter, pages 139–142, Enschede, Netherlands, November 2008.

19. S. Stanković, G. Roelkens, D. Van Thourhout, R. Baets and R. Jones. *Hybrid III-V/Silicon laser based on DVS-BCB die-to-wafer bonding.* In ePIXnet Spring School 2008: p. 42, Portoferraio, Elba Island, Italy, May 2008.

A.3 Publications in national conferences

20. S. Stanković. *DVS-BCB bonded, hybrid III-V/Si laser.* In 10th UGent-FirW PhD Symposium, pages 294–295, Ghent, Belgium, December 2009.