English text

Contents

Chapter 1

Introduction

1.1 Research context

1.1.1 Trends in interconnections

The transport of data over long distances using optics is currently booming. This is the result of the availability of high-performance light emitters and light detectors, and the availability of low-loss optical waveguides, in which the light is transported. It allows to transport multiple terabits per second data signals over a single fibre with a diameter of a quarter millimeter. This is the field of long-distance optical interconnects, which is the base of the internet.

Within a computer, large amounts of data are transported between the processing units, typically over metallic paths on Printed Circuit Boards (PCBs). However, there are limits to the performance of this type of short-distance interconnects. The performance of CMOS integrated circuits (ICs) increases exponentially as a function of time, as predicted by Moore's law. The individual transistors become smaller, resulting in higher processing density and increasing operation speed. This increasing processing density is joined with an increasing interconnect complexity. In general, the interconnect complexity of a digital system is described by Rent's Rule. The number of interconnections of a (sub)system depends on the number of basic elements inside this (sub)system [1]. This implies that, as the processing capability of CMOS based processors increases, the number of interconnections also do increase. As a result, the total input-output data rate of ICs increases rapidly. Moreover, it was found that there is a physical upper limit to the amount of data transmitted by metallic based interconnects[2]. The maximal bandwidth of a metallic interconnection is given by:

$$B = B_0 \frac{A}{L^2}$$

with A the overall cross-section, L the length of the transmission path, and B_0 a constant which depends on the resistivity of the metal. B_0 is typically 10^{15} bit/s

for MCM-type interconnections and 10^{16} bit/s for inter-chip interconnections. But more probably, the performance of electrical interconnects will be limited by power dissipation, weight or volume constraints. For example, the pitch of the connections on a chip package is limited by mechanical constraints. These problems exist for interconnections at all levels in a computing system: intra-chip interconnects, inter-chip interconnections, even intra-cabinet interconnections.

This issue is really a big problem. The ITRS[1] predicts the performance of future CMOS based chips in its famous roadmaps [3]. They admit that the interconnection between chips will run into difficulties starting from 2007, and completely new solutions need to be found. A few alternatives are enumerated: 3D interconnected chips, RF-interconnected chips and ... optically interconnected chips.

1.1.2   Light Emitting Diodes

In Light emitting Diodes (LEDs), light is generated through spontaneous emission. LEDs are robust light emitters, but they are known to be slow and inefficient light sources. Typically, the overall efficiency of planar LEDs is under 2 %. In case of fibre coupling applications, the efficiency is even smaller, due to the limited numerical aperture and small core diameter of the fibre.

It is clear that many applications need higher performance LEDs. Several advanced structures and techniques to enhance the efficiency of the LEDs have been proposed, as the embedding of the LED in an epoxy dome, or the use of advanced light outcoupling structures (such as the surface roughened LED, or the tapered LED), or by altering the internal light emission characteristics. Using these advanced structures, efficiencies of over 40 percent have been achieved.

In this work, an advanced LED will be studied: the Resonant-Cavity LED (RCLED) [4][5]. In the RCLED[2], the internal spontaneous emission characteristics are changed by putting the active layer in a short resonant cavity (or a microcavity). The simplest RCLEDs are planar devices, in which the active layer is placed in between two mirrors, typically a metal mirror or a Distributed Bragg Reflector (DBR)[3] (see figure 1.1). The microcavity effect can be used to enhance the optical efficiency, to change the far-field pattern, to enhance the coupling efficiency into fibres, or to reduce the spectral width of the emitted light.

The first RCLEDs were presented in the early nineties. Since then, many groups have realised RCLEDs, emitting light from visible blue to far-infrared (see table 1.1, a larger efficiency at 660 nm (up to 9 %) was presented by OSRAM at the EOS Summer School in Monte Verita, Switzerland, in 2000, but this

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[1]The International Technology Roadmap for Semiconductors, formerly known as SIA, the Semiconductor Industry Association, groups all important chip companies.

[2]in literature, the device is also known as the Micro Cavity LED (MCLED).

[3]A DBR is a semiconductor high-reflective structure, consisting of a stack of two quarter-wavelength layers with different refractive index. This will be discussed in detail in section 3.5.3.
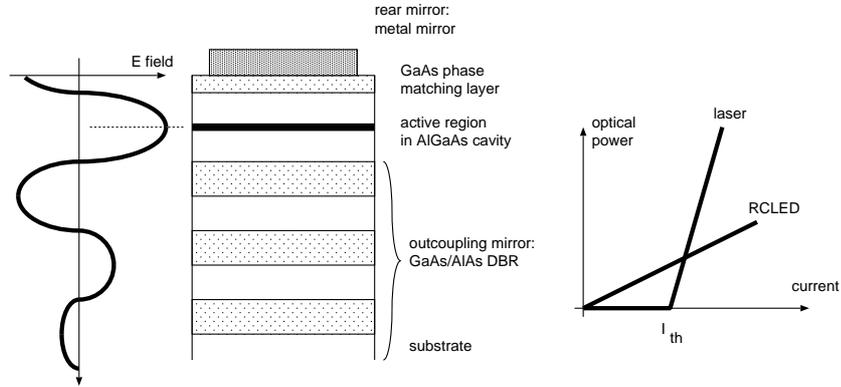
Figure 1.1: The layer structure of a RCLED, with the internal standing wave profile (left) and a comparison of output power as a function of the drive current, for a RCLED and a laser (right).

λ	efficiency	size	shape	remark	year	reference
500 nm			top	ZnSe based	1997	[6]
650 nm	5.23 %	200 μm	top	on germanium	2000	[8]
660 nm	5 %	84 μm	top		1998	[7]
850 nm	14.7 %	200 μm	top		1999	this work, [9]
850 nm	9 %	50 μm	bottom	substrate-removed	2000	this work
980 nm	22.4 %	2 mm	bottom	uses photon recycling	1997	[11]
980 nm	27 %	6 μm	top	AlO$_x$ DBR	1999	[10]
980 nm	10 %		top		1999	[12]
1300 nm	9 %		bottom		1999	[13]
1550 nm	7 %	80 μm	bottom		1997	[14]
3.2 μm	0.2 %		bottom	CdHgTe based	1995	

Table 1.1: Overview of the performance of RCLEDs with various emission wavelengths.

number was not published in literature to the knowledge of the author). In addition, several advanced components have been realised: RCLED based tunable light sources have been reported, both at short wavelength (940 nm range [16]) and at long wavelength (1500 nm range [17]). RCLEDs have been monolithically integrated in GaAs MESFET circuits [18], and gray scale micro displays have been realised [19]. RCLED devices are not limited to III-V semiconductors: devices have been realised on silicon using a porous-Si based active region [20], and using organic light emitting materials (Organic Light emitting Diode, OLED) [21]. During the course of this work, two companies announced RCLEDs in their product folio: Mitel and OSRAM. The devices emit light at visible wavelengths (orange - red), and are suitable as a light source for large-core POF communication, or as a high-brightness indicator.

1.2   Purpose of this work

At the time of the start of this work, RCLEDs were successfully optimised for a maximal overall efficiency. This success inspired to look for advanced applications for the devices. The need for short-distance optical links for high-performance computer systems is such an application. Therefore, RCLED based parallel inter-chip interconnect links were investigated in this work. This is a solution for the interconnect problem, which is suitable for integration in a broad range of electrical systems, as high-performance computing units and telecommunication switching equipment. This link transports large amounts of digital data over a short distance (typically a few tens of cm). Such links includes inter-chip interconnections, or intra-cabinet links in systems.

It is clear that two characteristics of RCLEDs are very important for this application. Firstly, it is not the overall efficiency, but the efficiency into the fibre that needs to be optimised. Highly efficient devices were available (efficiencies up to 22.4 % were reported). However, these devices were very large (2mm diameter), and therefore not suitable for fibre based optical interconnect applications. Secondly, the speed characteristics of the device need to be investigated and maximised. Moreover, large arrays of RCLEDs have to be mounted directly on the silicon chip. The influence of the integration technique on the performance of the RCLEDs was another research issue.

Finally, the RCLED based parallel interconnect links were investigated, both theoretically and experimentally.

1.3   Structure of this thesis

This thesis starts with a brief introduction on parallel optical interconnections in chapter 2. The first part of this book (chapters 3, 4 and 5) handles the efficiency and the realisation of RCLEDs and RCLED arrays. In chapter 3, the physics of the light emission in semiconductors and the microcavity effect are discussed, and a simple, but accurate, model for the extraction efficiency

of RCLEDs will be presented. This model allows to study the influence of the microcavity parameters in the optical properties of the RCLED. Chapter 4 presents the realisation and characterisation of RCLED arrays, suitable for flip-chip mounting on CMOS chips, and it compares the efficiency of different device structures, emitting light at 850 nm or 980 nm. In chapter 5, the advanced properties of RCLEDs are studied, such as the temperature influence and the scaling of the RCLED towards very small diameter devices.

In the second part, the speed properties of RCLEDs are investigated, and an adequate high-speed model is derived. This model is based on the rate equations. In chapter 6, these rate equations are derived, and their validity is discussed. The speed properties of RCLED were experimentally characterised, and compared to the theory. In chapter 7, a high-speed model suitable for use in electrical circuit design tools is presented, together with a parameter extraction procedure. Finally, CMOS-integrated driver circuits are discussed in chapter 8. Different driver circuits, optimised for RCLEDs using the high-speed model, have been realised and characterised.

In the last part, RCLED based interconnect links are investigated. In chapter 9, a simple simulator tool for such optical interconnect links is presented, and the design of the links using this software tool is discussed. The measurements and analysis of the interconnect links is presented in chapter 10, and the performance of RCLEDs in these links is compared to links that are based on another light source.

The most important conclusions of this work are summarised in chapter 11. It is found that RCLEDs are suitable light sources for plastic optical fibre based parallel optical interconnect links. However, the optical efficiency of the RCLED is rather small compared to other light sources, such as vertical lasers. This implies that the overall power budget of the RCLED based link is rather limited, resulting in severe requirements on the alignement and the tolerances of the optical pathway. The switching speed of the RCLEDs can be high, up to 1 Gbps if an optimised driver circuit is used. These characteristics, in combination with the modest requirements on the fabrication side, make the RCLED a promising candidate as light source for parallel optical interconnections, especially if the extraction efficiency of the device is boosted by using an advanced light extraction mechanism.

1.4 Overview of the publications

The results obtained within this work have been published in various papers and presented at various conferences. This paragraph gives an overview of the publications.

Parts of the results are described in a chapter of the following book:

1. P. Bienstman, R. Bockstaele and R. Baets: "Basics of Dipole Emission from a Planar Cavity", chapter in book "Confined Photon Systems: Fundamentals and Applications", eds. H. Benisty, J.-M. Gerard, R. Houdre, J. Rarity and C. Weisbuch, Springer, 1998

The following journal papers have been published, or are accepted for publication:

1. R. Bockstaele, C. Sys, J. Blondelle, B. Dhoedt, I. Moerman, P. Van Daele, P. Demeester and R. Baets: "Resonant Cavity LEDs Optimized for Coupling to Polymer Optical fibres", IEEE Phot. Techn. Lett., Vol 11, no 2 (feb 1999), pp 158-160

2. R. Bockstaele, A. Van Hove, T. Coosemans, C. Sys, I. Moerman, B. Dhoedt, R. Baets, P. Van Daele: "Microcavity LED Based Parallel Data Link Using Small Diameter (125 um) Plastic Optical Fibres", Journal of Optics A : Pure and Applied Optics, Vol 1, no 2 (febr 1999) pp 233-236

3. V. Baukens, G. Verschaffelt, P.Tuteleers. P. Vynck, H. Ottevaere, M. Kufner, S. Kufner, I. Veretennicoff, R. Bockstaele, B. Dhoedt, R. Baets and H. Thienpont: "Performance Simulations of Optical Multi-Chip-Module Interconnects : Comparing Guided-Wave and Free-Space Pathways", Journal of Optics A : Pure and Applied Optics, Vol 1, no 2 (febr 1999) , pp 255-261

4. R. Bockstaele, T. Coosemans, C. Sys, L. Vanwassenhove, A. Van Hove, B. Dhoedt, I. Moerman, P. Van Daele, R. Baets, R. Annen, H. Melchior, J. Hall, P. Heremans, M. Brunfaut and J. Van Campenhout: "Realisation and Characterisation of 8×8 Resonant Cavity LED arrays mounted onto CMOS drivers for POF based interchip interconnections", IEEE Journ. Sel. Top. Quant. Electr., Vol 5, no 2 (mar 1999), pp 224-235

5. Ronny Bockstaele, Joff Derluyn, Carl Sys, Steven Verstuyft, Ingrid Moerman, Peter Van Daele and Roel Baets: "Realisation of Highly Efficient 850 nm top-emitting Resonant Cavity Light Emitting Diodes", Electronics Letters, Vol 35, no 18 (june 1999), pp 1564-1565

6. T. Coosemans, A. Van Hove, R. Bockstaele, K. Vandeputte, L. Vanwassenhove, B. Dhoedt, R. Baets, P. Van Daele, J. Van Koetsem and L. Van den Torren: "MT-compatible connectorisation of VCSEL and RCLED arrays to plastic optical fibre ribbon for low cost parallel datalinks", Mat. Science in Semicond. Proc., Vol 3 (2000), pp 475-480

7. Ronny Bockstaele, Bart Moeyerszoon, Dirk Taillaert and Roel Baets: "A Large-signal Time-domain Model and its Implementation for Gigabit-per-second High-efficient RCLEDs", IEEE Journ. Quant. Electr., accepted for publication

The following papers have been presented at international conferences:

1. R. Bockstaele, C. Sys, J. Blondelle, H. De Neve, B. Dhoedt, I. Moerman, P. Van Daele and R. Baets: "Microcavity LEDs with an Overall Efficiency of 4 % into a numerical aperture of 0.5", LEOS Summer Topical Meetings, Montreal, Canada, 1997, pp 69-70

2. A. Van Hove, R. Bockstaele, T. Coosemans, B. Dhoedt, R. Baets and P. Van Daele: "Termination and Coupling experiments for a 1x12 small diameter (125 um) plastic optical fibre array and POF coupling to microcavity LEDs", LEOS Benelux Symposium, Eindhoven, The Netherlands, 1997, pp 113-116

3. R. Bockstaele, A. Van Hove, T. Coosemans, C. Sys, I. Moerman, B. Dhoedt, R. Baets, P. Van Daele: "Microcavity LED Based Parallel Data Link Using Small Diameter (125 um) Plastic Optical Fibres", Optics in Computing 98, Brugge, Belgium, Proc. SPIE Vol. 3490, 1998, pp 293-296

4. V. Baukens, G. Verschaffelt, P.Tuteleers. P. Vynck, H. Ottevaere, M. Kufner, S. Kufner, I. Veretennicoff, R. Bockstaele, B. Dhoedt, R. Baets and H. Thienpont: "Performance Simulations of Optical Multi-Chip-Module Interconnects : Comparing Guided-Wave and Free-Space Pathways", Optics in Computing 98, Brugge, Belgium, Proc. SPIE, Vol 3490, 1998, pp 412-415

5. V. Baukens, G. Verschaffelt, P. Tuteleers, P. Vynck, H. Ottevaere, M. Kufner, S. Kufner, H. Thienpont, I. Veretennicoff, R. Bockstaele, B. Dhoedt and R. Baets: "Guided-wave versus free-space pathways for optical intra-multi-chip-module interconnects: Performance simulations and design rules", OSA 1998 Summer Topical Meeting on Diffractive Optics and Micro-Optics, Kailua-Kona, 1998, pp 346-348

6. F. Berghmans, S. Coenen, B. Brichard, F. Vos, M. Decreton, G. Verschaffelt, A. de la Fuente, I. Veretennicoff, H. Thienpont, R. Bockstaele, P. Bienstman, C. Sys, B. Dhoedt, I. Moerman, R. Baets, P. Van Daele and J. Jonsson: "Preliminary results on high total dose testing of semiconductor photonic sources : a comparison of VCSELs and Resonant-Cavity LEDs", SPIE Annual Meeting, San Diego, USA, SPIE Proc. Vol. 3440, 1998, pp 47-56

7. R. Bockstaele, B. Depreter, J. Blondelle, B. Dhoedt, I. Moerman, P. Demeester, P. Van Daele and R. Baets: "High efficiency microcavity LEDs", CLEO/Europe, Glasgow, UK, 1998, paper CWA1 (invited)

8. R. Bockstaele, C. Sys, S. Verstuyft, L. Vanwassenhove, B. Dhoedt, I. Moerman, P. Van Daele and R. Baets: "Flip Chip Mounted Substrate-Removed 850 nm Bottom-Emitting 8×8 MCLED Arrays with Selectively Oxidised Current Windows", LEOS Benelux Symposium, Gent, Belgium, 1998, pp 97-100

9. V. Baukens, A. Goulet, U. Mezquíriz Navarro, I. Veretennicoff, W.R. Cox, C. Guan, R. Bockstaele, R. Baets and H. Thienpont: "Enhancing the transmission efficiency of parallel optical interconnection systems using drop-on-demand microlenses", LEOS Benelux Symposium, Gent, Belgium, 1998, pp 73-77

10. B. Dhoedt, R. Baets, I. Moerman, P. Van Daele, P. Demeester, T. Coosemans, A. Van Hove, R. Bockstaele, C. Sys and L. Vanwassenove: "Microcavity LEDs coupled to POF arrays for Parallel Optical Interconnects", LEOS Annual Meeting, Orlando, USA, 1998, pp 331-332

11. R. Bockstaele, C. Sys, L. Van Wassenhove, B. Dhoedt, I. Moerman, P. Van Daele, R. Baets: "Realisation of highly efficient and high-speed resonant cavity LEDs for coupling to plastic optical fibres", SPIE - Photonics West, San Jose, USA, Proc. SPIE Vol. 3621, 1999, pp 221-229

12. T. Coosemans, A. Van Hove, R. Bockstaele, K. Vandeputte, L. Vanwassenhove, B. Dhoedt, R. Baets, P. Van Daele, J. Van Koetsem and L. Van den Torren: "MT-compatible connectorisation of VCSEL and RCLED arrays to plastic optical fibre ribbon for low cost parallel datalinks", Proc. EMRS 1999, (2000), pp

13. A. Van Hove, T. Coosemans, R. Bockstaele, K. Vandeputte, L. Vanwassenhove, B. Dhoedt, R. Baets and P. Van Daele, J. Van Koetsem, L. Van den Torren: "Direct MT-compatible connectorisation of LED-arrays to plastic optical fibre ribbon for low cost parallel datalinks", ECTC 99, pp 1096-1102

14. D. Delbeke, B. Dhoedt, R. Bockstaele, I. Moerman, P. Van Daele, T. F. Krauss and R. Baets: "Electrically Pumped Photonic Crystal Micro-Cavity Light Emitting Diodes", LEOS Summer Topical Meetings, San Diego, USA, 1999, pp 71-72

15. T. Coosemans, A. V. Hove, R. Bockstaele, J. Derluyn, I. Moerman, R. Baets and P. V. Daele: "Optical Data Communication Using Substrate-removed 850 nm RCLEDs and Small Core Fibres", POF99, 1999, pp 246-249

16. Ronny Bockstaele, Dirk Taillaert, Bart Moeyersoon and Roel Baets: "A large-signal time-domain model and its implementation for 1 Gbit/s driving of highly efficient RCLEDs", LEOS Annual Meeting, San Fransisco, USA, 1999, pp 637-638

17. M. Brunfaut, J. Depreitere, W. Meeus, J. M. Van Campenhout, H. Melchior, R. Annen, P. Zenklusen, R. Bockstaele, L. Vanwassenhove, J. Hall, A. Neyer, B. Wittmann, P. Heremans, J. Van Koetsem, R. King, H. Thienpont, R. Baets: "A Multi-FPGA Demonstrator with POF based Optical Area Interconnect", LEOS Annual Meeting, San Fransisco, USA, 1999, pp 625-626

18. Thierry Coosemans, An Van Hove, Ronny Bockstaele et al: "850 nm LEDs and Fibre Coupling", SPIE - Photonics West, San Jose, USA, proc. SPIE Vol 3938 (2000), pp 160-168

19. D. Delbeke, K. Vandeputte, R. Baets, R. Bockstaele, B. Dhoedt, I. Moerman, P. Vand Daele and S. Verstuyft: "Holographically Defined Grating Assisted Microcavity Light Emitting Diodes", LEOS Benelux Symposium, Mons, Belgium, 1999, pp 159-162

20. M. Brunfaut, J. Depreitere, W. Meeus, J. M. Van Campenhout, H. Melchior, R. Annen, P. Zenklusen, R. Bockstaele, L. Vanwassenhove, J. Hall, A. Neyer, B. Wittmann, P. Heremans, J. Van Koetsem, R. King, H. Thienpont, R. Baets: "An optical area I/O enhanced FPGA with 256 optical channels per chip", OC2000, 2000

21. R. Bockstaele, R. Baets: "Simulation of interchip interconnections based on Resonant Cavity LEDs, Plastic Optical Fibres and CMOS interface circuits", LEOS Summer Topical Meeting on Electronically Enhanced Optics, Miami, USA, 2000, pp 39-40 ISBN 0-7803-6252-7

22. R. Bockstaele, M. Brunfaut, J. Depreitere, W. Meeus, J. M. Van Campenhout, H. Melchior, R. Annen, P. Zenklusen, J. Hall, A. Neyer, B. Wittmann, P. Heremans, J. Van Koetsem, R. King, H. Thienpont, L. Vanwassenhove and R. Baets: "Latency study of an optical area I/O enhanced FPGA with 256 optical channels per CMOS IC", LEOS Summer Topical Meeting on Electronically Enhanced Optics, Miami, USA, 2000, pp 27-28 (ISBN 0-7803-6252-7)

23. L. Vanwassenhove, R. Bockstaele, R. Baets, M. Brunfaut, W. Meeus, J. Van Campenhout, J. Hall, H. Melchior, A. Neyer, J. Van Koetsem, K. Ebeling and P. Heremans, Proc. Symp. IEEE LEOS Benelux, Delft, Nederland, 2000, pp 55-58

24. R. Bockstaele, R. Annen, D. Taillaert, B. Moeyersoon, M. Brunfaut, J. Van Campenhout, J. Hall, H. Melchior and R. Baets : "Design and Realisation of High-Speed Transmitter Arrays Based on CMOS Integrated Drivers and Resonant Cavity LEDs", LEOS Annual Meeting, Puerto Rico, USA, 2000, pp 173-174 (ISBN 0-7803-5947-X)

The following presentations were done at international symposia, without proceedings:

1. R. Bockstaele, C. Sys, J. Blondelle, H. De Neve, F. Goussaert, B. Dhoedt, I. Moerman, P. Van Daele and R. Baets: "Microcavity LEDs for Optical Interconnects", The Rank Prize Funds Mini-Symposium on Devices and Systems for Opical, Interconnects and Datalinks, Grasmere, UK, sept 1997

2. A. Van Hove, R. Bockstaele, T. Coosemans, B. Dhoedt, R. Baets and P. Van Daele: "Termination and Coupling experiments for a 1x12 small diameter (125 um) plastic optical fibre array and POF coupling to microcavity LEDs", URSI Forum 97, Gent, Belgium, dec 1997

3. R. Bockstaele : "Short-Wavelength, Highly-Efficient Microcavity LEDs and their applications in POFbased Parallel Optical Interconnects", IoP Meeting on Photonic Bandgaps and Related Phenomena, Glasgow, UK, may 1998

4. R. Bockstaele: "MCLEDs for POF based Interconnection Links", Summer School and EOS Topical Meeting on Semiconductor Microcavity Light Emitters, Monte Verita, Switserland, sept 1998

5. R. Bockstaele: "Flip Chip Mounted Substrate-Removed 850 nm Bottom-Emitting 8×8 MCLED Arrays with Selectively Oxidised Current Windows", URSI Forum 98, Brussel, Belgium, 1998

6. P. Bienstman, W. Bogaerts, R. Bockstaele, D. Delbeke, S. Goeman, B. Depreter, J. Derluyn, C. Sys, L. Vanwassenhove, B. Dhoedt, I. Moerman, P. Van Daele, R. Baets: "Microcavity and PGB-related activities at the University of Gent", COST 268 Workshop, Stockholm, Zweden, 1999

7. Marnik Brunfaut etc: "OIIC Demonstrator", ESPRIT Workshop, Athene, Griekenland 1999

8. R. Bockstaele : "Optically interconnected chips", First PhD Symposium, Gent, Belgium, 2000

Two presentations were awarded a prize:

1. "Best contributed Paper" at the "The Rank Prize Funds Mini-Symposium on Devices and Systems for Opical Interconnects and Datalinks", Grasmere, UK, 1 to 4 september 1997

2. "Laureaat Presentatieprijs", Eerste Doctoraatssymposium, Gent, Belgium, 5 december 2000

Chapter 2

Optical Interconnection

In this chapter, the characteristics and performance of the current and future parallel optical interconnections in and between digital systems will be discussed. Special attention will be given to the light source and the structure of optical links.

2.1   Optical interconnects: a systems point of view

Within computing systems, digital information needs to be transported between logical blocks. There are several solutions for this, as metallic interconnections on Printed Circuit Boards (PCBs) using standard CMOS signalling levels, interconnections using impedance matched metallic waveguides, or optical interconnections. Currently, metallic interconnections on PCBs is the standard approach for transmitting data between chips. This is the low-cost solution for low to moderate data rates. However, high-performance applications (which will be the standard systems of the future) need an advanced interconnect technology. Whatever kind of link is used, it has to fulfil several requirements:

- the data must be transmitted in a reliable way

- the interconnect solution must be cheap

- the solution must be easy to use: the interconnect link must be easily integrated in the design cycle and in the production process of the system.

- the operation speed and the power dissipation must fulfil the specifications, set by the system.

The design of the link is heavily influenced by the choice of the transmission medium. Examples of such media are coaxial cables, micro-strips on PCBs, or optical fibres. Each medium has its advantages and disadvantages, which may limit the overall performance of the link. There are many issues to be solved during the design of the link:

- degree of parallelism ? Data can be transmitted using many moderate-speed channels in parallel, or using a few ultra-high-speed channels. Multiplexing techniques can be used to fit the overall aggregate bandwidth over the available number of channels. However, multiplexing needs large, power-hungry and complex interface circuits.

- single-ended or differential signals ? Differential transmission can be used to reduce switching noise and to simplify the receiver design, but at the expense of an increased number of channels

- use of a data coding technique ? This is used to obtain a balanced signal and to reduce the switching noise.

- will the signal at the receiver signal be regenerated or re-timed ?

- will it be cheap, feasible and reliable ? repairable ?

In case of an optical interconnection, extra design choices need to be resolved:

- which technology will be used for the driver and the receiver circuits ?

- which devices will be used for the light emission and light detection ?

- direct modulation versus external modulation ?

- how will the subparts be integrated ?

- what optical pathway will be used ?

These issues will determine the success of the product, and should therefore be taken into account when designing the link.

For this thesis, only a few of these issues will be discussed. The main emphasis is on the light source and the driver circuit. They are part of a simple link architecture: a parallel link consisting of 8×8 array of point-to-point links, requiring a CMOS signal as input and generating a CMOS signal at the output. The optical pathway is a Plastic Optical fibre (POF) array.

2.2   Light emitters for optical interconnects

The main part of this thesis does not handle the design of the optical link, but the light source for optical interconnect links. The light emitters should operate close to the digital chip. This implies that the component must fulfil several requirements:

- the restricted available area requires compact components, suitable for two-dimensional integration. This condition excludes all edge-emitting devices for this application, both LEDs and lasers.

- the power dissipation must be minimised. This condition requires a high optical efficiency (this is a large optical power for a given current) and a low voltage drop across the device (implying a small series resistance).

- the electrical properties of the light emitters must be compatible with the CMOS circuitry. In practice, current CMOS technologies allow a 3.3 V supply voltage. The maximal voltage drop across the optical emitter should therefore be smaller[1].

- the modulation speed of the optical component should be at least compatible with the underlying CMOS circuitry. This is not necessarily related to the modulation speed of the individual components: the parallelism allows to use slower components, while multiplexing techniques can be used to exploit the available bandwidth of the high-speed interconnections.

- the realisation of the devices should be cost-effective. This implies that the yield and uniformity of the light sources should be large.

There are different vertical light emitters available: Light emitting Diodes (LEDs), semiconductor lasers (the Vertical-Cavity Surface-Emitting Laser, VCSEL), and light modulators. The properties of these sources will be discussed hereafter.

2.2.1 Light emitting Diodes

As mentioned in the first chapter, planar LEDs are robust but slow and inefficient light sources. They emit a broad far-field pattern, close to Lambertian, and they emit a broad emission spectrum, typically several tens of nanometer wide. The maximal modulation speed of advanced LEDs is limited to about 1 GHz. The emitted light is not coherent. An important advantage of LEDs is the absence of a threshold current. LEDs can be realised in various material systems, emitting light at various wavelengths, and are in principle easier to fabricate than lasers. However, their efficiency is rather low. Several advanced structures and techniques have been proposed to enhance the efficiency of the LEDs, as the surface roughened LED and the resonant-cavity LED (RCLED). The RCLED will be discussed in detail in the following chapter.

2.2.2 VCSELs and other lasers

The light emission in a laser is based on stimulated emission. This is fundamentally different from the spontaneous emission: the stimulated emitted

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[1]Future CMOS systems will use even smaller supply voltages (1V and below, as expected by the ITRS roadmap). Only (far) infrared emitting devices have a bandgap compatible with these voltages, but these devices are not efficient. Therefore, it is most likely that CMOS-based systems with integrated optical interconnects will include extra supply lines to drive the optoelectronic components. This will be discussed in chapter 7.
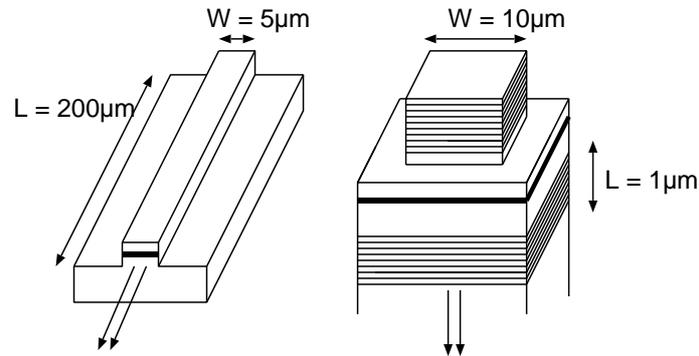
Figure 2.1: Comparison between a well-known edge-emitting laser (left) and newer vertical-cavity surface-emitting laser (right).

photons are coherent (they have the same wavelength, phase and propagation direction). This results in a large efficiency (typical values are 30-50 %[2]), a narrow emission spectrum and a narrow light beam. Moreover, lasers have large modulation bandwidth, if they are operated at a sufficiently high current. However, there is minimal carrier density in the active layer before the stimulated emission can start, resulting in a threshold current.

A special laser type is the VCSEL (Vertical-Cavity Surface-Emitting Laser). The structure of this laser is comparable to the structure of RCLEDs (see figure 2.1). VCSELs can be easily integrated in two-dimensional arrays, and are therefore useful as light source in parallel optical interconnections, just as RCLEDs. The performance of the VCSEL depends strongly on the device structure and the material system. The best-performing VCSELs are based on the AlGaAs material system, and emit light at 850 nm or 980 nm. Due to the small active volume, the gain per round-trip is much smaller compared to edge-emitting lasers. Therefore, all optical losses must be minimised, and highly reflecting mirrors must be used (typical reflection exceeds 99.9 %). The mirrors of the VCSEL are Distributed Bragg Reflectors, just as in RCLEDs, but the number of pairs must be larger to achieve the desired high reflection. In the AlGaAs material system, typically 20 pairs are necessary to achieve the high reflection at 850 nm or 980 nm. The combination of a small volume of the active region, and a small threshold current density (due to the high-quality cavity) results in an extremely small threshold current. In the AlGaAs system, emission wavelength 850 to 1000 nm, devices with a threshold current in the order of a few tens of μA have been realised. This small threshold current is particularly interesting in low-power applications, as interconnects.

In other material systems, it is more difficult to achieve high-quality mir-

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[2]Remark that this is comparable to the efficiency of state-of-the-art LEDs. However, the radiance (light per unit of emitting area, per unit of solid angle) of lasers is much larger. This is particularly useful in applications with a limited numerical aperture, as fibre coupling.

component	array size	single mode ?	λ [nm]	Ith [mA]	slope [W/A]	volt [V]	beam [deg]	speed [GHz]	series resist. [Ω]
CSEM	5×5	no	950	1.7	0.3	1.7	12	> 3	
CSEM	8×8	no	960	0.6	0.4	1.5	16	> 3	
TrueLight TSD-9A10	1	no	980	5	0.2	2.2	8		40
TrueLight TSD-8A12	1	no	850	3	0.2	2.0	8		30
TrueLight TSD-7A10	1	no	785	5	0.25	2.2	8		40
TrueLight TMC-5A40	1	no	850	3	0.25	1.92		> 2	30
LaserMate	1×8	no	850	<5		1.8	8	> 2	30-50
LaserMate VCT-F85B20	1	no	850	5	0.2	2.2	8		40
LaserMate VCT-F85A4X	1	no	850	3	0.25	1.9	8	> 1	30
Laser Components	1	yes	850	2	0.2	3	12	0.2	
Mitel 4D469 (prelim)	1×4	no	840	5.5	0.25	1.8	15	2	
Mitel 1A448*	1	no	840	3.5	0.05	1.9		2	
Mitel 2B455	1	no	840	3.5	0.2	1.9	15	2	
Honeywell HFE4080-321	1	no	850	3.5	0.25	1.8	15		25
Honeywell HFE409x-322	1	no	850	3	0.4	1.8	15	2.5	25
Honeywell SV3639	1	yes	850	0.2	0.3	1.8	20		150
Honeywell SV3641	1	yes	780	0.2	0.3	1.8	20		150
Metrodyne MSEL-085N12	1	no	850	<6	0.2	1.8	10	> 1	
Metrodyne MSEL-085C01	1	no	845	<6	0.2	1.8	10	> 1	
Avalon AVAP-1x10MM	1×10	no	850	2	0.4	1.7	16	> 3	45
Avalon AVAP-8x8MM	8×8	no	960	0.6	0.4	2	16	> 3	
Avalon AVAP760	1	yes	763	2	0.2	2.2	12	0.1	
Avalon AVAP-1x10SM	1×10	yes	850	2.5	0.3	1.8	12	> 3	
Avalon AVAP940	1	yes	940	1.7	0.2	2.0	16	0.1	
Mitel 1A466 (RCLED)	1	no	650		0.02	2.3	50	0.2	

Table 2.1: Overview of the performance of commercially available VCSELs, and a commercially available RCLED.

rors, due to the increased optical losses and the weak optical performance of DBR mirrors. This is the case for long-wavelength VCSELs (at 1.3 μm or 1.55 μm), and VCSELs emitting at visible wavelengths (at 650 nm). Currently, a lot of research is done to use new material systems to achieve the same performance level at these new wavelengths as at 980 nm.

VCSELs emitting at 850 nm and 980 nm are currently commercially available, even in dense arrays. Table 2.1 summarises the performance of commercially available VCSELs. The typical value for the threshold current of VCSELs is a few mA, the slope efficiency is 0.2 to 0.3 mW/mA. For comparison, the specifications of a red RCLED are also given (see the last row). The efficiency and the modulation speed is a factor 10 smaller compared to the VCSELs. The voltage drop across the device is slightly larger, but this is related to the larger bandgap of the active region.

2.2.3   Modulators

Modulators are devices in which the reflection or the transmission is controlled by an external voltage. The reflection spectrum of the modulator changes as a function of the applied voltage, due to the quantum-confined Stark effect. This change of reflection is relatively large at a well-defined (but narrow) wavelength range. In this way, an external light source is modulated. The heat dissipation caused by the electrical to optical power conversion is removed from the dense array of modulating devices. Furthermore, the voltage is applied to a reverse biased diode so that the power dissipation of the device itself is negligible when the modulated light output stays constant. Only when switching, significant power is required to charge the capacitors. The speed of modulators can be very high and is mainly limited by RC effects. The main problem with modulators is their temperature sensitivity: they only operate within a very limited temperature range.

2.2.4   The choice of wavelength

The emission wavelength of the light emitters should be chosen to maximise the performance of the complete link. This performance depends on the architecture of the link. For example, all effects in the fibre (as absorption and dispersion) are extremely important in long-distance transmission systems. The wavelength of long-distance optical links is thus chosen to minimise these effects. In practice, 1300 nm or 1550 nm light is used, corresponding to a minimal dispersion or minimal absorption for glass fibres. In parallel interconnect links, the power dissipation of the complete link is of extreme importance. Therefore, the optimal wavelength is determined by the efficiency of the components of the link. The most important factors are the emission efficiency of the light emitter, the transmission efficiency of the optical pathway and the sensitivity of the receiver.

Figure 2.2 shows a simplified analysis of a POF based interconnect link, based on the power budget, omitting bit rate dependent effects and assum-
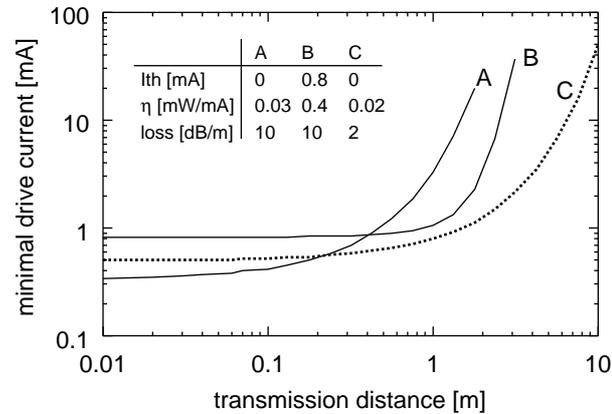
Figure 2.2: Comparison of the minimal drive current required for a single optical link, assuming a POF as the optical pathway. Case A corresponds to a 980 nm RCLED, case B to a 980 nm VCSEL and case C to a 650 nm RCLED.

ing the same coupling efficiencies. At 980 nm, the RCLED is the best choice for small transmission distances, up to 40 cm. The VCSEL should be chosen if the transmission distance is longer. However, if another wavelength is chosen (650 nm light), then the RCLED is always the best solution, in spite of its smaller efficiency, because of the reduced absorption in the fibre. This simple calculation shows the importance of the choice of wavelength. In this work, 980 nm and 850 nm RCLEDs will be studied. These wavelengths are (in combination with the plastic fibre) the best choice for very short-distance interconnections, due to the high efficiency of the devices.

2.3 Optical interconnections

In this paragraph, a few examples of parallel optical interconnect systems will be given. These can be divided into different categories, according to different classifications. An overview of the different optical links is given in figure 2.3.

2.3.1 Figures of merit

Before discussing the structure of an optical interconnection, an overview of the important figures of merit of optical interconnect links will be given. The best-known parameter of a link is its total bandwidth (this is the total bit rate, summed over all channels). This is also called '**aggregate bandwidth**'. For a typical link, this number is at least tens of Gbps, and typically a few Tbps. This parameter simply has to fulfil the requirements set by the application, and tend to increase on logarithmic scale as a function of time, as set by Moore's law. In synchronous systems, the total delay of the signal (or **'latency'**) is an important
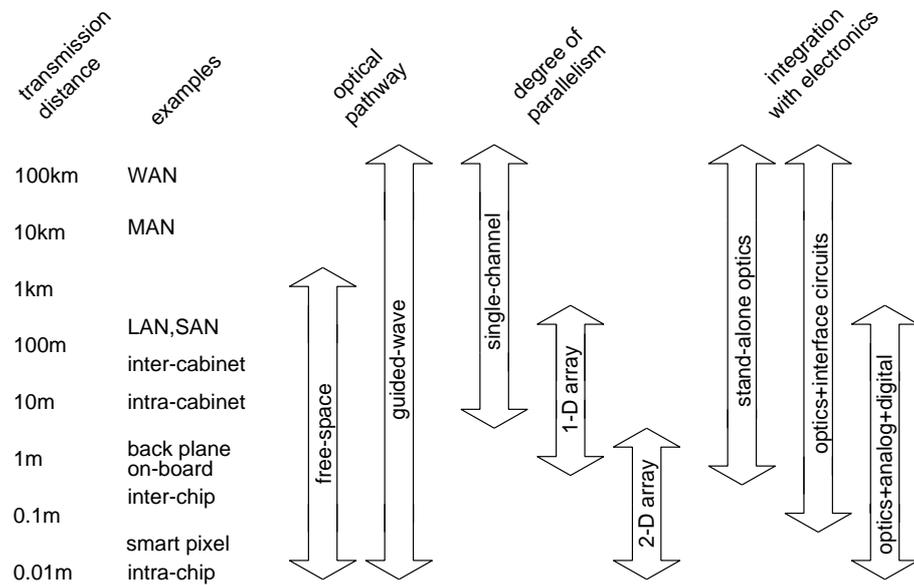
Figure 2.3: Classification of optical interconnect links.

parameter. The latency and the bandwidth are not necessarily related: a long-distance link has typically a very large latency, but can nevertheless support a very high bit rate.

The **power dissipation** is another critical parameter. The limits of the power dissipation are set by the thermal design of the system. Currently, the total power dissipation on chip is limited to about $10\,\mathrm{W/cm^2}$. The power dissipation might limit the maximal bit rate of an individual link.

The **chip area** of the total interconnect link should be minimised. This chip area (the real estate in CMOS terms) includes the area for the driver circuits, the area for the mounting (bond pads), and the area for the receiver circuits (including detector if it is integrated in the CMOS). This chip area is directly related to the cost of the total system.

The systems should fulfil the Electromagnetic Compatibility (**EMC**) rules: the link should be resistent to external noise sources, and it should generate no noise. This requirement might result in different circuit designs, influencing both the maximal operation speed, power dissipation and the chip area.

Finally, the **total cost** of the system should be minimised. This includes an optimisation of the yield of the individual processing steps and a minimisation of the cost of the individual processing steps and of the resources (as cost of the optoelectronic components, or the cost of the CMOS area). This total cost might be the most important factor determining the success of optical interconnects.

company	product	#channels	bitrate/ch.	aggr. bitrate	dissipation	light source
Hitachi		12	800 Mbps	10 Gbps	300 mW/ch	edge
Gore	nLIGHTEN	12	1.5 Gbps			VCSEL
Infineon	Paroli	12	1.25 Gbps	15 Gbps		VCSEL
Motorola	Optobus	10	400 Mbps	4 Gbps		VCSEL

Table 2.2: Overview of some commercially available parallel interconnect products.

2.3.2 Classification according to the parallelism

The optical links can be divided in single-channel links, one-dimensional links and two-dimensional links. The total amount of transported data ('the aggregate bandwidth') is proportional to the number of channels is the link. Currently, most of the optical interconnections are single-channel links. The multi-channel links are currently being introduced, mainly 1×8 arrays.

The parallelism allows to divide a certain aggregate bandwidth over a few high-speed channels, or over many moderate-speed channels. This might be advantageous, because it allows the use of low-cost interface electronics, which can have an important impact on the total price of the system.

2.3.3 Classification according to the transmission distance

A first classification uses the interconnect distance as the selection criterion. The different interconnections can be divided in intra-chip links (typical transmission distance is smaller than a few cm), inter-chip links (typically a few tens cm), links on the backplane level and intra-cabinet links (up to 1 m or more), inter-cabinet links (a few tens meter) and SANs (Storage Area Networks), Local Area Networks (LANs) and Metropolitan Area Networks (MANs) and the very-long-distance interconnections (WANs, Wide Area Networks).

The last two categories (LAN and MAN) are today already exclusively optics based, mostly using single-mode glass fibre systems. The bandwidth of the fibre is fully exploited by using Wavelength Division Multiplexing (WDM) techniques. The typical bandwidth is several tens of Gbps, up to Tbps. For LAN applications, optical fibre based systems are competing with copper wires (UTP Cat 5 and 6). The typical transmission distance is up to 300 m. The preferential optical approach uses 1.3 μm lasers or 850 nm lasers and glass multi-mode fibres. Alternative products use plastic fibre. The maximal bandwidth is typically a few hundreds Mbps up to 1 Gbps.

The other types of interconnections, over a shorter distance, are today exclusively metal based. However, the bandwidth of the copper based interconnects is limited (this is the interconnect bottleneck, which was introduced in the first chapter), and new products, using optics, are currently being introduced. An example of an optical product for intra-cabinet interconnections is the VCSEL based transceivers, which are typically used in Fibre Channel appli-

cations, Gigabit Ethernet, Very Short Range (VSR) SONET links (the interconnect approach of the terabit routers) and general intra-system links. The market for this type of interconnections is currently booming. There are many, commercially available, parallel transceivers, mostly based on a one-dimensional VCSEL array and a multi-mode glass fibre ribbon. A typical product contains 8 or 12 channels, each channel modulated at 1 to 2 Gbps. The aggregated bandwidth is typically a few tens Gbps. Table 2.2 gives an overview of some of these products. There are a few alternative products, as the SpectraLan product (from Agilent), which uses a single-fibre 4 channel WDM system using VCSELs.

In conclusion, there is a trend to use optical interconnects for transmission over increasingly shorter distances, due to the increased demand for bandwidth. Nowadays, optics in being introduced in inter-cabinet interconnection products. Currently, there are no products for optical interconnections for a smaller transmission distance (towards the inter-chip level). In this work, very-short-distance interconnections will be studied, mainly for this application.

2.3.4   Classification according to the optical path

The optical pathway determines the size and the view of the optical interconnect links, and can be used to classify the links. Roughly speaking, two categories exist: the free-space interconnections and the guided-wave interconnections. In free-space links, the light source is projected on the detector using an imaging system (based on lenses and mirrors, just as in a camera system). This approach has the advantage that the beams can cross each other, without interfering. This allows the realisation of very compact systems. However, the divergence limits the maximal transmission distance. Currently, single-channel free-space links are commercially available, for LAN applications. The typical transmission speed is a few hundred Mbps, the maximal transmission distance is up to a few hundreds meter. On the research level, many free-space demonstrator systems for intra- and inter-chip interconnects have been reported. Such free-space inter-chip interconnections are easily realised in large arrays. Figure 2.4 shows a free-space demonstrator.

The alternative approach uses waveguides to transport the light. Today, the vast majority of the interconnections uses waveguides. Far longer transmission distances can be achieved compared to free-space interconnections, especially if low-loss glass fibre is used. The waveguides can be divided into single-mode waveguides and multi-mode waveguides. The single-mode waveguides have a very small core diameter, which complicates the coupling of light into the fibre and tightens the tolerance requirements. But the single-mode fibre has superior transmission properties compared to multi-mode waveguides (because the multi-mode dispersion is avoided). Furthermore, the waveguides can be divided in flexible waveguides (such as glass fibre, plastic fibre or fibre image guides) and stiff waveguides (such as polymer waveguides in PCBs). The flexible waveguides have the advantage that the alignment of the waveguide to the emitter is independent on the alignment of the waveguide to the detector,
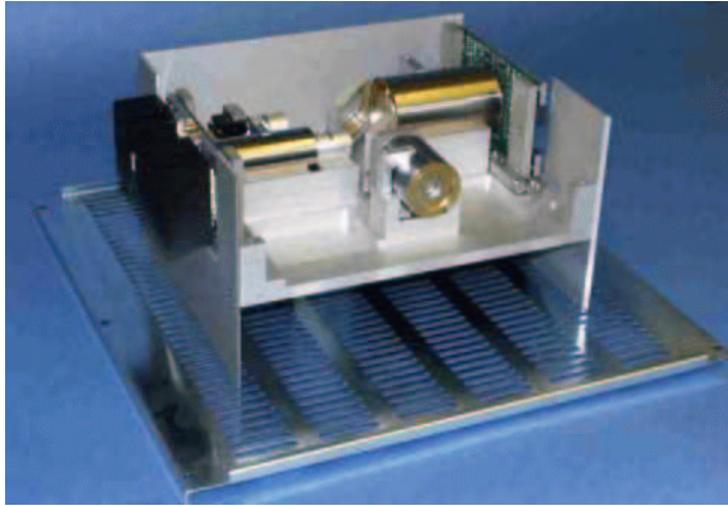
Figure 2.4: A free-space optical interconnect demonstrator: the SPOEC demonstrator (after [23]).

which simplifies the mechanical design of the system (this is the local alignment). Furthermore, flexible waveguides allow the realisation of connectors. An example of a guided-wave optical interconnect system is shown in figure 2.5.

Each optical transmission approach, free-space and guided-wave, is characterised by a certain numerical aperture (NA). This is the maximal propagation direction of the light which is guided by the system. Light propagates under other angles is lost, or disturbs the neighbouring channels in case of a parallel link. The numerical aperture of free-space systems is typically small (because the beam spreading must be minimised, to reduce the cross-talk). Waveguides allow a larger numerical aperture, especially polymer waveguides and plastic fibres. The large numerical aperture allows to realise shorter bends compared to low-NA waveguides, resulting in a more compact pathway. But the multimode dispersion increases, which may limit the maximal bandwidth. This allows the use of large NA light sources, such as LEDs. A special example is the fibre image guide, which consists of many very small fibres, glued together. This type of waveguide removes the alignment issues at one side of the optical link. The NA of such waveguides can be large (up to one).

In this work, an optical interconnect link based on a guided-wave optical pathway is investigated. The optical pathway is a 8×8 array of large-NA plastic fibre (with a diameter of 120 μm and a NA of 0.5). This allows to use large-NA light sources, as the resonant-cavity LED.

2.3.5   Classification according to the integration level

The optical component is always in some way connected to an electrical chip. This allows another classification of the interconnections. The first category includes single components, in a package, but not integrated with the driver chip. Currently, most of the lasers and LEDs are available in this way. High-speed lasers are available in butterfly packages, LEDs and VCSELs typically in TO-46 packages. The long-distance interconnections are typically based on such components.

The second category contains optical interconnections based on light sources, directly integrated on the chip. This is the hybrid integration: the light source and the driver electronics are realised using different semiconductor technologies. This chip contains the interface circuits (as the driver and the receiver). This approach results in compact and high-speed modules. The main advantage is the elimination of the parasitics between the analogue driver and receiver circuits and the light emitter. This approach allows a compact realisation of parallel optical interconnect modules, as the VCSEL based transceivers. These modules include the driver and receiver electronics, mostly a data coding and error correcting circuit. They are straightforwardly integrable onto printed circuit boards (PCBs).

A special category is the monolithically integrated transmitter module, in which the driver electronics and the light emitter are integrated in the same semiconductor technology, on the same substrate. An example is the ultra-high-speed InP-based transmitter (typically operating at 40 Gbps). The main advantage of this approach is the elimination of the parasitic effects, which is important at these ultra-high bit rates.

In a third category, the optics and the interface circuits are integrated together with the digital electronics. This allows the realisation of very compact and high-bandwidth modules. For these links, issues as power dissipation and die area are extremely important, due to tight integration with the digital circuitry. The applications of these parallel optical interconnection links are digital systems which need an ultra-high input-output bandwidth. Such links can be divided into two categories, according to the functionality of the transmission. A first group includes (parallel) interconnections systems, with a point-to-point link functionality. As an example, an optically interconnected router chip may include an on-chip optical interconnection to the other router chips. Such CMOS-integrated optical interconnections might also boost the performance of computer systems. However, several theoretical studies have shown that the advantage of using optical interconnects in Von Neumann computer architecture based PC is rather small. This is explained by the rather large latency of optical interconnections, and the optimisation of the current data access architectures using different levels of cache memory [22].

The second category of optical-analogue-digital integrated interconnections are massively parallel computing systems. This is the field of smart pixels: many, small processing units are optically interconnected. Such links are currently still in the development stage. Examples are the crossbar switch, in

which a variable connection between many input channels and many output channels is realised [23], like ATM switching units [25]. Parallel computing systems also benefit from the optical interconnects [24]. A special type of parallel computing system is the optoelectronic Field Programmable Gate Arrays (FPGAs) [27]. This kind of system will be discussed in next paragraph. Advanced vision systems use parallel optics to connect the detector array with the parallel image processing unit [29]. Finally, a computing system based on distributed sensors on microscopic scale ('smart dust') uses optics as communication channel, because of the smaller volume and better power budget compared to microwaves [30].

2.3.6 The OIIC demonstrator

An excellent example of an advanced computer system that makes use of optical interconnects is an FPGA system. An FPGA (Field Programmable Gate Array) consists of many elementary logical units and many interconnect blocks. The digital functionality of the logical units and the connections in the interconnect blocks must be programmed. Typical applications for FPGAs are the simulation of processors and rapid prototyping of digital systems. The performance of these systems depends strongly on the performance and parallelism of the interconnections between the logical units. Such systems need fast and massive parallel interconnections, in and between chips (in case of multi-chip FPGA systems). Optical interconnect is the solution to boost the performance of such systems [31].

A functional FPGA demonstrator has been built within the European funded OIIC project[3] [32][33]. This work will refer many times to this demonstrator, and therefore, some more details are given. The chip contains an FPGA, consisting of programmable logical blocks, programmable interconnect switches, and both metallic and optical interconnects between the switches. The demonstrator chip is realised in a 0.6 μm CMOS technology. The 8×8 RCLED and VCSEL arrays, emitting at 980 nm, and detector arrays are mounted onto the CMOS chip using a solder reflow flip-chip technique. The optical pathway is an 8×8 array of small core plastic optical fibres (POF, core diameter 120 μm, outer diameter is 125 μm). In the demonstrator, three such chips are optically interconnected (see figure 2.5).

2.4 Conclusion

The requirements of parallel optical interconnect links were discussed in this chapter. It was found that many design choices exist. This work will deal with a few of these choices, mainly related to the driver circuit and the light source. Several light sources for this type of interconnects were presented, and the choice of the wavelength was briefly discussed. It was found that this choice

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[3]OIIC stands for Optically Interconnect Integrated Circuits.

Figure 2.5: A guided-wave optical interconnect demonstrator: the OIIC system demonstrator.

is heavily determined by the type of optical pathway. Finally, an overview of parallel interconnect links was given. The links can be divided in several categories, depending on the transmission distance, the optical pathway and the integration level. In this work, the inter-chip optical interconnections will be discussed.

Chapter 3

Efficiency of RCLEDs

In this chapter, the optical properties of Resonant-Cavity Light emitting Diodes will be presented. This starts with a description of some basic LED characteristics, such as the efficiency and the voltage drop. Then, the properties of the spontaneous emission inside semiconductors will be discussed, because this is the foundation of the light emission in RCLEDs. Finally, the influence of the resonant cavity on the light emission characteristics of the RCLED will be investigated. This includes the derivation of a simplified expression for the extraction efficiency of RCLEDs. This chapter will end with a discussion on the design of RCLEDs, mainly for fibre coupling applications.

3.1 Introduction

3.1.1 The efficiency of LEDs

The efficiency of light emitters is an important number, because it allows to compare the performance of different light emitting devices. It can be defined in different ways, making the interpretation of the number sometimes cumbersome. In this work, the overall efficiency of a light emitter is defined as the ratio of the optical output power to the injected electrical current[1] . This overall efficiency should be maximised to minimise the drive current and the heat generation inside the device. The overall efficiency of LEDs depends on many different factors, such as the injection of the carriers in the active region, the internal light generation, and the extraction of the light. It depends also on the energy of the emitted photon. As a result, this figure is useless to compare the performance of devices emitting light at different wavelengths. A better characteristic of LEDs is the external quantum efficiency QE_{ext}. This dimensionless

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[1]In general, an *efficiency* is a dimensionless number. In this work, the 'overall efficiency' has the dimension of W/A. This is not an efficiency, a better word would be 'conversion factor'. However, the word 'efficiency' is used frequently in the field of optoelectronics, and is therefore also used in this work. In this thesis, a *quantum* efficiency is always a dimensionless number, because it describes the useful fraction of a number of quanta (electrons or photons). This definition will be introduced in the continuation of this paragraph.

number expresses the ratio of the number of extracted photons to the number of electrons injected in the device. The QE$_{ext}$ is a better figure to compare the performance of light sources emitting at different wavelengths, as it does not depend on the photon energy. This QE$_{ext}$ is in general given by (see figure 3.1):

$$QE_{ext} = \eta_{inj}\eta_{int}\eta_{extr} \qquad (3.1)$$

, where η_{inj} is the injection efficiency: this is the ratio of the useful current to the total injected current. A part of the injected current can be lost at parallel current paths. The injection efficiency is large if the device is carefully designed, and this injection efficiency is in most cases close to 100 %. The η_{int} is the internal quantum efficiency, this is the ratio of the number of photons generated inside the active layer to the number of recombinations. This number is limited by the non-radiative recombination mechanism. It depends on the quality of the active layer: typical values are in the order of 70 % to 99 %, depending on the material system. The next factor determining the overall efficiency is the extraction efficiency η_{extr}. This is the ratio of the number of photons emitted in air, to the number of generated photons inside the active layer. This number depends strongly on the shape of the LED, as will be discussed later on. Planar LEDs have a small extraction efficiency, typically a few percent. The rest of the generated light is absorbed somewhere in the semiconductor material.

In some applications, only a part of the extracted photons are useful. An example is an LED coupled to an optical fibre. Not all light emitted by the LED is coupled into the waveguide. This is expressed by a coupling efficiency η_{coupl}.

The optimisation of the external quantum efficiency QE$_{ext}$ requires a careful optimisation of each of these efficiencies. It is found that the extraction efficiency is the most important factor. In this work, the resonant-cavity LED is studied, which has an increased extraction efficiency compared to planar LEDs, as will shown in this chapter.

3.1.2   Output power as a function of the current

In this paragraph, the output power of the LED as a function of the drive current will be presented. This is derived from the balance equation, a standard procedure, as can be found in reference [34]. The balance equation describes the equilibrium between the injected and the disappearing (recombining) carriers in the active region of the LED. The number of injected carriers is determined by the drive current. The number of recombining carriers depends on the carrier density. The recombination rate is written as:

$$R(n) = An + Bn^2 + Cn^3$$

, with n the carrier concentration, A is the non-radiative recombination coefficient (which is the reciprocal of the non-radiative lifetime τ), B is the radiative
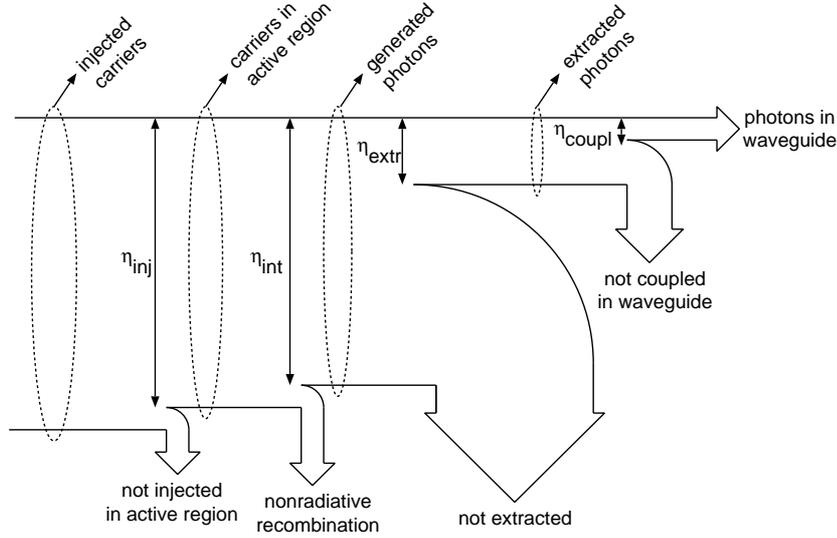
Figure 3.1: Flow of the electrons to photons conversion in an LED.

recombination coefficient (the bimolecular recombination coefficient[2]), and C presents the Auger recombination. The non-radiative recombination mechanism will be dominant at low carrier concentrations, the radiative recombination will be dominant at moderate carrier concentrations, and the Auger recombination will be dominant at very high carrier concentrations. This equation is valid for both bulk and quantum-confined structures. The Auger recombination is an important effect in long-wavelength active regions, due to the small bandgap [34]. In this work, mainly short-wavelength light emitters will be studied, and therefore the Auger recombination is always neglected (except if explicitly mentioned). The balance equation can be written as:

$$\frac{I_{inj}}{qVol} = \frac{n}{\tau} + Bn^2 \tag{3.2}$$

with I_{inj} the injected current, q the elementary charge, Vol the volume of the active region, τ the non-radiative lifetime and B the bimolecular recombination coefficient. This equation can be solved for the carrier density:

$$n = \frac{1}{2B\tau} \left(\sqrt{1 + \frac{4BI_{inj}\tau^2}{qVol}} - 1 \right) \approx \sqrt{\frac{I_{inj}}{BqVol}} \tag{3.3}$$

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[2]The word 'bimolecular recombination' would imply that two molecules are needed for the recombination. However, this word is used in a more general sense for all recombination effects in which two partners are needed, such as an electron and a hole.

The approximation is valid for large non-radiative lifetimes. This corresponds to high-quality active layers, in which almost all recombinations are radiative.

The output optical power is directly proportional to the radiative recombination term. This is valid if no time-dependent effects occur during the extraction of light. Such effects do occur in lasers: the optical cavity results in a short delay in the emission of the photons, written as a photon lifetime. This effect is neglected in case of LEDs[3]. The optical power is given by:

$$P_{out} = h\nu \eta_{extr} B n^2 Vol \qquad (3.4)$$

with $h\nu$ the photon energy and η_{extr} the extraction efficiency. The internal quantum efficiency, defined as the ratio of the radiative recombination to the total recombination, can be written as a function of the injected current:

$$\eta_{int} = \frac{Bn^2}{\frac{n}{\tau} + Bn^2} = \frac{\sqrt{1 + \frac{4BI_{inj}\tau^2}{qVol}} - 1}{\sqrt{1 + \frac{4BI_{inj}\tau^2}{qVol}} + 1}$$

The internal quantum efficiency increases as a function of the injected current, and approaches one at large injection current levels. At low current levels, the carrier concentration is low and the non-radiative recombination is dominant, as explained above. A "threshold" current (not to be confused with the threshold current of a laser diode) can be defined, at which the internal efficiency η_{int} is 0.9:

$$I_{min} = 25 \frac{qVol}{B\tau^2}$$

A typical value for τ for high-quality active layers is 10 ns to 1 μs. The corresponding minimal current density is typically a few A/cm^2.

For parameter extraction purposes, the relation between the optical power and the RCLED current can be transformed to a linear relation (see appendix A):

$$\sqrt{P_{out}} = \alpha\beta \frac{I_{inj}}{\sqrt{P_{out}}} \pm 2\sqrt{\alpha} \quad \alpha = h\nu\eta_{extr}\frac{Vol}{4B\tau^2}, \ \beta = \frac{4B\tau^2}{qVol} \qquad (3.5)$$

This equation can be used to estimate the non-radiative lifetime and the extraction efficiency, if the bimolecular recombination coefficient and the volume of the active region are known. Figure 3.2 shows a few measurements on two different LED types: RCLEDs emitting at 980 nm, and RCLEDs emitting at 850 nm. The extraction efficiency of the 980-nm RCLEDs is about 14 %, the extraction efficiency of the 850-nm RCLEDs is 7 %. The 850-nm RCLEDs have both a smaller extraction efficiency (the slope is smaller), and a smaller internal quantum efficiency (the zero point is larger). The origin of these effects will be discussed in the next chapters.

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[3]In case of RCLEDs, the photons are generated inside a cavity. The photon has a certain lifetime before it escapes the cavity. However, these cavities have a small Q-factor, and the corresponding photon lifetime is very small compared to the other time-effects in the RCLED.
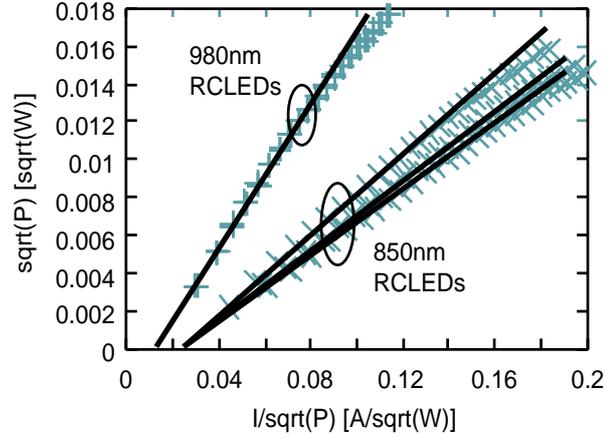
Figure 3.2: Measured efficiency curves, fitted to relation 3.5, for different RCLED devices with a 50 μm diameter.

3.1.3 Extraction efficiency

The extraction efficiency describes how well the internally generated photons are extracted from the device. In planar devices, only a part of the internally generated photons is extracted, the rest is lost due to the Total Internal Reflection (TIR) at the semiconductor-air interface, as dictated by Snell's Law. The maximal incidence angle at which the light is transmitted at the semiconductor-air interface is given by the critical angle:

$$\theta_{crit} = \arcsin \frac{n_1}{n_2}$$

with n_1 the refractive index of the outer material (in most cases n_1 is one, corresponding to air), and n_2 the refractive index of the semiconductor. Only the photons emitted into this escape cone will be extracted, the rest is bounced back at the interface due to the TIR. The extraction efficiency is given by the fraction of the photons emitted in the escape cone (assuming an isotropic power distribution inside the semiconductor $p(\theta)$):

$$\eta_{extr} = \frac{\int_0^{\arcsin \frac{1}{n}} p(\theta) 2\pi \sin(\theta)\, d\theta}{\int_0^{\pi} p(\theta)\, 2\pi \sin(\theta)\, d\theta} \approx \frac{1}{4n^2}$$

For example, planar LEDs based on a GaAs substrate (n=3.5) have an extraction efficiency of about 2 %. This extremely low extraction efficiency limits the employment of LEDs in many applications. Several solutions to increase the extraction efficiency have been proposed. They can be summarised as follows:

1. The critical angle can be increased by embedding the LED in a transparent epoxy dome with a high refractive index. This implies that more light
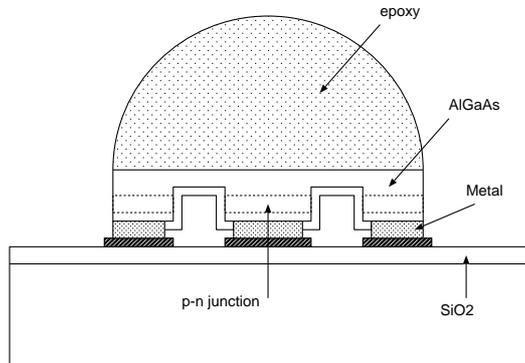
Figure 3.3: A commercially available, highly efficient LED structure with an epoxy dome.
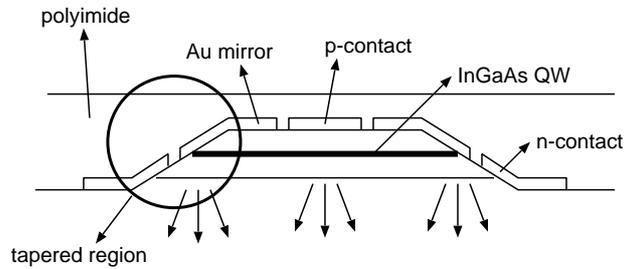
Figure 3.4: Drawing of a tapered LED (after [37]). The light is extracted at the active region (just like in conventional planar LEDs) and at the tapered regions (encircled on the drawing).
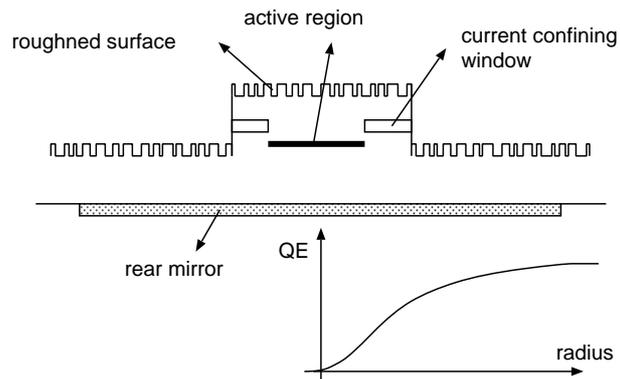
Figure 3.5: Drawing of an NRC-LED (after [39]). The light is extracted all over the roughened surface of the device.

escapes from the semiconductor into the epoxy. This technique would not help to increase the extraction efficiency of the LED if the epoxy layer was also planar, because of the TIR at the epoxy-air interface. But if the epoxy dome is curved and sufficiently large compared to the LED dimensions, then all light will hit the epoxy-air interface within the critical angle, and will be extracted [35] (see figure 3.3). This is the standard approach to increase the efficiency of indicator LEDs. However, the emission area increases, making this technique less useful in dense area applications.

2. The light can be extracted from multiple output planes [35]. In case of a cubic LED, the extraction efficiency can be up to 6 times larger if all planes are used to extract light. Advanced structures can be used to redirect the light inside the LED, to extract more light from the device. The simplest adaptation is the inclusion of a rear mirror in a planar LED. In this way, the extraction efficiency will be doubled. The optimum is a spherical LED: all generated light bounces perpendicularly to the semiconductor-air interface, and is thus extracted from the device. However, such components are hard to realise. Moreover, multiple output plane devices are not practical in parallel interconnect applications.

3. Other techniques alter the path of the photon until it hits the semiconductor-air interface within the extraction cone. Several techniques can be used to obtain a redistribution of the propagation directions of the photons: it can be done in a controlled way (as in deformed chips [36], or by using a taper [37]) or in a more randomised way (by using a surface roughening [38]). An example of a deformed chip is a truncated inverted pyramid structure. Due to the shape of the device, the light bouncing at a skew interface gets a different propagation angle. Using this approach, in combination with multiple-plane extraction, world-record efficiencies up to 55 % at room temperature (32 % without the epoxy dome) have been obtained [36]. In a tapered LED (see figure 3.4), the generated light propagates between 2 highly reflective mirrors, towards a tapered region. Light propagating in the taper will be reflected at skewer angles. At the end, the light hits the taper wall within the critical angle, and it will be extracted. Overall efficiencies (at 980 nm) up to 26 % have been measured, and up to 44 % if the tapered LED was encapsulated in an epoxy dome [37]. These components, however, need large taper regions. Typical device diameters are about 100 μm. In an NRC-LED (Non-Resonant-Cavity LED [39], see figure 3.5), the high extraction efficiency is achieved by the redistribution of light at the roughened surface. The efficiency can be further increased by roughening the surface next to the active region, as shown in figure 3.5. Overall efficiencies up to 41 % have been achieved, and up to 55 % if the NRCLED is covered with an epoxy dome[39].

4. The photons which undergo the total internal reflection can be reabsorbed by the active region, and the generated carriers can afterwards recombine

again, increasing the chance that the new photon is emitted into the good solid angle. This effect has been known for long, and has been used in LEDs to increase the efficiency [41] and in lasers to decrease the threshold current [40]. It should be mentioned that the reabsorption of the active region depends on the carrier density, and there is no absorption above the transparency carrier density [42]. Therefore, this technique works only if the device is driven at a low current density.

5. The angular power distribution inside the device can be altered, in such a way that more light is emitted in the extraction cone. This technique is used in RCLEDs, the devices which will be studied in this thesis. The microcavity effect changes the preferential propagation direction of the spontaneously emitted photons. More advanced devices use a combination of the microcavity effect and a (controlled) redistribution of light using a grating. Such devices are currently under development [43].

In this work, the RCLED was chosen as the light source for parallel optical interconnects. The RCLED has a large efficiency, it has a simple processing procedure and it is suitable for two-dimensional integration using a flip-chip technology.

3.2   The intrinsic spontaneous emission

This paragraph describes the properties of the intrinsic spontaneous emission inside semiconductors. This is the spontaneous emission in semiconductors without a microcavity. Different theories describe the spontaneous emission. This paragraph will summarise the most important results.

3.2.1   Spontaneous emission in atomic systems

Spontaneous emission is always related to a recombination effect: an electron and a hole recombine because the final state has a lower energy[4]. During the recombination, energy is released under form of a photon (light) or a phonon (a localised mechanical vibration, representing heat). The former corresponds to a radiative recombination, the latter to a non-radiative recombination. The transition probability of the radiative recombination given by Fermi's Golden Rule [44]:

$$W = \frac{2\pi}{\hbar} \left| \langle i \left| H \right| f \rangle \right|^2 \rho\left(E\right) \delta\left(E - E_{ph}\right)$$

E_{ph} is the photon energy, $\rho\left(E\right)$ is the density of final (optical) modes as a function of the energy of the photon (this is the mode density), and $\left| \langle i \left| H \right| f \rangle \right|^2$ describes the probability that a transition between initial state |i> and final state

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[4]only bipolar devices are taken into account. Another class of semiconductor-based light emitter are unipolar devices, in which photons are emitted during intra band transitions of a carrier between two quantum states in a (rather complex) quantum-well like structures.

|f> occurs in the system (this is also called the matrix element, or the matrix dipole element, also written as $|M_b|^2$). The term $\delta\left(E - E_{ph}\right)$ indicates that the energy of the emitted photons is E_{ph}. The Hamiltonian H describes the energy of the system. In case of emission into an optical mode corresponding to a planar wave, this matrix element is given by:

$$\langle i \,|H|\, f \rangle = \frac{q}{m_0} \sqrt{\frac{2\hbar}{\epsilon_0 n^2 \omega}} \frac{1}{2} \langle i \,|\overrightarrow{e} \cdot \overrightarrow{p}|\, f \rangle \tag{3.6}$$

with m_0 the mass of the electron, ϵ_0 the permittivity in free space, n the refractive index and ω the pulsation of the optical mode ($\omega = 2\pi f$, with f the frequency of the light). The vector $\overrightarrow{p}$ is the electron-momentum vector, and $\overrightarrow{e}$ is the unit vector, determining the polarisation of the electric field of the optical mode. The electron-momentum vector is determined by the properties of the material in which the emission occurs.

The mode density $\rho\left(E\right)$ describes the number of optical modes in a given energy interval. This mode density is altered by the microcavity effect, and is therefore further discussed. The mode density is easily visualised in k-space. In k-space, every point represents an optical mode (a planar wave), with wave number given by the distance from the origin to this point, and propagation direction given by the vector from the origin to this point. The wave number is related to the wavelength by $k = 2\pi/\lambda$. The intrinsic spontaneous emission is presented by a sphere in k-space (the emission wavelength (or wave number) does not depend on the emission direction).

In this section, the optical mode density in free space is considered [44]. Assume that the photons are emitted in a (large) volume $V = L^3$. The fundamental electromagnetic modes in this volume are planar waves, of which the amplitude of the electrical field is written as $E\left(\overrightarrow{r}\right) = E_0 \exp\left(-j\overrightarrow{k} \cdot \overrightarrow{r}\right)$, with $\overrightarrow{k}$ the wave vector. These modes must fulfil the boundary conditions. This results in the discretisation of the allowed wave numbers:

$$k_x = n_x \frac{2\pi}{L}, \; k_y = n_y \frac{2\pi}{L}, \; k_z = n_z \frac{2\pi}{L} \tag{3.7}$$

with n_x, n_y, n_z the mode numbers. In k-space, every mode occupies a certain volume $dk_x dk_y dk_z = \left(\frac{2\pi}{L}\right)^3$. The number of modes with an amplitude between 0 and k can be calculated, by dividing the total volume in k-space ($\frac{4}{3}\pi k^3$) by the volume of a single mode:

$$N_k = 2\frac{\frac{4}{3}\pi k^3}{\left(\frac{2\pi}{L}\right)^3} = \frac{k^3 L^3}{3\pi^2}$$

The factor 2 corresponds to the fact that every k-vector represents 2 polarisations, thus 2 modes. The mode density is defined as the number of modes, per unit volume and per unit of energy:

$$\rho\left(E\right) = \frac{1}{V}\frac{dN_k}{dE} = \frac{k^2}{\pi^2}\frac{dk}{dE} = \frac{8\pi}{\left(h\frac{c}{n}\right)^3}E^2$$
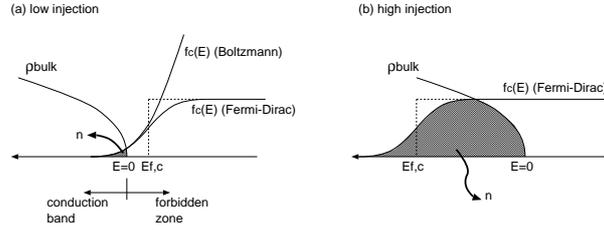
Figure 3.6: Schematic presentation of the density of states ($\rho\left(E\right)$) and the occupation probability ($f\left(E\right)$) in the conduction band, at very low injection levels (left) and at very high injection levels (right)

This mode density changes inside microcavities, and results in an increased or decreased spontaneous emission lifetime. The presence of the cavity results in different boundary conditions for the electromagnetic modes, and the allowed modes are not given by equation 3.7, but they depend strongly on these boundary conditions. This is the microcavity effect, which will be discussed in detail in section 3.5.1.

3.2.2   Properties of carriers in semiconductors

In a semiconductor, the electrons and holes are moving in a periodic stack of atoms, the crystal. This crystal results in a background electromagnetic field, which influences the behaviour of the carriers. It determines the density of states of the carriers (this is the number of electron states at a given electron energy level), and the dipole matrix element inside the semiconductor crystal. The behaviour of electrons in semiconductors is described by the Schrödinger equation. This equation has no closed-form solution, and even most approximate solutions in case of specific semiconductors are very complex. The simplest approximation is the effective-mass theory. In this approximation, the complete influence of the crystal onto the properties of the carrier is summarised into one parameter: the effective mass. The carriers behave as if they are in free space, but with a different mass. Using the effective-mass approximation, the energy of the carriers, E, is given by:

$$E(k) = \frac{\hbar^2 k^2}{2 m_{eff}}$$

The effective-mass approximation gives no information on the matrix dipole element. As stated before, the dipole moment describes the overlap between the initial and final state of the electron in a given system. More advanced approximations should be used to study the matrix dipole element. It is found that 4 important energy bands exist in III-IV semiconductors: one conduction band and three valence bands: the heavy holes, the light holes and the split-off holes.

In a semiconductor, the free electrons occupy a (broad) energy band. The number of electrons at a certain energy level depends on the total number of possible states at that energy level (the density of states DOS, $\rho\left(E\right)$), and on the occupation probability that an electron exists at an energy E ($f\left(E\right)$). The DOS is derived in the same way as the optical mode density. However, the electrons (holes) have a different (E,k) relation compared to photons.

$$\rho^{bulk}\left(E\right) = \frac{\sqrt{4m^3}}{\pi^2\hbar^3}\sqrt{E}$$

with m the mass of the carrier. $f\left(E\right)$ is the occupation probability, as a function of the carrier energy E. This probability is given by a Fermi-Dirac distribution:

$$f_c(E) = \frac{1}{1 + \exp\left(\frac{E-E_{f,c}}{kT}\right)} \approx \exp\left(-\frac{E-E_{f,c}}{kT}\right)$$

with $E_{f,c}$ the quasi-Fermi level of the carriers in the conduction band. The approximation (a Boltzmann distribution) is valid if $E > E_{f,c}$. The total number of electrons is given by the integration over all energy levels:

$$n = \int_0^\infty \rho^{bulk}\left(E\right) f_c\left(E\right) dE$$

with E=0 corresponding to the top of the conduction band. A similar expression exists for the hole concentration. In case of a bulk semiconductor, this integral has no closed-form solution. In case that $E_{f,c} < 0$ (Fermi level inside bandgap, this corresponds to the low-injection limit), an approximation for the carrier concentration and the occupation probability function can be found:

$$n \approx N_c \exp\left(\frac{E_{f,c}}{kT}\right) \Rightarrow f_c\left(E\right) \approx \frac{n}{N_c} \exp\left(\frac{E}{kT}\right) \tag{3.8}$$

with N_c the effective density of states. N_c depends on M_c, this is the number of equivalent minima in the conduction band and m_n is the electron mass:

$$N_c = M_c 2 \left(\frac{2\pi m_n kT}{h^2}\right)^{\frac{3}{2}}$$

The number of carriers, for a given Fermi level, depends on the effective mass. Therefore, the heavy holes will outnumber the light holes for a given Fermi level, due to the larger effective mass. In case of large injection ($E_f > 0$, corresponding to a degenerated semiconductor), the occupation probability function can be approximated by a step function:

$$f_c(E) \approx H\left(E - E_{f,c}\right) \tag{3.9}$$

with $H\left(E - E_0\right)$ the Heaviside function. In that case, the carrier concentration is given by:

$$n \approx \int_0^{E_f} \frac{\sqrt{4m_n^3}}{\pi^2\hbar^3}\sqrt{E}dE = \frac{\sqrt{4m_n^3}}{\pi^2\hbar^3}\frac{2}{3}E_f^{\frac{3}{2}} \tag{3.10}$$
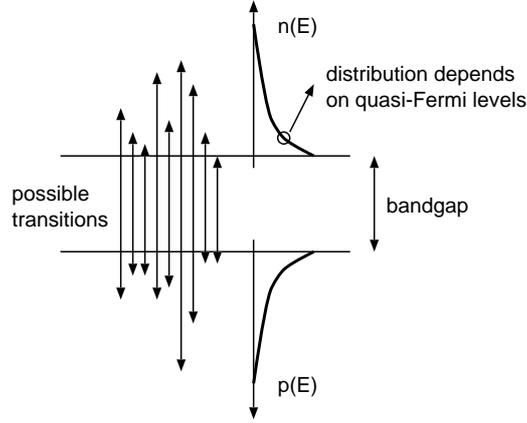
Figure 3.7: Influence of quasi Fermi levels on spontaneous emission spectrum.

3.2.3   Recombination in semiconductors

In this paragraph, the recombination rate in bulk semiconductors is discussed. The spontaneous emission rate in semiconductors is more complex compared to the mono-atomic system. Firstly, the matrix dipole element is determined by the properties of the crystal. And secondly, the rate has to be averaged over all energy levels of the carriers.

The transition between electrons and holes is calculated as the transition rate in a single particle case, multiplied by the number of holes (electrons) at the energy level. This is given by the electron (hole) density of states (ρ_c, ρ_v) and the occupation probability (f_c, f_v) [34].

$$R_{SpEm}\left(E, E'\right) = \frac{4\pi n q^2 E_{ph}}{m_0^2 \epsilon_0 h^2 c^3}\left|M_b\right|^2 \rho_c\left(E\right) f_c\left(E\right) \rho_v\left(E'\right) f_v\left(E'\right)$$

with $\left|M_b\right|^2$ the matrix dipole element. The total spontaneous emission rate at a photon energy E_{ph} is given by the integration over all energies E, assuming $E' = E - E_{ph}$. The overall emission rate R_{SpEm} is then found by integrating over all emission energies:

$$R_{SpEm} = \int_{E_g}^{\infty} R_{SpEm}\left(E_{ph}\right) dE_{ph}$$

This integral is a function of the Fermi levels of the electrons and holes, which depend on the electron and hole concentration. In this way, the emission rate depends on the carrier concentration. At low injection levels, the occupation probability functions for electrons and holes ($f_c\left(E\right)$ and $f_v\left(E'\right)$) are proportional to the electron and hole concentration (see equation 3.8). Therefore, the recombination rate is proportional to the product of the electron and

hole concentration, written as $R_{SpEm} = Bnp$. An expression for B can be found in reference [45].

At large injection levels, the occupation probability function can be approximated by a step function (equation 3.9). In that case, the recombination rate becomes linearly dependent on the carrier concentration. The recombination rate can be written as $R_{SpEm} = B(n)np$, and the bimolecular recombination coefficient depends on the carrier concentration. Following approximate description for the carrier concentration dependent bimolecular recombination coefficient was found [45]:

$$B = \frac{B_0}{1 + \frac{n}{n_0}} \tag{3.11}$$

The effect was experimentally confirmed [46]. Typical values (for AlGaAs material system) are $1.3 \cdot 10^{-10}$ cm^{3}s^{-1} for B and $4 \cdot 10^{19}$ cm^{-3} for n_0.

3.2.4 Recombination in quantum wells

Because of its extreme importance in experiments, the recombination in thin films (quantum well) is discussed. The quantum well (QW) alters the boundary conditions for the Schrödinger equation. As a result, only discrete energy levels for the carriers in the well are allowed. The energy relation E(k) of the carriers is changed compared to the bulk semiconductor. The corresponding density of states, for a carrier with mass m, is a staircase function:

$$\rho^{well}(E) = \frac{m}{\pi \hbar^2} \sum_n H(E - E_n)$$

At low carrier densities, only the lowest energy level (E_0, which is slightly higher compared to the conduction band edge, dependent on the well thickness) is populated. In that case, the carrier concentration is given by:

$$n = \int \rho^{well}(E) f_c(E) dE = \frac{4\pi m_n}{h^2} \int \frac{H(E - E_0)}{1 + \exp\left(\frac{E - E_f}{kT}\right)} dE \tag{3.12}$$

The total carrier concentration is found after integration over all energy levels:

$$n = N_c \ln\left(1 + \exp\left(-\frac{E_0 - E_f}{kT}\right)\right) \tag{3.13}$$

with N_c the effective density of states in a quantum well:

$$N_c = \frac{4\pi m_n kT}{h^2}$$

The recombination rate can be calculated as in the previous paragraph. It can be written as $R_{SpEm} = Bnp$ for small carrier concentrations. At large

injection levels, the spontaneous emission rate is also a linear function of the carrier concentration. Therefore, a similar expression as equation 3.11 exists for the bimolecular recombination coefficient.

The quantum well active layer has an important influence on the electron-momentum vector $\vec{p}$. The orientation of this vector determines the far-field pattern of the spontaneous emission. The field emitted during a recombination is, after averaging over many transitions into planar waves with a different propagation direction, the field of a dipole. This is explained by the $\vec{e} \cdot \vec{p}$ in the matrix element (equation 3.6). In a bulk active layer, the k-vectors of the carriers, and thus the electron-momentum vectors $\vec{p}$, are isotropically distributed. The resulting emission field is isotropic, due to the averaging of the dipole fields over all directions. In a quantum well, the electron energy levels, and thus the corresponding electron-momentum vectors $\vec{p}$, have discrete values in the direction perpendicular on the quantum wells [47]. This discretisation reduces the isotropic character of the spontaneous emission.

The anisotropy is described by an increased (or decreased) matrix element, as a function of the polarisation of the light [47]. The polarisation determines the allowed propagation directions of the planar waves. For light polarised parallel to quantum well (which corresponds to light propagating in the vertical direction), the matrix element is 1.5 times larger than in bulk. This corresponds to an enhancement of the light emission with far-field pattern of a horizontally oriented dipole. The matrix element of light polarised perpendicular to quantum well (which is propagating in the plane of the well), is almost zero. This corresponds to an inhibition of the light emission with far-field pattern of a vertically oriented dipole. The use of quantum wells is thus advantageous for vertical light emitters. This is valid for the heavy-hole electron transition, which is the dominant transition due to the large effective mass of the heavy holes.

Depending on the lattice mismatch between the quantum well material and the barrier material, a compressive or tensile strain can exist in the quantum well. This changes the energy of the system, and thus alters the band diagram and the dipole element. As a result, the energy levels of the heavy and light holes shift. Under compression, the energy of the heavy hole energy shifts upward and becomes dominant, and the emission of horizontal dipoles is even more enhanced [48][49]. This theory is experimentally validated, by investigating the influence of strain on the performance of horizontally emitting lasers [50]. It was shown that compressively strained quantum wells exhibit a larger gain. However, the threshold is reduced if tensile strained quantum wells are used. This is related to the enhanced spontaneous emission in the propagation direction of the laser light.

In conclusion, compressively strained quantum well active regions are superior as an active region for vertical light emitters, due to the intrinsic enhancement of the emission of light with the far-field pattern of a horizontal dipole.

3.2.5 The emission spectrum

Next to the emission rate, the emission spectra will play an important role in microcavity based devices. In general, the shape of a spontaneous emission spectrum is determined by two mechanisms: homogeneous and inhomogeneous broadening. Spontaneous emission is characterised by a certain lifetime τ. The time signal is described by a damped exponential function, and the corresponding spectral density is given by a Lorentzian distribution:

$$|S(f)|^2 = \frac{P_0^2}{\frac{1}{\tau^2} + (2\pi f - 2\pi f_0)^2}$$

with f_0 the emission frequency. This is the homogeneous broadening. This spectrum has a certain spectral bandwidth, given by:

$$BW = \frac{2}{\tau}[Hz] = \frac{2\lambda_0^2}{\frac{c}{n}\tau}[nm]$$

with λ_0 the emission wavelength in free space, and n the refractive index of the active material. This bandwidth is typically a few tens picmeter.

The inhomogeneous broadening is caused by the difference of the emission energies of the individual transitions in the system. In a semiconductor, this homogeneous broadening is mainly determined by the distribution of electrons and holes in the conduction and valence band, as was discussed in section 3.2.2. This implies that the broadening depends on the carrier density. This effect is called band filling. This type of broadening is typically much larger compared to the homogeneous broadening.

In case of a quantum well based active region, this broadening can be estimated as follows. The energy at which the carrier density $n(E)$ is half of the maximal value can be estimated from equation 3.12. The bandwidth (expressed in eV) is thus given by:

$$\Delta E = E_f - E_o + kT \ln\left(1 + 2\exp\left(\frac{E_0 - E_f}{kT}\right)\right)$$

The Fermi level E_f can be written as a function of the carrier concentration (see equation 3.13). In this way, the bandwidth is written as a function of the carrier density:

$$\Delta E = kT \ln\left(1 + \exp\frac{n}{N_c}\right) \tag{3.14}$$

The spectral bandwidth of the intrinsic spontaneous emission is, at large carrier concentrations (where the exponential function becomes dominant), thus proportional to the carrier concentration.

This band filling effect was characterised experimentally in [51] for InGaAs based 980 nm QW based active regions. In this work, these measurements
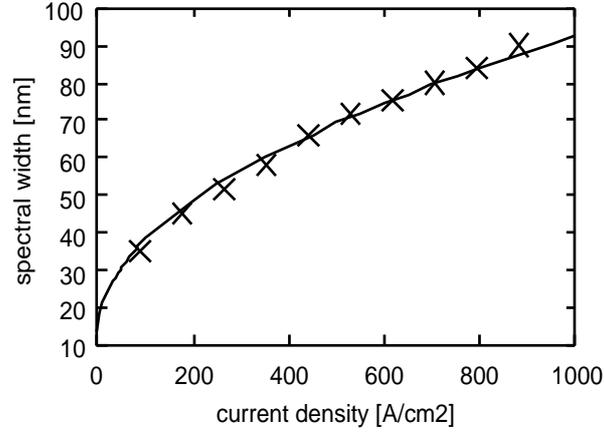
Figure 3.8: Fitted bandwidth of intrinsic spontaneous emission of InGaAs-based quantum wells (the measurements were derived from reference [51]).

were fitted to the proposed model. Equation 3.14 is approximated by a linear expression as a function of the carrier density. And the carrier density is given by the square root of the current density (see equation 3.3). This is valid if the non-radiative recombination is negligible, which is valid for high-quality active regions. Figure 3.8 shows the measured and fitted width of the intrinsic spontaneous emission spectrum. The expression for the bandwidth (in nanometer) is given by:

$$BW_{intr} = 13.4 \left(1 + \sqrt{\frac{J}{28.7}} \right) \tag{3.15}$$

The minimal spectral bandwidth, given by $\lambda^2 kT \ln 2/1240$, is 13.4 nm. A linear approximation (which fits better to the measurements at moderate current densities) is $BW_{intr} = 33$ nm $(1 + J/487)$, with J the current density, expressed in A/cm^2.

3.2.6 Advanced active regions

In the previous paragraphs, two active regions were discussed: the bulk active region, and the quantum well. Currently, a lot of research is done in the field of quantum dots [52][53]. A popular material system is the InGaAs dot on a GaAs substrate. Such an active region can be obtained using a self-organised island growth. The emission wavelength depends strongly on the shape and material properties of the dots. In this way, a broader wavelength range can be covered. This technique is a promising technology to achieve high-quality active regions emitting at 1300 nm, lattice matched on GaAs. Quantum dots have many advantages. There is the tight lateral confinement, omitting the lateral

carrier diffusion effect. This results in very small active regions (typical dimensions of dots is a few nm high, and about 10 nm wide). Theoretically, the dot active region has a very narrow emission spectrum, and it has no temperature dependent emission wavelength. This is not true in practice, due to important secondary effects such as carrier capture mechanisms.

Currently, the internal efficiency of quantum dot active regions is still smaller than that of quantum wells or bulk active layers. This is due to two effects: an important non-radiative recombination can occur (defects can be introduced during the growth, due to the rather large stresses in the system). Secondly, it is particularly difficult to achieve a good capture of carriers in the dots[5]. In fact, there are two competitive recombination channels: one resulting form carriers in the dots, and one resulting from carriers in the spacer layers (so called continuum states). These capture effects have also an important influence on the high-speed properties of the optoelectronic devices [52].

3.3 Voltage drop across LEDs

The voltage drop across the active region is a non-linear function of the carrier density inside the active region [34]. That relation depends on the structure of the active region. In case of a homojunction, the external voltage drop V_j[6] is given by the Shockley equation:

$$V_j\left(n\right) = \frac{kT}{q}\ln\left(\frac{n}{n_i}+1\right) \approx \frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \tag{3.16}$$

n_i is the intrinsic carrier density, a parameter which depends on the material properties of the semiconductor. In case of a quantum well active region, there is no simple expression for the voltage drop. However, if the junction is symmetric, and if only the lowest energy state of the quantum well is occupied, then the following relation holds [54]:

$$V_j\left(n\right) = \frac{E_{g,QW}}{q} + \frac{kT}{q}\ln\left(\left(\exp\frac{n}{N_c}-1\right)\left(\exp\frac{n}{N_v}-1\right)\right) \tag{3.17}$$

with $E_{g,QW}$ the bandgap of the quantum well material, N_c and N_v the effective density of states in the conduction and valence band. For small carrier densities, this equation reduces to:

$$V_j \approx 2\frac{kT}{q}\ln\left(\frac{n}{\sqrt{N_c N_v}\exp\frac{-E_{g,QW}}{2kT}}\right) = 2\frac{kT}{q}\ln\left(\frac{n}{n_i}\right)$$

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[5]In fact, it was once believed that the capture efficiency of quantum dots would be very small, implying that quantum dot emitters would never work. But nowadays, nice results with quantum dot based devices have been obtained.

[6]This should not be confused with the diffusion voltage (or the built-in voltage V_{bi}).

This expression will be used to estimate the voltage drop across the quantum well. A simple expression for the static voltage-current characteristic of a diode can be derived. Assume that only a non-radiative recombination mechanism occurs in the active region. Then the carrier density is given by $n = \frac{\tau J}{qd}$, and the voltage characteristic is given by:

$$V_j\left(n\right) = 2\frac{kT}{q}\ln\left(\frac{\tau J}{qdn_i}\right) = 2\frac{kT}{q}\ln\left(\frac{J}{J_{sat}}\right), \ J_{sat} = \frac{qdn_i}{\tau}$$

In case of a dominant bimolecular recombination, as in highly efficient RCLEDs, the steady-state carrier density is given by $n = \sqrt{\frac{J}{Bqd}}$, and the voltage characteristic is given by:

$$V_j\left(n\right) = 2\frac{kT}{q}\ln\left(\frac{1}{n_i}\sqrt{\frac{J}{Bqd}}\right) = \frac{kT}{q}\ln\left(\frac{J}{J_{sat}}\right), \ J_{sat} = Bqdn_i^2$$

In general, both radiative and non-radiative recombinations occur in the active region. The factor before the logarithm is written as mkT/q, m is the ideality factor, with a value between 1 and 2. In this work, the simple Shockley equation will be used to describe the voltage drop across a QW based active region.

The voltage drop across the LED-device is given by the sum of the voltage drop across the junction, and the voltage drop across the series resistance. This is written as:

$$V\left(I\right) = m\frac{kT}{q}\ln\left(\frac{I}{I_{sat}} + 1\right) + R_{series}I$$

m is the ideality factor and I_{sat} is the saturation current (defined as $I_{sat} = AJ_{sat}$, with A the area of the diode). In that case, there is no simple closed-form expression for the current as a function of the drive voltage. However, if the current is much larger than the saturation current of the diode, then it is possible to write the current using the Lambert-W[7] function[55]. This is interesting in particular cases, for example when studying the behaviour of the diode-resistor combination using mathematical tools that know the Lambert equation.

The differential resistance of the RCLEDs includes contributions from both voltage drops. It is possible to estimate the series resistance from a single voltage as a function of the current characteristic:

$$I\frac{dV}{dI} = m\frac{kT}{q}\frac{I}{I + I_{sat}} + R_{series}I \approx m\frac{kT}{q} + R_{series}I$$

From this expression, the series resistance of the device can be extracted. For example, figure 3.9 shows the measurement of the voltage characteristics,

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[7]The Lambert function w(x) is defined as the solution of the transcendent equation $w\exp w = x$
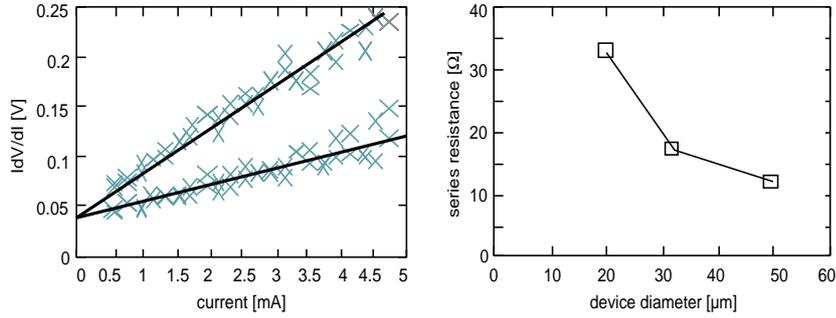
Figure 3.9: Extraction of series resistance from the voltage measurement (left plot, for 980-nm RCLEDs with a diameter of 50 μm (upper trace) and 20 μm (lower trace)), and measured series resistance as a function of the device diameter (right plot, for 980-nm RCLEDs).

done on 980 nm RCLED with different diameters. The series resistance decreases as a function of the device diameter, as expected.

In practice, the series resistance is not always linear. For example, the voltage characteristic of the DBR mirror or the metal-semiconductor contact is not always linear. In such cases, the interpretation of the fitting needs special attention.

3.3.1 The wall-plug efficiency

The wall-plug efficiency is defined as the ratio of the emitted optical power to the injected electrical power. This depends on the efficiency of the RCLED and on the series resistance. It is better to write the wall-plug efficiency as a function of the carrier density:

$$\eta_{wp} = \frac{P_{out}}{P_{in}} = \frac{h\nu\,\eta_{extr}\,Bn^2 Vol}{\left(\frac{mkT}{q} \ln\left(\frac{n}{n_i} + 1 \right) + R_{series}I \right) I} \tag{3.18}$$

The wall-plug efficiency can be written as a function of the drive current, using equation 3.3. The wall-plug efficiency decreases as a function of the drive current. The maximal wall-plug efficiency (at I=0) is given by:

$$\eta_{wp,max} = \frac{\frac{h\nu}{q}\eta_{extr}\left(\frac{B\tau^2}{qVol}\right)}{\frac{kT}{q}\frac{1}{n_i}\frac{\tau}{qVol} + R_{series}} \approx \frac{h\nu}{kT}\eta_{extr}\frac{B\tau n_i}{2}$$

The series resistance is negligible compared to the differential resistance of the diode at zero bias. This expression depends on the photon energy, the extraction efficiency η_{extr} and the ratio of the non-radiative lifetime τ to the radiative lifetime at the intrinsic carrier concentration $1/Bn_i$. This wall-plug efficiency
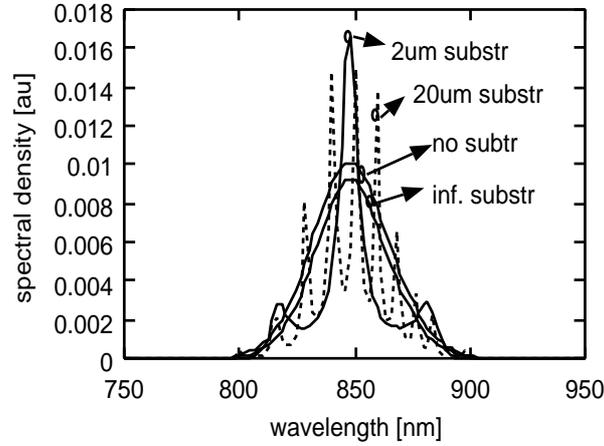
Figure 3.10: Calculated influence of the substrate thickness on the output spectrum. If no substrate is present, then a smooth output spectrum is emitted. In case of a substrate, extra fringes oscillate around the original spectrum. In case of an infinitely thick substrate, the fringes become invisible, and again a smooth spectrum is emitted.

can be large. Unfortunately, the drive current is extremely low, and the corresponding optical output power is negligible.

3.4   Interference effects

Interference effects are very important in devices based on resonance, such as RCLEDs. Interference is the sum of the planar waves. Three conditions must be fulfilled: the waves must be coherent in time (there must be a known relation between the phase of the wave over a 'long' time), the waves must be monochromatic (they must have the same frequency), and the polarisation must be the same.

Consider the interference between a wave packet and the reflection of that packet. Interference requires that the reflected wave packet overlaps with the original packet. This implies that the time-of-flight (ToF) of the reflected wave must be smaller than the coherence time of the packet (t_{coh}). If not, no interference will occur. The maximal distance of the reflecting interface, at which still some interference effects will be visible, is given by:

$$ToF \ll t_{coh} \Rightarrow L \ll \frac{t_{coh}}{2} \frac{c}{n}$$

with c/n the velocity of the light in the material.

In RCLEDs, the interference is caused by the mirrors of the cavity. However, a third reflection can affect the microcavity effect. This third reflection
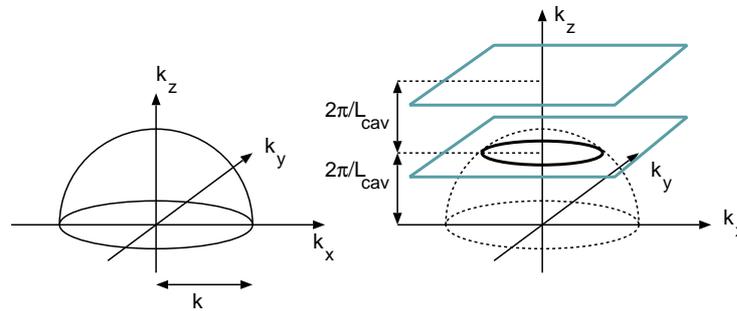
Figure 3.11: K-space presentation of the optical mode density in free-space (left) and in a perfect cavity (right). In case of a perfect cavity, only discrete k_z-vectors are allowed.

(the reflection at the backside of the substrate, for example) introduces a second cavity, resulting in a modulation of the reflection of the RCLED mirror (or 'fringes'). The modulation depth depends on the reflection of the third mirror. The period of these fringes depends on the distance between the reflecting surface and the RCLED mirror. If the period of the fringes is much smaller than the bandwidth of the emitted light, then the influence of the fringes can be neglected. There is thus a minimal distance between the RCLED and the reflecting surface, at which the influence of the third reflection can be neglected:

$$\Delta\lambda_{fringe} \ll BW_{em} \Rightarrow L \gg \frac{\lambda^2}{2n\,BW_{em}}$$

with BW_{em} the bandwidth of the emitted light. If the distance to the third mirror is even smaller, then the shape of the spectrum and the output power are heavily influenced by this distance. This is important if a small substrate is used, which causes an extra reflection close to the RCLED. Figure 3.10 shows the calculated influence of the reflections at the backside of the substrate on the output spectrum of the RCLED.

3.5 The microcavity effect

3.5.1 The k-space picture

The k-space picture was introduced in section 3.2.1, when the optical mode density in free-space was discussed. The mode density changes inside microcavities, and results in an increased or decreased spontaneous emission lifetime. This is easily visualised in k-space, as will be presented in this section.

The presence of the cavity results in different boundary conditions for the electromagnetic modes, and the allowed modes are not given by equation 3.7, but they depend strongly on these boundary conditions. Assume a perfect cav-
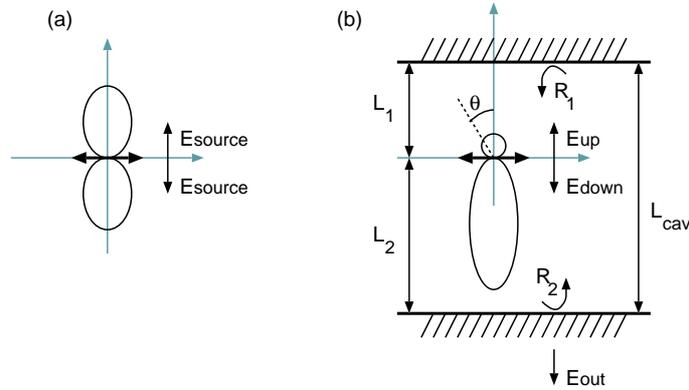
Figure 3.12: Principle of microcavity: (a) dipole emission in free space, (b) dipole emission in a cavity.

ity, consisting of 2 perfectly reflecting (and lossless) mirrors, at a distance L_{cav}. This boundary condition allows only a discrete k_z values inside the cavity:

$$k_z = n_z \frac{2\pi}{L_{cav}}$$

Other k_z values are not allowed, whilst the k_x and k_y are still uniformly distributed in the k-space. This implies that the allowed k-vectors are not uniformly distributed over the k-space, all allowed modes are concentrated in planes (see figure 3.11). The optical mode density (defined as the number of modes with k-value between k and k+dk), depends strongly on the wave number of the mode (and thus on the emission energy). If the emission wave number is increased from slightly smaller to slightly larger than the resonance wave number in perpendicular direction, then the optical mode density changes abruptly. Using this theory (the 'mode counting' theory), an expression for the optical mode density in perfect cavities is derived in reference [56].

If the cavity is sufficiently thick, then a number of resonance planes cut the intrinsic emission sphere. This results in extra modes, representing spontaneous emission in lateral propagation directions (the "guided modes"). This should be avoided, because it reduces the spontaneous emission in the vertical mode.

In practice, no ideal cavities exist, and if they did, they would be completely useless. There is no light extracted from ideal cavities, because of the perfectly reflecting mirrors (R=1). However, there is still a comparable effect in realistic microcavity devices. This will be described in the next section.

3.5.2   Description of the microcavity effect in RCLEDs

The cavity consists of a spacer, in between a highly reflecting back mirror with reflection R_1 and a moderately reflecting outcoupling mirror with reflection

R_2 (see figure 3.12). The spacer material contains the active layer, in which the electrons are converted into photons, and the carrier confinement layer. The spacer has typically a large bandgap to allow a good carrier confinement, and thus a low refractive index. As discussed in the previous paragraph, the microcavity around the active layer changes the internal emission profile: the spontaneous emission in the resonant mode is enhanced. This is expressed by an enhancement factor. This factor is related to the electrical field amplitude inside the cavity (built up from the successive reflections at the back mirror and outcoupling mirror). The output field of the microcavity, as a function of the source field in the active region[8] is given by:

$$\frac{E_{out}}{E_{source}} = t_2 \exp\left(-jk_z n L_2\right) \frac{1 + r_1 \exp\left(-jk_z n L_1\right)}{1 - r_1 r_2 \exp\left(-jk_z n L_{cav}\right)} \tag{3.19}$$

with r_1 the amplitude reflection coefficient of the rear mirror, r_2 the amplitude reflection coefficient of the outcoupling mirror, t_2 the transmission coefficient of the outcoupling mirror, $k_z = k_0 \cos\theta$ is the azimuthal projection of the k-vector ($k_0 = 2\pi/\lambda$), n the refractive index of the cavity spacer material, L_1 the distance from the rear mirror to the active layer, L_2 the distance from the active region to the outcoupling mirror, and $L_{cav} = L_1 + L_2$ the total thickness of the cavity. In general, all the reflection and transmission coefficients depend on the wavelength and the propagation angle. This relation shows how the external (emitted) field depends on the cavity parameters, and can be used to calculate the beam profile.

The ratio of generated optical power in the cavity to the generated power as if there was no cavity is inversely proportional to the change in spontaneous emission lifetime[5]. The larger the generated power inside the cavity, the faster the recombination rate. This is, next to the change of the internal emission profile, the second important effect of the microcavity on the spontaneous emission characteristics. The total emitted power by the active region is found by integrating the emitted power over all propagation directions and wavelengths. In general, the evanescent waves emitted by the radiating dipole should also be taken into account. These waves can transport energy if a metal or high-index material is placed close to the active layer. In this way, these evanescent waves change the total emitted power of the dipole, and thereby the emission lifetime. This evanescent coupling is neglected in this work, because the active layer in the devices is sufficiently far away from high-index materials or metal layers.

Therefore, the total emitted optical power can be written as:

$$P_{tot} = \int_0^{\frac{\pi}{2}} |E_{up}|^2 \, 2\pi \sin\theta d\theta + \int_{\frac{\pi}{2}}^{\pi} |E_{down}|^2 \, 2\pi \sin\theta d\theta$$

whilst the emitted power in the free space case is given by:

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[8]This expression assumes symmetric sources. This is not valid in case of vertically oriented dipoles. However, it is valid for parallel dipoles, which are dominant in quantum well based active layers.
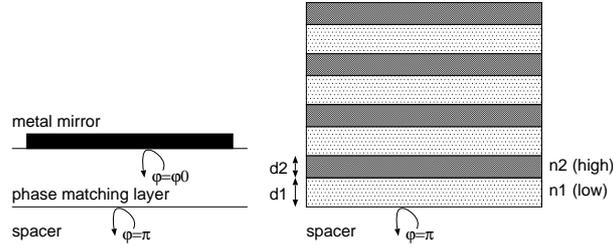
Figure 3.13: Reflection at (a) a metal mirror, (b) a Distributed Bragg Reflector (DBR).

$$P_{free} = \int_0^\pi |E_{source}|^2 \, 2\pi \sin\theta d\theta$$

Several numerical simulation tools for calculating the change of the spontaneous emission characteristics have been developed [57]. In these tools, the intrinsic dipole emission profile is written as a sum of planar waves. The reflection of the planar waves at the multilayer mirrors is calculated, mostly using a matrix formalism, from which the enhancement is calculated (as defined in equation 3.23). Finally, the overall enhancement is found by integrating the enhancement over all planar wave components.

Depending on the layer structure, one or several guided modes exist inside the cavity. To calculate the total emitted power, the power into these modes should be taken into account. However, the angular discretisation algorithm of the dipole emission field should be sufficiently clever, so that all these guided modes are found. This is not obvious, especially if the Q-factor of the guided mode is large (corresponding to a narrow resonances). The simulation program sometimes had problems with this: in some cases, not all guided modes were recognised, resulting in a coarse integration of the internal field profile, and unreliable results.

In this work, such a numerical tool was used to design the microcavities for different applications. However, these tools need a large calculation time, and are not suitable to study the influence of the cavity parameters on the performance of the RCLEDs. Therefore, a new and simple analytical expression for the extraction efficiency of RCLEDs is derived. But firstly, the characteristics of the mirrors of the RCLEDs will be discussed.

3.5.3   Properties of mirrors

Firstly, the properties of mirrors will be discussed. Two different types of mirrors are used to build the cavity: the metallic mirror and the Distributed Bragg Reflector (DBR). A metallic mirror is assumed to have a constant reflection,
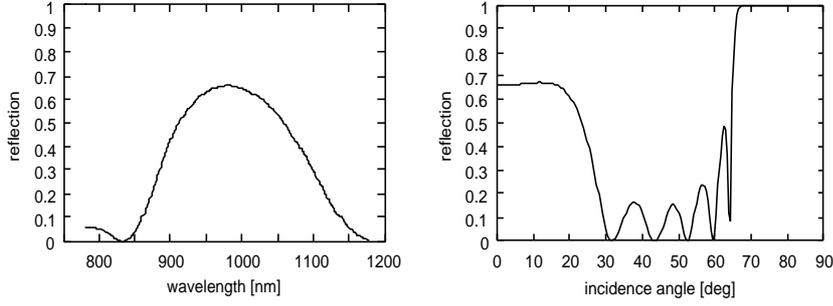
Figure 3.14: Calculated reflection characteristics of a 6-pair AlAs/GaAs DBR.

with a certain phase of reflection. Therefore, a phase-matching layer is included, so that the reflection equals π. A DBR consists of a periodic stack of alternating high and low refractive index materials. The reflection of the DBR is a complex function of the incidence angle and the wavelength. The mirror can be highly reflective, but only over a limited wavelength and incidence angle range. Figure 3.14 shows the calculated reflection characteristics of a DBR mirror. The reflection is maximal at the central wavelength $\lambda_{DBR} = 4n_1 L_1 = 4n_2 L_2$, and the reflection increases as a function of the number of DBR pairs. For wavelengths close to the central wavelength, the reflection is more or less constant, and the phase of the reflection is a linear function of the wavelength.

The reflection characteristic of the DBR can be approximated by an idealised mirror with constant reflection, equal to peak reflection of the DBR, placed at a distance L_{pen}, the penetration depth of the mirror. This distance simulates the linear phase of the reflection of the DBR. The reflection of the DBR in perpendicular direction can be written as (assuming $\Delta k = k - k_{DBR}$):

$$r_{DBR}(k) \approx r_{max} \exp\left(-j\varphi(k)\right)$$
$$\varphi(k) = 2\left(k - k_{DBR}\right)nL_{pen}^k = 2\Delta k n L_{pen}^k$$

with k the wave number in free space. L_{pen}^k is negative, the phase of the reflection decreases as a function of the wave number. r_{DBR} is the amplitude reflection coefficient of the DBR, the power reflection coefficient is given by $|r_{DBR}|^2$. The phase can also be written as a function of the wavelength (assuming $\Delta\lambda = \lambda - \lambda_{DBR}$):

$$\varphi(\lambda) = -\frac{4\pi n}{\lambda^2}\left(\lambda - \lambda_{DBR}\right)L_{pen}^k = -\frac{4\pi n}{\lambda^2}\Delta\lambda L_{pen}^k$$

A similar expression can be derived to express the reflection as a function of the incidence angle:

$$r_{DBR}(\theta) \approx r_{max}\exp\left(-j\varphi(\theta)\right)$$
$$\varphi(\theta) = 2k\cos\theta n L_{pen}^\theta \approx 2k\left(1 - \tfrac{1}{2}\theta^2\right)nL_{pen}^\theta$$

L_{pen}^k and L_{pen}^θ are two different definitions for the penetration depths, which are not equal for a given DBR. Moreover, the name penetration depth is somewhat misleading: it is not related to the decrease of energy as a function of the propagation into the mirror structure [58]. All penetration depths increase when the contrast of the DBR is reduced, because the reflections at the successive layers decrease. If the DBR was a perfectly reflecting mirror, then the penetration depths would be zero.

This is the hard mirror approximation for DBRs, which is only valid over a limited wavelength range around the peak reflection wavelength, and over a limited incidence angle range (only incidence angle round the perpendicular direction). These approximations are useful when studying the influence of DBRs onto the extraction of RCLEDs.

3.5.4   The analytical approach

In this paragraph, a simple closed-form expression for the extraction efficiency of RCLEDs is presented[9].

The starting point for this analysis is the resonance condition, describing that the phase of a round trip in the cavity must equal an integer times 2π:

$$-2k\cos\theta\, nL + \varphi\left(k,\theta\right) = N2\pi \ \left(\varphi = \varphi_1 + \varphi_2\right)$$

with k the wave number, θ the propagation angle, n the refractive index of the spacer material, L the cavity length (distance between the two mirrors), φ_1 and φ_2 the phase of the reflection of the two mirrors (at the given wave number and incidence angle) and N an integer number, describing the order of the resonance. The enhancement (as defined in equation 3.23) reaches a local maximum if this resonance condition is fulfilled. It is assumed that the cavity is resonant in perpendicular direction at $k = k_{cav}$, and the sum of the phase of the reflections equals 2π at the resonance wave number and in perpendicular direction. This determines the cavity length L:

$$-2k_{cav}nL + 2\pi = N2\pi \ \Rightarrow \ L = N\frac{\pi}{nk_{cav}} = N\frac{\lambda_{cav}}{2n} \tag{3.20}$$

With N the order of the resonance. The cavity length must equal an integer times the half wavelength. Furthermore, it is assumed that the cavity resonance wavelength equals the peak reflection wavelength of the DBR. Assume now a small deviation from the propagation direction and the cavity thickness. This will result in a change of the resonance wave number Δk:

$$-2\left(k_{cav} + \Delta k\right)\left(1 - \frac{\theta^2}{2}\right)n\left(L + \Delta L\right) + \varphi\left(k,\theta\right) + \frac{d\varphi}{dk}\Delta k + \frac{d^2\varphi}{d\theta^2}\frac{\theta^2}{2} = N2\pi$$

The change of the resonance wave number can be calculated as a function of these deviations:

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[9]An alternative expression for the extraction efficiency of RCLEDs was derived in parallel with this work [59].

$$\frac{\Delta k}{k_{cav}} = \frac{-\Delta L}{L - \frac{1}{2n}\frac{d\varphi}{dk}} + \frac{L + \frac{1}{nk_{cav}}\frac{d^2\varphi}{d\theta^2}}{L - \frac{1}{2n}\frac{d\varphi}{dk}}\frac{\theta^2}{2} = \frac{-\Delta L}{L - L_{pen}^k} + \frac{L + L_{pen}^\theta}{L - L_{pen}^k}\frac{\theta^2}{2} \qquad (3.21)$$

This equation shows how the cavity resonance wave number (this is the wave number at which the cavity enhancement will reach a local maximum) changes as a function of the cavity thickness and the propagation angle. This equation is simplified using the definitions of the penetration depth of the mirrors (see section 3.5.3). In fact, L_{pen}^k represents the sum of the penetration depths of the top mirror and the bottom mirror. The cavity thickness can be replaced by an effective cavity length $L_{eff} = L - L_{pen}^k$, which is larger than the physical cavity thickness because L_{pen}^k is negative. The corresponding change of the resonance wavelength is given by:

$$\frac{\Delta\lambda_{cav}}{\lambda_{cav}} = \frac{\Delta L}{L - L_{pen}^k} - \frac{L + L_{pen}^\theta}{L - L_{pen}^k}\frac{\theta^2}{2} \qquad (3.22)$$

If the mirrors were perfectly reflecting, then the penetration depth equals zero, and the resonance wave number would increase as a function of the propagation angle like $1 + \theta^2/2$. If this was presented in k-space, then all resonance vectors would lie on a plane (as presented in figure 3.11). However, DBRs are not perfect mirrors, and the resonance plane curves slightly. This bending determines how the resonance wavelength changes as a function of the propagation angle. This has an important influence on the far-field pattern and the efficiency. The bending is changed if the cavity length is small compared to the penetration depth L_{pen}^k. This effect is used in the RC^{2}LED [60], where a small cavity (N=1) and an advanced, non-periodic reflector (based on AlO$_x$) is used to enhance the coupling to a small numerical aperture. However, this effect is negligible if AlAs/GaAs DBRs are used (as in this work), due to the smaller index contrast in the DBR.

The microcavity effect results in an increase (or decrease) of the optical power in a certain direction. This is expressed by an enhancement (see equation 3.23):

$$enh\,(\lambda, \theta) = \left|\frac{E_{out}}{E_{source}}\right|^2 \qquad (3.23)$$

Assuming the cavity is resonant at k_{cav} (by choosing the cavity length), then the maximal enhancement is given by:

$$enh_{max} = \frac{\xi}{2}\frac{\left(1 + \sqrt{R_1}\right)^2\left(1 - R_2\right)}{\left(1 - \sqrt{R_1 R_2}\right)^2} \qquad (3.24)$$

The factor ξ describes the spatial overlap of the optical field and the active layer: it equals 2 for quantum wells positioned in the antinode, 0 for quantum wells positioned in the node, and 1 for large active layers (large compared to

the period of the standing wave in the cavity). $R_1 = |r_1|^2$ is the power reflection of the rear mirror, $R_2 = |r_2|^2$ is the power reflection of the outcoupling mirror. This equation is also derived in [5]. The enhancement is an increasing function of R_1. Therefore, the reflection of the back mirror is chosen as high as possible, typically a highly reflecting metal mirror, or a DBR consisting of many pairs is used.

The cavity enhancement has a certain spectral width (the cavity bandwidth), given by:

$$\Delta\lambda_{cav} = \frac{\lambda^2}{2\left(L - L_{pen}^k\right)} \arccos\left(-\frac{1 - 4\sqrt{R_1 R_2} + R_1 R_2}{2\sqrt{R_1 R_2}}\right) \qquad (3.25)$$

Here, λ is the cavity resonance wavelength, L the cavity length en L_{pen}^k the penetration depth. The cavity bandwidth is a decreasing function of the reflection of the output mirror (remember that the rear mirror reflection is chosen as high as possible). A large reflection corresponds to a small cavity bandwidth and a large enhancement, defined as a high-Q cavity.

The overall enhancement into a certain propagation direction is given by the overlap of the cavity enhancement spectrum and the intrinsic emission spectrum. This overlap is simply the product of the cavity enhancement spectrum $enh(\lambda, \theta)$ and the intrinsic spontaneous emission spectrum $SE(\lambda)$. In this way, the enhancement is averaged over all emission wavelengths. The enhancement in a certain direction is thus given by:

$$enh(\theta) = \int enh(\lambda, \theta)\, SE(\lambda)\, d\lambda$$

The integrand can be written as a Gaussian function, see appendix A. The angle-dependent enhancement can be found by integrating the emission spectrum. It is given by:

$$enh(\theta) = \frac{enh_{max}}{\sqrt{1 + \frac{\Delta\lambda_{SE}^2}{\Delta\lambda_{cav}^2}}} \exp\frac{-\left(\lambda_{SE} - \lambda_{cav}(\theta)\right)^2}{\Delta\lambda_{SE}^2 + \Delta\lambda_{cav}^2} \qquad (3.26)$$

This enhancement determines how the amplitude of the emitted field varies as a function of the propagation angle. This is the far-field pattern. The overall enhancement enh_{tot} is found by averaging the enhancement $enh(\theta)$ over all propagation angles. This integration results in:

$$enh_{tot} = \frac{\int_{\Omega_{em}} enh(\theta)\, d\Omega}{\int_{\Omega_{em}} d\Omega} = \frac{\int_0^{\theta_{em}} enh(\theta)\, 2\pi \sin(\theta)\, d\theta}{2\pi\left(1 - \cos\theta_{em}\right)} \approx enh\left(\frac{\theta_{em}}{2}\right) \quad (3.27)$$

The approximation is a single-step trapezoidal solution of the integration. This is only valid for small emission angles. This simple expression gives an approximation for the enhancement of the spontaneous emission into a (small) solid angle, as a function of the cavity parameters. The expression is only
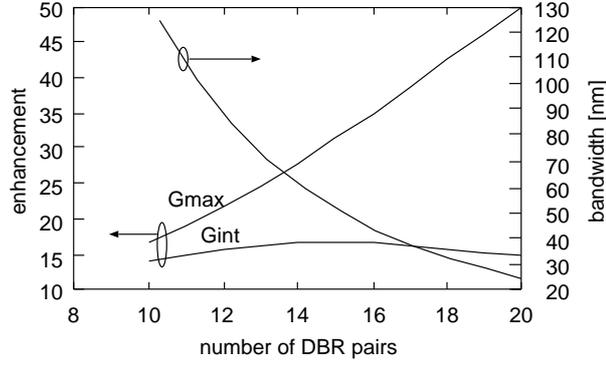
Figure 3.15: Calculated enhancement and cavity bandwidth as a function of the number of DBR pairs of the outcoupling mirror.

valid for emission around the cavity resonance wavelength and around the perpendicular direction. This description is not accurate for the enhancement of the emission at very skew angles (like the emission into the laterally guided modes). Consequently, these equations can not be used to calculate the total spontaneous emission rate, as this needs the integration of the emission over all propagation angles.

The extraction efficiency is a better figure to characterise the optical power of RCLEDs. Therefore, the extraction efficiency must be expressed as a function of the enhancement. The extraction efficiency is given by the ratio of optical power emitted within a certain numerical aperture, to the total emitted power. This can be written as:

$$\eta_{extr} = \frac{\int_0^{\theta_0} p_{cav}\left(\theta\right) d\Omega}{\int_0^{\pi} p_{cav}\left(\theta\right) d\Omega} \frac{\int_0^{\pi} p_{free}\left(\theta\right) d\Omega}{\int_0^{\pi} p_{free}\left(\theta\right) d\Omega} = \frac{\tau_{cav}}{\tau_{free}} \frac{\int_0^{\theta_0} p_{cav}\left(\theta\right) 2\pi \sin\theta d\theta}{\int_0^{\pi} p_{free}\left(\theta\right) 2\pi \sin\theta d\theta}$$

This expression uses the fact that the change in emitted power is inversely proportional to the change in emission lifetime. The denominator is easily computed in case of isotropic light emission ($p_{free}\left(\theta\right) = p_0$) and in case of a dipole light emission ($p_{free}\left(\theta\right) = p_0 \cos\theta$):

$$\int_0^{\pi} p_{free}\left(\theta\right) 2\pi \sin\theta d\theta = \begin{cases} 4\pi p_0 & (isotropic) \\ 2\pi p_0 & (dipole) \end{cases}$$

In case of extraction into a small NA (or in case of high-index materials), the nominator can be approximated as:

$$\int_0^{\theta_0} p_{cav}\left(\theta\right) 2\pi \sin\theta d\theta = 2\pi \int_0^{\theta_0} p_{free}\left(\theta\right) enh\left(\theta\right) \sin\theta d\theta \approx \pi p_0 \theta_0^2 enh\left(\frac{\theta_0}{2}\right)$$

This expression holds for both isotropic and dipole emitters, because both sources emit (approximately) the same field in perpendicular direction. Fi-
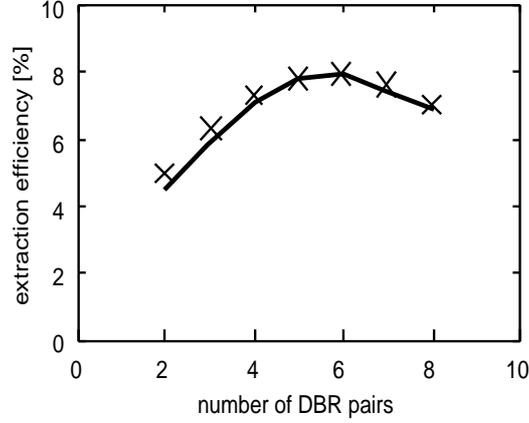
Figure 3.16: The extraction efficiency of an RCLED as a function of the number of DBR pairs in the outcoupling mirror, calculated using the simple model (crosses) and the numerical tool (full line).

nally, the extraction efficiency can be derived. In case of an isotropic intrinsic light emission, this is written as:

$$\eta_{extr} \approx \frac{\tau_{cav}}{\tau_{free}} \frac{\pi p_0 \theta_0^2 enh\left(\frac{\theta_0}{2}\right)}{4\pi p_0} \approx \frac{\tau_{cav}}{\tau_{free}} \frac{\theta_0^2}{4} enh\left(\frac{\theta_0}{2}\right) \tag{3.28}$$

, whilst in case of a dipole distribution of the intrinsic light emission, the extraction efficiency is given by:

$$\eta_{extr} \approx \frac{\tau_{cav}}{\tau_{free}} \frac{\pi p_0 \theta_0^2 enh\left(\frac{\theta_0}{2}\right)}{2\pi p_0} \approx \frac{\tau_{cav}}{\tau_{free}} \frac{\theta_0^2}{2} enh\left(\frac{\theta_0}{2}\right) \tag{3.29}$$

This is, in both cases, a factor $enh\left(\frac{\theta_0}{2}\right)$ larger compared to the extraction efficiency from a planar LED (without a microcavity). The change of the emission lifetime inside a cavity is rather small for one-dimensional microcavities, due to the limited reflection range of the DBR ($\tau_{cav} \approx \tau_{free}$). This will be discussed in detail in section 6.4.1. This allows to write the extraction efficiency as:

$$\eta_{extr} \approx \eta_{extr}^{planar} enh\left(\frac{\theta_0}{2}\right)$$

This expression is independent on the shape of the intrinsic light emission.

3.5.5 Comparison of the model with numerical calculations

The results obtained with the model were compared with the calculted extraction efficiency of planar RCLEDs, using the software tool develloped by De Neve [57]. A good agreement was found if the recycling of photons in the

layerstructure was not taken into account[10]. Figure 3.16 shows the calculated extraction efficiency as function of the number of DBR pairs in the outcoupling mirror, using the simple model and the software tool. Both results led to the same optimal number of DBR pairs. However, there was a small difference for the optimal cavity thickness using the two techniques (not shown on the figure). The optimisation using the simple model always resulted in a smaller optimal cavity thickness. This is explained by the absence of the modelling of the overall spontaneous emission lifetime in the simple model. It was found that a large cavity thickness results in smaller lifetimes (and thus larger efficiencies). However, this effect is small. The difference between the optimal cavity thickness of the two models was maximally 2.6 nm.

3.6 Influence of the photon recycling effect

Light emitted by the active region can be reabsorbed by the active region. This effect occurs in devices with a thick active region (as double heterostructure based LEDs). The generated carriers can then recombine again, releasing a new photon. Quantum-well based devices have in general no influence of this reabsorption effect, due to the extremely thin active region, decreasing the chance that emitted light is reabsorbed. However, the situation is different in microcavities. Depending on the cavity structure, a part of the generated light is emitted into laterally guided modes. These modes will be reabsorbed after a certain propagation distance. This effect has been observed in experiments [57], and is beneficial: it results in an important increase of the overall device efficiency.

In this section, the recycling effect will be investigated theoretically. This is done by deriving balance equations for the electron and photon densities, as an extension to equation 3.2. All generated photons are divided into 3 categories: the extracted photons f_{extr}, the laterally guided photons f_{guid} and the leaky photons f_{leak}. The leaky photons are not guided by the cavity and are not extracted into air, they will be absorbed somewhere in the device. The corresponding efficiencies are η_{extr}, η_{leak} and η_{guid}, with $\eta_{extr} + \eta_{leak} + \eta_{guid} = 1$.

Two balance equations determine the number of carriers in the active region and the number of photons in the guided modes. The number of carriers is determined by the difference between the generated carriers per unit of time (the injected current and the reabsorbed guided modes) and the number of disappearing carriers per unit of time (through various recombination mechanisms). The number of generated guided photons per unit of time equals the number of disappearing guided photons (described by an absorption time τ_{abs}). The balance equations can be written as:

$$\frac{I_{inj}}{qVol} + \gamma \frac{f_{guid}}{\tau_{abs}} = \frac{n}{\tau} + B n^2$$

---

[10]This recycling has a strong influence on the overall efficiency of the RCLEDs, as will be discussed in the next paragraph.

$$\eta_{guid} B n^2 = \frac{f_{guid}}{\tau_{abs}}$$

I_{inj} is the injected current, Vol is the volume of active layer, B is the bimolecular recombination coefficient, τ is the non-radiative lifetime (which is assumed to be independent on the current density), γ is the part of guided modes that will be absorbed in the active region (some of the guided modes will be absorbed elsewhere, or will escape the microcavity before it is absorbed), and τ_{abs} is the lifetime of guided photon. This factor depends on the absorption coefficient of the active region (which depends on the carrier density). The factor γ is small for small RCLEDs, as almost all guided modes escape the cavity laterally before they are reabsorbed. This factor γ is close to one in case of a wide RCLED.

The number of photons in the guided modes are given by:

$$f_{guid} = \tau_{abs} \eta_{guid} B n^2$$

and the carrier density is determined by the following equation:

$$\frac{I_{inj}}{qVol} = \frac{n}{\tau} + B \left(1 - \gamma \eta_{guid}\right) n^2$$

Therefore, the bimolecular recombination coefficient should be replaced by an effective coefficient $B_{eff} = B\left(1 - \gamma \eta_{guid}\right)$[11]. The outgoing optical power is given by:

$$P_{out} = \frac{h\nu}{q} \eta_{extr} \frac{1}{1 - \gamma \eta_{guid}} I_{inj} \left(\frac{\sqrt{\frac{4 B_{eff} I_{inj} \tau^2}{qVol}}}{\sqrt{1 + \frac{4 B_{eff} I_{inj} \tau^2}{qVol}} + 1} \right)^2$$

An 'apparent extraction efficiency' η_{extr}^{app} can be defined:

$$\eta_{extr}^{app} = \eta_{extr} \frac{1}{1 - \gamma \eta_{guid}}$$

To estimate the maximal increase of the efficiency due to the recycling effect, assume that no leaky modes are emitted ($\eta_{leak} = 0$), and all reabsorbed light is re-emitted (γ=1). The apparent extraction efficiency is then given by:

$$\eta_{extr}^{app} = \frac{\eta_{extr}}{1 - 1\left(1 - \eta_{extr}\right)} = 1$$

This indicates that all generated photons will be extracted. However, the internal efficiency decreases slightly, because the number of carriers in the active region decreases. This corresponds to a slower radiative recombination. Figure 3.17 shows the calculated extraction efficiency as a function of the reabsorption ($\gamma \eta_{guid}$). The apparent extraction efficiency increases as a function of the reabsorption, but the internal efficiency decreases slightly.

[11]this is only valid to calculate the static properties of the RCLED, this is not valid to use this to calculate the speed properties of the device.
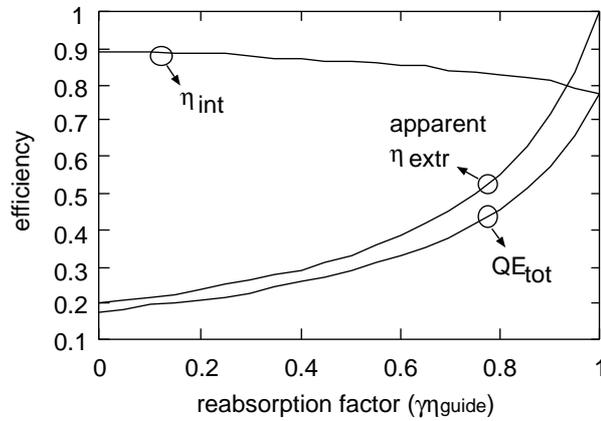
Figure 3.17: Influence of the photon recycling on the overall quantum efficiency (QE_{tot}, as was defined in equation 3.1), assuming no leaky modes are emitted.

In general, only a part of the guided modes will be reabsorbed. The most important loss factor is the part of the mode that escape the RCLED laterally before it is reabsorbed. This depends on the absorption length, which depends on the absorption coefficient of the active region and the overlap between the profile of the guided mode and the active region. A typical value for the absorption length is 100 μm, which is typically larger than the dimensions of the RCLEDs studied in this work. Furthermore, the absorption coefficient of the active region depends on the carrier density. If the active region is pumped above transparency, no reabsorption occurs at all. In conclusion, this recycling effect is important if a large RCLED (several hundreds micrometer diameter), pumped at a small current density, is used.

3.7 Design of RCLEDs

The most important part of the design of a RCLED is the definition of the layer structure. This determines the properties of the optical cavity, and thus the extraction efficiency of the RCLED. The important design parameters are the reflectivity of the mirrors, and their separation. An approximate expression for the extraction efficiency was derived in section 3.5.4, and will be used in this section to explain the design rules.

During the design of the layer structure, the cavity parameters are chosen so that the extraction efficiency is maximised for the desired propagation angles or emission wavelengths. This depends, of course, on the design goal. In this paragraph, general rules for the design of RCLEDs for different applications are given.

3.7.1   General design rules

Some first rules on the design of microcavities can be derived from the k-space picture (see figure 3.11). The amount of power emitted in the desired mode depends on the number of resonant modes in the cavity. Firstly, the number of modes in the z-direction should therefore be minimised, to maximise the emission in the desired mode. This implies that the cavity thickness should be as small as possible. Furthermore, the emitted modes are given by the overlap of the intrinsic spontaneous emission sphere with the resonance plane. The preferential emission directions are easily found using the k-space picture. The emission in vertical direction should be enhanced, because these modes propagate within the escape cone of the semiconductor, and will therefore be extracted. This implies that the resonance plane should touch the top of the sphere in k-space (the cavity resonance wavelength should equal the intrinsic emission wavelength).

The active layer should be placed at the antinode position of the internal standing wave pattern. The smallest cavity corresponds to a first order cavity (N=1 in equation 3.20). The phase of the reflection of the mirrors should be equal to π, otherwise the active layer (placed in the middle of the cavity) would sit at a node position, which results in an inhibition of the spontaneous emission. This implies that the DBR mirror should start with a high refractive index layer (high compared to the low refractive index of the spacer material).

3.7.2   Design for maximal efficiency

The design of RCLEDs for maximal efficiency has been discussed in detail in previous works [57]. This is repeated in this work, but this time based on the analytical expression for the extraction efficiency, derived in paragraph 3.5.4. From equation 3.27, it is found that a large extraction efficiency requires a large maximal enhancement enh_{max}, a large cavity bandwidth $\Delta\lambda_{cav}$, and a good cavity tuning. However, the first two requirements are conflicting: a large maximal enhancement requires a large reflection of the outcoupling mirror, resulting in a small cavity bandwidth. Therefore, there is an optimal reflection (about 50 % to 60 % in case of 980 nm RCLEDs). It is found that the optimum reflection of the outcoupling mirror corresponds to a cavity bandwidth approximately equal to the bandwidth of the intrinsic spontaneous emission spectrum. Therefore, a small bandwidth of the intrinsic spectra is desired, allowing a large mirror reflection and thus a large maximal enhancement.

A second factor determining the extraction efficiency is the detuning, this is the difference between the peak wavelength of the intrinsic emission and the cavity resonance wavelength in perpendicular direction. This parameter is related to the cavity thickness, and the analytical model allows to estimate the optimal detuning for a maximal enhancement. It was found that the extraction efficiency into a desired NA is maximised if the enhancement at propagation direction $\theta = \frac{1}{2}\theta_{NA}$ is maximised (see equation 3.27). This condition defines the optimal detuning. This implies that, to maximise the emission into a given
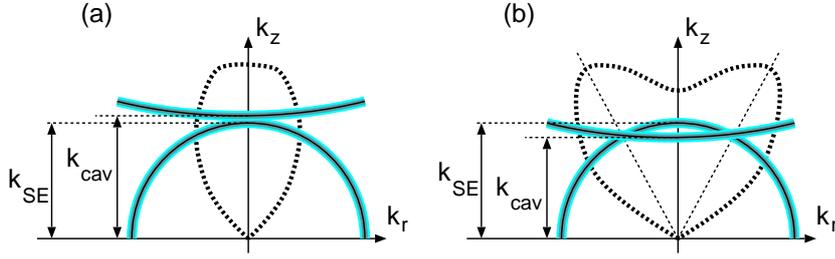
Figure 3.18: Influence of detuning on the emitted far-field pattern, for an undertuned cavity (left) and an overtuned cavity (right).

NA, the cavity resonance wavelength must not match the intrinsic emission wavelength. The optimal detuning is given by:

$$\lambda_{cav}\left(\theta = \frac{\theta_{NA}}{2}\right) = \lambda_{SE}$$

with λ_{cav} the cavity resonance wavelength in the given propagation direction, and λ_{SE} the intrinsic spontaneous emission wavelength. The cavity thickness can be found from equation 3.22:

$$L = L_0 + \Delta L = L_0 + \left(L_0 - L^k_{pen}\right)\left(\frac{\lambda_{SE}}{\lambda_{cav}\left(\theta = 0\right)} - 1 + \frac{L_0 + L^\theta_{pen}}{L_0 - L^k_{pen}}\frac{1}{8}\theta^2_{NA}\right)$$

$\lambda_{cav}\left(\theta = 0\right)$ is the cavity resonance wavelength in perpendicular direction, which equals the DBR peak reflection wavelength. L_0 is the corresponding nominal cavity thickness (see equation 3.20). A maximised enhancement in the perpendicular direction (NA=0) requires a perfectly tuned cavity. In that case, the cavity resonance wavelength matches the intrinsic spontaneous emission spectrum. A maximised enhancement over a broader solid angle requires a positively detuned cavity. The cavity thickness should be larger. This corresponds to a larger cavity resonance wavelength at perpendicular direction, compared to the intrinsic spontaneous emission wavelength. The enhancement in perpendicular direction is thus smaller, and the corresponding far-field pattern has a double lobed profile (see figure 3.18). This profile has been given different names in literature: a butterfly profile, or rabbits ears. This emission profile might be adverse for applications needing a small emission bundle, as RCLEDs optimised for coupling to a fibre.

Figure 3.19 shows the calculated extraction efficiency as a function of the thickness of the phase-matching layer and the number of DBR pairs, and the calculated far-field pattern as a function of the spacer thickness. For this calculation, the numerical tool was used. The corresponding cavity structure is shown in figure 1.1. The design of the layer structure of different RCLEDs will be discussed in the next chapter.
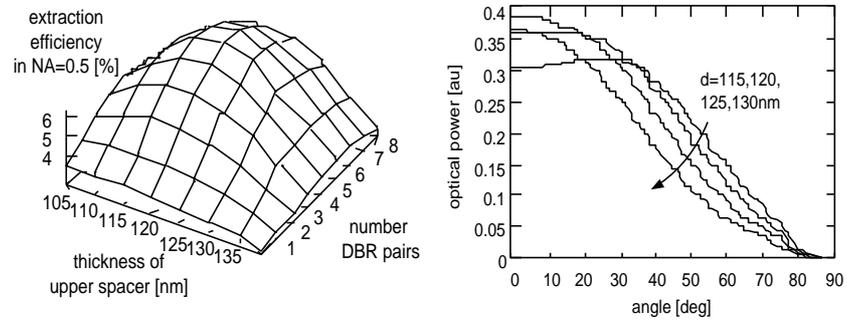
Figure 3.19: Calculated extraction efficiency into NA=0.5 of an AlGaAs-based RCLED (left) and far-field pattern as a function of the cavity thickness (right).
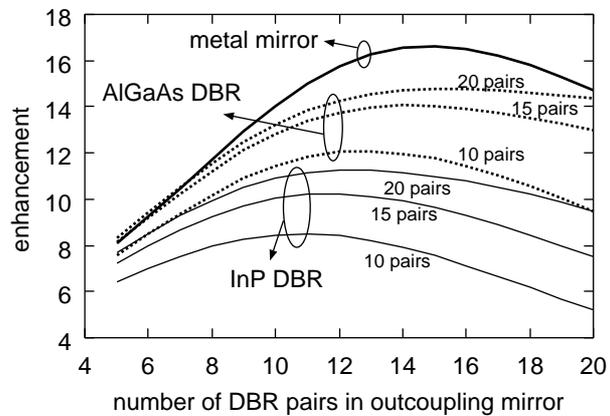
Figure 3.20: Calculated enhancement as a function of the number of DBR pairs in the outcoupling mirror, for a long-wavelength RLCED with several back mirror options.
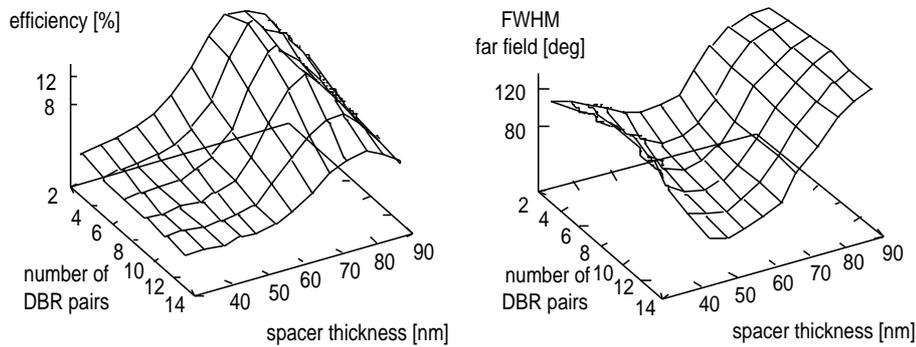
Figure 3.21: Optimisation of the RCLED parameters for a small beam divergence: calculated overall extraction efficiency (left), and calculated FWHM angle (right).

3.7.3 Choice of mirror type

The mirror properties have an important influence on the performance of the device. For example, consider the design of a long-wavelength RCLED. The cavity is designed to emit light at 1550 nm, using an InGaAsP quantum well based active region. Several top-mirrors can be integrated in the device: a lattice-matched InGaAsP/InP DBR, an AlGaAs/GaAs DBR[12] or a metal mirror. The first type of DBR has a small refractive index contrast ($n_1 = 3.43$, $n_2 = 3.17$), implying a large number of DBR pairs to get a high reflection, and a large penetration depth. The contrast of the AlGaAs/GaAs DBR is larger ($n_1 = 3.37$, $n_2 = 2.95$). Figure 3.20 summarises the maximal enhancement as a function of the number of DBR pairs in the outcoupling mirror, for different types of DBRs.

The calculation shows that a metal back mirror leads to the highest enhancement. The cavity with a low-contrast DBR has the smallest enhancement: the large penetration depth leads to a larger effective cavity thickness and a decreasing cavity bandwidth. The cavity bandwidth must equal the intrinsic bandwidth, and therefore, the reflection of the outcoupling mirror should be smaller, to compensate for the small cavity bandwidth. This explains why the low-contrast DBR has a smaller optimum number of DBR pairs. This leads to a smaller overall enhancement.

3.7.4 Design for small beam divergency

In this section, the design of cavities emitting very narrow far-field patterns is examined. Figure 3.21 shows the calculated overall extraction efficiency and the FWHM angle of the far-field pattern as a function of the cavity parameters. Divergence angles of 40° can be obtained, the corresponding overall extraction

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[12]This DBR could be bonded to the InP-based device, or the DBR could be grown directly onto the InP-based devices (a metamorphic growth).
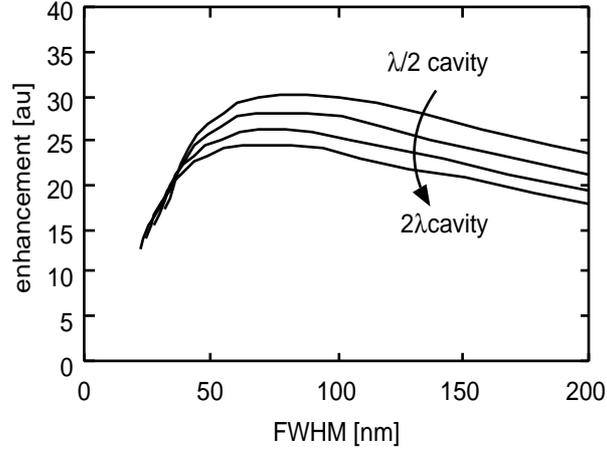
Figure 3.22: Calculated enhancement as a function of the cavity bandwidth, for long-wavelegnth RCLEDs, for different cavity lengths and for an increasing reflection of the outcoupling mirror.

efficiency (into NA=1) equals 2.7 %. A cavity optimised for a small divergence beam has typically many DBR pairs, and is heavily undertuned (the cavity thickness is too small). In fact, the cavity resonance wavelength is close to anti-resonance (the phase of the round trip equals π (plus an integer times 2π), in stead of an integer times 2π). If the cavity was chosen even smaller, then the far-field pattern starts to broaden again. This is explained using the k-space picture (see figure 3.11). All resonance planes elevate if the cavity thickness is decreased. At a certain point, the lower order mode will be sufficiently elevated to enhance the spontaneous emission in the extraction cone. The corresponding far-field pattern becomes suddenly very broad, as shown by the simulations.

3.7.5   Design for optimised spectral properties

The previous analysis were intended to optimise the output power of the RCLED into certain directions. No attention was paid to the wavelength properties. This paragraph discusses the design of the RCLED for a given output spectral bandwidth.

The spectral bandwidth of the emitted light is given by (see appendix A):

$$\Delta\lambda_{em} = \frac{\Delta\lambda_{SE}\Delta\lambda_{cav}}{\sqrt{\Delta\lambda_{SE}^2 + \Delta\lambda_{cav}^2}} \approx \Delta\lambda_{cav} \; (\Delta\lambda_{SE} > \Delta\lambda_{cav})$$

A small emission bandwidth requires a small cavity bandwidth. This corresponds to a high Q-factor (large reflections) or a long cavity. A plot with the

averaged enhancement as a function of the cavity bandwidth is shown in figure 3.22, in case of a 1.5 μm RCLED. This plot shows that the enhancement is maximised if the cavity bandwidth equals the bandwidth of the intrinsic spontaneous emission spectrum, as was mentioned before. If the cavity length is increased (towards a higher order cavity) for a given reflection of the output mirror, then the enhancement decreases. Therefore, choosing a longer cavity length is no solution to provide an efficient and small output spectrum.

In conclusion, the design of a RCLED with a limited emission spectrum requires a highly reflective mirror and a short cavity length. The corresponding spectral density of the optical power is larger compared to a cavity optimised for maximal overall light extraction.

3.7.6   Design for coupling to fibre

The coupling efficiency into a fibre is given by the product of the extraction efficiency into the numerical aperture of the fibre and a geometrical overlap factor. This factor is given by the ratio of the fibre core area and the light spot area at the fibre facet. The light spot area at the facet depends on the RCLED diameter and the distance between RCLED and fibre facet. The power coupled into the fibre is thus given by:

$$
P_{fibre} = \begin{cases} \frac{h\nu}{q}\eta_{int}\frac{NA_{fibre}^2}{4n^2}enh\left(\frac{\theta_{NA}}{2}\right)\frac{R_{fibre}^2}{R_{spot}^2}I & \left(R_{fibre} < R_{spot}\right) \\ \frac{h\nu}{q}\eta_{int}\frac{NA_{fibre}^2}{4n^2}enh\left(\frac{\theta_{NA}}{2}\right)I & \left(R_{fibre} > R_{spot}\right) \end{cases} \tag{3.30}
$$

with R_{spot} the spot diameter and R_{fibre} the fibre core diameter. An optimisation of the fibre coupling requires that the power in the numerical aperture is optimised. This was discussed in section 3.7.2.

3.8   Lenses and microlenses on RCLEDs

In this section, the influence of a lens on the fibre coupling efficiency of RCLEDs will be studied. A special lens is the microlens: this is a small lens, which is integrated on the RCLEDs. They are extremely suitable in array-applications. The presence of the lenses redirects the light, which is beneficial in applications where the light beam properties are important, as in fibre coupling.

In this work, only microlenses are considered. This corresponds to a single (small) lens per optical channel in the array. The size of the lenses is determined by the pitch of the array. Macroscopic lenses, which project the light emitted by several RCLEDs on several fibre facets, are not considered here.

3.8.1   Introduction on lenses

A lens projects a source onto an image (see figure 3.23). In case of an imaging system, the distance between the source and the lens (L_1), the distance between
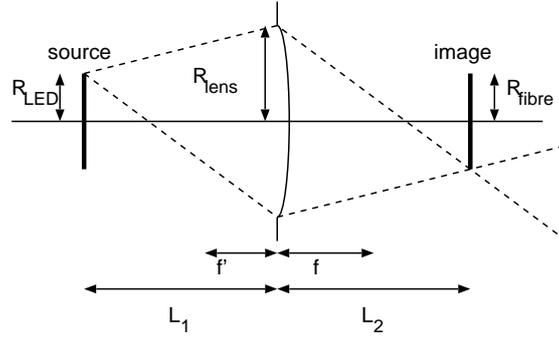
Figure 3.23: Overview of lens system.

the lens and the image and lens (L_2) and the focal point of the lens are related by:

$$\frac{n_1}{L_1} + \frac{n_2}{L_2} = \frac{1}{f}$$

with f the focal distance. This focal distance depends on the curvature of the lens, and on the refractive index of the lens material. It can be written as:

$$f = \frac{R_{curv}}{n_2 - n_1} = \frac{\alpha R_{lens}}{n_2 - n_1}$$

The curvature of the lens has a lower limit, set by the lens diameter. A parameter α is introduced ($\alpha > 1$). The RCLED is projected onto the fibre facet by the imaging system. The magnification is defined as the ratio between the image size R_{fibre} (the fibre core) and the source size R_{LED} (the RCLED):

$$M = \frac{R_{fibre}}{R_{LED}} = \frac{n_1}{n_2}\frac{L_2}{L_1}$$

The distance from the RCLED to the lens can be written as a function of the magnification and the focal distance:

$$L_2 = n_2\,(M+1)\,f, \quad L_1 = n_1\left(\frac{M+1}{M}\right)f$$

The distance to the lens L_1 and the size of the lens R_{lens} determine the capture efficiency of the lens system. The efficiency into the lens (the capture efficiency) in the centre of the RCLED is given by:

$$\eta_{capt} = \sin^2\theta \approx \left(\frac{R_{lens}}{L_1}\right)^2 = \left(\frac{1}{\alpha}\frac{n_2-n_1}{n_1}\frac{M}{M+1}\right)^2$$

From this simple expression, following conclusions can be drawn:

- a large capture efficiency needs a large magnification M. This implies that small RCLEDs are required.

- the difference between n_1 and n_2 should be as large as possible. The most effective is a very large n_1.

- α should be small, thus the lens curvature should equal the lens diameter. This corresponds to a demi-sphere lens shape.

However, there is an upper limit to the magnification. All light that is coupled in the fibre should pass through the lens. If the lens is too small, then the capture efficiency would decrease. There is thus a minimal lens diameter, corresponding to a minimal pitch. The larger the NA of the fibre, the larger the minimal lens diameter. In that case, no light from other lenses will be coupled into the fibre. In this way, optical cross-talk is avoided. This implies a condition for the minimal lens diameter:

$$R_{lens} > R_{fibre} + L_2 \tan \frac{\theta_{NA}}{n_2}$$

The distance from the lens to the fibre L_2 is written as a function of the lens diameter:

$$R_{lens} > R_{fibre} + n_2 \left(M + 1 \right) \frac{\alpha R_{lens}}{n_2 - n_1} \tan \frac{\theta_{NA}}{n_2}$$

If this condition is not fulfilled, then only a part of the light captured by the lens will be coupled into the fibre. From this expression, a maximal magnification is found:

$$M < \frac{R_{lens} - R_{fibre}}{\alpha R_{lens}} \frac{n_2 - n_1}{\theta_{NA}} - 1$$

For example, assume a lens diameter of 250 μm (equals the pitch of the array), and a numerical aperture of 0.5, and a fibre diameter of 60 μm (120 μm). The corresponding maximal magnification is 3.0 (1.9). This number increases if the lens diameter increases.

3.8.2 Coupling to fibre with a lens

An upper limit of the performance of the lens system is found using the radiance of the system. The radiance is the emitted optical power per unit of emission area, and per unit of solid angle. It is known that the radiance cannot increase due to the use of lenses or other optical components. The radiance of a RCLED in perpendicular direction is given by the radiance of a planar LED, multiplied with the cavity enhancement (with π the solid angle of the half space):

$$rad = \frac{P_{LED}}{A_{LED} \, d\Omega} = \frac{\frac{h\nu}{q} \eta_{int} \frac{1}{4n^2} e \, nhI}{\pi R_{LED}^2 \pi}$$

with enh the cavity enhancement in perpendicular direction. This enhancement depends on the propagation direction of the light, as was discussed in the previous paragraphs. However, this dependency is neglected as only the (almost) perpendicular travelling light is coupled in the lens system. Assume that the lens system projects this radiance onto the fibre core. The power coupled into fibre is then given by:

$$P_{fiber} = rad\,\Omega_{fiber} A_{fiber} = \frac{h\nu}{q}\eta_{int}\frac{NA_{fiber}^2}{4n^2}enh\frac{R_{fiber}^2}{R_{LED}^2}I \qquad (3.31)$$

This estimation is an upper limit for the coupled power into the fibre: it assumes that all emitted light by the RCLED is captured by the lens.

Equation 3.31 expresses the maximal power coupled into a fibre, when a lens system is used. This expression should be compared to equation 3.30, which expresses the fibre-coupled power when no lens system is used. The improvement is given by:

$$\frac{P_{fiber}^{lens}}{P_{fiber}^{nolens}} = \begin{cases} \frac{R_{spot}^2}{R_{LED}^2} & (R_{fiber} < R_{spot}) \\ \frac{R_{fiber}^2}{R_{LED}^2} & (R_{fiber} > R_{spot}) \end{cases}$$

This implies that the improvement decreases with increasing RCLED diameter. The lens is advantageous if the fibre spot is much larger than the fibre diameter. Keep in mind that this is an upper limit: it assumes that a radiance-preserving lens system can be designed. This design will be limited by the maximal lateral dimension of the system, as was discussed in the previous section. An extensive discussion on the coupling from RCLEDs to a limited numerical aperture, including numerical simulations using a ray-tracing software tool, is presented in [61].

3.9   Conclusion

In this chapter, the efficiency of RCLEDs was studied theoretically. This includes a study of the properties of spontaneous emission in semiconductors, and a study of the extraction efficiency of RCLEDs. It was shown that the microcavity has an important influence on the extraction efficiency. An analytical expression for the extraction efficiency was derived. This expression is only valid if the change of the total emission lifetime in the microcavity is negligible compared to the emission lifetime without a cavity. Fortunately, this is valid for DBR based RCLEDs. The influence of the recycling effect on the extraction efficiency was also studied, and the design of microcavities for different applications was presented, with emphasis on the design for coupling to limited numerical aperture. Finally, the influence of microlenses on the coupling into fibres was briefly discussed.

Appendix A: The derivation of the fitting expression

The output optical power is a function of the carrier density, as given by equation 3.4. The carrier density is a function of the injected current, as given by equation 3.3. Combining both equations:

$$P_{out} = \frac{h\nu}{q} \eta_{extr} \left(\frac{qVol}{4B\tau^2} \right) \left(\sqrt{1 + \frac{4BI_{inj}\tau^2}{qVol}} - 1 \right)^2$$

Introducing two new parameters:

$$\alpha = h\nu\eta_{extr} \frac{Vol}{4B\tau^2}, \ \beta = \frac{4B\tau^2}{qVol}$$

Then the output power can be written as:

$$P_{out} = \alpha \left(\sqrt{1 + \beta I_{inj}} - 1 \right)^2$$

This equation can easily be transformed to:

$$\left(\pm \sqrt{\frac{P_{out}}{\alpha}} + 1 \right)^2 = 1 + \beta I_{inj}$$

$$\sqrt{P_{out}} = \alpha\beta \frac{I_{inj}}{\sqrt{P_{out}}} \mp 2\sqrt{\alpha}$$

This linear expression allows a simple extraction of the extraction efficiency from the measurements.

Appendix B: Calculation of the integrated enhancement

In this appendix, a closed-form expression for the cavity enhancement is derived. Assume that the intrinsic spontaneous emission spectrum and the cavity enhancement spectrum can be written as a Gaussian function. Both spectra are written as:

$$SE(\lambda) = \frac{1}{\sqrt{2\pi}\Delta\lambda_{SE}} \exp \frac{-(\lambda - \lambda_{SE})^2}{2\Delta\lambda_{SE}^2}$$

$$enh(\lambda, \theta) = enh_{max} \exp \frac{-(\lambda - \lambda_{cav}(\theta))^2}{2\Delta\lambda_{cav}^2}$$

with $\Delta\lambda_{SE}$ the bandwidth of the intrinsic spontaneous emission spectrum (this has been discussed in paragraph 3.2.5[13]) and λ_{SE} the intrinsic emission peak wavelength. The enh_{max} is the maximal enhancement (given by equation 3.24), $\Delta\lambda_{cav}$ is the bandwidth of the cavity enhancement (given by equation 3.25) and $\lambda_{cav}(\theta)$ is the cavity resonance wavelength (given by equation 3.21). The emission spectrum in a certain propagation direction is given by $p_{RCLED}(\lambda,\theta) = enh(\lambda,\theta) SE(\lambda)$, which is also a Gaussian function. This emission spectrum can thus be written as:

$$p_{RCLED}(\lambda,\theta) = em_{max} \exp\left(-\frac{1}{2}\left(\frac{\lambda - \lambda_{em}}{\Delta\lambda_{em}}\right)^2\right)$$

λ_{em} is the emission wavelength, $\Delta\lambda_{em}$ is the bandwidth of the spectrum, and em_{max} is the maximal emission. These parameters can be written as:

$$em_{max} = \frac{enh_{max}}{\sqrt{2\pi}\Delta\lambda_{SE}} \exp\left(-\frac{1}{2}\frac{(\lambda_{SE} - \lambda_{cav})^2}{\Delta\lambda_{SE}^2 + \Delta\lambda_{cav}^2}\right)$$

$$\lambda_{em} = \frac{\lambda_{SE}\Delta\lambda_{cav}^2 + \lambda_{cav}\Delta\lambda_{SE}^2}{\Delta\lambda_{cav}^2 + \Delta\lambda_{SE}^2}$$

$$\Delta\lambda_{em} = \frac{\Delta\lambda_{SE}\Delta\lambda_{cav}}{\sqrt{\Delta\lambda_{SE}^2 + \Delta\lambda_{cav}^2}}$$

This is thus the shape of the emitted spectrum into a given direction.

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[13]this parameter is not the bandwidth (the FWHM - full width at half maximum). The FWHM is related to $\Delta\lambda_{SE}$ by $FWHM = 1.66\Delta\lambda_{SE}$

Chapter 4

Realisation and characterisation of RCLEDs

In this chapter, the realisation and characterisation of RCLEDs optimised for coupling to plastic optical fibres is presented. This includes the design of top- and bottom-emitting RCLEDs, emitting light at 980 nm or 850 nm. Special attention is given to the substrate-removal process, and to the use of selectively oxidised AlAs in the RCLED device. The performance of the different devices is compared.

4.1   Introduction

The microcavity effect can be used to enhance the emission properties of an active layer in a material system, as long as it is possible to integrate the active layer in a cavity. However, if the effect is used to obtain a high efficiency, then the material system has to fulfil some specific conditions:

- The intrinsic light emission should be highly efficient. The microcavity effect enhances the extraction efficiency with a factor of about 10, but it does not enhance the internal quantum efficiency.

- The technology should allow to realise extremely small cavities (of the order of the wavelength of the emitted light).

- The technology should allow the integration of low-loss and highly reflecting mirrors.

Different technologies can be used to realise RCLEDs. This paragraph will discuss some of these technologies.

4.1.1   Structure of the RCLED

The RCLED is essentially a vertical light emitter, due to the enhancement of the light emission in the vertical direction. But the propagation direction of the

light can be freely chosen: light can be extracted at the top of the RCLED, or at the backside (through the substrate). This choice has important consequences for the design of the mirrors. For example, it determines whether the top mirror needs to be transparent. Different mirror types are available, and their details are summarised here:

- A metal mirror has a high reflection coefficient over all wavelengths and incidence angles. In practice, gold or silver is used. Gold is preferred, in spite of the slightly smaller reflection (94 % at 980 nm) compared to silver (97 %), but silver oxidises fast, and needs therefore an extra protection. Other metals have a smaller reflection: there is more light absorbed in the mirror. In some cases, this metal mirror is also the electrical contact. The metal can only be used as a back mirror, because it is not transparent. Moreover, it is only a top mirror: it is not possible to grow semiconductor structures on the metal.

- An alternative is a semiconductor DBR (Distributed Bragg Reflector, see paragraph 3.5.3). This type of mirror is easily integrated with the RCLED. It is electrically conductive, although in most cases special attention must be paid to the design of the DBR, to minimise the voltage drop across the successive layers, especially for p-type DBRs. The big advantage is its optical transparency (although a small absorption cannot be avoided[1]). Its disadvantage is the limited wavelength and angle range over which the DBR is highly reflective. This is due to the limited refractive index contrast, as explained in paragraph 3.5.3.

- An alternative is a dielectric DBR. The dielectrics are chosen to maximise the index contrast, improving the reflection properties of the mirror. Examples are the Si/SiO_2 or the $ZnSe/CaF_2$ [62] stack. However, these types of DBR are in general not electrically conducting, and are not integratable as bottom mirror. Furthermore, the thermal properties of the dielectrics need to be matched with the underlying semiconductor, to reduce thermal stresses.

If a bottom-emitting RCLED configuration is used, then the emitted light travels through the substrate. Special attention must be paid to reduce the absorption of light in the substrate, and to avoid the reflection losses at the substrate-air interface. For substrate-emitting RCLEDs on GaAs substrate (emission wavelength 980 nm, well above the bandgap wavelength of GaAs), the absorption coefficient is about 30 cm^{-1}, corresponding to a 22 % absorption after propagation through a 500-μm thick substrate. In some cases, the substrate is removed completely to reduce excessive absorption losses. It is also possible to use any mirror type as bottom mirror if the substrate is removed, and the

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[1]an important example is the p-type GaAs/AlGaAs DBRs, due to the band tailing effect. This effect is caused by excessive p-type doping, and results in a smaller bandgap, implying that light with photon energy larger than the bandgap will also be absorbed. Therefore, a n-type DBR is used as the outcoupling mirror.
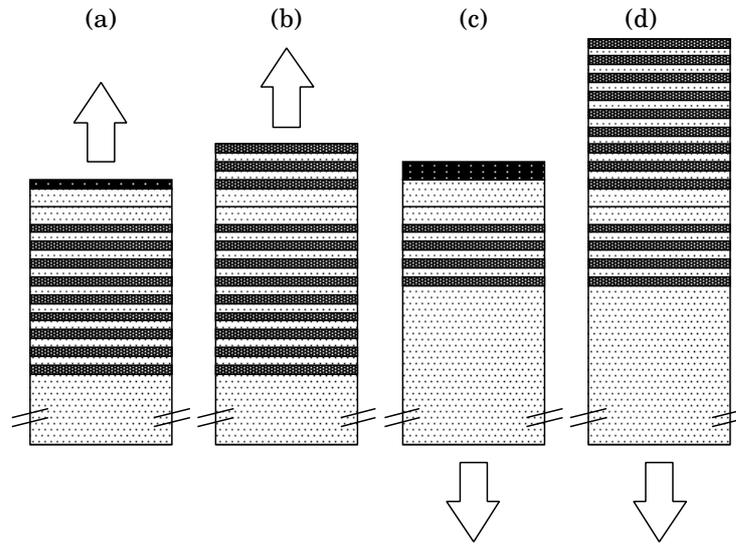
Figure 4.1: Different RCLED structures: (a) top-emitting using a metal/DBR cavity, (b) top-emitting using a DBR/DBR cavity, (c) bottom-emitting using a metal/DBR cavity and (d) bottom-emitting using a DBR/DBR cavity.

bottom mirror is added afterwards. This has been used to make RCLEDs with two metal mirrors [63]. A thin metal sheet is used as the outcoupling mirror, its thickness is optimised to minimise the absorption losses, but to maximise the reflection.

The choice of the mirror determines the type of electrical contacts. A metal top mirror can act as the electrical top contact. However, if the RCLED is top-emitting, or if a dielectric top mirror is used, then a transparent contact or a ring contact should be used. There are several conducting and transparent materials available (such as Indium Tin Oxide, ITO). In case of a ring contact, special care must be taken to confine the current, so that the light emission occurs mainly in the cavity and not under the metal contacts. A current confining structure, based on selectively oxidised AlAs, can be used. An alternative is a grid contact. In that case, a part of the emitted light is shielded by the contact, decreasing the efficiency. A bottom electrical contact is in general easier to realise. In most cases, an electrically conducting substrate is used, and a metal contact at the backside of the substrate is sufficient. In some applications, the bottom contact needs to be accessible at the top-side. An example are devices that need to be flip-chip mounted. In that case, a more complex processing scheme has to be used, including 'intra-cavity contacts'. In some specific cases, such as non-conducting top-mirrors, two intra-cavity contacts will be used.

The standard processing approach for RCLEDs results in common-n arrays: the devices are grown on a n-type substrate, and all devices have a common n-contact. This has the advantage that only one n-pad needs to be electrically

contacted. However, it might be advantageous to have an array with a common p-contact. In that case, a driver with better transistors could be designed (see chapter 8). This requires the availability of p-type substrates, and the calibration of the epitaxial growth system. N-on-p devices have been presented in literature. An alternative is the realisation of electrically isolated devices, but with two contacts per device. This approach needs one or more intra-cavity contacts.

4.1.2 Growth issues

Two important growth techniques are used to realise the layer structure of RCLEDs: Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapour Deposition (MOCVD). A comparison of the properties of both growth techniques goes beyond the scope of this work. There are some specific requirements to be fulfilled, which are independent on the growth technique. Firstly, it is important that the layer thicknesses are grown as accurately as possible. In practice, a small deviation caused by minuscule temperature non-uniformities over the wafer is inevitable. This deviation is typically a few percent or smaller. Secondly, the grown material must be of high-quality, to reduce the optical absorption losses and to increase the internal quantum efficiency of the active layers.

The deviation on the layer thicknesses results in a cavity detuning: the cavity resonance wavelength differs from the desired value. This results in a deviation on the efficiency and the beam properties of the RCLED. Several techniques have been proposed to solve this problem. Firstly, the design of the reactor could be optimised to maximise the uniformity of the growth over the wafer. For example, the use of rotating wafers results in a better spreading of the heat over the wafer. Secondly, an in-situ measurement of the layer thickness could be used to control the layer structure during growth. A third technique makes use of a two-step growth technique. The structure is grown with an intentionally thinner top layer, resulting in a shorter cavity resonance wavelength. Afterwards, the resonance wavelength of this structure is determined and a regrowth thickness can be calculated, which compensates for all deviations in the layer structure. A short regrowth (typically in the order of 10 nm) is performed to tune the cavity resonance wavelength to the desired value. Alternatively, the top layer can be grown too thick, and the thickness of the top layer can be tuned afterwards using a short etch step. The main difficulty is the determination of the resonance wavelength of the layer structure. One technique has been proposed in [51]. The original wafer is cut into pieces, and a small part of it is processed. The detuning is determined from the measured emission spectrum, and the rest of the samples is regrown. However, this is a destructive technique, and a lot of material is lost due to extra edge effects introduced during the regrowth.

In this work, a non-destructive technique is investigated, in which the regrow thickness is calculated from the measured reflection spectrum of the layer structure. The principle is as follows: it is assumed that there is a uniform de-
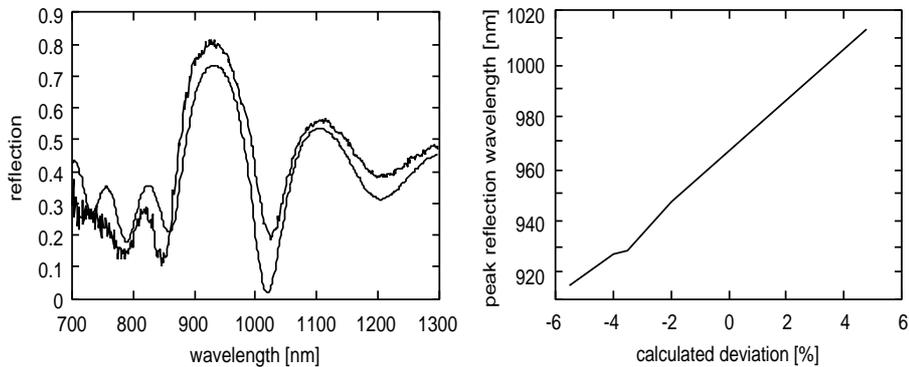
Figure 4.2: Comparison between the measured and the fitted reflection spectrum of the unprocessed layer structure (left), and the peak reflection wavelength as a function of the calculated deviation on layer thicknesses (right).

viation on the thickness of the layers in the structure. The reflection spectra of the structure are calculated for different deviations. After the layer structure is grown, its reflection spectrum is measured, and fitted to the calculated spectra. A measured and fitted reflection spectrum is shown in figure 4.2. From this fitting, the relative deviation on the thickness of the layers is found, typically a few percent. This allows to estimate the true thicknesses of the layers in the structure. Secondly, the optimal regrowth thickness as a function of the deviation on the layer thicknesses is calculated using the software tool for calculating the extraction efficiency of RCLEDs.

It was found that the calculated deviation depends linearly on a reflection peak in the measured reflection spectrum. Therefore, the numerically intensive fitting of the spectrum can be replaced by a simple measurement of a reflection peak. However, the determination of the deviation is still necessary for a given type of layer structure, to calibrate the relation between the measured peak wavelength of the layer structure and the deviation on the thicknesses of the layers in the structure. Figure 4.2 shows the result: the measured reflection peak (before the processing of the device) is plotted as a function of the calculated deviation. There is a linear relation between both parameters, allowing to use the reflection wavelength as a reference to determine the regrowth thickness.

4.2 Realisation of 980-nm bottom-emitting RCLEDs

In this paragraph, the realisation of bottom-emitting RCLEDs emitting at 980 nm, optimised for coupling to a plastic optical fibre (POF), is discussed. Several variants have been realised during this thesis: devices with an AlAs/GaAs DBR, devices with an AlO_x/GaAs DBR, and devices with a selectively oxi-
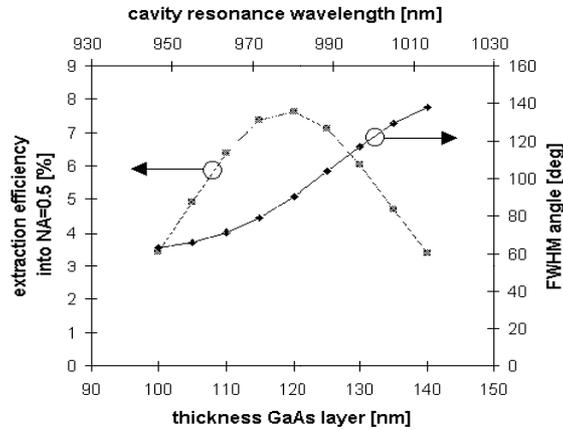
Figure 4.3: Calculated extraction efficiency in the numerical aperture of the POF and FWHM of the emission beam of 980-nm RCLEDs, as a function of the thickness of the upper GaAs layer (the corresponding cavity resonance wavelength is given at the top of the plot).

dised current window. The processing and the device-specific results will be discussed in this paragraph.

4.2.1   Design of the layer structure

The 980-nm bottom-emitting RCLED consists of a metal rear mirror and an AlAs/GaAs outcoupling DBR. The design of the RCLED involves the determination of the number of DBR pairs, and the thickness of the cavity. Extensive numerical simulations have been done to optimise the layer structure for a maximal extraction efficiency into NA=0.5 (the numerical aperture of the POF)[2]. Figure 4.3 shows the calculated extraction efficiency into the numerical aperture of the fibre, and the calculated full width at half maximum (FWHM) angle. For this calculation, no reabsorption in the active layer was taken into account.

As explained in the previous chapter, there is a trade-off between a small beam divergence angle and a large extraction efficiency. It was found that the efficiency into the numerical aperture is maximised if the cavity is almost perfectly tuned (the cavity resonance wavelength equals the intrinsic spontaneous emission wavelength). The extraction efficiency into the numerical aperture is 7.3 %, the corresponding FWHM is 88 degrees. The far-field pattern is close to the field pattern of a Lambertian emitter.

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[2]It should be noted that the coupling efficiency into the numerical aperture is an upper limit for the coupling efficiency to the fibre. In practice, effect such as the overlap of the emitted light spot and the fibre core diameter (as was discussed in paragraph 3.7.6), and reflections at the fibre facet, result in a decreased coupling efficiency.

thickness	material	doping level	remarks
40 nm	GaAs	p++	contact layer
68 nm	GaAs	p-doped	phase matching layer
50 nm	$Al_{40}Ga_{60}As$	30 nm p-doped	spacer
		20 nm intrinsic	spacer
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
50 nm	$Al_{40}Ga_{60}As$	20 nm intrinsic	spacer
		30 nm n-doped	spacer
5x (70 nm	GaAs	n-doped	5-pairs AlAs/GaAs DBR
+ 84.5 nm)	AlAs	n-doped	
	GaAs		buffer layer

Table 4.1: Layer structure of RCLED with AlAs/GaAs DBR.
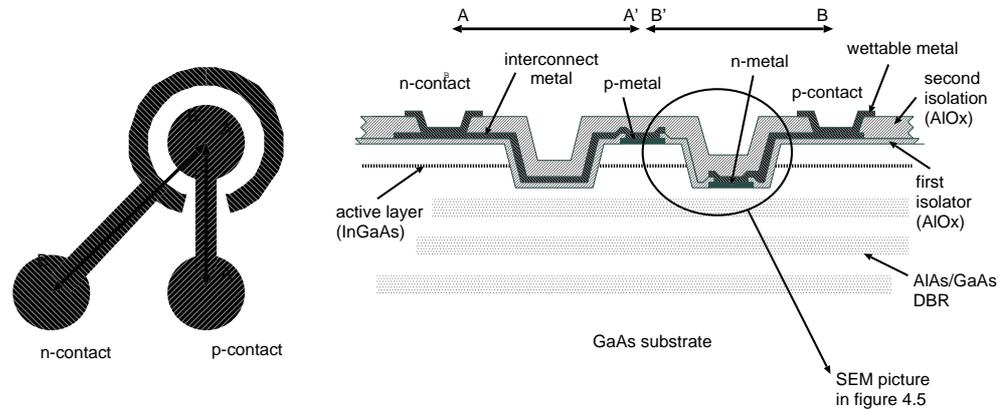
Figure 4.4: Top-view of RCLED (left) and section of RCLED over lines A-A' and B-B' (right). The circle points to the view of the SEM photograqph (see figure 4.5).

The layer structure is given in table 4.1. The optimal DBR consists of 5 DBR pairs. This is different compared to the optimal DBR of RCLEDs optimised for maximal overall extraction efficiency (6 pairs was the optimum [57]). In this work, a broader intrinsic spontaneous emission spectrum is used, because the devices will be driven at a rather large current density.

This calculated extraction efficiency is rather small: still over 92 % of the generated light is lost. This is explained by the fact that the numerical aperture of the POF corresponds to a very narrow solid angle inside the semiconductor, centred around the vertical axis. However, due to symmetry, the resonance wavelength is constant around the vertical axis. This implies that the emission in other emission directions than the NA of the POF is also reasonably enhanced. This explains the relatively broad emission pattern, and the relative small extraction efficiency into a small NA. Nevertheless, the extraction efficiency of an isotropic light emitter inside a planar LED into NA of 0.5 is about 0.5 %. The microcavity results in a more than tenfold increase of the extraction efficiency.

4.2.2   Processing of the RCLEDs

The layer structure was grown in a horizontal MOCVD reactor. More information can be found in [51]. Within this work, 2 different processing schemes for RCLEDs have been used. Firstly, a simple processing scheme, developed in [51] and [57] , was used to do elementary tests on the RCLEDs. Secondly, a new processing scheme for RCLED arrays, suitable for flip-chip mounting, was developed. The flip-chip compatibility implies important differences compared to the old processing scheme, as the intra-cavity n-contact and the introduction of interconnect tracks and extra isolation layers. A new mask set was designed,
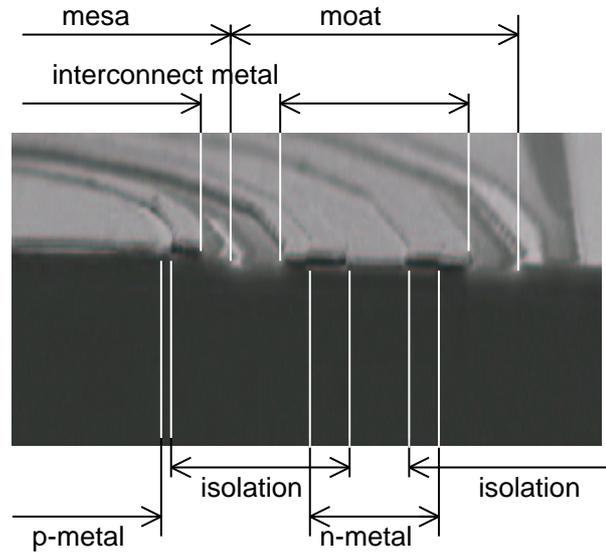
Figure 4.5: SEM close-up of processed RCLED. The isolation is transparent, and thus not visible.

including seven 4×8 arrays, two of them can be grouped into an 8×8 array. Three different mesa and mirror diameters are available: 70 μm mesa (with 50 μm diameter mirror), 52 μm mesa (with 32 μm diameter mirror) and 40 μm mesa (with 20 μm diameter mirror). In this work, the mirror diameter will be used to indicate the device diameter. The mirror diameter is 20 μm smaller than the mesa to reduce the non-radiative surface recombination by reducing the current density at the border of the device. This also influences the injection efficiency, since a part of the current will flow next to the mirror. Several test structures were included in the mask set, to test the electrical properties of the contacts, and to investigate the efficiency of very small and very large RCLEDs.

A cross-section of the RCLED is shown in figure 4.4. The processing starts with the definition of the mesa by etching circular moats using a wet chemical etch. The depth of the moat etch is important: the etching should at the n-type GaAs layer, to allow a good electrical n-contact. The depth of the wet etch is controlled by an accurate timing. The n-metallisation (Au/Ge/Ni) is deposited in the moat, followed by a fast alloy step. This is a high-temperature treatment at 440 °C, to reduce the ohmic resistance of the contact. Then the gold p-metal, also serving as highly reflecting mirror, is deposited. The metal is about 200 nm thick. The series resistance of the p-contact is decreased by a heavy p-doping of the upper 40 nm of the GaAs top layer of the layer structure. After that step, no high-temperature steps are allowed, because this would degrade the highly reflective GaAs-Au interface. At this stage, the RCLED is defined and testable.

The maximum temperature before the reflection of the Au-mirror starts to degrade is about 200°C. Afterwards, a first isolation layer (120 nm thick Al_2O_3) is deposited, using E-beam evaporation at room temperature. However, during the evaporation of the dielectric, the temperature increases to 40-50 degrees. This does not degrade the Au-mirror. Other dielectrics as nitride, polyimide could also be used, but Al_2O_3 was chosen, as it was the only available dielectric which could be deposited at this low temperature in a reliable way. On this dielectric, the interconnect wiring (40 nm Ti / 400 nm Au) is deposited. This wiring connects the RCLED contacts with the flip-chip bumps. The width of this interconnect is chosen as wide as possible, to reduce the series resistance. Finally, a second isolation (400 nm Al_2O_3) is deposited, and opened above the contact pads. At this stage, the RCLEDs are finished. The SEM picture (figure 4.5) shows a photograph of the moat of the RCLED, including the n-contact.

The post-processing of the devices, necessary for the flip-chip mounting, depends on the flip-chip technology. A solder reflow technique or a gold-bump technology can be used (for an overview, see [64]). In the first approach, a solder alloy is deposited at low temperature, which is heated afterwards. The solder curls due to the surface tension force, and nice bumps are formed. In the second technology, gold bumps are deposited using a plating technique. The typical height of the bumps is 2 to 5 μm. Both techniques need a different preparation of the sample. In case of a solder flip-chip mounting technique, a wettable metal is deposited above the contact pads, on which the solder will stick. In a first processing, Pt was used as diffusion barrier. In order to relief the stresses induced by the Pt, a rather complex metallisation stack was used: Ti/Cu/Ti/Pt/Au. In further processing, this was replaced by a 40 nm Ti / 150 nm Ni / 60 nm Au stack. Finally, a 5 μm thick Sn/Pb solder was deposited. In case of a gold-bump flip-chip technique, the bumps are put on the other chip (the carrier), and no special preparation of the RCLED chip is necessary. As a last step, the arrays were thinned to 100 μm to reduce the absorption of light in the substrate, and an anti-reflection coating was deposited.

4.2.3   980-nm RCLEDs with selectively oxidised AlGaAs

AlGaAs with a high aluminium concentration oxidises spontaneously if it is exposed to the atmosphere. The resulting oxide, AlO_x, is usually of a bad quality, full of cracks. However, if the oxidation is done in a controlled water vapour atmosphere at a specific temperature, a high-quality oxide is formed [65][66]. This discovery has resulted in a better performance of many optoelectronic components. In this work, the use of this selective oxidation technique in the realisation of RCLEDs was studied. The oxidation technique can be used in 2 ways:

- a current-confining window can be realised, by partially oxidising a single layer in a circular mesa. This should result in a better carrier confinement, necessary for the realisation of small-diameter devices. This technique is currently the standard approach to realise highly efficient

VCSELs. In these laser structures, the current aperture has a double function: it confines the current profile and the optical profile (it acts as a lens). The low refractive index of the doughnut-shape AlO_x acts as a lens, which helps to concentrate the optical field. These two functions led to an important improvement of the VCSEL characteristics, resulting in sub-$100\mu A$ threshold currents and truly longitudinal and lateral single-mode light emission. In RCLEDs, the lens-function of the current window will be negligible, due to the large lateral dimensions of the RCLED (typically a fews tens to a few hundreds micrometer).

- the AlO_x has a low refractive index (typically 1.55). This material can be used in a large contrast DBR. As mentioned in the previous chapter, large contrast DBRs result in smaller penetration depths, and better enhancements.

In this paragraph, the design of RCLEDs with a current confining window is discussed, in the next paragraph, the design of RCLEDs with selectively oxidised DBRs will be discussed.

The design of RCLEDs with a current window doesn't differ a lot compared to the design of standard RCLEDs. The layer structure is shown in table 4.2. The first layer of the outcoupling DBR containing a high aluminium concentration is reserved for a partial oxidation. If the AlAs layer was included in the i-region of the diode, then an extra barrier would be created, resulting in a bad carrier confinement and an increased voltage drop across the junction. This problem is avoided by placing the AlAs layer into the p-doped DBR.

In this design, the oxidised window is put under the active layer. In an alternative approach, the oxidised window can be placed above the active region. However, this would need more layers between the active region and the metal mirror, increasing the cavity thickness. This results in a decreased microcavity effect.

The oxidisable layer contains a little gallium: an $Al_{95}Ga_{05}As$ layer was chosen. Its thickness is determined by the reflection wavelength of the DBR. It was found that this little gallium improved the mechanical quality of the oxide [67]. On the other hand, the oxidation speed reduces as a function of the Ga-content [68]. Thus a larger oxidation time is necessary. Around the $Al_{95}Ga_{05}As$ layer, a 25 nm-thick graded transition from the GaAs layer to the $Al_{95}Ga_{05}As$ is included. This grading region increases the quality of the oxide. This layer is oxidised after the alloying of the n-contacts, but before the p-contact was deposited. The oxidation temperature was 440°C, the water vapour is generated by bubbling N_2 through water (80°C). The oxidation was done after the mesa etch. The rest of the processing is the same as the one presented in the previous paragraph.

4.2.4 980-nm RCLEDs with AlO_x/GaAs DBR

A bottom-emitting RCLED with a single AlO_x/GaAs pair was reported at the start of this work [69], but no optimisation for maximal efficiency was done. In

thickness	material	doping level	remarks
40 nm	GaAs	p++	contact layer
68 nm	GaAs	p-doped	phase matching layer
50 nm	$Al_{40}Ga_{60}As$	30 nm p-doped	spacer
		20 nm intrinsic	spacer
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
2 nm	GaAs	intrinsic	barrier
6 nm	InGaAs	intrinsic	QW
2 nm	GaAs	intrinsic	barrier
50 nm	$Al_{40}Ga_{60}As$	20 nm intrinsic	spacer
		30 nm n-doped	spacer
60 nm	GaAs	n-doped	contact layer
25 nm	GaAs->$Al_{95}Ga_{05}As$	n-doped	to be oxidised
54 nm	$Al_{95}Ga_{05}As$	n-doped	to be oxidised
25 nm	$Al_{95}Ga_{05}As$->GaAs	n-doped	to be oxidised
60 nm	GaAs	n-doped	second DBR pair
84.5 nm	AlAs	n-doped	
3x (70 nm	GaAs	n-doped	3-pairs GaAs/AlAs DBR
+84.5 nm)	AlAs	n-doped	
	GaAs		buffer layer

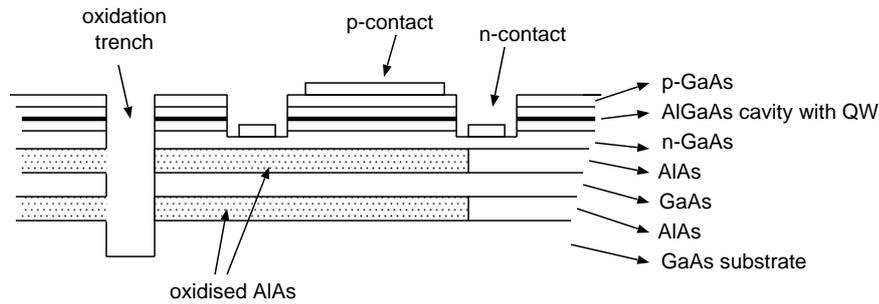Table 4.2: Layer structure of RCLED with AlAs/GaAs DBR and current confining window.

Figure 4.6: Structure of the AlO_x DBR RCLED, with the trenches, necessary for the oxidation.

the course of this work, a highly efficient RCLED with AlO_x/GaAs DBRs was reported [10]. The top-emitting RCLEDs had two AlO_x/GaAs DBRs, and a tunnel junction to confine the current under the DBRs. In this work, a bottom-emitting RCLED with an AlO_x/GaAs outcoupling DBR and a metal back mirror was investigated.

The use of an oxidised DBR has important complications on the design of the layer structure. The largest difference is the fact that the outcoupling mirror is not electrically conductive. Therefore, an intra-cavity contact should be used. Secondly, an extra trench is necessary through which the AlAs is oxidised. And finally, the thickness of the DBR layers must be adapted to the refractive index of the material after the oxidation. The refractive index of the AlO_x is 1.55.

Simulations were done to optimise the RCLED structure for maximal coupling into NA=0.5. The RCLED consists of a metal top mirror and an AlO_x/GaAs DBR outcoupling mirror. The first simulations were done using a $\lambda/4$ AlO_x/GaAs DBR. It was found that the optimal DBR counted 2 DBR pairs. The extraction efficiency in air is 22.5 %, whilst the extraction efficiency into NA=0.5 is 10.4 %. It was found that up to 28 % of the internally emitted light is absorbed into the metal mirror.

Secondly, the layer thicknesses of the outcoupling AlO_x/GaAs DBR were changed to tune the reflection of the mirror. It was found that the reflection of a single AlO_x/GaAs DBR pair is about 30 % and the reflection of the 2 pairs AlO_x/GaAs DBR is about 81 %. The optimal reflection for maximal extraction efficiency is about 50 %. Therefore, the thickness of the last DBR pair was changed in order to match the desired reflection at the given wavelength, without increasing the penetration depth of the mirror. The complete layer structure is given in table 4.3. The overall extraction efficiency of RCLEDs with optimised AlO_x/GaAs DBR mirror was calculated. The total extraction efficiency increased to 23.3 %, but the absorption into the metal mirror increased stronger, to 32 %. It is clear that this absorption in the metal mirror limits the extraction efficiency of the RCLEDs. This absorption could be minimised by reducing the optical field amplitude at the mirror. However, this can only be

thickness	material	doping level	remarks
200 nm	gold		metal mirror
119 nm	GaAs	50 nm p++ (1e19)	contact layer
		69.3 nm p(5e18)	phase-matching layer
69 nm	$Al_{40}Ga_{60}As$	20 nm p=1e18	spacer
		20 nm p ramp down	spacer
		29 nm undoped	spacer
2 nm	GaAs	undoped	barrier
6 nm	InGaAs	undoped	active layer
2 nm	GaAs	undoped	barrier
69 nm	$Al_{40}Ga_{60}As$	29 nm undoped	spacer
		20 nm ramp up	spacer
		20 nm n=5e18	spacer
60 nm	GaAs	n=1e18	first layer of DBR
20 nm	GaAs -> $Al_{95}Ga_{05}As$	p-doped	graded interface
133.1 nm	$Al_{95}Ga_{05}As$	p-doped	to be oxidised
20 nm	$Al_{95}Ga_{05}As$ -> GaAs	p-doped	graded interface
30 nm	GaAs	p-doped	
20 nm	GaAs -> $Al_{95}Ga_{05}As$	p-doped	graded interface
233.3 nm	$Al_{95}Ga_{05}As$	p-doped	to be oxidised
20 nm	$Al_{95}Ga_{05}As$ -> GaAs	p-doped	graded interface
xx nm	GaAs		buffer layer

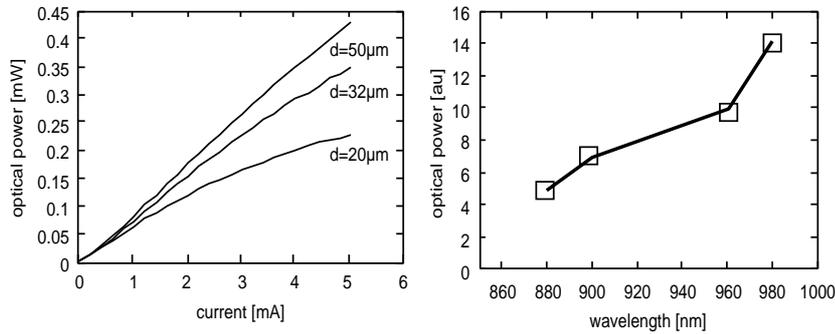Table 4.3: Layer structure of RCLED with selectively oxidised DBR.

Figure 4.7: Measured output power of 980-nm RCLEDs with an AlAs/GaAs DBR as a function of the drive current, for different device diameters (left), and influence of detuning on efficiency for 50 μm RCLEDs, driven at 3 mA (right).

achieved by introducing new reflections between the active layer and the metal mirror, and thus by increasing the distance between the quantum wells and the mirror. In this way, the overall cavity thickness increases, and the microcavity enhancement increases. Alternatively, a better metal (with less absorption) could be used.

The processing scheme is slightly different compared to the processing of standard 980 nm RCLEDs. Firstly, deep trenches are etched, through which the oxidation will occur. Secondly, the RCLED is defined by etching the moat, and the n-metal is deposited and alloyed. The depth of the moat must be precisely controlled. The etching should stop in the upper part of the GaAs contact layer (which is also the first layer of the DBR), to allow for a good contact. Otherwise, there would be an extremely thin GaAs layer between the metal contact and the underlying AlO_x. Then, the DBR is oxidised. The n-contact remains intact during the oxidation. The oxidation technique is similar to the technique used to oxidise the current window. However, a longer oxidation time was used (about 1 hour). Finally, the rest of the processing was done, as described in paragraph 4.2.2.

4.2.5 Measurement results

In this section, the efficiency measurements on all 980-nm RCLEDs will be presented. The optical power characteristics for three 980-nm bottom-emitting RCLEDs with an AlAs/GaAs DBR are shown in figure 4.7. The quantum efficiency at 3 mA is 13.4 % for the 50 μm RCLED, 11.8 % for the 32 μm RCLED and 8.6 % for the 20 μm RCLED. The efficiency decreases as a function of decreasing RCLED diameter. Efficiencies up to 16 % were measured on 85 μm RCLEDs (realised using the test mask). This is explained by the higher current density, resulting in a broader intrinsic spontaneous emission spectrum (and thus a decreased overlap with the cavity enhancement).
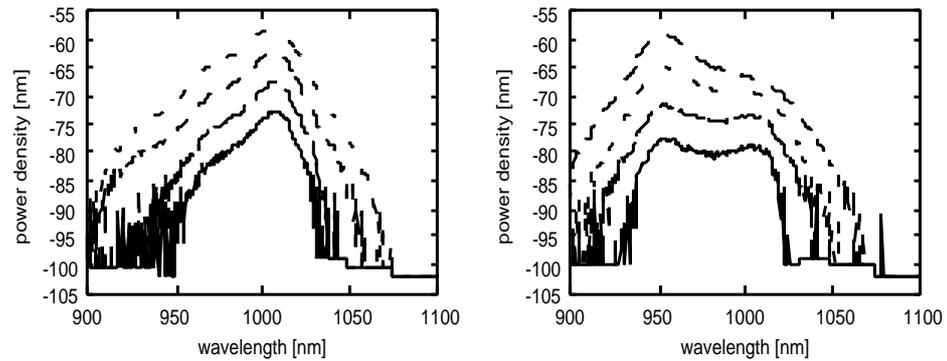
Figure 4.8: Measured emission spectra of RCLEDs with a current window for different injection currents (1, 3, 10 and 30 mA), large devices (200 μm diameter, left) versus small devices (50 μm, right).

The measured efficiency is smaller than the calculated extraction efficiency. An extraction efficiency of 22 % was expected. The difference is explained by the internal quantum efficiency, the current spreading in the mesa structure, the slightly detuned cavity, the residual absorption in the substrate, and the non-ideal anti-reflection coating.

The emission spectrum of the RCLED has a peak at 984 nm, and its spectral width is 21 nm. The spectral width does not depend on the current level or RCLED diameter, indicating the filter effect of the microcavity on the intrinsic spectrum. Figure 4.7 shows the influence of the cavity detuning on the overall quantum efficiency. Some parts on the wafer have a smaller cavity resonance wavelength, due to non-uniformities during the growth. This measurement clearly shows that undertuned cavities have a reduced extraction efficiency.

4.2.5.1   Influence of the current window

The design of RCLEDs with a current window has been discussed in the previous paragraph. The current window confines the injected current, resulting in a decreased light emission next to the metal mirror. Figure 4.8 shows the measured emission spectrum of RCLEDs with an oxidised current window. Two different emission peaks are visible. Both emission peaks are cavity peaks. This was confirmed by measuring the spectra as a function of the external temperature - both peaks drift as a function of the temperature at the same speed. The long wavelength peak is assigned to the metal covered part of the mesa, the short wavelength peak is assigned to the oxidised part of the mesa. This implies that there is still light emission under the selectively oxidised current window. The effect is even stronger for smaller RCLEDs, where the area of the oxidised part of the mesa is relatively more important compared to large RCLEDs.

This effect can be explained by lateral current spreading or lateral carrier diffusion. Due to these effects, a part of the injected carriers recombine next to the metal mirror. In this work, it is believed that the lateral carrier diffusion is the dominant effect. The lateral current spreading is neglected, because of the large lateral series resistance between the junction and the current window. After all, there is only a very thin n-doped AlGaAs layer between the active layer and the current window. As an example, the series resistance of a 100 nm thick n-type GaAs ring, with inner radius of 10 μm and outer radius of 15 μm, is about 300 Ω[3]. This series resistance would be larger if the GaAs was p-doped, because of the larger resistivity of p-type GaAs. Due to this large series resistance, little current will flow through it. Therefore, the lateral carrier diffusion is expected to introduce the light emission next to the mirror.

This lateral carrier diffusion is also present in VCSEL structures, and is one of the limiting factors in decreasing the diameter of the VCSELs. However, in VCSELs, the influence of this diffusion is only important at very small device diameters (diameter < 5 μm). The RCLEDs have a larger diameter compared to VCSELs, and therefore this effect was not expected.

The diffusion effect is described by a diffusion length, which expresses the spread of the carriers into the lateral direction. The one-dimensional diffusion equation and the solution, assuming $n(x=0) = n_0$ and neglecting the non-radiative recombination effects, is written as:

$$D\frac{d^2 n}{dx^2} - Bn^2 = 0 \;\Rightarrow\; n(x) = \frac{6D}{B} \frac{1}{\left(x + \sqrt{\frac{6D}{Bn_0}}\right)^2} \tag{4.1}$$

D is the effective diffusion constant. This effective diffusion describes the diffusion of the carriers, taking into account the charge neutrality condition. Due to this condition, the number of electrons equals the numer of holes at each location. The effective diffusion constant is determined by the diffusion coefficients of the electrons and holes, and the mobility of the electrons and holes:

$$D_e = \frac{\mu_n D_p + \mu_p D_n}{\mu_n + \mu_p} = \frac{2D_n D_p}{D_n + D_p}$$

with D_n and D_p the diffusion of the electrons and the holes, and μ_n and μ_p the mobility of the electrons and the holes. This expression is simplified usign the Einstein relation ($D = \mu\frac{kT}{q}$). For GaAs, D_e is found to be 19.1 cm^{2}s^{-1}. In literature, the diffusion coefficient of InGaAs based active regions was found to be 11 cm^{2}s^{-1}[70].

The distance at which the carrier concentration is reduced to 10 % of n_0 can be found from equation 4.1, and is given by:

$$L_{10\%} = \sqrt{\frac{28.05D}{Bn_0}}$$

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[3]The series resistance R of a ring is given by $R = \frac{\rho}{2\pi d} \ln \frac{R_{out}}{R_{in}}$, with ρ the resistivity, d the thickness of the ring, R_{out} the ring outer diameter and R_{in} the ring inner diameter.
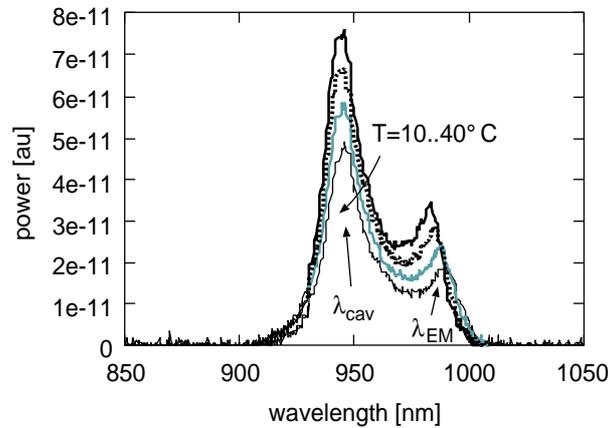
Figure 4.9: Measured spectra of AlO_x-DBR RCLED, driven at a constant current, as a function of the ambient temperature.

Assuming $D = 11\ \text{cm}^2\text{s}^{-1}$, $B = 1.3 \cdot 10^{-10}\ \text{cm}^3\text{s}^{-1}$ and $n_0 = 3 \cdot 10^{18}\ \text{cm}^{-3}$, a lateral diffusion length of 8.9 μm is found. This rather large diffusion length is explained by the slow radiative recombination at small carrier densities. In VCSELs, the main recombination effect is the stimulated emission, which is much faster compared to the spontaneous emission. This results in a shorter diffusion length in the VCSEL case, which explains the reduced influence of this lateral diffusion in VCSELs.

It is found that the selectively oxidised current window does not improve the emission efficiency of the RCLEDs in case of very small devices (typically 15 μm or smaller). This is related to the lateral carrier diffusion effect in the active layer. However, due to the larger carrier lifetime, the effect is more important in RCLEDs, compared to VCSELs[4]. The solution is the use of an active region with a decreased lateral diffusion. Quantum-dot based active regions have been proposed, and efficient small-diameter VCSELs using a quantum-dot active region have been realised.

4.2.5.2   Characteristics of 980-nm RCLEDs with AlO_x/GaAs DBR

The emission spectra of 980-nm RCLEDs with an oxidised DBR are shown in figure 4.9. Again, two emission peaks are visible. In this case, the short-wavelength peak is the cavity resonance wavelength, the long-wavelength peak is the intrinsic spontaneous emission wavelength. This is confirmed by measuring the spectrum as a function of the temperature: both peaks drift at a different speed. Unfortunately, there is a large detuning: the intrinsic spontaneous emission is centred at 1010 nm, whilst the cavity resonance wavelength

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[4]Another experimental proof for this lateral carrier diffusion in RCLEDs will be discussed in chapter 6, when discussing the small-signal response of RCLEDs.
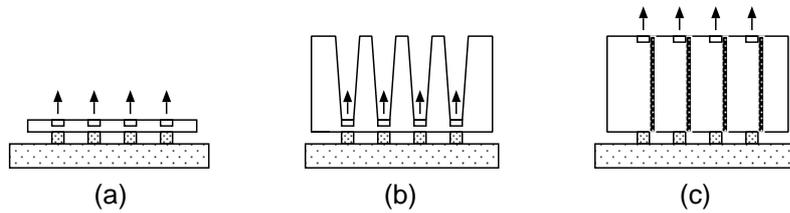
Figure 4.10: Different approaches for bottom-emitting 850-nm RCLEDs, mounted on a carrier: (a) complete substrate removal, (b) partial substrate removal (optical holes) and (c) through-hole metallisation.

is centred around 970 nm.

Nevertheless, the overall quantum efficiency of 50 μm devices was 6.5 %. Taking into account the detuning, the absorption in the substrate and the reflection at the semiconductor-air interface, a maximal efficiency of 15 % is estimated. This is similar to the performance of AlAs/GaAs RCLEDs, as expected from the simulations. This implies that the oxidation process has no adverse effect on the quality of the active layer.

4.3 Realisation of substrate-removed RCLEDs

4.3.1 Introduction

For some commercial reasons[5], devices emitting at 850 nm seem to be more interesting than devices emitting at 980 nm. In this work, RCLEDs emitting at 850 nm, based on the AlGaAs material system, were developed. However, there is a big problem with the AlGaAs material system at 850 nm: the GaAs substrate absorbs all light at that wavelength, inhibiting the realisation of bottom-emitting RCLEDs.

Therefore, a transparent substrate has to be used, or the substrate has to be removed. Several possibilities are summarised in figure 4.10. The substrate can be removed completely (figure 4.10,a), or partially (figure 4.10,b). In the last case, the light is emitted through holes. These holes can be filled with a transparent material to reduce the spreading of the beam. Another technique uses the holes for electrical contacts (figure 4.10,c). This approach needs an important processing on the backside of the wafer. In another technique (not on the figure), the devices are bonded on a transparent substrate, such as GaP or SiC. Afterwards, the original (GaAs) substrate is removed, and the contacts are defined on the AlGaAs film on the new substrate. The bonding is done using a fusion process at elevated temperatures. If the bonding interface is

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[5]850nm is a standard wavelength for optical transmission using the Ethernet protocol (as defined in IEEE 802.3z standard), mainly because the availability of low-cost Si-based detectors. 980nm is - purely technical speaking - a better wavelength, it allows a longer transmission distance. However, economical rules have lead to a worse-performing standard wavelength.

part of the electrical contact, then the electrical properties of the new substrate are very important (such as the doping profile at the surface), in order to reduce the voltage drop across the fusion-junction.

Each approach has its advantages and disadvantages. The partial substrate removal can occur before the mounting, and allows the optical testing of the devices before they are mounted. However, this approach requires more processing steps. For this reason, complete substrate removal is believed to be more production-ready. The remaining thin-film RCLEDs could eventually be mechanically isolated, by etching a deep trench in between the components before the mounting. This was proposed to reduce possible mechanical stresses in the RCLEDs.

In this work, substrate removal is used to realise bottom-emitting 850-nm RCLEDs. This technique was used to remove the substrate of flip-chip mounted modulators and to remove the substrate of VCSELs on CMOS circuits.

4.3.2   Substrate-removal process

The substrate is removed using a high-speed wet chemical etch technique. Table 4.4 gives an overview of different substrate-removal experiments, found in literature. The most popular etching mixture for the removal of GaAs substrates is $NH_4OH/H_2O_2/H_2O$, in combination with a high Al-content AlGaAs etch stop layer. The largest selectivity is obtained for a pure AlAs etch stop layer. However, during the etching, the AlAs is converted in an oxide, introducing large stresses in the remaining thin-film RCLED. To avoid this, an AlGaAs etch stop layer is used, or even a DBR-like structure consisting of a few AlAs/GaAs pairs. Alternatively, an InGaP etch stop layer has been proposed. It was found that the larger selectivity results in a better uniformity.

The substrate removal starts with the flip-chip mounting of the RCLED arrays, followed by a mechanical polishing to reduce the substrate thickness to 50 μm. Then the rest of the substrate is removed by chemical etching. A $NH_4OH/H_2O_2/H_2O$ etching mixture was used (4:96). The pH value of the mixture was rather high, resulting in large etching speed. The etching was done is two steps. First, a high-speed mixture was used, with an etching rate of about 4 to 5 μm/min. The rest of the substrate is removed by a slower mixture (with less NH_4OH). During the etching, the sidewalls of the GaAs chip were protected using a varnish (Q16). Finally, the etch-stop layer (an oxidised AlAs) is removed using a HF/H_2O mixture (1:4).

In this work, different etch-stop layers have been used. In first experiments, the AlAs/GaAs DBR was used as the etch-stop layer. This resulted in a bad yield after substrate removal (typically about 50 %). In the following experiments, an extra etch stop layer (100 nm thick AlAs) was included, without success. Experiments showed that this was too thin to withstand the etching. Finally, a thick $Al_{15}Ga_{85}As$ layer was included as a mini-substrate, to enhance the mechanical stability of the device during and after the removal process ($Al_{15}Ga_{85}As$ was used, because it is transparent for 850-nm light, and the difference in lattice constant is small compared to active layer material GaAs).

Table 4.4: Overview of substrate-removal techniques.

etch-stop layer	mechanically thinned ?	thickness [μm]	etching mixture	concentration	pH	rate [μm/m]	protection	ref
100 nm AlAs + 3pairs (250 nm $Al_{50}Ga_{50}As$ +250 nm GaAs)	yes	??	$NH_4OH/H_2O_2/H_2O$	??	8.05-8.10	1-2	wax	[75]
100 nm AlAs + 4pairs (250 nm $Al_{50}Ga_{50}As$ 250 nm GaAs)	yes	100	$NH_4OH/H_2O_2/H_2O$	??	8.5	??	??	[74]
1500 nm $Al_{30}Ga_{70}As$ + 250 nm $Al_{50}Ga_{50}As$	yes	200	$NH_4OH/H_2O_2/H_2O$	1:100	??	1.5h	resist AZ4210	[73]
1000 nm AlAs	yes	50	$NH_4OH/H_2O_2/H_2O$	3:100	??	1	wax	[76]
1500 nm $Al_{30}Ga_{70}As$	yes	??	$NH_4OH/H_2O_2/H_2O$	1:100	??	??	silica epoxy	[77]
500 nm $In_{49}Ga_{51}P$	??	??	H_3PO_4	??	??	3.5	epoxy	[81]
750 nm AlAs	??	??	$NH_4OH/H_2O_2/H_2O$	??	8.3-8.6	2.6-3	wax	[78]
750 nm AlAs	??	??	citric acid-H_2O_2	K=4	??	0.4	wax	[78]
100 nm AlAs	Br-Meth polish	??	citric acid-H_2O_2	??	??	??	wax	[79]
500 nm $Al_{50}Ga_{50}As$	??	??	$NH_4OH/H_2O_2/H_2O$	??	??	??	??	[80]
100 nm AlAs + 4pairs (250 nm $Al_{50}Ga_{50}As$ 250 nm GaAs)	yes	100	$NH_4OH/H_2O_2/H_2O$	??	7.85	??	??	[71]
100 nm AlAs	??	??	$NH_4OH/H_2O_2/H_2O$	30:1	??	??	??	[72]

Figure 4.11: Measured spectra from substrate-removed 850-nm RCLEDs. (a) is a RCLED with the stabilisation layer, (b) is a RCLED with the stabilisation layer and an anti-reflection coating, (c) is a RCLED without the stabilisation layer.

Two different etch stop layers were used, in combination with the mechanical stabilisation layer: 1000 nm AlAs (as the safe solution, which surely would withstand the etching), and a 500-nm thick $Al_{70}Ga_{30}As$ (with a reduced difference in lattice constant between the etch stop layer and the active layer). Experiments showed that both layer structures performed very well, no difference in RCLED characteristics were found.

4.3.3 Performance of substrate-removed components

The substrate-removal process has several important consequences. The RCLED becomes extremely thin (only a few μm, even including the mechanical stabilisation layer), which has an important effect on the electrical and the thermal behaviour of the device.

Figure 4.11 shows the measured spectra of substrate-removed, bottom-emitting RCLEDs, processed in 3 different ways. Case (a) presents a RCLED with a 2 μm thick stabilisation layer, which is clearly a multi-mode cavity. The optical cavity thickness is set by the reflection at the semiconductor-air interface. This multi-mode cavity results in a decreased extraction efficiency. In case (b), an anti-reflection coating is deposited onto the stabilisation layer. The spectrum (measured in perpendicular direction) becomes mono-modal, but there is no big increase of the efficiency. This is explained by the fact that the AR works only for the perpendicular propagation direction. In the other directions, as seen from within the semiconductor, there is still the semiconductor-air interface dictating the cavity thickness. Internally, the cavity remains multi-mode. In case (c), the stabilisation layer is etched away, and the emission spectrum is mono-modal. However, the yield of the 8×8 array decreases.
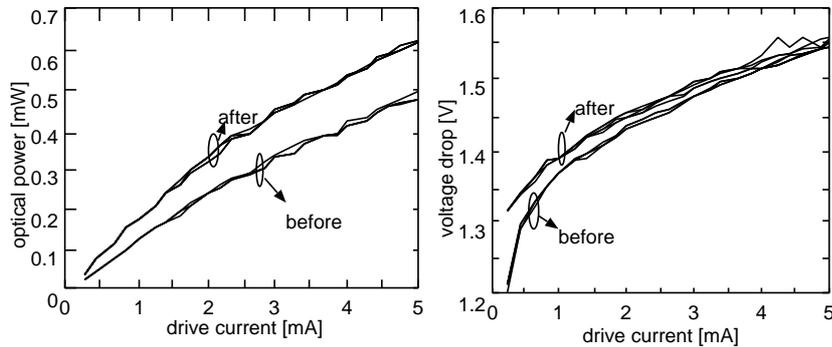
Figure 4.12: Measured voltage characteristics (left) and optical power characteristics (right) of substrate-removed 980-nm RCLEDs before and after the removal of the substrate.

Figure 4.12 shows the measured power and voltage characteristics of 980-nm RCLEDs, before and after the substrate removal. The device structure includes a 500 nm $Al_{70}Ga_{30}As$ etch stop layer and a 2 μm thick mechanical stabilisation layer. The use of 980 nm RCLEDs has the advantage that the optical properties can be measured before and after the removal process. It is found that the efficiency increases, due to the absence of the absorption in the substrate and the absence of the reflections at the backside, but in spite of the multi-modal character of the cavity. The voltage drop across the RCLED increases slightly. The uniformity of the RCLED properties over the array before and after the substrate removal is comparable.

4.3.4   Design of the 850-nm active region

An active region emitting at 850 nm had to be developed, based on GaAs quantum wells and AlGaAs confinement layers. The design of the first 850-nm RCLED used 10 nm thick GaAs quantum wells, with 8 nm $Al_{20}Ga_{80}As$ barriers in between, and $Al_{20}Ga_{80}As$ as the cavity spacer material. This design was based on reference [57], in which top-emitting 850-nm RCLEDs were realised using an MBE growth technique. The performance of our devices, based on this active layer, was extremely bad. This was attributed to the small carrier confinement (due to the small bandgap difference between the well material and the barrier material). This was confirmed by the simulation of the recombination rate in the active region, using the SimWindows software tool [82]. Figure 4.13 shows the radiative recombination rate as a function of the current density, for different spacer compositions. The recombination rate decreases if the aluminium concentration of the spacer layer is smaller than 40 %. According to this software tool, an $Al_{40}Ga_{60}As$ spacer results in a sufficiently high
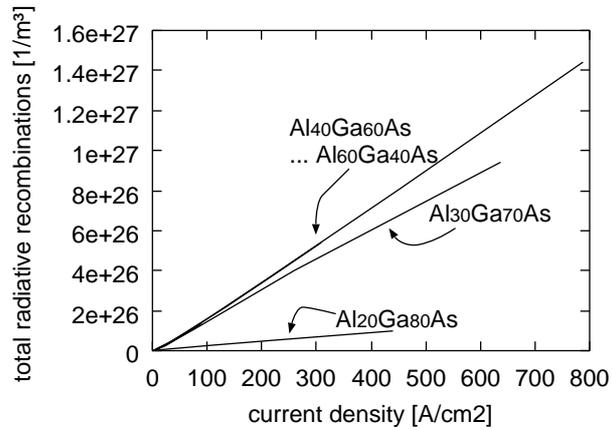
Figure 4.13: Calculated radiative recombination rate of 850-nm active regions, as a function of the spacer material (using SimWindows).
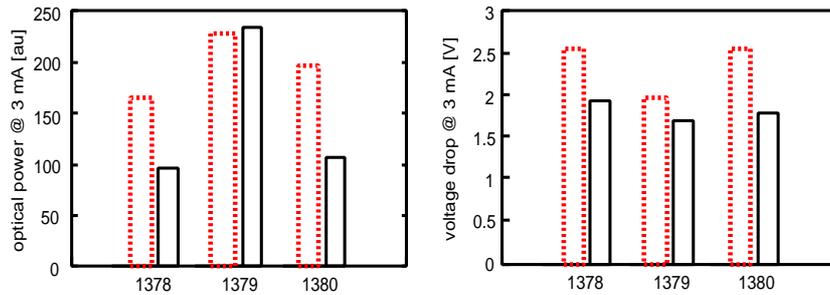
Figure 4.14: Comparison of the different 850-nm active regions (defined in table 4.5), before substrate removal (processed as top emitter, dashed lines), and after substrate removal (full lines).

energy barrier to confine the carriers[6].

In the following tests, $Al_{40}Ga_{60}As$ was chosen as the spacer material. The barrier material between the wells remained $Al_{20}Ga_{80}As$. Using this active region, both bottom- and top-emitting RCLEDs were realised. The top-emitting RCLEDs performed well (see next paragraph). However, there was no improvement of the optical properties of the bottom-emitting RCLEDs. This was explained by the combination of the short distance between the active region and the metal mirror, and the small carrier confinement (the energy barrier

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[6]In literature, efficient devices with a 20% aluminum concentration in the barriers have been presented. This is in disagreement with the presented simulations. However, the devices were 'long diodes', whilst the diodes studied in this work are 'short diodes', at least at the p-side, where the distance from the wells to the metal contact is only a few hundred nanometer. It is believed that this explains the difference.

run nr	well	barrier	well-spacer interface	upper spacer
1378	8 nm GaAs	10 nm $Al_{20}Ga_{80}As$	20 nm $Al_{20}Ga_{80}As$	50 nm $Al_{40}Ga_{60}As$
1379	8 nm GaAs	10 nm $Al_{20}Ga_{80}As$	20 nm $Al_{20}Ga_{80}As$	170 nm $Al_{40}Ga_{60}As$
1380	8 nm GaAs	10 nm $Al_{20}Ga_{80}As$	2 nm $Al_{20}Ga_{80}As$	50 nm $Al_{40}Ga_{60}As$

Table 4.5: Overview of the layer structure of different active regions at 850 nm.

is still too small). In the next tests, a larger confinement, using $Al_{60}Ga_{40}As$ spacer material, was used. This is not an optimal solution, due to the important difference in lattice constant between the well and the spacer material, and due to the large difference in growth temperature of both materials. Therefore, a small $Al_{20}Ga_{80}As$ barrier was included between the well and the spacer. Finally, three different active layers were grown, in which both the interface layer between the well and the spacer, and the thickness of the spacer layer between the well and the material were varied. The composition of the active regions is summarised in table 4.5.

The optical and electrical properties of all three devices are summarised in figure 4.14. The efficiency before the substrate removal was measured by processing the structure as a top-emitting RCLED, using a fast processing technique (the metal top mirror was omitted in this processing, and a simple ring contact was used to inject the current). It was found that the best active region has a thick spacer between the active region and the metal mirror, and a rather thick interface layer between the well and the spacer.

4.3.5 Measurements on 850-nm bottom-emitting RCLEDs

The layer structure of the 850-nm bottom-emitting RCLEDs is given in table 4.6. In comparison to the 980-nm bottom-emitting RCLEDs, the layer structure is altered in two ways: a mechanical stabilisation layer is included to improve the yield of the substrate-removal process, and a thick spacer layer is used to improve the internal quantum efficiency. Both adaptations result in an increase of the effective cavity length, and a decrease of the extraction efficiency.

Figure 4.15 shows the measured optical power on 850-nm substrate-removed RCLEDs. The 850-nm RCLEDs with mechanical stabilisation layer have an overall efficiency of 7 %. If the mechanical stabilisation layer is also removed, the overall efficiency increases to 9 %, but the yield of the array decreases. In the latter case, the coupling to a small-core POF is also shown. A coupling efficiency of 10 μW/mA was found.

4.4 Realisation of top-emitting RCLEDs emitting at 850 nm

In parallel with this work, several 850-nm top-emitting RCLEDs were reported. Work done in Lausanne lead to a large RCLED with an epoxy lens (see refer-

thickness	material	doping level	remarks
20 nm	GaAs	p-doped	contact layer
40 nm	GaAs->$Al_{60}Ga_{40}As$	p-doped	graded
173.5 nm	$Al_{60}Ga_{40}As$	p-doped	spacer
21 nm	$Al_{60}Ga_{40}As$	11 nm p-doped	spacer
		10 nm intrinsic	spacer
20 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
20 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
21 nm	$Al_{40}Ga_{40}As$	10 nm intrinsic	spacer
		11 nm n-doped	spacer
50.7 nm	$Al_{15}Ga_{85}As$	n-doped	DBR
20 nm	$Al_{15}Ga_{85}As$ -> $Al_{95}Ga_{05}As$	n-doped	current window
48.85 nm	$Al_{95}Ga_{05}As$	n-doped	current window
20 nm	$Al_{95}Ga_{05}As$ -> $Al_{15}Ga_{85}As$	n-doped	current window
50.7 nm	$Al_{15}Ga_{85}As$	n-doped	DBR
67.8 nm	$Al_{85}Ga_{15}As$	n-doped	DBR
2x (60.7 nm	$Al_{15}Ga_{85}As$	n-doped	2-pairs $Al_{15}Ga_{85}As$/AlAs DBR
69.3 nm)	AlAs	n-doped	
2003 nm	$Al_{15}Ga_{85}As$	n-doped	mechanical stabilisation
500 nm	$Al_{70}Ga_{30}As$	n-doped	etch stop layer
	GaAs		buffer layer

Table 4.6: Layer structure of bottom-emitting 850-nm RCLED with etch stop layer and stabilisation layer.

Figure 4.15: Measured optical-power characteristics of 850-nm substrate-removed RCLEDs: overall optical power in air and optical power coupled to a small-core plastic optical fibre (fibre diameter is 62 μm).

ence [83]). The device was optimised for use in IRDA applications. Efficiencies up to 20 % (including the epoxy lens, which enhances the extraction efficiency) were reported.

4.4.1   Design of the layer structure

The top-emitting RCLED consists of a highly reflective DBR bottom mirror, and a moderately reflective top DBR. Because of its high absorption at 850 nm, the use of GaAs layers in the cavity was minimised. Therefore, an $Al_{15}Ga_{85}As/AlAs$ DBR was used instead of the standard GaAs/AlAs DBR. The back mirror consists of 20 DBR pairs, the corresponding optical power reflection at 850 nm is 96 %. The active layer was placed in a separate confinement structure, at the anti-node position of the internal standing wave pattern in the cavity. An $Al_{40}Ga_{60}As$ spacer was used. The front mirror was an $Al_{15}Ga_{85}As/AlAs$ DBR in combination with the semiconductor-air interface.

Simulations using the numerical tool were done to determine the cavity parameters for maximal extraction efficiency (this includes number of DBR pairs in the front mirror and thickness of the cavity). The calculated maximal extraction efficiency into air was found to be 17.8 %. The corresponding front mirror has 1.5 DBR pairs, and the cavity resonance wavelength is 858 nm (8 nm detuning). When the extraction efficiency is maximised for coupling into the numerical aperture of a Plastic Optical fibre (NA=0.5), the corresponding front mirror has 1.5 DBR pairs, and the cavity resonance wavelength is 851 nm (1 nm detuning) while the extraction efficiency into NA=0.5 is 5.8 %. A standard planar LED has an extraction efficiency into NA=0.5 of about 0.5 %. This means that the microcavity effect increases the extraction efficiency by a factor 10.

The layer structure is summarised in table 4.7. A GaAs top layer was in-

thickness	material	doping level	remarks
58.7 nm	GaAs	p++ doped	contact layer/DBR
69.3 nm	AlAs	p-doped	DBR
60.7 nm	$Al_{15}Ga_{85}As$	p-doped	DBR
21 nm	$Al_{40}Ga_{60}As$	11 nm p-doped	spacer
		10 nm intrinsic	spacer
20 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
6 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
10 nm	GaAs	intrinsic	QW
20 nm	$Al_{20}Ga_{80}As$	intrinsic	barrier
21 nm	$Al_{40}Ga_{60}As$	10 nm intrinsic	spacer
		11 nm n-doped	spacer
20x (60.7 nm	$Al_{15}Ga_{85}As$	n-doped	20-pairs $Al_{15}Ga_{85}As$/AlAs DBR
69.3 nm)	AlAs	n-doped	
	GaAs		buffer layer

Table 4.7: Layer structure of the 850-nm top-emitting RCLED.

cluded, to allow for a good electrical contact. The outcoupling mirror has fewer DBR pairs compared to the bottom-emitting RCLED (1.5 compared to 5 pairs). This is explained by the highly reflective semiconductor-air interface at the top DBR. This extra reflection has an important influence on the total reflection of the DBR. This interface is not present in the outcoupling DBR of the bottom-emitting 980-nm RCLEDs, implying that more DBR layers are necessary to obtain the desired reflection. The smaller top DBR of the top-emitting 850-nm RCLED results in a thinner current spreading layer, which might result in a large series resistance and a non-uniform current injection profile. This is the case for 650-nm RCLEDs, where a thicker current injection layer is included to improve the electrical behaviour of the RCLED. Unfortunately, this reduces the extraction efficiency of the device.

The theoretical performance of the top-emitting RCLEDs is smaller compared to bottom-emitting RCLEDs. This is explained by the large penetration depth of the highly reflecting rear DBR mirror. In the previous chapter, it was shown that the cavity bandwidth decreases as a function of the penetration depth of the mirror (see equation 3.25). This implies that the reflection of the mirrors must be smaller to set the cavity bandwidth equal to the bandwidth of the intrinsic spontaneous emission. And the smaller reflection decreases the maximal enhancement, as shown in equation 3.24.
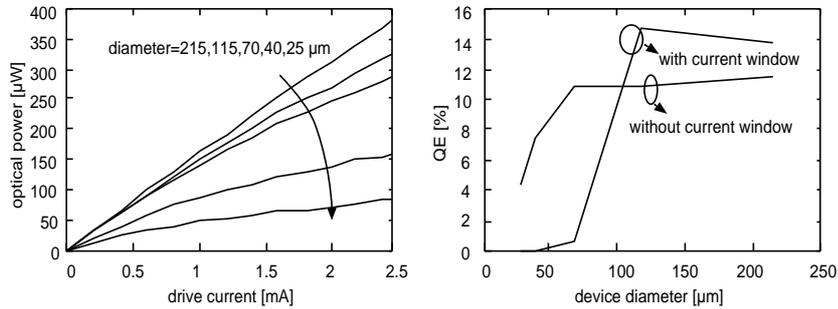
Figure 4.16: Measuremed optical power of top-emitting 850-nm RCLEDs without current-confining window as a function of the drive current, for different device diameter (left), and measured quantum efficiency of top-emitting 850-nm RCLEDs with and without current-confining window (as a function of the device diameter, right).

4.4.2 Realisation of the devices

The devices are grown in an MOCVD system on n-GaAs substrates. The processing started with the wet etching of mesa structure. Afterwards, the selective oxidation of the current window was done, up to 10 μm deep. This current window is included in the design to reduce the current injection under the metal contact. In this way, no light is generated under the contacts, which should result in an increased efficiency. This oxidised aperture has, unlike in VCSELs, no optical function, because the opening of the aperture is much larger than the wavelength of the light emission. For comparison, samples without oxidised current windows have also been processed. Finally an isolation layer and the metal contacts were deposited.

4.4.3 Measurements

The maximum quantum efficiency into air of the RCLEDs without current window is 11.7 %, the devices with a current window show an overall QE of 14.6 % (device diameter is 200 μm). Epoxy lenses would even increase this efficiency. The efficiency of the RCLEDs without current window decreases for small diameters, because the ratio of the emitting area to the area of the mesa decreases: relatively more light is generated under the metal contact, and is consequently lost. As expected, the efficiency of the RCLEDs with oxidised current window is larger, but only for the largest devices. The smallest devices have a very poor overall QE.
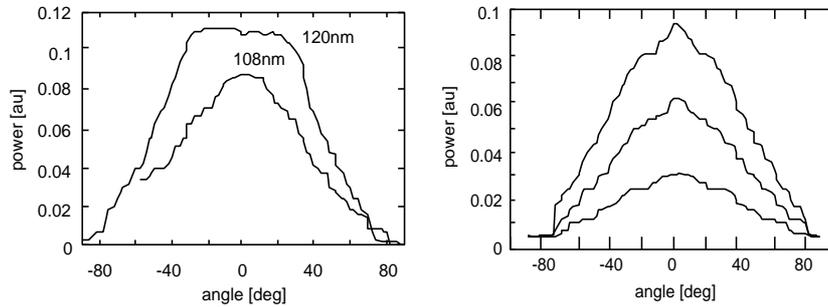
Figure 4.17: Measured far-field pattern of flip-chip mounted RCLEDs, as a function of the cavity detuning (for 85-μm RCLEDs with a 105 μm and 120 μm thick spacer layer, left) and as a function of the drive current (for a 85-μm RCLED, driven at 1, 3 and 5 mA, right)

4.5   Measurements on RCLEDs

In this section, the measurements of some characteristics that are not directly related to the extraction efficiency are presented: the far-field pattern, the coupling efficiency to fibres and the voltage characteristics.

4.5.1   Far-field pattern

The far-field pattern is related to the cavity detuning, as was discussed in paragraph 3.7.2. An overtuned cavity, in which the cavity resonance wavelength is slighter larger than the intrinsic emission wavelength, has a larger extraction efficiency and a broad, double-lobed far-field pattern (the rabbit ears, or the butterfly pattern). Calculations have shown that the cavity, optimised for maximal efficiency into the NA of 0.5, has a far-field pattern comparable to a Lambertian emitter. Nevertheless, a larger coupling efficiency to an NA of 0.5 was found for the RCLED (40 % compared to 25 % for a Lambertian emitter). This is explained by the smaller power emitted at very skew angles (> 60°) in case of the RCLED. The influence of the detuning onto the far-field pattern is shown in figure 4.17, in which the measured far-field pattern of two RCLEDs with different cavity thickness (and thus a different resonance wavelength) is shown. The thinnest cavity has a narrow far-field pattern, as expected from theory.

The measured far-field pattern of flip-chip mounted RCLEDs is shown in figure 4.17. There is an extra emission peak, centred around the vertical axis. This peak origins from light which is emitted next to the metal mirror. Due to the absence of the metal mirror, the cavity resonance is shifted towards shorter wavelengths. The corresponding detuning results in the emission of a very narrow far-field pattern, which is added to the emitted far-field pattern of the metal-covered part of the RCLED. There is thus some emission next to the mir-
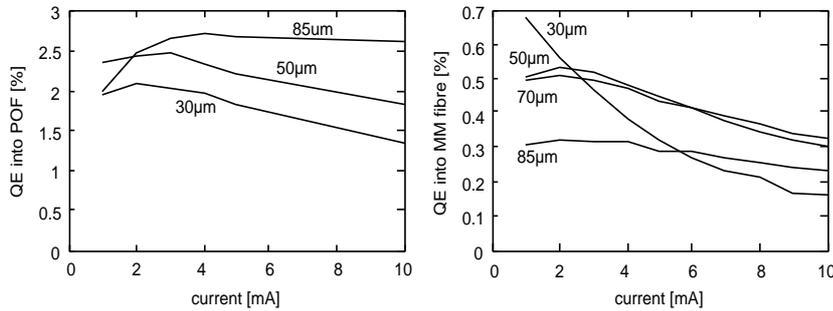
Figure 4.18: Measured coupling efficiency to a fibre as function of the drive current, for a plastic optical fibre (left) and for a glass multi-mode fibre (right), for different device diameters.

ror, due to the current spreading and the lateral carrier diffusion. Although this peak seems rather important on the figure, it represents only a very small amount of light. The solid angle in which this extra light is emitted is very small.

4.5.2 Coupling to a fibre

In this work, the coupling from RCLEDs to different fibres was investigated experimentally. The RCLEDs were flip-chip mounted on a glass substrate and the fibre was aligned to the RCLED using a translation stage. Using this set-up, the coupling efficiency was measured as a function of fibre diameter and drive current. Different fibres have been used: Plastic Optical Fibre (POF) and multi-mode glass fibre. A difficulty in the coupling experiments with the POFs is the repeatability of the fibre facet quality. A hot knife technique was used, followed by a polishing step, to obtain smooth POF surfaces. More information on the preparation of the POF facet can be found in [88] and [89]. Firstly, the absorption losses of the POF were measured, using the cut-back method. The measured absorption loss of the POF is about 12 dB/m, independent of the diameter of the fibre.

The measured overall quantum efficiency at 3 mA drive current into a 125 μm diameter POF (POF core diameter is 120 μm) is 2.8 %. This corresponds to a POF-coupled power to current ratio of 35 μW/mA. A value of 3.7 % was expected from the numerical integration of the measured far-field pattern. The difference can be explained by the Fresnel losses at the POF-air interface (about 4 %) and scattering at the non-perfect fibre facet.

Figure 4.18 shows the measured quantum efficiency into fibre for different RCLED diameters. This expresses the ratio between the number of injected carriers in the devices, to the number of photons coupled into the fibre. In case of coupling to a plastic fibre (core diameter is 120 μm, numerical aperture NA=0.5), the highest quantum efficiency (2.8 %) is obtained for a rather large
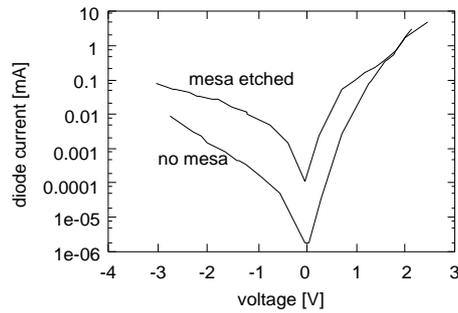
Figure 4.19: Measured voltage characteristics of 50 μm RCLEDs, with and without an etch through the active layer. The device with an etched mesa shows a larger current at low and inverse voltages, indicating important effects at the edge of the mesa.

RCLED diameter. In case of a glass fibre (core diameter is 62.5 μm, NA=0.2), the highest coupling is obtained for much smaller RCLEDs (30 μm). Not all light from the larger RCLED is coupled into the fibre, due to the size difference between the RCLED and the fibre core.

The coupling efficiency of RCLEDs with oxidised mirrors to plastic optical fibres was also investigated, and an efficiency of 1.3 % was found for a 120-μm POF with a numerical aperture of 0.5. In theory, a larger value was expected. This is explained by the detuning of the cavity (see section 3.7.2). Therefore the coupling efficiency could only be estimated. An overall efficiency into the POF was estimated at 3.5 %.

4.5.3 Voltage characteristics and wall-plug efficiency

The series resistance of 980-nm RCLEDs with an AlAs/GaAs DBR at 3 mA is 48 Ω for the 20-μm RCLED, 35 Ω for the 32-μm RCLED and 30 Ω for the 50-μm RCLED. The voltage drop across the devices is small. The series resistance of 980-nm RCLEDs with an AlO$_x$/GaAs DBR is larger, with values varying from 120 to 200 Ω. This is related to the lateral current spreading from the n-contact towards the active region.

The voltage characteristic gives more information on the device performance. For example, figure 4.19 shows the absolute value of the measured current (on a logarithmic scale) as a function of the applied voltage, for a RCLED with and without an etched mesa through the active layer. The current is larger in case of an etched mesa structure, indicating the existence of surface recombination effects. However, at large forward biases, the current is mainly determined by the (radiative) diode current, which increases faster as a function of the voltage.

This plot clearly shows the influence of the etched mesa structure around the RCLED. Fortunately, the parallel current is much smaller than the radiative

type	λ	DBR	EE total	EE NA=0.5
bot	980 nm	AlAs/GaAs	22.4 %	7.6 %
bot	980 nm	AlO_x/GaAs	23.3 %	7.3 %
bot	850 nm	AlAs/AlGaAs	18.6 %	6.3 %
top	850 nm	AlAs/AlGaAs	17.8 %	5.8 %

Table 4.8: Calculated extraction efficiency (EE) in full NA and in NA=0.5, of different RCLED structures.

type	λ	DBR	substr ?	overall eff.	diameter	remark
bot	980 nm	AlAs/GaAs	yes	13.4 %	50 μm	
bot	980 nm	AlO_x/GaAs	yes	6.4 %	50 μm	40 nm detuning
bot	850 nm	AlAs/AlGaAs	no	9.0 %	50 μm	
top	850 nm	AlAs/AlGaAs	yes	14.7 %	200 μm	

Table 4.9: Measured characteristics of different RCLED structures.

diode current.

4.6 Conclusion

In this chapter, the design, realisation and characterisation of highly efficient RCLEDs was discussed. The conclusions are summarised in table 4.8, in which the calculated extraction efficiencies of different RCLED structures are presented. The RCLEDs with the highest efficiency consist of a high-contrast DBR and a metal mirror. Other configurations have a smaller efficiency, due to the increased penetration depth of the mirrors. Table 4.9 shows the measured results, for RCLEDs during this work. There is a reasonable agreement between the calculated extraction efficiency and the measured overall efficiency, if the different non-idealities (such as the undesired cavity detuning and absorption losses in the substrate) are taken into account.

The presented processing scheme for RCLED arrays, suitable for flip-chip mounting, allows to realise highly efficient light emitters. However, there are some indications that the lateral carrier diffusion affects the efficiency: this is visible in the far-field pattern, and in the measured voltage characteristics. Furthermore, it was found that 850-nm RCLED arrays require (too?) many adaptations to the layer structure, resulting in a decreased extraction efficiency. 850-nm RCLEDs with an excellent performance have been realised, indicating that the intrinsic quality of the 850-nm active regions is good.

Chapter 5

Advanced characteristics of RCLEDs

In this chapter, some more advanced properties of the realised RCLEDs will be discussed, as the thermal behaviour of the devices, the scaling properties of the RCLEDs and the yield and the uniformity of the devices.

5.1 Thermal properties of RCLEDs

The thermal properties of RCLEDs are very important in almost all applications. They determine the operation temperature range of the component. It is believed that LEDs have a better temperature behaviour compared to lasers, especially VCSELs. In this section, a detailed study of the thermal behaviour of RCLEDs is performed.

5.1.1 Influence of temperature on the efficiency

The efficiency of RCLEDs is determined by the internal quantum efficiency and the extraction efficiency (the injection efficiency is assumed to be 100 %). Both factors determine the temperature behaviour of the output power of the device:

$$P_{out} = \frac{h\nu}{q} \eta_{int}(T) \eta_{extr}(T) I_{inj}$$

The internal quantum efficiency decreases as a function of the temperature, due to the increased non-radiative recombinations and the increased carrier overflow. In the literature, the internal quantum efficiency is presented as an exponential function, decreasing with temperature. It is possible to define a characteristic temperature T_0, as given in equation 5.1. This characteristic temperature is frequently used to described the temperature dependency of light
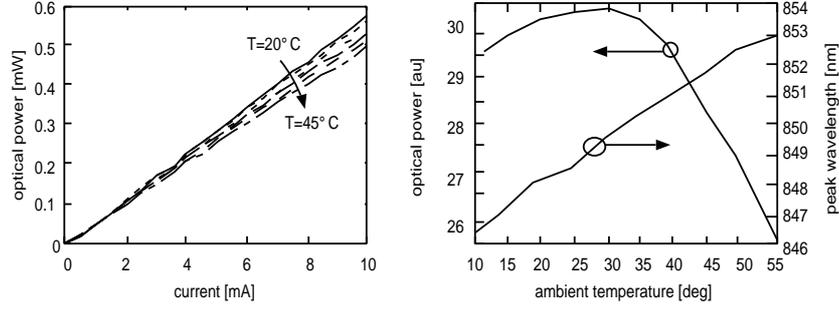
Figure 5.1: Measured output power characteristic of a 980-nm RCLED, as a function of the ambient temperature (left) and measured optical power and peak wavelength of an 850-nm RCLED, as a function of the ambient temperature (right).

emitting devices. In practice, the temperature behaviour is not exactly given by an exponential decreasing function, and the characteristic temperature is not a constant. Nevertheless, the parameter can be used to compare the influence of the ambient temperature at room temperature.

$$\eta_{int} = \eta_{int,0} \exp\left(-\frac{T}{T_0}\right) \Rightarrow \frac{1}{\eta_{int}}\frac{d\eta_{int}}{dT} = -\frac{1}{T_0} \tag{5.1}$$

The extraction efficiency depends on the temperature, because the intrinsic spontaneous emission wavelength and the cavity resonance wavelength shift as a function of the temperature, both at a different rate. This results in a temperature-dependent detuning, and thus a temperature-dependent extraction efficiency. The temperature coefficient of the emission wavelength is about 0.33 nm/K for GaAs and InGaAs based active layers [85]. The main mechanism of this shift is the decrease of the bandgap. The cavity resonance wavelength also shifts towards long wavelengths, but at a slower rate. This shift is caused by the thermal expansion and the change of the refractive index of the materials. In the AlGaAs material system, the thermal expansion is the most important parameter. As a result, the cavity resonance peak shifts at 0.087 nm/K [85].

The temperature dependency of the internal efficiency and the extraction efficiency of RCLEDs is therefore given by:

$$\eta_{int}\left(T\right) = \eta_{int,0} \exp\left(-\frac{T}{T_{0,int}}\right)$$
$$\eta_{extr}\left(T\right) = \eta_{extr,0} \exp\left(-\frac{(\lambda_{SE}(T) - \lambda_{cav}(T))^2}{\Delta\lambda_{SE}^2 + \Delta\lambda_{cav}^2}\right) \tag{5.2}$$

It is possible to choose the detuning of the microcavity to minimise the temperature coefficient of the RCLED. If the cavity resonance wavelength is chosen larger than the intrinsic spontaneous emission wavelength, then the detuning
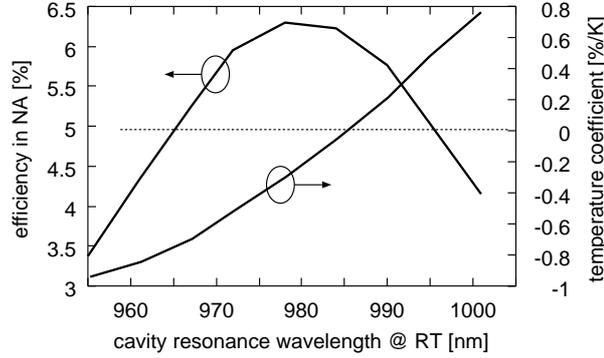
Figure 5.2: Calculated extraction efficiency and calculated temperature coefficient of the extraction efficiency (at room temperature) of 980-nm RCLEDs optimised for coupling to a limited NA, as a function of the cavity resonance wavelength at room temperature.

will initially decrease as a function of the temperature, resulting in an increasing extraction efficiency. This increasing extraction efficiency can compensate for the decrease of the internal quantum efficiency. This is only valid for a limited temperature range. At large temperatures, the emission wavelength will become larger than the cavity resonance, and the extraction efficiency starts to decrease again. This is shown in figure 5.1, where the measured optical power of 850-nm RCLEDs initially increases as a function of the temperature, but finally starts to decrease. Unfortunately, the undertuning results in a smaller extraction efficiency at room temperature and a broad emission profile. Figure 5.2 shows the calculated efficiency at room temperature, and the temperature coefficient of the extraction efficiency as a function of the resonance wavelength. A large resonance wavelength at room temperature implies a positive temperature coefficient for the extraction efficiency.

5.1.2 Thermal dynamics

The temperature inside RCLEDs is determined by the ambient temperature T_{amb} and the internal heating. The internal heating depends linearly on the total power dissipation P_{diss} inside the RCLED. This linearity is described by a thermal resistance R_{th}. The power dissipation includes the ohmic heating in the series resistance of the device and the power dissipated by the non-radiative recombination processes. The junction temperature can be written as:

$$T_{junct} = T_{amb} + R_{th}P_{diss} = T_{amb} + R_{th}\left(R_{series}I_{LED}^2 + (1 - \eta_{wp})V_jI_{LED}\right)$$
(5.3)
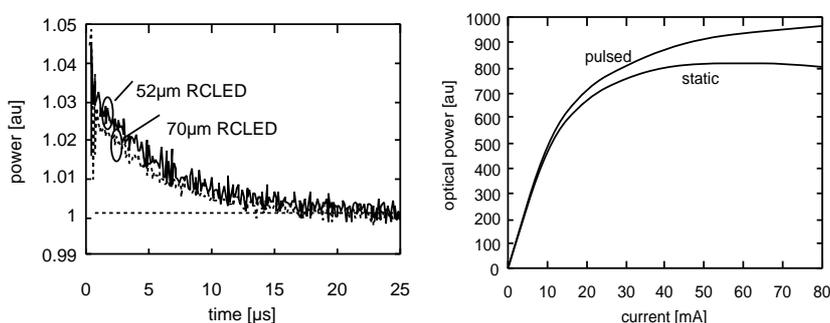
Figure 5.3: Measured temperature transient of two RCLEDs driven at 20 mA (left) and influence of pulsed operation on the output power of RCLEDs (right).

with η_{wp} the wall-plug efficiency, as defined in equation 3.18. This junction temperature determines the efficiency of the RCLED, as described in the previous paragraph. Equations 5.2 and 5.3 together determine the temperature inside the RCLED.

The internal heating of the RCLED occurs not immediately: it takes a while before the static temperature is obtained inside the device. This is described by a first-order system. Figure 5.3 shows the measured temperature transient, for 2 different RCLEDs driven by a stepwize current increase from 0 to 20 mA. There is a small optical overshoot, as the initial (cold) cavity has a better detuning and thus a larger extraction efficiency. The power dissipation heats up the device, and a regime is reached after 20 μs. Both devices have a similar thermal time constant. This effect can, in worst case, have a negative impact on the quality of the eye-diagram. However, in this case, the thermal overshoot is negligibly small, in particular at small drive currents. The same plot shows the output power of the RCLED, driven with a constant current source and with a pulsed current source. If the RCLED is driven by a pulsed current source, then more optical power is emitted (the measured optical power is corrected for the duty cycle of the pulsed current), because the internal heating is reduced. However, the increase of the optical power is only important at large drive currents (I > 50 mA).

5.1.3   Thermal cross-talk

Thermal cross-talk in arrays is defined as the decrease of the efficiency of a RCLED, due to the heating generated in a neighbouring RCLED[1]. The thermal cross-talk was evaluated experimentally by measuring the change of the optical power of a RCLED when a neighbouring RCLED is driven, as a function of the distance to that neighbouring RCLED. The heating of the neighbouring

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[1]The thermal crosstalk can also be induced by the environment (as the driver circuit). This is not treated in this paragraph.
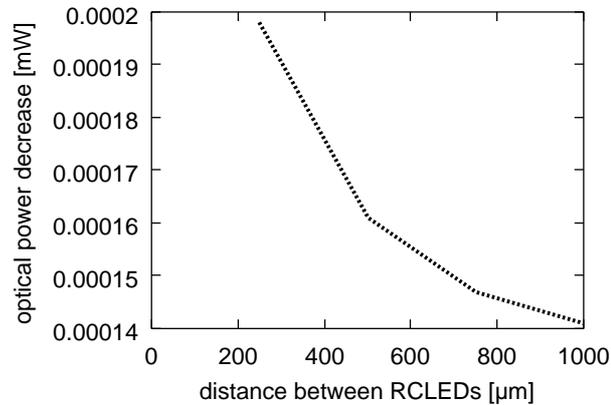
Figure 5.4: Measurement of the thermal cross-talk of 50 μm RCLEDs on a 350 μm thick GaAs substrate, as a function of the distance between the components.

RCLED causes a temperature increase in the RCLED and thus a decreased efficiency. As a result, the efficiency of the RCLED increased as a function of the distance to the neighbouring RCLED.

This thermal cross-talk was determined for 980-nm RCLEDs, flip-chip mounted onto a glass carrier, with a thick GaAs substrate (the substrate was not removed). A cross-talk coefficient Υ (defined as $P = P_0(1 - \Upsilon I)$, with I the current through the neighbouring RCLED) was measured: $\Upsilon = 1.9$ A^{-1} for 250 μm RCLED distance (RCLED device diameter was 50 μm). This cross-talk coefficient depends on the distance to the neighbouring RCLED. The following expression fits the measurements reasonably well:

$$\Upsilon = \left(\frac{3150}{R[\mu m]} \right)^{0.25}$$

Even at 10 mA, the decrease in optical power due to the thermal cross-talk between 2 neighbouring RCLEDs is only 0.2 %. The relative decrease of the efficiency is under 2 %, even if all nearest neighbouring RCLEDs are in the on-state. As a conclusion, this type of cross-talk is negligible for standard RCLED arrays, driven at a small current (typically a few mA). This cross-talk will be even smaller for RCLEDs with a thinned substrate, or a removed substrate, as the lateral thermal resistance increases.

5.2 Scaling properties

An important feature of RCLEDs is their scaling behaviour. This is related to the saturation power of RCLEDs. In this section, an empirical study of the scaling behaviour is presented.

5.2.1   One-dimensional analysis

In the simplest approach, a one-dimensional model for RCLEDs can be used. All characteristics and parameters are expressed per unit of area. For example, current densities are used in stead of the current. In that case, the output optical power per unit of emitting area is given by:

$$\frac{P}{A} = \frac{h\nu}{q}\eta_{int}\left(J,T\right)\eta_{extr}\left(J,T\right)J$$

The emitted power per unit area is determined by the current density and the temperature. The temperature depends on the ambient temperature, and the self-heating of the device (which depends on the generated power and the thermal resistance towards the environment). This is based on equation 5.3, as was derived in the previous paragraph:

$$T = T_{amb} + R_{th}P_{diss} = T_{amb} + \rho_{tot}d_{tot}\left(1 - \eta_{wp}\left(J,T\right)\right)V_j\left(J,T\right)J$$

with ρ_{tot} the thermal resistivity and d_{tot} the total thickness of the material between the active layer and the thermal environment. These two equations determine the efficiency of the device. Unfortunately, this set of equations has no closed-form solution. Figure 5.5 shows the calculated temperature increase and output optical power as a function of the current density, for different values of the thermal resistance. The extraction efficiency was chosen as 5 %, a plausible value for the extraction efficiency into a POF. The typical saturation power density is a few μW/μm^2, but it depends strongly on the thermal impedance. For example, the thermal conductivity of GaAs is 0.81 W/cm°C. Assume that the substrate (500 μm thick) is glued on an ideal heat sink (with a good thermally conductive glue). The corresponding thermal resistance is given by 0.062 K/W. This corresponds to curve (c) in figure 5.5. According to this model, the maximal power in a large core POF (diameter 500 μm, assuming that the RCLED has the same diameter) is given by 30 mW, the corresponding drive current is 3 A.

5.2.2   Experimental results

Figure 5.6 shows the measured saturation of the optical power of 980-nm RCLEDs, for different device diameters (ranging from 300 μm to 10 μm). The saturation power density is a few μW/μm^2, in agreement with the calculation presented in the previous paragraph. This implies that the maximal output power of small RCLEDs is limited to a few hundreds μW. The relation between the efficiency and the current density does not depend on the device diameter (see figure 5.6).

There is a slightly larger efficiency than expected for very small diameters (diameter is 10 μm). This can be explained by two factors: the average carrier density in the active region is smaller than expected (due to diffusion), or the thermal resistance is smaller (due to the lateral spreading of the heat). In
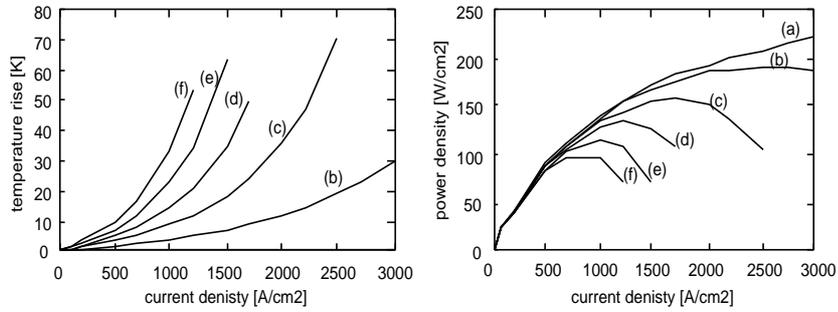
Figure 5.5: Temperature increase and emitted optical power density as a function of the current density, for different values of the thermal impedance of RCLED towards its ambient (a)=0K/W, (b)=0.02K/W, ... (f)=0.1K/W.
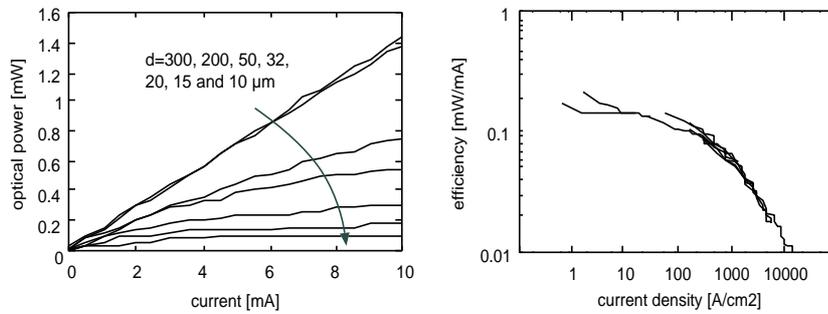
Figure 5.6: Measured optical power for RCLEDs with different diameters, and measured efficiency as a function of the current density for the same 980-nm RCLEDs.

conclusion, it is found that the saturation is mainly determined by the increase of the carrier density (resulting in a reduced microcavity enhancement) and thermal effects.

5.3   Uniformity, yield and reliability of RCLEDs

5.3.1   Uniformity of RCLED and RCLED arrays

The uniformity of the RCLED characteristics over an array is very important. For example, all channels in the parallel link should behave similarly, because there is no room for a feedback circuit for every channel in the system. Moreover, cost-effective production of the arrays asks for highly uniform devices over the full wafer.

During the realisation of the component, several parameters can deviate from the design value:

- the thickness of the layers in the stack, and the composition of the material can change slightly from run to run, or even on the same wafer. This determines both the cavity resonance wavelength and the intrinsic emission peak wavelength. The on-wafer variation is typically under one percent. This problem is solved by optimisation of the layer growth technique. For example, the VCSEL growth process at Honeywell - the largest VCSEL producer in the world - is being continuously optimised. In 1996, the standard deviation on the cavity peak wavelength on a single wafer was 14 nm, in 1997 it was 5 nm, and in 1999 it was 1.5 nm [86].

- small deviations during the processing can have an influence on the dimensions of the device. This includes the dimensions of etched moats or the depth of the selectively oxidised AlAs layers. These factors can lead to important variations on the lateral dimensions of the devices.

The uniformity over a quarter wafer was measured, both the optical efficiency and the reflection wavelength is shown in figure 5.7. The variation of the optical power over the wafer is within +/- 5 %. The variation within a single 8×8 array is even smaller. There is some deviation towards the edge of the wafer, where the efficiency is slightly larger. This is explained by the fact that the layers are thicker at the border of the wafer. This was confirmed by the spectral measurements.

5.3.2   Yield of RCLED arrays

Reliability is of extreme importance for the RCLED in commercial applications: the number of failures should be extremely small. In general, failures can be divided into two categories: freak failures, leading to a fast death, and wear-out failures. Freak failures are caused by several factors, as mechanical damage during processing or epitaxy layers with a bad quality. The number of freak
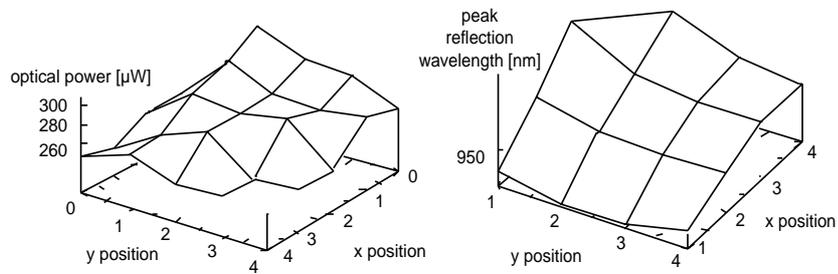
Figure 5.7: Measured uniformity of the emitted optical power over a quarter wafer (left, at 3 mA) and the peak reflection wavelength of the unprocessed layer structure at the same locations over a quarter wafer (right).
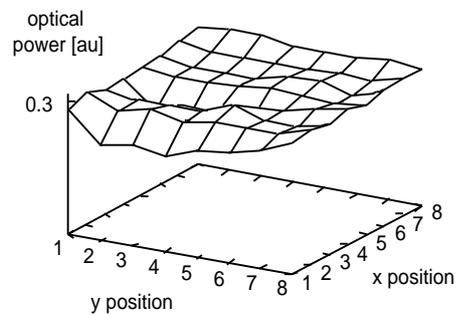
Figure 5.8: Measured uniformity of an 8×8 array of 980-nm RCLEDs (with a diameter of 50 μm), driven at 3 mA.
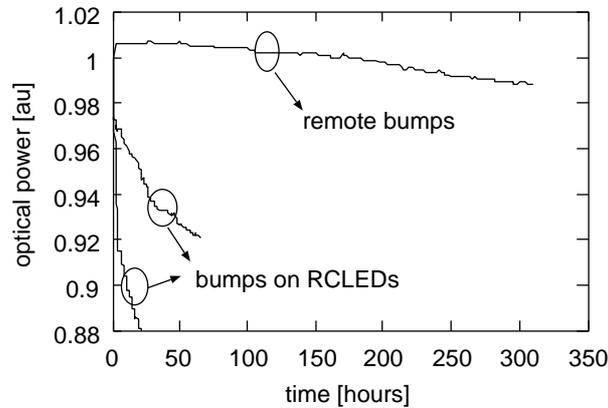
Figure 5.9: Long-term behaviour of flip-chip mounted 85-μm RCLEDs, driven at 10 mA, for different mounting techniques.

failures is related to the yield, this is the number of usable device to the total number of processed devices. Measurements in the previous paragraph showed that the yield of flip-chip mounted 8×8 arrays is 100 % (see figure 5.8). The number of wear-out failures is related to the lifetime of the devices. This will be discussed in the next paragraph.

5.3.3 Lifetime tests

The determination of the long-term behaviour of RCLEDs (as the mean time-to-failure, MTTF) is a very labour-intensive and time-consuming task. The lifetime of semiconductor light sources is typically large (up to millions of hours), thus an experiment to determine the mean lifetime takes at least of few times this period. This would take many years, and this is not practical. Two techniques are used to obtain better estimations of the lifetime on a shorter timescale. First, many devices could be tested in parallel. A failure of a few devices in the set allows to estimate the lifetime of the complete set. Secondly, tests could be carried out at elevated temperatures, to speed up the ageing of the devices ("accelerated ageing"-technique). The reliability can be calculated back to room temperature using the Arrhenius relation:

$$MTTF \sim \exp \frac{-kT}{E_{act}}$$

Experiments on VCSELs resulted in an activation energy E_{act} of 0.7eV [87]. It was found that the distribution of the lifetime of VCSELs can be described by a lognormal distribution: the natural logarithm of the time-to-failure is described by a normal distribution. This is described by two parameters: μ is the mean of the natural logarithm of the TTF, and σ is its standard deviation.

dose 1	dose 2	dose 3	dose 4	dose 5
161	690	1276	6216	12337

Table 5.1: Accumulated radiation total doses for the different irradiations, expressed in 10^3 Gy.

A reliable estimation of the mean lifetime of the RCLEDs can thus only be done by measuring many devices (over hundred) during many hours (over thousands) in a temperature-controlled environment. An academic environment has neither the time nor the resources for such experiments. However, a few experiments have been carried out, just to estimate the behaviour of the RCLEDs. Figure 5.9 shows the normalised output power of 3 RCLEDs over a few days. This shows the influence of the mounting technique on the device performance. Two of the RCLEDs had the flip-chip bumps directly above the active region, implying the presence of some mechanical stress in the device. This clearly has a bad influence on the longterm behaviour.

Next to the lifetime test, the optoelectronic components must withstand other tests to be qualified. These include thermal cycling, damp heat storage (e.g. 85 degrees C at 85 % humidity), and ESD sensitivity (withstand a certain charge at a certain initial voltage, 300 V for example, to simulate the discharge of a human being over the device). The test conditions are summarised in the 'Bell Core' standards.

5.4 Radiation hardness of RCLEDs

Optical interconnects has - among others - the advantage of being lightweight compared to metallic interconnections. This is a big advantage in space applications. However, the environment in space is very different compared to the earth surface : there is much more radiation present.

The influence of the radiation on the RCLEDs was measured in cooperation with the SCK·CEN in Belgium, Mol. The RCLEDs were irradiated using a 60Co radiation source, at a dose rate of 28.3 kGy/h. Table 5.1 summarises the accumulated total doses received by the RCLEDs in successive irradiation steps. After each irradiation step, the P-I characteristics of the RCLEDs were measured at room temperature in a radiation-free environment.

After an irradiation dose of $6.2 \cdot 10^6$ Gy, the larger diameter RCLEDs showed a significant burn-in period: the optical output power of the RCLEDs after the radiation was initially zero, and the output power increased linearly as a function of operation time. The power saturated at values proportional to the burn-in current. Figure 5.10 shows the measured output power as a function of time for 85-μm devices, at $6.2 \cdot 10^6$ Gy and $1.2 \cdot 10^7$ Gy. Smaller devices have a much shorter burn-in time. This could be related to thermal effects: smaller devices exhibit higher temperature increase, and thus faster annealing.

Figure 5.11 shows the evolution of the RCLED output power as a function of
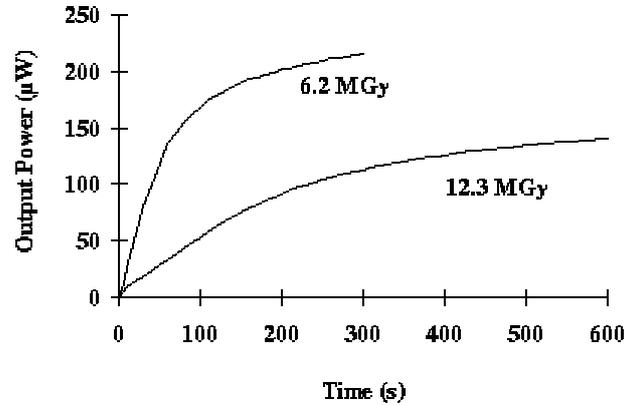
Figure 5.10: Output power of a 85-μm RCLED as a function of the operation time in an irradiation-free environment, after a irradiation of 6.2·106 Gy and 1.2·107 Gy. After this long irradiation, there is a significant burn-in effect.

total dose. These values were recorded after stabilisation of the output power. There is a trend towards increased loss as a function of the total dose rate, up to 13 % for the largest devices. The lower loss value recorded at $6.2 \cdot 10^6$ Gy is thought to be due to external influences. The application of RCLEDs in high gamma total dose environments is therefore not compromised, provided that burn-in effects are taken into account. These could be eliminated by biasing the RCLEDs during the irradiation.

5.5 Detection efficiency of RCLEDs

A device which can act both as a light emitter and as a light detector allows the realisation of truly bidirectional optical links, making the optical link more attractive. The RCLED contains a p-n junction, which can act as a light detector. In this paragraph, the detection efficiency of the RCLEDs will be discussed. Light of a flip-chip mounted RCLED was coupled to a multi-mode fibre, and the optical power through the fibre was measured using a power detector. Next, the fibre was aligned to a second RCLED, and the current through that detecting RCLED was measured. The RCLEDs have an etched mesa structure, and the inverse current is of the order of the detector current (see figure 4.19) . Therefore, no inverse biasing was applied to the detecting RCLED. Figure 5.12 shows the measured RCLED current as a function of the detected light. The quantum efficiency of the detecting RCLED decreases slightly as a function of the input current. This is a result of the heating in the emitting RCLED, which shifts the emission spectrum towards longer wavelengths. As a result, the overlap of the emitted spectrum and the filter characteristic of the detecting
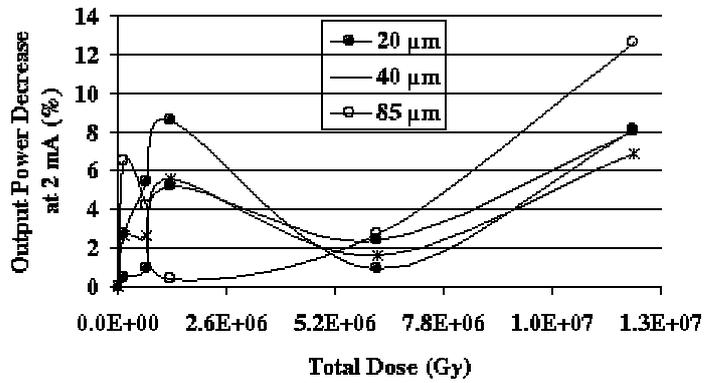
Figure 5.11: Evolution of the output power decrease at 2 mA as a function of total dose for 20-μm, 40-μm and 85-μm RCLEDs.
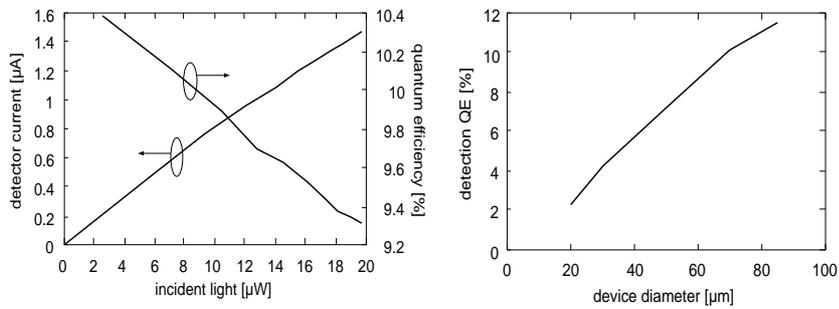
Figure 5.12: Measured detector current and quantum detection efficiency of a 70-μm RCLED, illuminated by a multi-mode glass fibre, as a function of the fibre-coupled power (left), and measured detection efficiency as function of the detector diameter (right).

RCLED decreases.

Although the measured quantum efficiency of the RCLED is not that small, it is still a factor 4 to 5 smaller than that of standard detector diodes. This is explained by the non-optimal cavity structure. Therefore, these devices are not applicable in the low-power inter-chip interconnections.

5.6 Conclusion

In this chapter, some advanced properties of RCLEDs were studied. Firstly, the temperature behaviour of RCLEDs was studied. It was found that the RCLED temperature influences both the internal quantum efficiency and the extraction efficiency of the device. The cavity detuning can be chosen so that the extraction efficiency increases initially as a function of the temperature, thereby compensating for the decreasing internal efficiency. However, this technique also reduces the efficiency at room temperature. Next, the internal heating and the thermal cross-talk in arrays were investigated. Both effects are negligible in inter-chip interconnect links, because the power dissipation in the individual devices is very small, due to the small drive current. Next, the scaling of RCLEDs towards small diameters was investigated. It was found that this is limited by the saturation of optical power, due to a broadening of intrinsic spontaneous emissions spectrum, and the temperature-dependent detuning. This depends strongly on the thermal impedance between the active region and the environment of the RCLED. The uniformity and yield of RCLEDs and RCLED arrays were discussed. It was found that these parameters depend strongly on the growth and processing technologies. Finally, advanced properties as radiation hardness and detection efficiency were measured.

Chapter 6

High-speed properties of RCLEDs

In this chapter, the high-speed properties of RCLEDs[1] are discussed. This chapter starts with a literature overview of high-speed LEDs. Next, the basic equations describing the LED dynamics are given, and some solutions are discussed. The theoretical results are compared to the measured speed response of RCLEDs, both using a current driver and a voltage driver. The small-signal response of RCLEDs is studied, and compared to measurements. Finally, several driving techniques for RCLEDs are compared.

6.1   Introduction

The speed response of RCLEDs and LEDs is comparable. Unfortunately, LEDs (and thus RCLEDs) are known as slow light emitters compared to lasers. The maximal modulation speed of the commercially available LEDs is typically a few tens up to a few hundreds Mbps, whilst the maximal modulation speed of lasers is typically a few up to a few tens Gbps. This slow response of LEDs is related to the large spontaneous emission lifetime. Typical values are a few nanoseconds. This spontaneous emission lifetime depends on the carrier concentration: larger carrier densities result in shorter recombination lifetimes. The obvious way to increase the modulation speed is to increase the current levels, by applying a biasing current. However, this approach results in an increased power dissipation. Several alternative approaches have been proposed:

- Firstly, small active regions can be used to increase the carrier density. This is easily achieved by using quantum wells as active region or by using small-diameter devices [90]. However, the output power of small LEDs is limited by saturation effects.

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[1]The results presented in this and following chapters are valid for both LEDs and RCLEDs, except explicitly mentioned.

- The carrier density inside the active region can be increased by doping the active region. This results in an increase of the carrier concentration, thus in a decrease of the spontaneous emission lifetime. However, this technique is limited by the introduction of 'killer centres'. If the semiconductor crystal is heavily doped, then the excessive incorporation of the doping atoms results in the creation of non-radiative recombination centres. These non-radiative recombination centres decrease the internal efficiency of the LED, which is not desirable. This effect depends on the particular doping atoms and on the growth conditions. Careful design can result in large (>1 GHz) modulation speeds without a significant decrease of the internal quantum efficiency [91][92]. As an alternative, selectively doped quantum-well active regions can be used, in which the doping is physically separated from the active region, but in which the free carriers can drift into the active region, increasing the carrier density [93]. These techniques have proven to be useful, but they require careful calibration of the growth conditions of the active region, which is beyond the scope of this thesis.

- As an alternative, the doping can be applied to decrease the non-radiative lifetime, decreasing the overall response time, but at the expense of a dramatically reduced efficiency [94][95][96]. This technique is used in commercial LEDs serving as a light source in long-wavelength fibre-optic transmission systems. Typical transmission speed is 622 Mbps. However, there is an important power penalty, making this technique completely useless for highly efficient RCLEDs.

- The structure of the diode can be altered, so that the injection and extraction of the carriers in the active region is accelerated. Several LED-types based on this principle have been proposed. In the tunnelling-barrier LED, the charge is accumulated before it tunnels into the active region [97][98]. Alternatively, a three-contact device can be used, similar to a bipolar transistor [99]. However, the efficiency of these devices is low, due to the many parallel current paths in the device.

- Finally, the speed of the LED can be increased by optimising the driver circuit. An example is the use of a pole cancellation circuit [100]. In this technique (also named 'active matching' [101]), the low pass filter characteristics of the LED is compensated by the pole cancellation circuit.

In this work, techniques for increasing the modulation speed without decreasing the efficiency will be discussed. But first, some general expressions for the speed behaviour of RCLEDs will be presented.

6.2 Dynamics of carriers inside an active region

In this paragraph, the dynamics of the carriers inside the active region is discussed, starting from the rate equations.

6.2.1 Derivation of the rate equations

The dynamics of the carriers in a semiconductor is described by the drift-diffusion equation:

$$\frac{dn}{dt} = G - U + \frac{1}{q} \nabla \cdot J = 0 - \left(\frac{n}{\tau} + Bn^2 \right) + D \nabla^2 n \tag{6.1}$$

G is the generation of electrons per unit of volume, U is the net recombination rate per unit of volume (both non-radiative and radiative recombination is taken into account), and J is the current density. This current consists of the drift current and the diffusion current. The drift current is neglected, because there is no lateral field applied to the device. In this work, no generation of electrons through absorption of light is considered, thus G=0. D is the effective diffusion coefficient, as was defined in section 4.2.5.1.

This equation must be solved to know the carrier density as a function of time and space coordinates. The appropriate boundary conditions need to be used. This expression can be simplified by integrating both sides of the equation over the active region. The definition of the active region depends on the structure of the RCLED. In case of a quantum-well based diode, all carriers are confined in the quantum well, and the integration is done over the volume of the quantum well. In case of a homojunction, the electrons (holes) are located in the p (n) type semiconductor, and the integration is done over that volume. The drift-diffusion equation reduces to:

$$\frac{d}{dt} \int_{Vol} n dV = -\frac{1}{\tau} \int_{Vol} n dV - B \int_{Vol} n^2 dV + D \int_{Vol} \nabla^2 n dV$$

The last volume integral can be rewritten as an integration over the surface of the active layer using Green's theorem. This allows to use a simpler boundary condition:

$$D \int_{Vol} \nabla^2 n dV = D \int_{Surf} \vec{\nabla} n \cdot \vec{e_n} dS = \int_{Surf} \frac{1}{q} \vec{J_{inj}} \cdot \vec{e_n} dS$$

with $\vec{e_n}$ the normal vector, and $\vec{J_{inj}}$ the injected current. If the carrier concentration is constant over the active region, then the integration is fairy simple, and the drift-diffusion equation reduces to:

$$\frac{dn}{dt} = -\frac{n}{\tau} - Bn^2 + \frac{J_{inj}}{qd} \tag{6.2}$$

with d the thickness of the active region. The constant carrier concentration assumption is valid if the diffusion effects in the active volume are negligible ($D \nabla^2 n = 0$). The carrier concentration should therefore be constant in the horizontal direction (in the plane of the active region) and in the vertical direction (in the direction of the current injection). In the vertical direction, the constant carrier concentration assumption is valid if the thickness of the active region is smaller compared to the diffusion length. Such active regions

are single quantum wells or thin, double heterostructure active layers. In case of multiple quantum wells, the carrier concentration should be uniform over all wells, implying a good exchange of carriers between the wells. This corresponds to a small tunnelling time for the carriers[2]. Simulations using the SimWindows software tool showed that this is valid, except for very small carrier concentrations or for a large number of wells. In the horizontal direction, the carrier concentration is constant if the current injection profile is constant, which is valid for the devices studied in this work[3]. In conclusion, the constant carrier concentration over the active region is assumed to be valid for the active regions which are studied in this thesis.

Equation 6.2 is the rate equation, describing the dynamics of the carriers inside the active region of the RCLED. The dynamics of the light emission is derived from the carrier density, as given by equation 3.4.

6.2.2   Current-driven RCLEDs

In this paragraph, some solutions of the rate equation (equation 6.2) will be presented. The solution depends on the input current density J_{inj}. Assume a simple step input $J_{inj}(t) = J$. The resulting equation is a second order differential equation with constant coefficients. The solution is easily found (assume initial condition $n(t = 0) = n_0$):

$$n_{on}(t) = \frac{n_0\sqrt{1 + \frac{4B\tau^2 J}{qd}} + \left(\frac{2\tau}{qd}J - n_0\right)\tanh\left(\frac{t}{2\tau}\sqrt{1 + \frac{4BJ\tau^2}{qd}}\right)}{\sqrt{1 + \frac{4B\tau^2 J}{qd}} + (1 + 2B\tau n_0)\tanh\left(\frac{t}{2\tau}\sqrt{1 + \frac{4BJ\tau^2}{qd}}\right)} \tag{6.3}$$

At the off-switching transient, the equation reduces to:

$$n_{off}(t) = n_0\left(\frac{1 - \tanh\left(\frac{t}{2\tau}\right)}{1 + (1 + 2B\tau n_0)\tanh\left(\frac{t}{2\tau}\right)}\right) \tag{6.4}$$

In case of a negligible non-radiative lifetime (limit $\tau \to \infty$), the rising edge is given by:

$$n_{on}(t) = \sqrt{\frac{J}{Bqd}}\left(\frac{n_0 + \sqrt{\frac{J}{Bqd}}\tanh\left(t\sqrt{\frac{BJ}{qd}}\right)}{\sqrt{\frac{J}{Bqd}} + n_0\tanh\left(t\sqrt{\frac{BJ}{qd}}\right)}\right) \tag{6.5}$$

and the falling edge is given by:

$$n_{off}(t) = \frac{n_0}{Bn_0 t + 1} \tag{6.6}$$

---

[2]The tunnelling time describes the probability that the carrier travels from a well to a neighbouring well.

[3]A special case of a non-uniform carrier profile is the lateral carrier diffusion at the edge of the active region. This could be taken into account by defining an effective area, slighty larger than the area of the active region.

From these equations, the rise and fall times of the optical response can be calculated. First, the delay is calculated, this is the time difference between the moment the carrier density reaches α % of its static value and the start of the current pulse. If the initial condition for the carrier density is 0 (the active region is empty at the beginning of the current pulse), then the delay is given by:

$$t_\alpha = \frac{2\tau}{\sqrt{1 + \frac{4BJ\tau^2}{qd}}} \tanh^{-1} \frac{\alpha\sqrt{1 + \frac{4B\tau^2 J}{qd}}}{1 - \alpha + \sqrt{1 + \frac{4BJ\tau^2}{qd}}} \approx \sqrt{\frac{qd}{BJ}} \tanh^{-1} \alpha \qquad (6.7)$$

The delay at the downward transition is given by:

$$t_\beta = 2\tau \tanh^{-1} \frac{1 - \beta}{1 + \beta\sqrt{1 + \frac{4BJ\tau^2}{qd}}} \approx \sqrt{\frac{qd}{BJ}} \frac{1 - \beta}{\beta} \qquad (6.8)$$

For practical reasons, the rise time is defined as the time interval between the moments the optical signal reaches 10 % and 90 % of the static optical power. This corresponds to the interval between the 31.6 % and 94.8 % value of the static carrier density, because the optical power is proportional to the square of the carrier density. In case of a negligible non-radiative recombination, the rise time is given by:

$$t_{rise} = 1.49\sqrt{\frac{qd}{BJ}} \qquad (6.9)$$

This implies that large current densities are required to obtain a short response time of current-driven RCLEDs. This is an unfavourable situation: highly efficient LEDs, as RCLEDs, need a small current, and are consequently slower compared to less-efficient devices. The fall time, defined as the 90 % to 10 % time, is calculated as:

$$t_{fall} = 2.11\sqrt{\frac{qd}{BJ}} \qquad (6.10)$$

This factor is larger than the rise time. This is explained by the nonlinear character of the bimolecular recombination. At the off-switching transient, the carrier density is initially large, resulting in a short radiative lifetime and a faster initial decrease of the carrier density. But at the end, the carrier density is small, resulting in a long carrier lifetime, and thus a slowly decreasing tail. This tail determines the long fall time. The calculated rise and fall times for RCLEDs are plotted in figure 6.1. For these calculations, d was assumed to be 20 nm and B was .

It is interesting to write the rise time as a function of the steady-state carrier density. If the non-radiative recombination effects are neglected, then the rise time is given by:
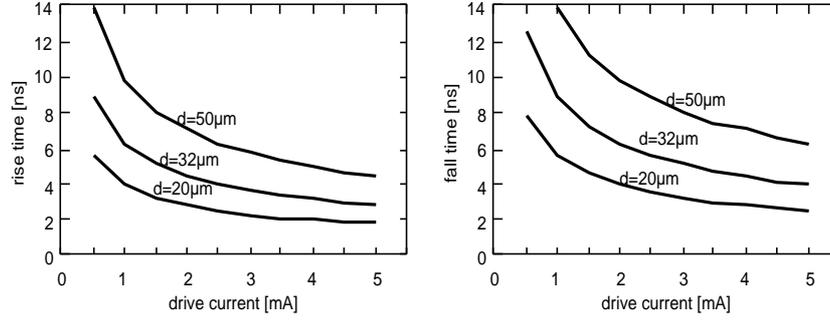
Figure 6.1: Calculated rise and fall time of current-driven RCLEDs with different diameters.

$$t_{rise} = 1.49 \frac{1}{Bn_{regime}} \tag{6.11}$$

This is an important result: the rise time of a current-driven RCLED depends just on the steady-state carrier density. This expression does not depend on the device diameter, which is strange at first sight, because the previous expressing showed that small RCLED are faster. However, a constant carrier density requires a larger current for large RCLEDs.

6.2.3 Voltage-driven RCLEDs

In case of a voltage-driven RCLED, the injected current is determined by the voltage drop across the diode V_j, the series resistance R_{series} and the driving voltage:

$$I_{inj} = \frac{V_{source} - V_j}{R_{series}}$$

An expression for the voltage drop across the active region was given in section 3.3. The rate equation needs to be solved, taking into account the relation between the current and the voltage drop. This results in a non-linear differential equation, and there is no known closed-form solution. However, it is possible to estimate the rise time if a linear approximation for the voltage drop across the junction is used:

$$V_j = \begin{array}{ll} V_{j,0}\left(1 + \frac{n}{n_0}\right) & n > 0 \\ 0 & n < 0 \end{array} \tag{6.12}$$

For an InGaAs based active region, it was found that $V_{j,0} = 1.31$ V and $n_0 = 1 \cdot 10^{19}$ cm^{-3}. In this way, the rate equation can be written as:

$$\frac{dn}{dt} = \frac{1}{qVol}\frac{V_{source} - V_{j,0}}{R_{series}} - \frac{1}{qVol}\frac{V_{j,0}}{R_{series}}\frac{n}{n_0} - \frac{n}{\tau} - Bn^2$$

The transient of the voltage-driven RCLED is described as a current-driven RCLED with an effective non-radiative lifetime. This allows to estimate the rise and fall times, using the expressions for the current driven RCLEDs. It is possible to define a capacitance C_{LED}:

$$C_{LED} = \frac{dQ_{LED}}{dV} = \frac{d\left(qVoln\right)}{d\left(V_{j,0}\left(1 + \frac{n}{n_0}\right)\right)} = \frac{qVoln_0}{V_{j,0}}$$

This capacitance is not related to a physical charge stored in the device. It corresponds to a linear capacitance on which a charge $qVoln_0$ is stored at the voltage $V_{j,0}$. This is a large carrier concentration (the corresponding voltage drop over the junction is twice the turn-on voltage!), the corresponding capacitance per unit of area is also large, typically 25 fF/μm^2 in case of an InGaAs active region. Using this definition, the effective non-radiative lifetime τ_{eff} is written as:

$$\frac{1}{\tau_{eff}} = \frac{1}{qVol}\frac{V_{j,0}}{R_{series}}\frac{1}{n_0} = \frac{1}{R_{series}C_{LED}}$$

If the series resistance is very small, then the effective lifetime decreases and the response of the RCLED becomes faster. The resulting rise and fall times of voltage driven RCLEDs can be much shorter compared to current driven RCLEDs. This can be explained in another way. After the turn-on, the voltage drop across the junction increases from 0 to V_j. Consequently, the RCLED current decreases from V_{source}/R_{series} to $\left(V_{source} - V_j\right)/R_{series}$. There is a peaked current waveform, resulting in a faster optical response. The larger the driving voltage, the smaller the difference between the initial current and the steady-state current, and the smaller the influence of that peaked current onto the rise time. This will be studied in detail in section 6.7.4.

The equivalent rate equation is valid for n>0, and can be used to estimate the rise and fall time. The fall time is calculated as the time until the carrier density reaches 0. During the off-switching transient using a voltage source, an inverse current will discharge the RCLED. The amplitude of this inverse current depends on the series resistance. Thus the carriers in the active region can disappear by two means: or by a recombination mechanism, or by the inverse current.

6.3   External and parasitic effects

In the previous paragraph, the time-domain response of the active region of RCLEDs was discussed. The response of the carrier concentration, due to the injection of carriers into the active region, was investigated. In reality, the active region is part of a p-n junction, figure 6.2 shows a schematic representation of the active region. The complete device determines the dynamics of the RCLED. These external factors will be discussed in this paragraph.
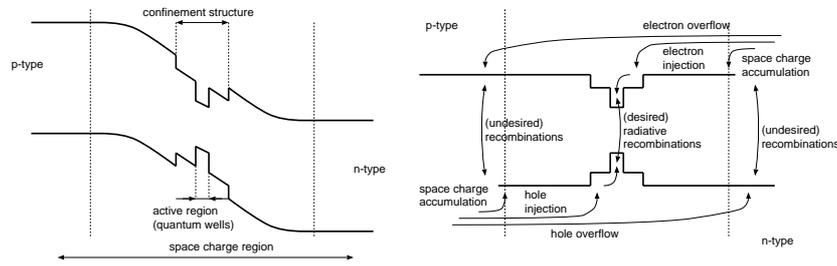
Figure 6.2: Schematic representation of the active region of a RCLED, in a zero-biasing regime (left), and in a forward-biasing regime (right).

6.3.1   The electrical confinement structure

As mentioned before, the active region (consisting of one or several quantum wells, or a double heterostructure) is placed in a p-n junction. The active region is placed in a confinement region (see figure 6.2). This confinement region must be designed to:

- inject the carriers without inducing excessive voltage drops

- inject carriers efficiently and fast

- minimise carrier overflow effects

The carrier overflow can be neglected for the active regions studied in this work, because of the large difference in bandgap between the active region and the barrier layers. This is not always true: in other material systems (such as AlGaInP-based red-emitting active regions), there is only a small energy difference. In that case, the overflow effect is important. It results in recombinations in the bulk p-type (or n-type) semiconductor. These recombination are adverse because of two reasons: the internal efficiency is typically small, and the recombinations are not located in the anti-node of the microcavity, resulting in a reduced microcavity effect.

In a forward biasing regime, the carriers are injected from the contacts into the semiconductor, from where they diffuse towards the active region. In the literature, the carrier exchange between the semiconductor and the active region is described by a 'carrier capture' time [103][104]. This capture time is typically a few tens of picoseconds. If the voltage drop across the junction is very high, some carriers will have enough energy to escape from the active region and diffuse further into the other side of the junction, where they recombine (as in a homojunction). This effect is described in literature by a 'carrier escape' time [105][106]. The influence of these effects on the emission dynamics are described by a set of coupled rate equations: one equation describing the dynamics in the region around the active region, and one describing the dynamics in the active region[103].
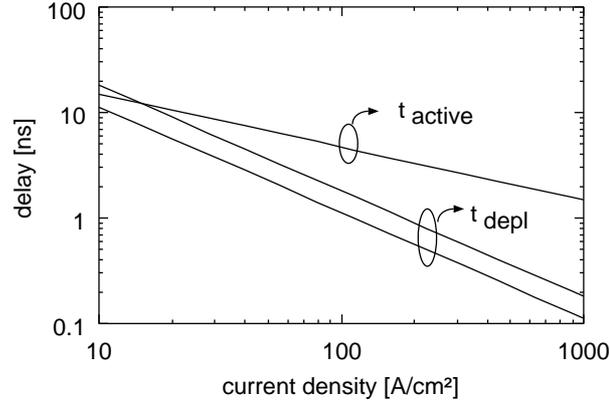
Figure 6.3: Calculation of the delay caused by the depletion capacitance (t_{depl}, assumes W_i=60 nm (upper) and W_i=100 nm (lower)), and by the active layer (t_{active}).

In this work, these effects are neglected, because they occur on a smaller timescale compared to the RCLED dynamics. An exception is the off-switching dynamics using voltage drivers. This will be discussed in the next chapter.

6.3.2 Depletion capacitance

During the transient, a part of the diode current charges the depletion capacitance. This capacitance origins from the charge charge accumulation, at the borders of the space charge region (see figure 6.2). This results in an extra delay of the optical signal, which is proportional to the area of the diode. The influence of this delay will be estimated in this section. The RCLED is a PiN diode, and the depletion capacitance per unit area in case of a PiN junction is given by:

$$\frac{C_{depl}}{A} = \frac{c_0}{\sqrt{\frac{W_i^2}{d_i^2} + 1 - \frac{V_j}{V_{bi}}}}, \quad c_0 = \sqrt{\frac{q\epsilon\epsilon_0}{2V_{bi}}\frac{N_a N_d}{N_a + N_d}}, \quad d_i = \frac{\epsilon\epsilon_0}{c_0} \tag{6.13}$$

With A the area of the RCLED, W_i the width of the undoped (intrinsic) layer, V_j the voltage drop across the junction, V_{bi} the built-in voltage (depends on the doping concentrations), d_i the effective thickness of the depletion layer, and N_a and N_d the doping concentration of the donors and acceptors. The delay time to charge the depletion capacitance (t_{depl}) is estimated as:

$$\int_0^{t_{depl}} i_0\, dt = \int_0^{V_j} C\left(V\right) dV$$

If the depletion capacitance is driven by a constant current source i_0, then the delay t_{depl} is given by:

$$t_{depl} = \frac{2Ac_0V_{bi}}{i_0}\left(\sqrt{\frac{W_i^2}{d_i^2}+1} - \sqrt{\frac{W_i^2}{d_i^2}+1-\frac{V_j}{V_{bi}}}\right)$$

This delay is inversely proportional to the drive current, whilst the delay caused by the filling of the active region depends on the inverse of the square root of the drive current (see equation 6.9). This implies that the delay associated with the charging and discharging of the depletion capacitance will be dominant at small currents. A typical trade-off current density is about 10 A/cm^2 (see figure 6.3). This number is smaller than the operating current density of RCLEDs in interconnect applications, indicating that the delay caused by the depletion capacitance can be neglected[4].

The standard expression for the depletion capacitance reaches infinity at $V = \left(W_i^2/d_i^2 + 1\right)V_{bi}$, this corresponds to heavily forward biased RCLEDs. This singularity is due to some approximations in the diode theory. However, at these biasing conditions, the dominant capacitance is the diffusion capacitance: much more charge is stored into the active region, compared to the charge stored at the boundaries of the space charge region.

6.4   Influence of the active region

The speed response of RCLEDs depends on the square root of B, the bimolecular recombination coefficient. The origin of this coefficient was discussed in section 3.2.3, and if was found that it depends on the material properties and on the microcavity effect.

6.4.1   Influence of the microcavity effect

A microcavity alters the optical mode density, resulting in an increased or decreased recombination lifetime. However, it was found that in one-dimensional microcavities with a leaky mirror (as the DBR), the change of the overall recombination lifetime is marginal. In best case, at a single emission wavelength and for a single polarisation, a 20 % decrease of the recombination lifetime can be achieved [107]. Figure 6.4 shows the calculated change of the recombination rate, as a function of the normalised cavity thickness. To increase the emission rate, the cavity resonance wavelength should be chosen slightly larger than the emission wavelength. If the cavity is slightly undertuned, then the recombination rate decreases, implying a slower emission. There is no change off the emission rate if the cavity is perfectly tuned. This corresponds to a RCLED optimised for fibre coupling. These calculations imply that the change of the

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[4]the same conclusion can be drawn when comparing the equations for the depletion and diffusion capacitance of standard homojunction p-n diodes.
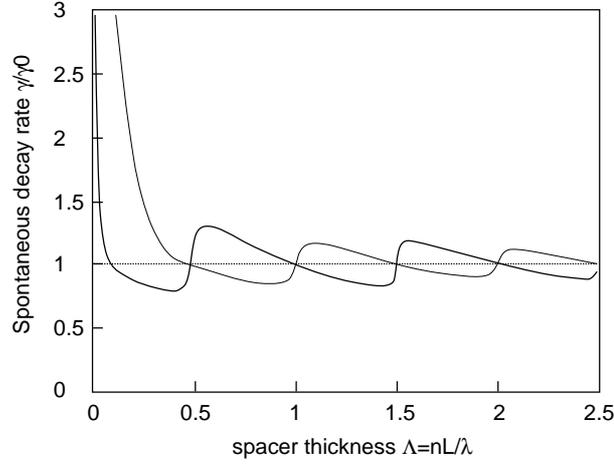
Figure 6.4: Calculated emission rate as a function of the cavity thickness, for a metal mirror/DBR cavity (after [107]).

recombination lifetime is negligible for the cavities studied in this work. The influence of the detuning on the emission rate is very small, certainly if the emission rate is averaged over the complete emission spectrum.

If the high-Q cavity is used (corresponding to a small cavity bandwidth), then the influence of the detuning on the recombination lifetime is more important. The effect on the emission rate has been experimentally characterised in [108] using PL-measurements at room temperature. A high-Q cavity was used, and the recombination lifetime decreases for off-resonance cavities. In [109][110], the PL-measurements were done at low temperatures. The intrinsic spontaneous emission spectral bandwidth is smaller at these temperatures, resulting in a stronger effect on the emission lifetime. Depending on the detuning, the decay time changed from -10 % at short emission wavelengths compared to resonance wavelengths, to +20 % for overtuned cavities (from 0.7 to 0.9 ns).

6.4.2 Influence of the material parameters

In this chapter, the bimolecular recombination coefficient is assumed to be constant. However, as mentioned in section 3.2.3, this coefficient depends on the carrier density. As a result, the rise time of the current-driven RCLED is given by:

$$t_{rise} = 1.49 \frac{1}{\frac{B_0}{1 + \frac{n_{regime}}{n_0}} n_{regime}} \approx 1.49 \frac{1}{B_0 n_0} \ \left(n_{regime} \to \infty \right)$$

with B_0 and n_0 defined in section 3.2.3. The rise time cannot be made arbitrary small by increasing the carrier density: there is a lower limit. For a GaAs based
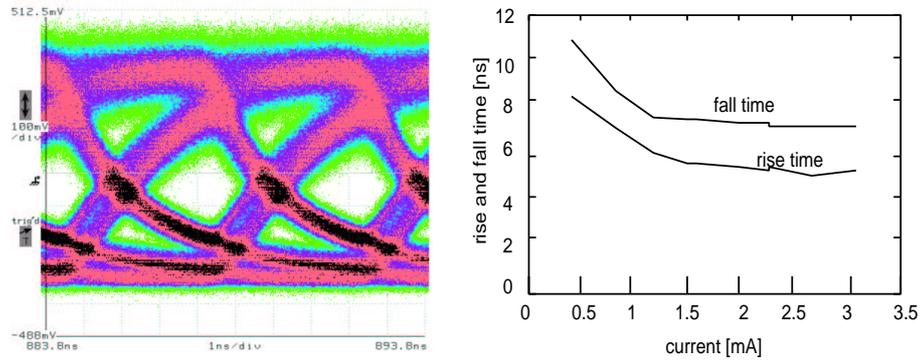
Figure 6.5: Measured speed characteristics and eye-diagram at 250 Mbps of a 32-μm RCLED, driven at 3 mA current.

active region, B_0 is $1.3 \cdot 10^{-10}$ cm^{3}s^{-1}, n_0 is $4 \cdot 10^{19}$ cm^{-3}, and the minimal rise time is 310 ps. This is smaller compared to the rise and fall times discussed in the work, and therefore this effect is neglected.

6.5   Experimental results

In this section, the theoretical results will be compared with measurements on current and voltage-driven RCLEDs.

6.5.1   Current-driven RCLEDs

Figure 6.5 shows the measured rise and fall times of a 32-μm RCLED as a function of the drive current, and an eye-diagram of the same RCLED, driven at 3 mA. The rise time of the current signal is about 300 ps. The measurements were done using a short POF, coupled to a high-speed APD photo receiver (with bandwidth 1 GHz). The measured rise and fall times for a 32-μm RCLED are in agreement with the theory (see figure 6.1).

The eye-diagram is still open at 250 Mbps. The shape of the eye-diagram is in agreement with the theoretical predictions. There is a small inter-symbol interference (ISI): the rising edge consists of 2 separate traces, depending on the number of preceding ZEROs. If the bit rate is sufficiently large, and if only one ZERO occurred before the ONE bit, then the carrier density inside the active region is not completely removed at the end of the ZERO bit. This results in a faster rise time. This effect is not visible at the falling edge. This indicates that the off-switching transient takes a longer time.

The large asymmetry between the rise and fall time is explained by the non-linear V(n) relation. At the on-switching transient, the junction voltage increases rapidly to a value close to V_j, as soon as there are 'some' carriers in the active region. This results in a fast decrease of the peaked current waveform,
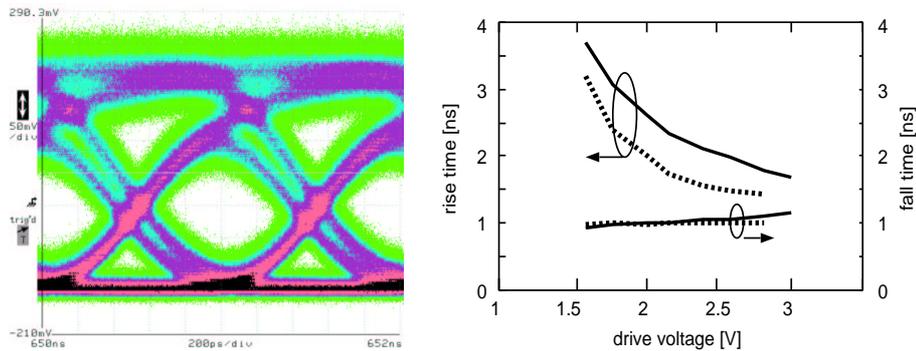
Figure 6.6: Measured eye-diagram at 1 Gbps of voltage-driven RCLED (32-μm diameter), and measured rise and fall time for 32-μm RCLED (full line) and 20-μm RCLED (dashed line).

to the static current. On the other hand, the voltage across the junction remains close to V_j, as long as there are 'some' carriers in the active region. This results in a much longer inverse current duration, and a stronger reduction of the fall time.

6.5.2 Voltage driven RCLEDs

Figure 6.6 shows the measured rise and fall times of a voltage-driven RCLED (with a diameter of 32 μm), and a measured eye-diagram at 1 Gbps. The rise and fall time of the voltage pulses is 60 picoseconds. Much shorter rise and fall times are achieved compared to the current-driven RCLED. This is explained by the current peaking at the rising edge, and the inverse current at the falling edge, as mentioned in paragraph 6.2.3.

In this case, the falling edge of the optical signal is faster. Therefore, the inter-symbol interference (ISI) is first visible at the falling edge. The measured fall time seems to be independent on the device diameter. However, the bandwidth of the receiver is not negligible at these operating speeds, and limits the response. It is believed that the fall time of the optical signal is smaller than the fall time of the measured recevier signal.

6.6 Small-signal response of RCLEDs

6.6.1 Optical small-signal response

Small-signal impedance measurements offer a simple technique to study and characterise the high-speed properties of RCLEDs. In this characterisation technique, the response of a quantity to a small variation of the input current (around a certain biasing setting) is measured. In optical small-signal measure-

ments, the variation of the optical power is measured. A theoretical expression for the small-signal response can easily be derived from the rate equations. Assume a small, harmonic variation on the biasing settings:

$$\frac{d}{dt}\left(n_0 + \Delta n e^{j\omega t}\right) = \frac{I_{inj} + \Delta I e^{j\omega t}}{qVol} - B\left(n_0 + \Delta n e^{j\omega t}\right)^2 - \frac{n_0 + \Delta n e^{j\omega t}}{\tau}$$

with n_0 the static carrier density (determined by the biasing current I_{inj}), and Δn the amplitude of the harmonic deviation ($n_0 \gg \Delta n$). This expression can be solved if the second order terms are neglected. The frequency-dependent variation of carrier density is written as:

$$\Delta n\left(\omega\right) \approx \frac{\Delta I}{qVol}\frac{1}{j\omega + \omega_0} \tag{6.14}$$

with ω_0 the cut-off frequency, defined as:

$$\omega_0 = 2Bn_0 + \frac{1}{\tau} = \sqrt{\frac{1}{\tau^2} + \frac{4BI_{inj}}{qVol}}$$

The output optical power is written as $P = P_0 + \Delta P e^{j\omega t}$, the frequency dependent optical small-signal response is given by:

$$\Delta P\left(\omega\right) \approx h\nu\eta_{extr}B2n_0\Delta n V = \frac{h\nu}{q}\eta_{extr}\Delta I\frac{\omega_0 - \frac{1}{\tau}}{j\omega + \omega_0} \tag{6.15}$$

The 3 dB cut-off frequency depends on the square root of the bias current, if the radiative recombination is dominant. The response at high-frequencies decreases as $1/\omega$. Figure 6.7 shows the measured optical small-signal response. The DC response decreases as a function of the biasing current, due to saturation effects. Unfortunately, the measurements were heavily influenced by electrical parasitics, which exhibit a resonance at 600 MHz. This did not allow to extract any data from the results. Nevertheless, a small-signal -3 dB frequency of 200 to 300 MHz at a biasing current of 8 mA is estimated.

6.6.2   Impedance measurements

A straightforward measurement on electrical devices is the S-parameter measurement, from which the impedance is easily calculated. For these measurements, the calibration techniques are well-known, minimising the influence of parasitics on the measurements. The small-signal impedance of the diode can be calculated as:

$$Z\left(\omega\right) = \frac{dV}{dI} = \frac{\frac{dV}{dn}}{\frac{dI}{dn}} = \frac{nkT}{q}\frac{1}{n_0 + n_i}\frac{1}{qV}\frac{1}{j\omega + \omega_0} \tag{6.16}$$

This expression has the same frequency dependency as the optical small-signal response (equation 6.15), and should therefore give the same information on the dynamics of the RCLED. The devices were directly probed on chip,
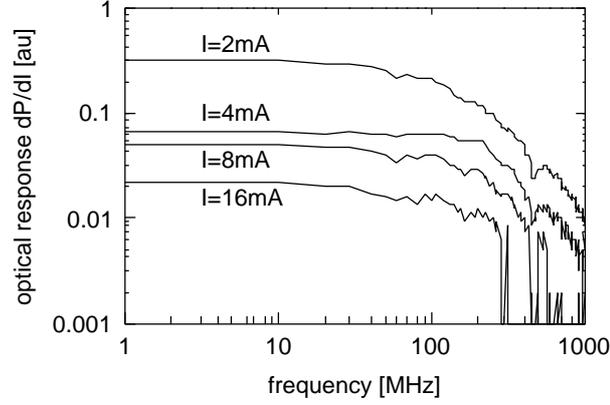
Figure 6.7: Measured optical small-signal response as a function of the biasing current (device diameter is 50 μm).

thereby reducing the parasitic effects. Therefore, it is assumed that the measured impedance is the intrinsic impedance of the RCLED, and all external parasitics are neglected. This is justified because no resonance effects are visible for f>1 GHz.

Figure 6.8 shows the measured small-signal impedance of the diode, for a 980-nm RCLED without and a 850-nm RCLED with a selectively oxidised current window. Figure 6.9 shows the extracted 3 dB frequency as a function of the square root of the biasing current. The 3 dB frequency increases super-linearly as a function of the square root of the biasing current. This is in contradiction with equation 6.14. Furthermore, the small-signal measurements show that the impedance decreases as $1/\sqrt{\omega}$ at large frequencies. This explains why the optical response is larger than expected, but not the origin of this $1/\sqrt{\omega}$ relation.

To investigate this behaviour, a simple analysis of carrier diffusion is done. In an unpumped homogeneous semiconductor region (as a heterostructure active region, or even a set of quantum wells), the one-dimensional (in-plane) drift-diffusion equation is given by equation 6.1 (by setting the generation term to zero). This equation can be linearised, just as the standard rate equations were transformed into a small-signal equation. The equation describing the small-signal response is given by:

$$D\frac{d^2 n}{dx^2} + \left(j\omega + \omega_0\right) n = 0$$

The solution for the carrier density, taking into account the boundary conditions, is derived in appendix A. The small-signal impedance is given by:

$$Z\left(\omega\right) = \frac{V}{AJ} = \frac{mkT}{q}\frac{1}{n_0 + n_t}\frac{1}{qD\sqrt{\frac{\omega_0 + j\omega}{D}}\tanh\left(L\sqrt{\frac{\omega_0 + j\omega}{D}}\right)}$$
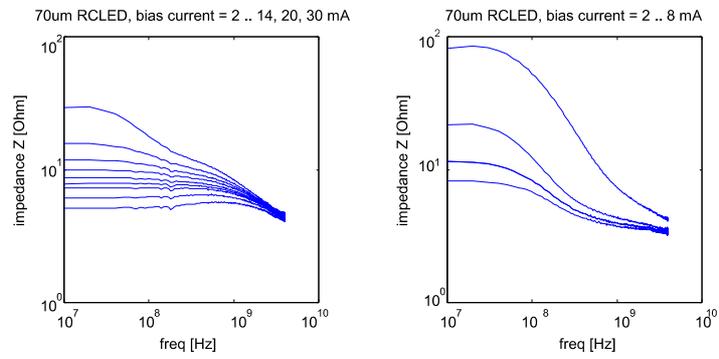
Figure 6.8: Measured impedance as a function of the frequency, for different biasing currents, for a 980-nm RCLED without (left) and a 850-nm RCLED with selectively oxidised current window (right).

Figure 6.9: Measured 3 dB frequency (from the impedance measurements), for different RCLED diameters.

For this equation, two regimes can be found:

- in case of a short distance to the border of the diode (L small), the accumulated charge is determined by the confinement, and the impedance decreases as $1/\omega$:

$$L^2 \ll \frac{D}{\sqrt{\omega_0^2 + \omega^2}} \Rightarrow Z(\omega) = \frac{1}{AL}\frac{mkT}{q}\frac{1}{q(n_0 + n_i)}\frac{1}{\omega_0 + j\omega}$$

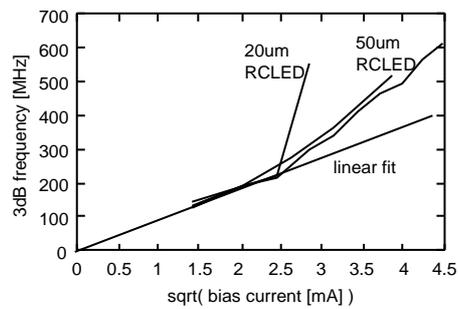This corresponds to the expression derived from the rate equations (equation 6.16).

- in case of a long diode, the expression reduces to the well-known equation for the small-signal impedance of diodes [111]. The charge accumulation is now determined by the diffusion of the minority carriers, and the frequency response decreases as $1/\sqrt{\omega}$:

$$L^2 \gg \frac{D}{\sqrt{\omega_0^2 + \omega^2}} => Z(\omega) = \frac{1}{A\sqrt{D}}\frac{mkT}{q}\frac{1}{q(n_0 + n_i)}\frac{1}{\sqrt{\omega_0 + j\omega}}$$

In conclusion, it is found that the $1/\omega$ behaviour corresponds to a confinement-limited charge accumulation, whilst the $1/\sqrt{\omega}$ is related to a diffusion-limited charge accumulation. Furthermore, at very high frequencies, the small-signal impedance is always diffusion-limited. This can be explained as follows: when the bit period is very short, the total charge in the active region is determined by the diffusion time of the carriers. In case of long bit periods, the minority carriers have plenty of time to fill the active region, and the response is confinement-limited.

These measurements give more information: at low current densities, the frequency response starts to decrease as $1/\omega$ (thus confinement-limited), but at higher frequencies, it decreases as $1/\sqrt{\omega}$. This effect is strongest for RCLEDs with an oxidised current-confinement structure. This is explained by the lateral diffusion in the active region: at low current densities, the current injection is uniform over the RCLED area, and the frequency response is confinement-limited. However, at higher current levels, the current injection is non-uniform (the injected current is larger at the border of the RCLED). This is because the voltage drop in lateral direction (representing the horizontally flowing current under the active layer) is not negligible at high current densities, and this reduces the effective voltage drop across the quantum well in the middle of the RCLED. This reduced voltage drop results in a reduced injected current in the centre of the RCLED. In that case, the carriers diffuse laterally in the quantum well from the border towards the centre of the RCLED, and the charge injection is diffusion-limited.

These conclusions are in agreement with the spectral measurements on RCLEDs with an oxidised current window, which also shows the existence of
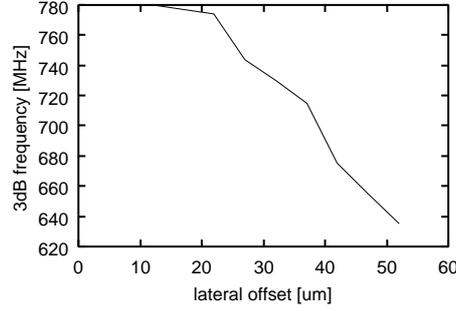
Figure 6.10: Measured 3 dB frequency of the fibre-coupled RCLED, as a function of offset.

the lateral carrier diffusion. Another proof of this lateral carrier diffusion is shown in figure 6.10, where the 3 dB frequency of a voltage-driven RCLED is plotted as a function of the lateral offset between the RCLED and the POF. The maximal modulation speed decreases as a function of the offset, because more light generated by lateral carrier diffusion is coupled into the fibre. The response of this light is slower due to a smaller carrier density and the diffusion effects.

6.7 Optimal operation conditions for RCLEDs

In this paragraph, some operation conditions for highly efficient RCLEDs will be discussed.

6.7.1 Determination of optimal current density

In the previous paragraphs, it was found that the extraction efficiency of the RCLED decreases as a function of the current density, whilst the speed response increases as a function of the current density. It is clear that an optimal current density exists for which the enhancement-speed product is maximised, assuming that the RCLED is driven by a constant current density. No pulse-shaping or biasing is taken into account. Assume that the enhancement decreases due to the broadening of the intrinsic spontaneous emission spectrum. The decrease of the enhancement as a function of the temperature is neglected. The enhancement is then given by:

$$ enh(J) = enh_0 \frac{1}{\sqrt{1 + k^2 \left(1 + \frac{J}{J_1}\right)^2}}, \quad k = \frac{\Delta\lambda_{SE}^2}{\Delta\lambda_{cav}^2} $$

and the 3 dB bandwidth of the RCLED is given by:

$$BW_{3dB}(J) = BW_0 \sqrt{\frac{J}{J_0}}$$

The enhancement-bandwidth product can be optimised. The optimal current density is given by:

$$J_{opt} = J_1 \sqrt{\frac{\Delta\lambda_{SE}^2}{\Delta\lambda_{cav}^2} + 1}$$

For example, the optimisation of the operating point of a 980-nm RCLED is given. Assume that the broadening of the intrinsic spontaneous emission spectra is described by $J_{opt} = 490$ A/cm^2 (valid for InGaAs QW based active regions), and $\Delta\lambda_{SE} = 33$ nm (see section 3.2.5), and assume that the cavity bandwidth is given by $\Delta\lambda_{cav} = 25$ nm, then the optimal current density is about 810 A/cm^2. This corresponds to about 5 mA drive current for a 32-μm diameter RCLED. The corresponding rise time is about 3 ns. The optimal current density is slightly smaller if thermal effects are taken into account.

6.7.2 Influence of a biasing on current-driven RCLEDs

In this paragraph, the influence of a biasing current on the performance of the RCLEDs is investigated. As mentioned in the previous paragraph, the biasing results in a faster switching, due to the larger carrier concentration and the smaller recombination lifetime. Assume that the RCLED current is switched from I_0 to I_1, and that the non-radiative recombination is negligible. The transient of the carrier density is derived from equation 6.3, and the rise time is given by:

$$t_\alpha = \sqrt{\frac{qV}{BI_1}} \tanh^{-1} \frac{\sqrt{(1-\alpha)I_0 + \alpha I_1} - \sqrt{I_0}}{\sqrt{I_1} - \sqrt{(1-\alpha)I_0 + \alpha I_1}\sqrt{\frac{I_0}{I_1}}}$$

The peak-to-peak optical response is given by:

$$P(t) = \frac{h\nu}{q}\eta_{extr}(I_1 - I_0)$$

Figure 6.11 shows the calculated rise time, as a function of the biasing current, for different peak-to-peak current variations. The rise time decrease as a function of the biasing current is strongest for a small peak-to-peak current variation. However, applying a biasing current is not an efficient way to decrease the rise time. The same plot shows the ratio between the bandwidth (defined as the inverse of the sum of the rise and fall time) and the averaged RCLED current. If the current consumption is an important parameter, then the use of a biasing current is an inefficient way to enhance the speed response of the RCLEDs.
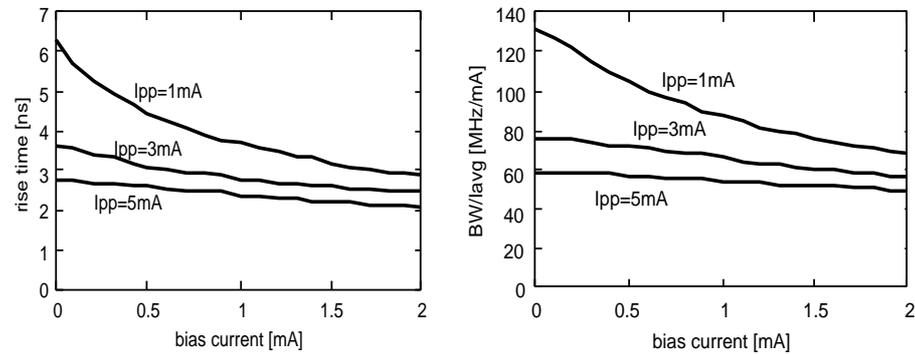
Figure 6.11: Calculated rise time and bit rate to average current ratio, for a 32-μm RCLED, as a function of the biasing current, for different peak to peak currents.

6.7.3 Doped active regions

An alternative way to decrease the rise time is the use of a background doping in the active region. This is an attractive technique, as it does not increase the average RCLED current.

The rate equation can be written as [102]:

$$\frac{dn}{dt} = -\frac{n}{\tau} - Bn\left(n + N_d\right) + \frac{J_{inj}}{qd}$$

with N_d the doping concentration in the active region. The influence of the doping can be written as a non-radiative lifetime. Figure 6.12 shows the calculated rise time as a function of the background doping level. This plot shows that a doping concentration of at least $5 \cdot 10^{19}$cm^{-3} is desired to obtain a significantly decrease of the rise time. This can be explained by the rate equation: N_d should be at least of the same order as the carrier concentration, in order to have a significant influence on the recombination rate.

6.7.4 Voltage-driven RCLEDs

The measurements showed that voltage-driven RCLEDs have much smaller rise and fall times than current-driven RCLEDs. In this section, the performance of voltage-driven RCLEDs will be discussed. The basic equations for the speed response of voltage-driven RCLEDs are the rate equation together with the relation between the junction voltage and the carrier density. It was found that no closed-form solutions exists. Therefore, a software tool (MathCad) was used to integrate the differential equation, and the rise time was determined by hand from the calculated optical trace.

Figure 6.13 shows the results. The rise time depends strongly on the series resistance of the device, and the rise time of voltage-driven RCLEDs approx-
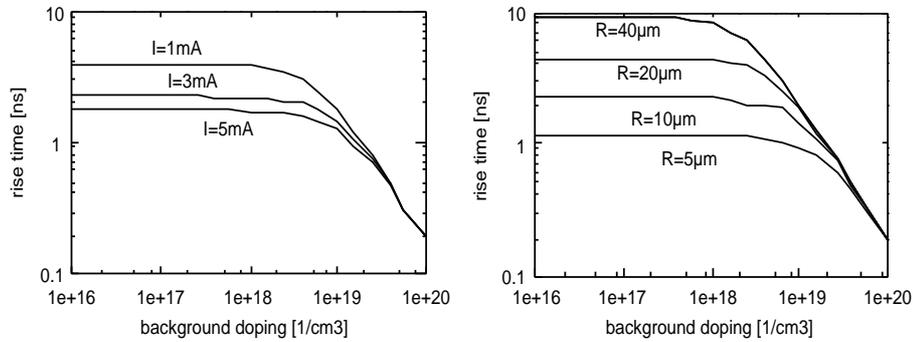
Figure 6.12: Influence of background doping on the rise time, as a function of the drive current (assuming R=10 μm) and the device radius (assuming I=3 mA).
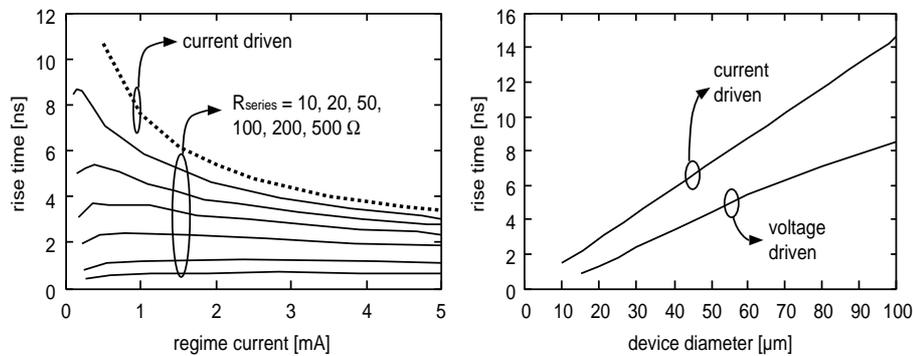
Figure 6.13: Calculated rise time of voltage-driven RCLED (30 μm diameter) as a function of the series resistance (left), and calculated rise time as a function of the device diameter (at 3 mA regime current).
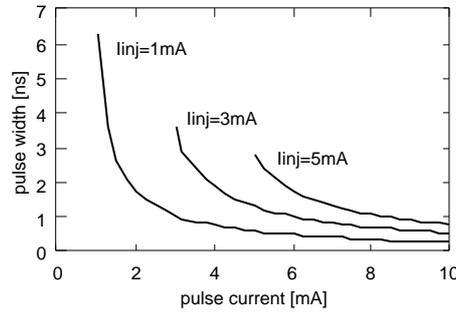
Figure 6.14: Calculated pulse width as a function of the pulse current, for a 32-μm diameter RCLED, for different injection currents.

imates the rise time of current-driven RCLEDs, if the series resistance is very large. This is obvious, because a voltage source with a large internal impedance behaves as a current source. The series resistance determines the amplitude of the peak current transient. This faster response goes together with an increased voltage drop across the devices, due to the larger series resistance. The same plot shows the calculated rise time as a function of the device diameter. The series resistance was constant, 100 Ω. The drive voltage was adapted to obtain 3 mA current after the current peak, so that both devices emit the same static optical power. The voltage-driven RCLED has a smaller rise time, even at the smallest device diameters.

6.7.5   Pulsed current-driven RCLEDs

It was found that voltage-driven RCLEDs have a faster response, due to the peaked current pulse, especially at low driving voltages. In this section, the influence of a pulsed current shape will be investigated. The current shape is defined as follows: at the beginning of the bit period, a current I_{pulse} is driven, during a time T_{pulse}. During the rest of the bit, a current I_{inj} is driven to the RCLED.

The minimal pulse duration is defined as the time at which the carrier density equals the static carrier density, which is determined by the injection current. The pulse duration is calculated from the rate equation. The pulse duration is plotted in figure 6.14. Very short pulse widths are found, especially if the injection current is small.

An approximate expression can be found as follows. In the beginning of the transient, the carrier density increases linearly as a function of time. All recombination effects can be neglected, and the carrier density is given by:

$$n\left(t\right) = t\frac{I_{pulse}}{qVol}$$

The steady-state carrier density is given by equation 3.3. If the non-radiative

recombination is neglected in this expression, then a simple equation for the pulse duration can be determined:

$$t_{pulse} \approx \sqrt{\frac{qVol}{BI_{inj}} \frac{I_{inj}}{I_{pulse}}}$$

From this equation, it is clear that the pulse width is a few times shorter than the rise time of the signal as if there was no pulse applied. This effect is more pronounced if the injected current is small. This implies that this technique is useful for RCLEDs driven at small current densities. Compared to other techniques, this pulsed driving principle is the only solution that works better at small current densities.

6.8 Conclusion

In this chapter, the switching dynamics of RCLEDs were described. Starting from the rate equations, closed-form solutions for the rise and fall time were determined, valid for different driving conditions. It was found that the response of RCLED is slower if the device is driven at a small current density. These theoretical results have been compared to the measurements on current- and voltage-driven RCLEDs. The small-signal response of RCLEDs was investigated, and it was found that there is an important influence of the lateral carrier diffusion in the active region at very high frequencies (>1 GHz). Finally, several advanced driving principles have been studied. The peaked current pulse is an interesting driver technique for RCLEDs, as it is the only technique that results in a faster response at smaller current densities. This is in particular interesting for the highly efficient RCLEDs, which are driven at a lower current compared to less efficient devices.

Appendix A: The solution of the small-signal diffusion equation

The equation describing the small-signal diffusion effect is given by:

$$D\frac{d^2n}{dx^2} + (j\omega + \omega_0)\, n = 0$$

With D the diffusion coefficient, and ω_0 is defined as:

$$\omega_0 = 2Bn_0 + \frac{1}{\tau} = \sqrt{\frac{1}{\tau^2} + \frac{4BI_{inj}}{qVol}}$$

Realistic boundary conditions must be used to solve this equation. The minority carrier concentration at the border of the active region (x=0) is constant,

and the minority diffusion current at the end of the semiconductor (x=L) is zero.

$$n\left(x = 0\right) = \Delta n_0$$
$$J\left(x = L\right) = qD\frac{dn}{dx}\left(x = L\right) = 0$$

The frequency-dependent variation on the carrier density is:

$$\Delta n\left(x, \omega\right) = \Delta n_0 \frac{\exp\left(\sqrt{\frac{\omega_0 + j\omega}{D}}x\right) + \exp\left(\sqrt{\frac{\omega_0 + j\omega}{D}}\left(2L - x\right)\right)}{1 + \exp\left(2L\sqrt{\frac{\omega_0 + j\omega}{D}}\right)}$$

The current is given by:

$$\Delta J\left(\omega\right) = qD\frac{dn}{dx}\left(x = 0\right) = qD\Delta n_0 \sqrt{\frac{\omega_0 + j\omega}{D}}\tanh\left(L\sqrt{\frac{\omega_0 + j\omega}{D}}\right)$$

The variation of the voltage drop across the device is:

$$V\left(n\right) = \frac{mkT}{q}\ln\left(\frac{n}{n_i} + 1\right) \Rightarrow \Delta V = \frac{mkT}{q}\frac{1}{n + n_i}\Delta n_0$$

And the small-signal impedance is:

$$Z\left(\omega\right) = \frac{\Delta V}{A\Delta J} = \frac{1}{A}\frac{mkT}{q}\frac{1}{n + n_i}\frac{1}{qD\sqrt{\frac{\omega_0 + j\omega}{D}}\tanh\left(L\sqrt{\frac{\omega_0 + j\omega}{D}}\right)}$$

Chapter 7

A high-speed model for RCLEDs

In this chapter, an adequate high-speed model for RCLEDs is introduced. This model allows to optimise the electrical interface circuit for RCLEDs. First, an overview of the large signal modelling of diodes is given, followed by the derivation of the high-speed model for RCLEDs. A parameter extraction procedure to obtain the model parameters is presented, and the model is compared to several measurements.

7.1 Introduction

An adequate equivalent model for RCLEDs is an essential tool, necessary to design a suitable driver circuit. It allows to calculate the behaviour of the component, taking into account the interaction between the light emitter and the driver circuit. The accuracy of the model is very important if the components are driven at the limits of their intrinsic performance.

In literature, few publications are found on equivalent models for LEDs, and even fewer on models for RCLEDs. The few articles present the equivalent circuit of an LED as a resistor and a capacitance in parallel. This model is accurate for frequencies up to a few megahertz, but this model gives no information on the optical signal. Moreover, new applications for RCLEDs demand gigabits-per-second data rate. This is feasible, as was shown in the previous chapters. Therefore, a new model, valid at these operation frequencies, has to be derived. The model must satisfy some specific issues:

- the model must describe the behaviour of the RCLEDs accurately, especially in the time-domain.

- the model must be user-friendly: it should be integrated with the circuit design software, to allow the optimisation of the RCLED driver circuit

- the model should be based on a simple mathematical description. This will result in a better convergence and a shorter calculation (simulation) time.

- there should be a reliable and fast way to determine the model parameters. This is of course related to the simplicity of the model equations.

In this chapter, a model for RCLEDs will be derived, that fulfils these requirements. But first, an overview of different diode models is given.

7.2   Circuit-level models for diodes

A good model for a standard p-n diode is already available in all circuit simulators. These models include the electrical and thermal behaviour of the devices. In this paragraph, high-speed modelling of diodes is discussed.

7.2.1   The SPICE diode model

The SPICE model of a diode is a current source with in parallel a voltage controlled capacitor [112]. The expression for the static diode current is based on the Shockley equation, including improvements for the high-current injection levels, and for breakdown (at inverse voltages). These effects are modelled in an empirical way: the equations fit reasonably well to the measurements, but they do not include the physical background. The time-domain behaviour is modelled by a single (non-linear) capacitor. The expression for the capacitor is presented in table 7.1. The diode capacitor is the sum of the transit time capacitance C_T and the junction capacitance C_J. The transit time capacitance represents the diffusion capacitance, and is written as a function of the static diode current I_{diode}. In the standard diode theory, the diffusion capacitance of a diode is defined as:

$$C_{diff} = \frac{dQ}{dV} = \tau \frac{dI}{dV}$$

Q is the total charge in the active region, which is written as τI. τ is the recombination time. The SPICE model uses this expression for the diffusion capacitance, but the recombination time is replaced by the transit time TT. This allows to model other time-dependent effects. This approach assumes a constant transit time. This is not valid for RCLEDs, as the recombination time depends on the carrier density. However, it is valid for diodes with a dominant non-radiative recombination (such as silicon diodes).

The junction capacitance is based on the standard expression, as given by equation 6.13. This equation has a singularity for large forward voltages. Therefore, an alternative expression is used at large forward voltages.

diode capacitance	$Cd = Ct + area \cdot Cj$
transit time capacitance	$Ct = TT \cdot \frac{dI_{diode}}{dVd}$
junction capacitance	if $(Vd < FC \cdot VJ)$ then $Cj = CJ0\frac{1}{\left(1-\frac{Vd}{VJ}\right)^M}$ else $Cj = CJ0\frac{1-FC \cdot (1+M)+M\frac{Vd}{VJ}}{(1-FC)^{(M+1)}}$

Table 7.1: Definition of the diode capacitances in the SPICE model.
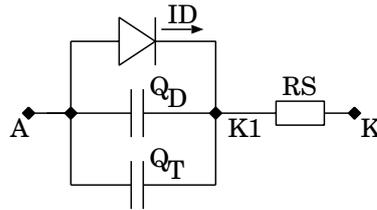
Figure 7.1: Equivalent circuit for diode: the L500 model.

7.2.2 The 'Diode Model Level 500'

This diode model has been developed at Philips [113]. The model for the diode current includes the ideal forward current (as given by the Shockley equation), the forward tunnelling current, a detailed description of the reverse biasing currents (including trap-assisted tunnelling, Shockley-Hall-Read recombination, band-to-band tunnelling and avalanche multiplication), breakdown effects, temperature scaling and noise models. The modelling of the diode current is more physics based compared to the SPICE model.

The transient is modelled using two capacitors, connected in parallel (see figure 7.1). The modelling is based on the charge of the capacitors. The expressions are summarised in table 7.2. The diffusion capacitance is described in exactly the same way as the SPICE diode model. The description of the depletion capacitance is more complex, although the approach is the same as the SPICE model: a two-region definition is used to prevent the singularity at a large forward voltage. However, in this model a better expression is used, taking into account the effects of the doping gradient in the diode.

7.3 High-speed models for LEDs and lasers

There are many models for the high-speed behaviour of lasers, with different levels of sophistication. The base of each model is an equivalent circuit, derived from the laser rate equations [114]. This approach is extended in [115] to model the behaviour of quantum-well based lasers [116]. More advanced models include the modelling of carrier-capture and carrier-escape effects, as was described in section 6.3.1. Finally, comprehensive models including the

diffusion charge	$Q_D = TAU_T \cdot Id_f$
depletion charge	if $V_{AK1} < FC \cdot VD_T$
	then $Q_T = Q_{AT} \left(1 - \left(1 - \frac{V_{AK1}}{VD_T} \right)^{(1-P)} \right)$
	else $Q_T = Q_L + C_L \left(V_{AK1} - V_L \right) \left\{ 1 + \frac{P(V_{AK1} - V_L)}{2VD_T(1-FC)} \right\}$
with	$FC = 1 - \left(\frac{1+P}{3} \right)^{\frac{1}{P}}$
	$Q_{AT} = CJ_T \left(\frac{VD_T}{1-P} \right)$
	$C_L = CJ_T \left(1 - FC \right)^{-P}$
	$Q_L = Q_{AT} \left(1 - (1 - FC)^{(1-P)} \right)$

Table 7.2: Definition of the diode capacitances in the L500 diode model.

thermal and optical behaviour have been developed [117][118][119]. However, most models are only valid for lasers in a biased operation, as they assume that the laser operates in its linear region. These models are not suitable to study the large-signal modulation response of RCLEDs. Only very recently, a few advanced and adequate large-signal laser models have been proposed [120][121].

7.4   Derivation of the high-speed LED-model

In this section, the derivation of the high-speed model for RCLEDs is presented. The starting point is the rate equation (equation 6.2) and the voltage-carrier density relation (equation 3.16). Substituting the voltage relation in the rate equation, and rearranging the terms:

$$\frac{I}{qVol} = \frac{n_i}{\frac{mkT}{q}} \exp \left(\frac{qV}{mkT} \right) \frac{dV}{dt} + \frac{n_i}{\tau} \left(\exp \left(\frac{qV}{mkT} \right) - 1 \right) + Bn_i^2 \left(\exp \left(\frac{qV}{mkT} \right) - 1 \right)^2$$

The voltage V is the voltage drop across the active region, and I is the injected current in the active region. The injected current is written as the sum of three terms. The first term is the current through a voltage dependent capacitor. This capacitor represents the storage of carriers in the active region. This is the equivalent of the diffusion capacitance in the standard diode models. The second and third term represent the non-radiative and the radiative recombination currents. These last two terms can be represented by a voltage dependent current source. These three voltage-controlled circuit elements are the base of the equivalent circuit. This equivalent circuit describes the relation between the injected current in the active region, and the voltage drop across the active region.

The external current to the RCLED also includes the depletion current. This is modelled by placing this depletion capacitance (as defined in 6.13) in parallel with the basic equivalent circuit. Finally, a series resistance is included. This
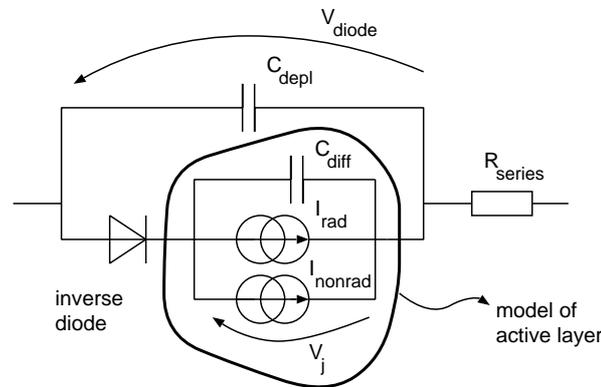
Figure 7.2: Circuit representation of the high-speed RCLED model, including the inverse current limiting diode (see paragraph 7.4.1).

implies that the drift-diffusion effects in the confinement region around the active region are neglected. In the next paragraph, an extension to the model will be introduced, which allows to model a drift-diffusion effect in the confinement structure. The resulting equivalent circuit is shown in figure 7.2.

7.4.1 The inverse current

As mentioned in the previous chapter, the inverse current of the RCLED at the off-switching transient is not well modelled by the simple RCLED rate equation. During the off-switching transient, the diode is connected to the ground by a series resistance. The carriers see a lower potential in the external circuit, and are extracted from the active layer. This is the inverse diode current. But these carriers must first overcome an energy barrier, which originates from the confinement structure in the RCLED, before they can flow into the external circuit (see figure 7.3). This energy barrier is not included in the model. In this paragraph, an extension of the model is presented, which allows a better modelling of the optical power at the falling edge.

The rate equation at the off-switching transient is given by:

$$\frac{dn}{dt} = -\frac{n}{\tau_{esc}} - \frac{n}{\tau} - Bn^2$$

The first term represents the carriers that are extracted from the active region. τ_{esc} is the carrier escape time, which is determined by the barrier height of the active region, and the inverse voltage over the RCLED. The second and third term represent the non-radiative and radiative recombination channels. The inverse voltage over the RCLED is determined by the external circuit. The inverse current is written as:
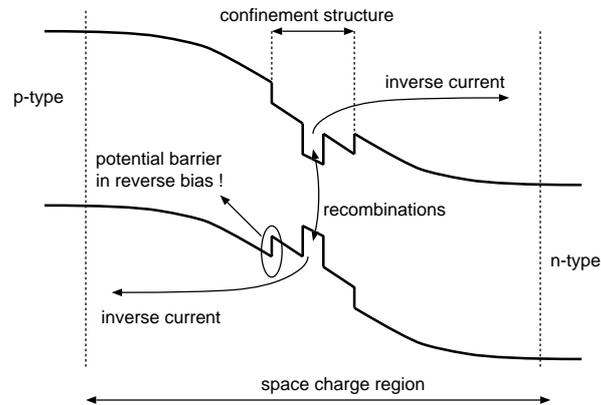
Figure 7.3: Band diagram of RCLED, at the off-switching transient.

$$I_{inv} = qVol\frac{n}{\tau_{esc}} \tag{7.1}$$

There are two competing carrier escape mechanisms: tunnelling and thermionic emission. Each mechanism is characterised by its escape time. The shape of the band diagram determines the dominant escape mechanism. In the RCLED, the band diagram is bended at the off-switching transient, due to the external voltage. The carriers in the confinement structure see a triangular potential barrier. This implies that the dominant mechanism is the tunnelling mechanism.

This energy barrier limits the inverse current from the RCLED. In an electrical diode, there is a (small) inverse current at the inverse regime, which acts as a current delimiter. This is exactly the functionality of the desired extra component in the model. Therefore, an extra diode is included in the model. The saturation current of this diode is given by the inverse current, as defined in equation 7.1. In practice, the escape time depends on shape of the band diagram, as explained above. However, in the model, a constant escape time is assumed. If was found that this approximation was sufficiently accurate to model the fall time of voltage-driven RCLED. The thermal voltage of the extra diode is chosen very small (5 mV), to minimise the influence of this diode in the forward regime of the RCLED.

Figure 7.4 shows the calculated fall time of the optical response of a voltage-driven 30-μm RCLED as a function of the escape time τ_{esc} (which is assumed to be constant). This fall time increases with increasing escape time. The calculated fall times are consequent with the measurements presented in section 6.5.2, in the sense that the measurements give an upper value for the fall times, which is in agreement with the calculations. This upper limit results from the limited bandwidth of the receiver in the experiments.
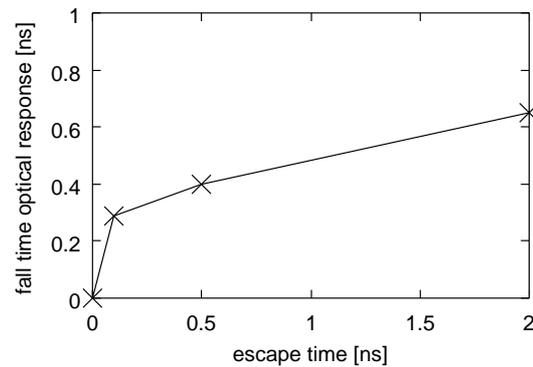
Figure 7.4: Calculated fall time of the optical response of a voltage-driven 30-μm RCLED, as a function of the escape time.

7.4.2 Implementation of the model

The model needs to be implemented so that the design engineer can use it in a fast, simple and reliable way to design the RCLED driver circuit. An implementation compatible with design software for electronic circuits is highly desirable. In this work, various implementations have been examined.

The biggest difficulty encountered during the development of the model was the implementation of the voltage - carrier density relation. In most circuit simulators, an Euler based integration method is used. The simulator calculates the carrier concentration at every time step, from which the voltage is calculated in the next time-step. However, depending on the operating condition and if the time step is too large, a negative carrier concentration can occur. Due to the nature of the (V, n)-relation, no voltage can be found for negative carrier concentrations. This situation can occur if the time-step for the integration is too large, or if there is an abrupt change in the drive current (during the off-switching behaviour, for example). A smaller time-step could solve this problem, but it was found that extremely short time steps were necessary to avoid the problem. Although most circuit simulators use advanced techniques to avoid such problems, it is the experience of the author that equivalent electrical circuits using non-linear function blocks experience major difficulties with these problems. Even mathematical tools as MatLab have problems with the equations. The Verilog-AMS[1] model was found to be quite robust against these problems.

Verilog-AMS is a mixed-signal behavioural modelling language: it allows to describe any system, independently on the physical properties of that system, at several abstraction levels [122]. It has a syntax for the set of nonlinear differential equations which describe the system, and it includes a calculation engine to solve the equations. There are two popular modelling languages:

---

[1] AMS stands for Analog Mixed-Signal.
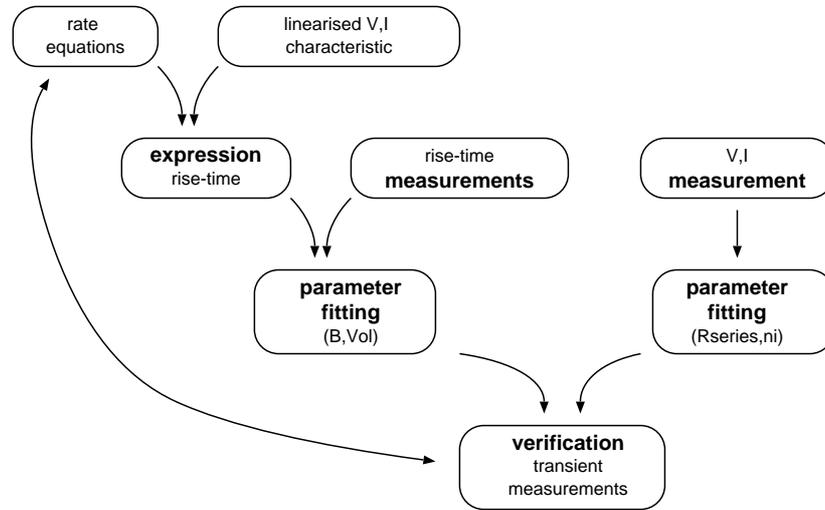
Figure 7.5: Flow-chart of the parameter extraction procedure.

VHDL-AMS (which is an extension of the VHDL modelling language for digital systems), and Verilog-AMS (an extension of the Verilog language). Such a modelling language is suitable to describe the RCLED high-speed model. In this work, Verilog-AMS was chosen, because of the seamless integration with the Cadence design environment for the design of electrical circuits. The complete modelling code is given in appendix A.

7.5   Parameter extraction procedure

In the previous paragraph, a high-speed model for LEDs (and RCLEDs in particular) was derived. Several parameters, such as the volume of the active region, were introduced. In this paragraph, a parameter extraction procedure is proposed, which allows to determine the unknown parameters of a device using a few simple measurements. This procedure is summarised in figure 7.5.

Firstly, some parameters were derived from DC-measurements. This was done using the technique presented in section 3.3. This allows to estimate the series resistance and the diode ideality factor (the m from mkT/q), from a single (V, I)-measurement. Once these parameters are known, the intrinsic carrier concentration in the active region (n_i, a parameter from the (V, n)-relation) is found by a manual fitting. Finally, parameters B and Vol can be estimated by fitting the measured rise time as a function of the drive voltage to the analytical expression, derived in paragraph 6.2.3. The fitting was done using an Excel sheet, by minimising an error between the measurements and the calculated rise times. The fitting of the rise time is done against an approximated expression, which might imply a loss of accuracy. However, this approach al-

RCLED	V_0	dV/dn	R_{series}	B	Vol	τ_{esc}
32 μm	1.31 V	1.10^{-19} cm^{-3}	17 Ω	1.3^{-10} cm^{3}s^{-1}	3.03^{-11} cm^3	600 ps
20 μm	1.31 V	1.10^{-19} cm^{-3}	20 Ω	1.3^{-10} cm^{3}s^{-1}	2.02^{-11} cm^3	600 ps

Table 7.3: Extracted RCLED parameters.
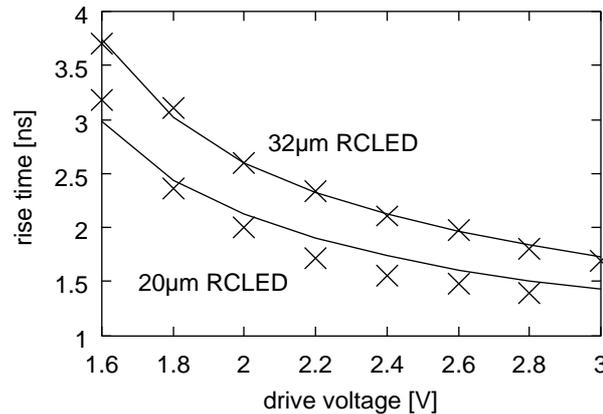
Figure 7.6: Measured and fitted rise times of voltage-driven RCLEDs.

lows much shorter calculation times compared to the use of the Verilog-AMS model, resulting in a faster fitting procedure. The measurement of the rise time was preferred, as it was a relatively simple and reproducible measurement. The expression for the rise time seemed to fit reasonably well to the measurements. Finally, the escape time was found by fitting the calculated fall time to the measurements. For this fitting, the Verilog-AMS model was used. The calculation did not take a long time, because only one parameter had to be found. The calculated fall times show a good agreement with the measurements for τ_{esc}=600 ps, for both devices.

The extracted RCLED parameters are summarised in table 7.3. The fitted volume of the active region is in agreement with the expected value. Figure 7.6 shows the measured and the fitted rise time, for the two RCLED types. The fitting is better for the largest devices.

7.6 Examples

In this paragraph, some results obtained using the high-speed model are shown. This first example is the fitting of the rise time of voltage-driven RCLEDs, as shown in the previous paragraph (figure 7.6). The high-speed model fits reasonably well to the measurements.

Figure 7.7 shows the calculated eye-diagram of a voltage-driven RCLED (diameter is 32 μm). This plot has to be compared with the measurement, as
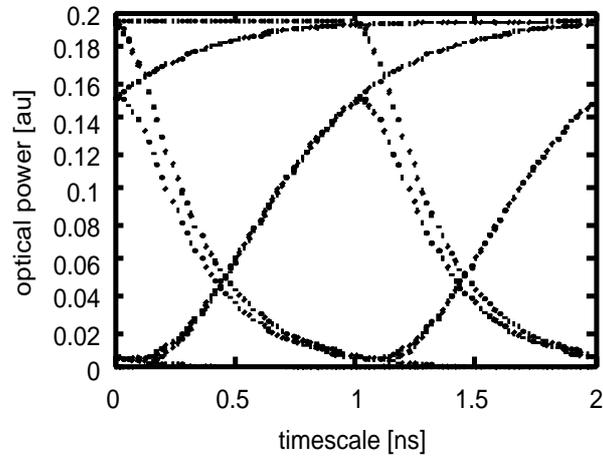
Figure 7.7: Calculated eye-diagram of voltage-driven RCLED using the high-speed model (to be compared with figure 6.6).

shown in figure 6.6. The calculated eye-diagram has the same specific features as the measurements: a slower rising edge, and a doubling of the falling edge due to the inter-symbol interference.

A third application of the high-speed model is the calculation of the small-signal response of RCLEDs. In experiments, a strange behaviour at low current densities is observed, as shown in figure 7.8. The calculation using the high-speed model shows the same behaviour. The origin of this effect is related to the measurement setup. A voltage signal is fed into the biased RCLED, with an amplitude of typically a few hundreds mV. This implies that the measurement is a good small-signal measurement if the characteristics of the device are (more or less) linear over that voltage range. This is not the case for diodes driven at a low current density: the voltage characteristic is highly non-linear at small current densities. In that case, the measurement setup resembles a voltage-driven RCLEDs, which results in much faster response times, as described in the previous chapter. This effect was also recognised by using the VerilogA high-speed model for RCLEDs.

7.7 Conclusion

In this chapter, a high-speed model for RCLEDs was presented. The derivation of the model was discussed, and compared to other diode models. The model was implemented in VerilogA, an mixed-signal behavioural modelling language, and compared to measurements. It was found that the modelling of the falling edge for voltage-driven RCLEDs needed special care. This was related to the barrier in the active region of the diode. A modification to the
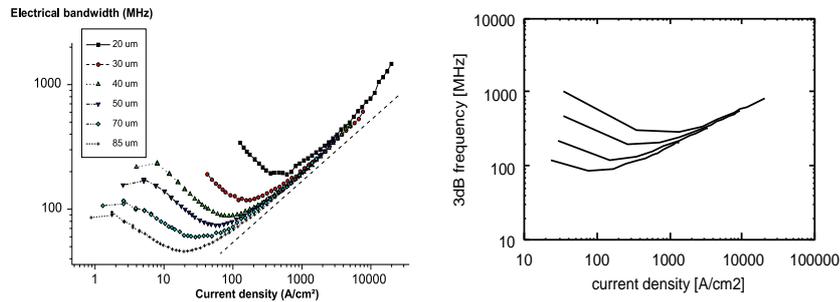
Figure 7.8: Measured (left, after [51]) and calculated (right) small-signal bandwidth as a function of the device diameter. The diameter corresponding to the calculated data are 10, 20, 50 and 100 μm.

RCLED model was proposed, which allows to model this behaviour in a better way. A parameter extraction procedure is proposed, which allows to determine all parameters in the model. Finally, the validation of the model was tested in three experiments, with a reasonable good agreement between the theory and the measurements.

Appendix A: Verilog-A code of the RCLED model

```
// VerilogA for "test", "ledmodel", "veriloga"
'include "constants.h"
'include "discipline.h"
//pins npin and ppin are the n and p contact of the LED
//pins pout and ref are contact of a current source, with current
//proportional to the output light power
module LED_betermodel(p_qw, pout, ref, npin, ppin);
output p_qw;
electrical p_qw;
output pout;
electrical pout;
output ref;
electrical ref;
inout npin;
electrical npin;
inout ppin;
electrical ppin;
// interne knoop
//electrical p_qw;
electrical p_hulp1;
electrical p_hulp2;
// parameters
```

```
parameter real kt_q=0.052;
parameter real q=1.6E-19;
parameter real ni=2E7;
parameter real R_um=10;
parameter real d_nm=20;
parameter real tau=10E-9;
parameter real b=1.3E-10;
parameter real cj_F_cm2=0.5E-07;
parameter real phi_V=2;
parameter real Vt=0.005;
parameter real tau_esc=0.6e-9;
parameter real hw_q=1.2;
parameter real n_extr=0.05;
// interne variabelen
real I_Cdepl;
real I_Cdiff;
real I_Rnonrad;
real I_Rrad;
real volqw;
real Cdepl;
real I_sat;
real n_qw;
analog begin
volqw = 3.1415*d_nm*1E-7*pow(R_um*1E-4,2);
Cdepl = cj_F_cm2*(3.1415*pow(R_um*1E-4,2));
V(p_hulp1,npin) <+ ddt(q*V(ppin,npin));
V(p_hulp2,npin) <+ ddt(q*V(p_qw,npin));
n_qw = ni*(exp((V(p_qw,npin))/kt_q)-1);
I_Cdepl = Cdepl/sqrt(abs(1-V(ppin,npin)/phi_V)) *V(p_hulp1,ref)/q;
I_Cdiff = q*volqw*ni*((1/kt_q)*exp(V(p_qw,npin)/kt_q))*V(p_hulp2,ref)/q;
I_Rnonrad = q*volqw*n_qw/tau ;
I_Rrad = q*volqw*b*n_qw*n_qw;
I_sat = q*volqw*(ni+n_qw)/tau_esc;
I(ppin,npin) <+ I_Cdepl;
I(ppin,p_qw) <+ I_sat*(exp((V(ppin)-V(p_qw))/Vt)-1);
I(p_qw,npin) <+ I_Cdiff+I_Rrad+I_Rnonrad;
I(ref,pout) <+ I_Rrad*hw_q*n_extr;
end
endmodule
```

Chapter 8

CMOS-integrated RCLED drivers

In the previous chapters, the speed performance of RCLEDs was studied, both theoretically and experimentally. This study resulted in the development of an accurate model for the transient response of RCLEDs. In this chapter, driver circuits for RCLEDs in CMOS technology will be developed and discussed. The design makes use of the RCLED model.

8.1 Requirements for drivers for parallel optical inter-chip links

The driver circuits for inter-chip parallel interconnects are strongly different from the standard driver circuits for stand-alone optoelectronic components. The design must fulfil different requirements:

- the circuits must be small: they will be integrated in the digital circuitry, and therefore the size is an important factor in the cost and the yield of the end product. This is a different situation compared to standard driver chips for single LEDs and lasers, where a larger die area is available.

- the driver circuit must be fast. The operation speed is determined by the digital circuitry. Currently, the typical data rates in computer busses is few hundreds Mbps, and high-speed busses operating at over 500 Mbps have been reported [123]. This data rate is assumed to increase further in the near future, as dictated by Moore's Law.

- the latency (this is the total delay) must be as small as possible. The delay generated in the driver and receiver circuits is more important in parallel optical interconnect links compared to long-distance interconnect links. In long-distance interconnects, the delay is mainly the time-of-flight of

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the optical pulse in the waveguide (typically 5 μs/km for glass fibres), and extra delays in the interface circuits are not so important. In short-distance optical interconnect links, the latency of the driver and receiver circuit is relatively more important.

- due to the compact size, there is less room for advanced cooling equipment. Therefore, the circuit must be efficient: the power dissipation and heat generation must be minimised.

- the circuit must fulfil the Electro Magnetic Compatibility (EMC) requirements: it must be immune to external noise sources, and it must generate no (or as small as possible) noise on the chip. The most important noise introduced in the circuits is the switching noise on the power supply lines.

These requirements are mostly in contradiction: a high-speed design requires a large current density, thus large power dissipation, whilst EMC compatibility requires advanced circuit designs, requiring a larger chip area.

8.2 Properties of CMOS

Today, CMOS is the most popular technology to realise integrated circuits. The scaling of the transistor towards smaller dimensions results in a larger performance increase compared to other technologies, as bipolar or GaAs based technologies. Therefore, it is very likely to assume that the next generations microprocessors in the foreseeable future will be realised in a CMOS technology. The electrical interface circuits of the parallel optical link will therefore be designed and realised in CMOS. In this paragraph, the basic properties of CMOS transistors will be given.

8.2.1 nMOS and pMOS transistors

In a nMOS transistor [111][124], a capacitor plate (the gate) is placed above a p-type semiconductor (see figure 8.1,A). The other plate of the capacitor is the p-type semiconductor. If the correct electrical field is applied (if the gate is positively charged compared to the bulk semiconductor), then the holes will drift away from the gate under the influence of the electric field, and a n-type channel is formed under the gate. This channel allows a current to flow between two predefined n-type islands in the p-type semiconductor. The conductivity of that n-channel is thus controlled by the gate voltage. The bulk is typically connected to the ground, and a current flows between the two n-type islands if a positive voltage is applied to the gate. By definition, the n-type contacts are the drain and the source, and the current flows from the drain to the source. This is the transistor operation of the nMOS transistor.

A pMOS transistor is similar to the nMOS transistor, but it is realised on a n-type semiconductor. This implies that the gate must be negatively charged
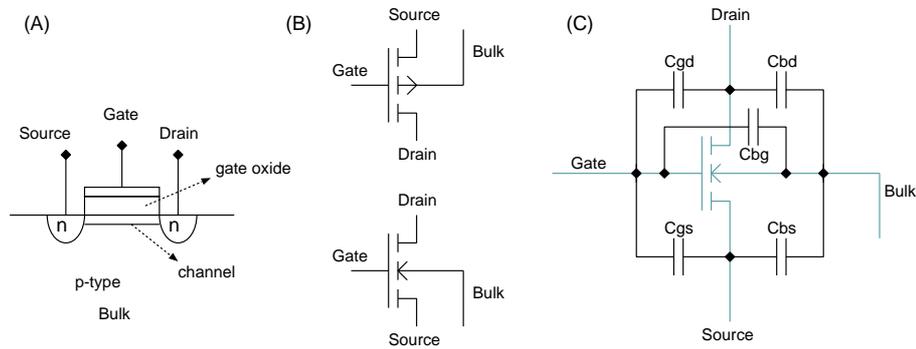
Figure 8.1: (A) Principle of nMOS transistor, (B) circuit symbol of pMOS (top) and nMOS (bottom), (C) high-speed model of nMOS.

region	condition	current
cut-off	$V_{GS} < V_t$	$i_{DS} = 0$
triode	$V_{GS} > V_t$, $V_{DS} < V_{GS} - V_t$	$i_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left[2\left(V_{GS} - V_t\right) V_{DS} - V_{DS}^2 \right]$
saturation	$V_{GS} > V_t$, $V_{DS} > V_{GS} - V_t$	$i_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_t\right)^2$

Table 8.1: Schichman-Hodges model for the nMOS transistor current.

compared to the semiconductor to build up a p-channel in the n-type bulk semiconductor. Therefore, the bulk semiconductor is connected to the supply voltage. Both transistors are available in a CMOS process (Complementary Metal Oxide Semiconductor). In general, the processing starts on a p-type silicon wafer. The nMOS transistors are easily fabricated on a p-type substrate, but they all share the same bulk semiconductor. The pMOS transistors are realised in a n-well, defined in the p-type semiconductor by an implantation. The wells of the pMOS transistors are thus easily isolated.

8.2.2 Current characteristics

In this section, a model for the drive current of the nMOS transistor will be presented. The simplest model (the Schichman-Hodges model [124]) describes the behaviour of the transistor in 3 regions. It is assumed that the source is connected to ground. The expression for the drain-source current is given in table 8.1. μ is the carrier mobility, C_{ox} the gate capacitance (per unit of area), W and L the width and length of the transistor, and V_t the threshold voltage. Sometimes, a parameter β is used, defined as $\frac{1}{2}\mu C_{ox}$. The transistor current is proportional to the carrier mobility. For silicon, the electron mobility is a factor 2.5 to 3 larger compared to the hole mobility. This implies that the nMOS transistor is capable to drive a 2.5 to 3 times larger current for a given W/L ratio compared to a pMOS transistor. This means that a pMOS transistor must be 2.5 to 3 times larger to drive the same current, implying a larger input capacitance

and a slower response. The drain-source current depends linearly on W, the width of the transistor. The current driving capability is sometimes expressed per unit of W. Typical values are 200 μA/μm. This is a rather small number: larger transistors should be used to drive moderate current levels.

In practice, the length of the gate must be replaced by the effective gate length, which takes into account the lateral diffusion of the n-type source and drain islands. The effective channel length is given by $L_{eff} = L - 2L_d$, with L_d the diffusion distance. The effective channel length has to be used if the properties of the channel are discussed. If the length of the gate oxide is discussed, then the true gate length L has to be used.

There is a small variation of the drain-source current with the drain-source voltage. The width of the space-charge region of the drain diffusion varies, resulting in a variation on the channel length. This is the Early effect. The drain-source current is written as:

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_t\right)^2 \left(1 + \frac{V_{DS}}{V_{early}}\right) = I_{DS,0} \left(1 + \frac{V_{DS}}{V_{early}}\right)$$

V_{early} is the Early voltage, typically a few tens of Volt. From this relation, an output impedance of the transistor can be defined:

$$R_{out} = \frac{dV_{DS}}{dI_{DS}} = \frac{V_{early}}{I_{DS,0}}$$

The threshold voltage V_t depends on the voltage at the source of the transistor (this voltage cannot exceed 0.7V: if the source-bulk voltage would be larger, then a large current would flow into the bulk). The threshold current is given by:

$$V_t = V_{t,0} + \frac{\sqrt{2q\epsilon N_A}}{C_{ox}} \left(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}\right)$$

The bulk might be biased in order to increase or decrease the threshold voltage. This might be beneficial to reduce leakage effect, or to enhance the current driving capability of the transistor.

These expressions are only valid for large transistors. Several adaptations and refinements have been proposed to match the equations with the experiments for sub-micrometer transistors [111]. In spite of the reduced accuracy, these simple equations will be used in this work to analyse driver circuits. This should allow to estimate the behaviour of the circuits. For the design of the driver circuits, and the determination of the transistor dimensions, a circuit simulator and advanced sub-micron models for MOS-transistors will be used.

8.2.3   The high-speed model for CMOS transistors

The time-dependent behaviour of CMOS transistors is complex. In first approximation, which is presented in most textbooks on transistors, linear capacitances are added to the equivalent circuit (see figure 8.1). Table 8.2 gives the

	cut-off	linear	saturation
C_{GB}	$C_{ox}WL_d$	0	0
C_{GS}	$C_{ox}WL_d$	$C_{ox}WL_d + \frac{1}{2}WLC_{ox}$	$C_{ox}WL_d + \frac{2}{3}WLC_{ox}$
C_{GD}	$C_{ox}WL_d$	$C_{ox}WL_d + \frac{1}{2}WLC_{ox}$	$C_{ox}WL_d$
C_{SB}	C_{jSB}	$C_{jSB} + \frac{1}{2}C_{CB}$	$C_{jSB} + \frac{2}{3}C_{CB}$
C_{DB}	C_{jDB}	$C_{jDB} + \frac{1}{2}C_{CB}$	C_{jDB}

Table 8.2: Overview of capacitance in CMOS transistor.

expressions for these capacitances. C_{jSB} and C_{jDB} represent the capacitance of the n-type source and drain diffusions in the bulk semiconductor. These junction are not biased, or reversely biased. The dominant factor is the depletion capacitance, as given by equation 6.13.

The most important parasitic capacitance of the transistor is the input capacitance of the transistor, given by $C_{GS} + G_{GD}$. In the saturation regime, this is given by:

$$C_{gate} = 2C_{ox}WL_d + \frac{2}{3}WLC_{ox} \approx \frac{2}{3}WLC_{ox}$$

This expression assumes that the under-diffusion distance of the source and drain regions is negligible compared to the transistor gate length.

The capacitance seen at the drain is given by:

$$C_{drain} = C_{GD} + C_{DB} = C_{ox}WL_d + C_{jDB}$$

Both capacitances depend linearly on the width of the transistor.

8.2.4 Non-uniformities

Due to several process-dependent factors, there is always a (small) difference between the characteristics of two transistors with identical dimensions within a circuit. This is in particular important when discussing the uniformity of the performance of circuits in arrays. In general, these deviations depend on the device size. The larger the devices, the more the local variations are averaged out, and the smaller the deviation on the transistor characteristics. The characteristics of the transistor are not described by a single number, but by random variables (typically a normal distribution). Table 8.3 shows the definition of the variation on the two most important transistor characteristics.

The non-uniformities can be generated by the circuit. Consider a non-uniform heat generation on the chip. This will result in a temperature gradient, and two transistors on a different place on the chip will see a different temperature, resulting in an extra non-uniformity. This might be important in some analogue circuit applications.

parameter	definition variation		typical value
threshold voltage	$\sigma_T = \sigma\left(\delta V_T\right)$	$\sigma_T^2 = \frac{A_T^2}{WL} + S_T^2 D^2$	$A_T = 10 \dots 20\ \mathrm{mV}\mu\mathrm{m}$
transconductance	$\sigma_\beta = \sigma\left(\frac{\delta\beta}{\beta}\right)$	$\sigma_\beta^2 = \frac{A_\beta^2}{WL} + S_\beta^2 D^2$	$A_\beta = 2 \dots 3\ \%\mu\mathrm{m}$

Table 8.3: Definition of the statistical variation on device parameters of CMOS transitors, and dependency of the variation on the dimensions (W,L) of the CMOS transistor parameters and the distance D between two transistors [126].

8.2.5 Future trends in CMOS transistors

The size of the transistor decreases continuously, as is forecast by the semiconductor roadmap [3]. This results in a faster transistor response: the gate capacitance decreases due to the smaller area, and the drive current increases due to the better W/L ratio. However, thinner gate oxides are used, and the drive voltage must also decrease, to prevent for transistor damage due to avalanche breakdown. Nowadays, the most advanced technologies (a 0.13 μm technology) use a 1.5 V supply voltage or even smaller. This implies that these processes provide special transistors for the input/output circuits, which are compatible with the 3.3 V swing signalling. The interface circuits for the optoelectronic devices in future CMOS based chips will certainly make use of these high-voltage transistors. However, the speed characteristics of the I/O transistors do not necessary scale like the digital transistors.

Next, advanced circuit techniques could be used to increase the current driving capability of the transistors. For example, a biasing of the bulk semiconductor can be used to decrease the threshold voltage of the transistor [127]. However, a smaller threshold voltage results in an increased leakage current, which is undesirable. Therefore, circuits are included to bias the bulk only if the transistor must drive the large current. For this technique, the bulk potential of the individual transistors need to be controlled. This is only possible if the bulk are electrically isolated. This is the case for pMOS transistors (which are realised in a n-well on a p-substrate). This techniques cannot be applied to nMOS transistors, because all bulks are electrically connected (expect if a double-well technology is used). As an alternative, a bootstrapping circuit can be used. The gates of the transistor are driven with a larger gate voltage, enhancing I_{DS} [128].

8.3 Overview CMOS driver circuits

In this section, several CMOS driver circuits will be presented. This includes the standard CMOS buffer, and an overview of literature on LED and laser drivers.
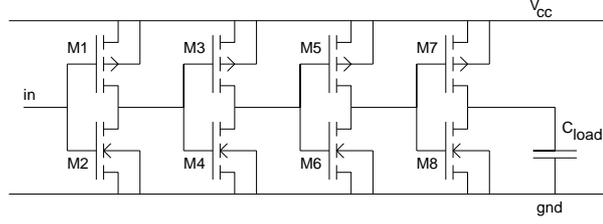
Figure 8.2: Circuit diagram of a tapered buffer circuit.

8.3.1   The CMOS buffer

As mentioned before, CMOS transistors are basically not suitable for driving high current levels. Due to the small μC_{ox}, a wide transistor has to be used for a given drive current level. Wide transistors have a large gate capacitance, which slows down the transistor response. The standard approach to speed up the response of a large transistor is the use of a tapered buffer (see figure 8.2), consisting of several inverter stages with successively larger transistor width.

For a given start and final value of the width of the transistors, an optimal number of stages can be calculated. Assume that N buffers are used, and that the first buffer has minimal dimensions (the length and the width of the transistor are equal to L_{min}). The output current of that minimal dimension inverter is i_0, and the input capacitance of the first buffer is given by C_0. The W/L of each buffer is a factor α larger, and the input capacitance of the final load is C_{load} (this is the input capacitance of the drive transistor of the RCLED). The drive current of stage n is given by $i_n = i_0\alpha^n$, the input capacitance of the same stage is given by $C_n = C_0\alpha^n$. The delay of stage n (which loads stage n+1) and the total delay are given by:

$$t_{delay,n} = \frac{\alpha^{n+1}C_0\Delta V}{\alpha^n i_0} \Rightarrow t_{delay,tot} = N\alpha\frac{C_0\Delta V}{i_0}$$

The number of stages is determined by the ratio of the load capacitance and the input capacitance of the first stage, and the α factor:

$$C_{load} = \alpha^N C_0$$

This allows to minimise the total delay as a function of α. The optimal value is given by $\alpha_{opt} = e$, from which the number of stages can be determined. A better analysis is given in reference [129]. There, it is shown that

- the rise time of a buffer is mainly determined by the linear regime of the transistor. The charging in the saturation regime is much faster. A better estimation for the delay is given by:

$$t_{delay} = \frac{2C_{load}V_t}{\mu C_{ox}\left(V_{dd} - V_t\right)^2} + \frac{C_{load}}{\mu C_{ox}\left(V_{dd} - V_t\right)}\ln\frac{19V_{dd} - 20V_t}{V_{dd}}$$

with V_{dd} the supply voltage.

- the delay between 2 stages is not a constant function.

In this work, tapered buffers will be used in the design of RCLED driver circuits. The approximated expression will be used to determine the taper circuit parameters. It was found that this approach gives good results.

8.3.2   LED and laser driver circuits

In this paragraph, a literature overview of driver circuits for active optical components will be presented. The driver circuits for optoelectronic components can be divided into two categories: the first group includes moderate-speed modules - up to a few hundreds Mbps - using standard technologies (mostly CMOS) and lasers or LEDs. Such circuits include several analogue or digital functions, as power monitoring circuits or data coding logic. The application fields of these circuits are optical LANs and optical access networks, for example for use in FTTH applications. The second group drivers are ultra-high-speed drivers, up to tens of gigabit, using very advanced semiconductor technologies, as SiGe transistors or InP or GaAs based MESFETs, HEMTs or HBTs [130]. The application fields of these advanced circuits are the ultra-high-speed long-distance telecommunication links. Currently, there is a trend to use the (low-cost) CMOS circuits at increasing bit rates, and CMOS-based circuits operating at 1.25 Gbps have been reported. In this work, only the first category will be discussed.

The simplest driver is a single transistor, as shown in figure 8.3. This circuit has been used by Kiamilev (reference [131]), as a VCSEL driver. The biasing current is set by a second drive transistor, connected in parallel with the modulating transistor. Modulation speeds up to 1 Gbps have been reported. However, this type of driver has, in spite of its simplicity, an important disadvantage. The RCLED current is set by the transistor dimensions and the supply voltage. In standard CMOS technologies, which are mostly optimised for digital circuits, the variation on these parameters can be quite high (see paragraph 8.2.4). This implies that there is a relative large uncertainty on the driver current, which is not desirable in parallel interconnects.

As an alternative, an external controlled current source can be included in the circuit (figure 8.3, b) [28]. The two pMOS transistors share the same gate voltage, and have therefore, the same output current. This is a current mirror. This circuits allows to multiply the reference current with a constant factor, simply by changing the (W/L) value of the output transistor. The deviation on the drive current will be much smaller. However, this driver might be more sensitive to cross-talk and external noise sources, because the reference signals are typically transported over long wires on the chip. Furthermore, this driver type induces large switching noise on the supply lines, just as the single-transistor driver. This can be compensated by including an extra capacitance on the supply lines. An alternative is shown in figure 8.3, c, where a differential pair is included in the circuit to switch the current between the RCLED
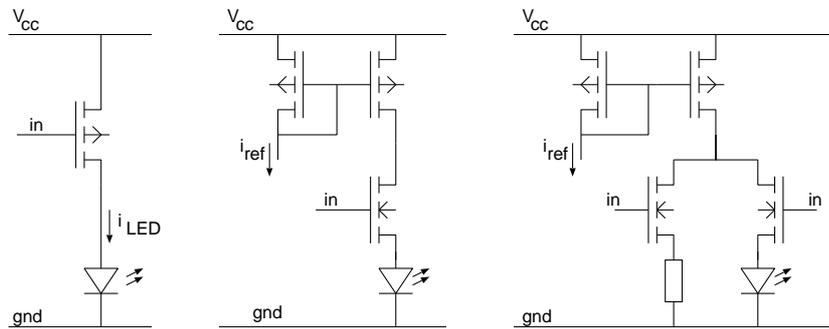
Figure 8.3: Overview of constant-current driver circuits.
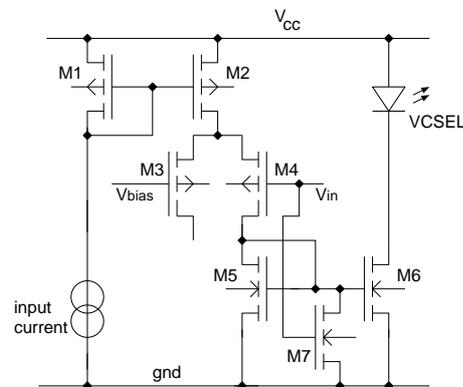
Figure 8.4: Circuit diagram of the Chen driver (after reference [133]).

and a dummy load. This driver circuit has been used in RCLED based parallel interconnect links [132]. However, there is a continuous power dissipation.

An advanced driver was reported by Chen [133]. The driver is shown in figure 8.4. The differential pair (M3 and M4) switches the input current between a dummy load and the second stage of the driver. The input voltage of transistor M3 (V_{bias}) has nothing to do with a biasing current: it is a reference voltage to switch the differential pair. The second stage is a current mirror (M5 and M6), which multiplies the input current and drives the VCSEL. This extra current mirror reduces the static power dissipation. An extra transistor M7 speeds up the off-switching transient by discharging the gates of transistor M5 and M6. The last stage of the current mirror (M5 and M6) is built up from nMOS transistors, allowing a faster switching of the VCSEL. However, this implies that the light emitters must be electrically isolated, or they must have a common p-contact.

An alternative driver circuit is shown in figure 8.5. This is the shunt-driver, in which the drive current is set by a source transistor, and the modulation
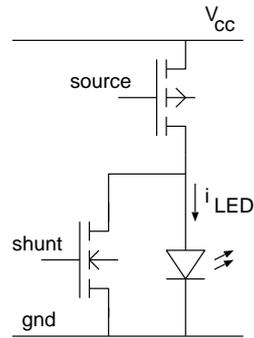
Figure 8.5: Circuit diagram of the shunt driver for VCSELs (after [134]).

CMOS	source (diameter)	speed	power dissipation	reference
0.8 μm	1.3-μm LED (I=80 mA)	155 Mbps	?	[28]
0.8 μm	980-nm RCLED	250 Mbps	15 mW	[132]
1.2 μm	1.3-μm edge-emitter	1 Gbps	4.3 mW @ 1 Gbps	[133]
1.2 μm	850-nm VCSEL	200 Mbps	5 mW @ 200 Mbps	[133]
0.5 μm	850-nm VCSEL	2.5 Gbps	7 mW @ 2.5 Gbps	[135]
?	VCSEL (3 μm)	1 Gbps	?	[136]
0.6 μm	850-nm VCSEL (I=8 mA)	1.25 Gbps	45 mW @ 500 Mbps	[131]
0.5 μm	960-nm VCSEL	1.25 Gbps	17.5 mW @ 3.3 V	[134]

Table 8.4: Overview driver circuits for optoelectronic light emitters (*) including buffers and VCSEL.

is achieved using the shunt transistor [134]. The switching is obtained using a nMOS transistor, allowing a faster response compared to pMOS transistors. Open eye-diagrams up to 1.25 Gbps have been achieved using this driver and flip-chip bonded VCSELs.

Table 8.4 gives an overview of different driver circuits for parallel optical interconnects found in literature, mostly for driving VCSELs.

In some circuits, the driver is designed to optimise the performance of the complete link, by shaping the optical pulse. The goal is to achieve a pulsed optical power waveform, to compensate for the limited bandwidth of the channel (the optical pathway). This is the optical equivalent of the pulsed current shape which compensates for the limited bandwidth of the light emitter. However, it is not possible to realise a negative optical power: the optical pulsing is only possible at the rising edge of the signal. This type of driver is sometimes called a pre-equalisation driver. An example of such a driver circuit has been proposed in [136]. During every first ONE-bit after the transmission of a ZERO-bit, a larger current is driven to the light emitter (see figure 8.6). Using this circuit technique, a 9.5 % greater eye-opening at 1 Gbps is achieved. It is interesting to note that this pre-equalisation principle is an alternative to the pulsed-current
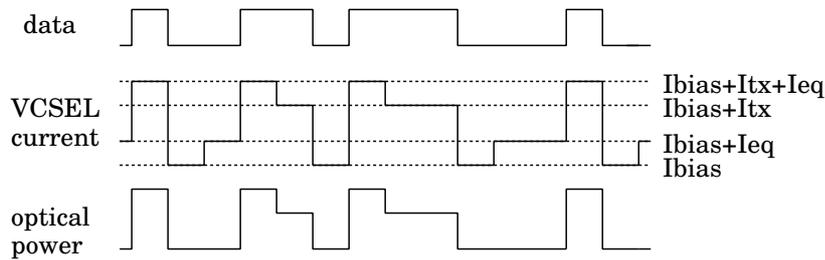
Figure 8.6: Pre-equalisation driver principle (after [136]).
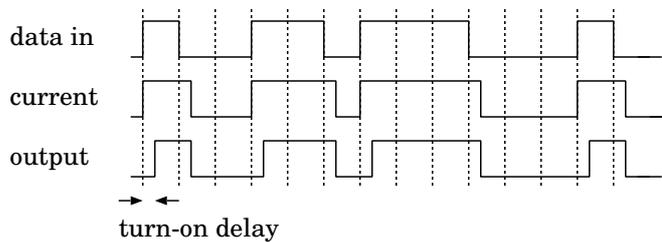
Figure 8.7: Turn-on delay compensation circuit.

principle discussed in the previous chapter. In this circuit, the pulsing is done in the data domain: the amplitude of the individual bits is adapted. This is different from the pulsed driver approach, discussed in section 6.7.5, where the pulsing was done inside the bit.

Laser drivers include sometimes advanced circuitry to compensate for the turn-on delay of the optoelectronic device. Two techniques can be used: the shape of the driving pulse is optimised, or the bit sequence is monitored, and a variable delay is inserted in the bit string depending on the bit sequence: the drive transistor starts to drive the laser earlier if a new one symbol has to be transmitted [137] (see figure 8.7).

8.4 Influence of CMOS parasitics on driver performance

During the switching, the optoelectronic component is charged or discharged. In the same time, the parasitic capacitances of the driver circuit are also charged or discharged. This charging takes away a (small) current from the driving transistor, slowing down the response of the optoelectronic component. In this section, the influence of the driver parasitics on the switching of the RCLED is investigated.
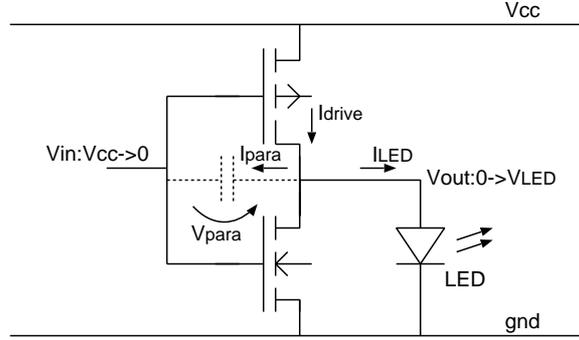
Figure 8.8: Circuit diagram of a RCLED-driver stage, including the parasitic capacitance.

8.4.1 The parasitic capacitance

The RCLED is driven by a CMOS stage, as given in figure 8.8. The parasitic capacitance of the driver is mainly determined by the drain-gate overlap capacitor. During switching, the parasitic capacitance is discharged. The charge injected in the parasitic capacitor depends on the capacitance C_{para} and the voltage swing ΔV_{para}:

$$\Delta Q_{para} = C_{para} \Delta V_{para} = C_{para}(V_{cc} + V_{led}) = C_{eq} \Delta V_{out}$$

An equivalent capacitance C_{eq} is introduced, which is connected to the ground, in which the same amount of charge is accumulated during the switching as in the parasitic capacitance:

$$C_{eq} = C_{para} \frac{V_{cc} + V_{led}}{V_{led}}$$

This equivalent capacitance is thus larger than the physical capacitance in the circuit. This is explained by the fact that the physical capacitance is connected to a floating node: the input node of the CMOS stage. This implies that there is a larger voltage swing over the parasitic capacitance, compared to an equivalent capacitor connected to the ground.

8.4.2 Influence on the RCLED dynamics

At the on-switching transient, the pMOS transistor will drive a current, that charges both the RCLED and the parasitic capacitance of the CMOS driver. The current relation during start-up is given by:

$$I_{drive} = C_{eq} \frac{dV}{dt} + I_{inj}$$

With V the voltage drop across the junction, and I_{inj} the RCLED current. The voltage over the RCLED is approximated by the linear relation 6.12, the injected current is written as a function of the carrier density, as given by the rate equation 6.2. The expression reduces to:

$$\frac{dn}{dt}\left(1 + \frac{C_{eq}V_{j,0}}{qVoln_0}\right) = \frac{I_{drive}}{qVol} - \frac{n}{\tau} - Bn^2$$

This is the adapted version of the rate equation for the RCLED, taking into account the parasitics of the driver circuit. The expression $qVoln_0/V_{j,0}$ has the dimension of a capacitance, and is written as C_{LED} (see section 6.2.3). The resulting equation has the same form as the original rate equation. Assume that the non-radiative recombination is negligible, then the rise time is given by:

$$t_{rise} = 1.49\left(1 + \frac{C_{eq}}{C_{LED}}\right)\sqrt{\frac{qVol}{BI_{drive}}}$$

The rise time depends linearly on the parasitic capacitance of the driver circuit. The output capacitance of the driver circuit should be minimised, by decreasing the width of the output transistor. However, this also reduces the output current, which results in a slower RCLED response. There is thus an optimal transistor width, for which both effects are minimised. Both the equivalent output capacitance of the driver C_{eq} and the drive current I_{drive} can be written as a function of the width of the output transistor, and the rise time can be minimised as a function of this width. The optimal width of the output transistor is given by:

$$w_{opt} = \frac{C_{LED}}{C_{ol}}$$

with C_{ol} the overlap capacitance of the output transistor, per unit of width. This capacitance is typically very small, resulting in a large optimal width of the output transistor. This implies that the influence of the parasitic capacitance of the output transistor is only important for very wide transistors (in the mm range). Consequently, the influence of the this output capacitance can be neglected.

The most important parasitic effect in the driver is the (internal) charging of the gate capacitance of the output transistor. This is shown in figure 8.9, where the simulated rise time is shown as a function of the width of the driving transistor. The simulations were done using the Cadence Design suite, and the AMS 0.6 μm library, and the high-speed RCLED model developed in the previous chapter.

At the off-switching transient, it is assumed that the off-switching transistor works in its linear regime. The voltage drop across the transistor is V_{LED}, typically 1.4V. At the off-switching transient, the transistor is connected to this RCLED. This implies that the drain-source voltage of this transistor is equal to
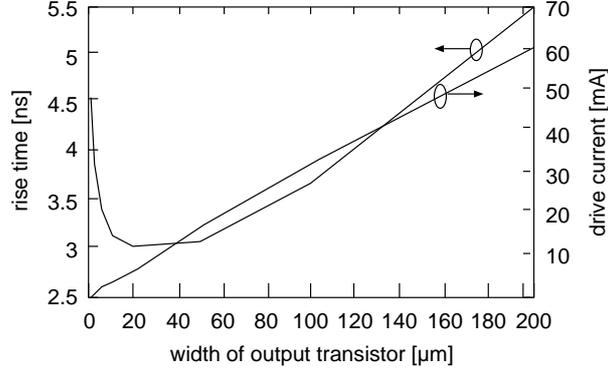
Figure 8.9: Simulation of the optical rise time of a RCLED driven by a CMOS transistor, as a function of the width of the output transistor.

V_{LED}. This transistor works in its linear regime, since $V_{LED} < V_{GS} - V_t$. The channel resistance R_{ch} is given by:

$$R_{ch} = \frac{V_{DS}}{I_{DS}} \approx \frac{1}{\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_t\right)}$$

This resistance is typically a few hundred Ω.

The inverse current from the RCLED is the resistive current over the transistor, and the capacitive current which discharges the parasitic capacitances from the driver circuit:

$$0 = C_{eq}\frac{dV}{dt} + \frac{V}{R_{ch}} + I_{inj}$$

This expression can be transformed in an equivalent rate equation, which is given by:

$$\frac{dn}{dt}\left(1 + \frac{C_{eq}}{C_{LED}}\right) = -\frac{1}{qVol}\frac{V_{j,0}}{R_{ch}} - \frac{V_{j,0}}{R_{ch}}\frac{n}{qVoln_0} - \frac{n}{\tau} - Bn^2$$

This equation is valid as long as the carrier density is positive. The fall time can be found by solving the differential equation, and calculating the time at which the carrier density equals zero:

$$t_{fall} = \left(1 + \frac{C_{eq}}{C_{LED}}\right) R_{ch}C_{LED} \ln\left(\frac{n_{ini}}{n_0} + 1\right)$$

n_{ini} is the initial condition for the carrier density in the active region, this is determined by the steady-state current. This equation shows that the influence of the output capacitance is negligible, because $C_{eq} < C_{LED}$ for a realistic width of the output transistor.

8.5 Design of high-speed RCLED driver circuits

In this section, the design of circuits optimised for driving RCLEDs is presented. The key feature of the drivers is their ability to generate a peaked current pulse, both at the on-switching and off-switching transient. This pulsed-current driver principle allows a high-speed operation of RCLEDs, as was discussed in paragraph 6.7.5. The on-switching transient is accelerated by injecting a current pulse, which fills the active layer (almost) immediately. The off-switching transient is accelerated by applying an inverse current pulse, which empties the active layer much faster than any recombination mechanism. In all driver designs, the inverse current is obtained by using a short-circuit transistor. It was found that this works very well. The generation of the on-switching current pulse is different for the designed driver circuits. Two principles are used: two pulses can be combined to form a pulsed current, or a current can be subtracted from the original current pulse.

In this thesis, three driver circuits were designed, as cells which can be integrated in any design. The cells were designed using the Cadence software system. Three different designs were done in a CMOS 0.6 μm technology from AMS[1], type CUB CX06AA [138]. This process includes 0.6 μm minimal feature size, and starts from a p-substrate (thus nMOS is easily done, a pMOS is made in a n-well). The maximal supply voltage is 5 V. It includes two metal layers (for interconnects) and one polysilicon layer (for the transistor gates). A single gate delay is 0.12 ns (a NAND gate), according to the specifications.

8.5.1 The combined pulse driver

This type of driver is based on reference [131], where it is used to drive VCSELs. The driver consists of 2 transistors, one driving the biasing current, one driving the modulation current to the VCSELs. In this work, one transistor drives the injection current, the other transistor drives the peak current (see figure 8.10). A delay line is implemented in the design, to drive the pulse transistor. Both transistors are driven by an inverter chain, as discussed in paragraph 8.3.1, to minimise the delay of the driver.

The dimensions of the transistor were obtained by simulations using the Cadence design environment and the high-speed model for RCLEDs. Rise times as small as 375 ps and fall time of 410 ps were obtained, for a 20-μm RCLED and 3.3 V supply voltage. Unfortunately, this driver introduces a large current variation on the supply lines, which increases the on-chip noise. This can be compensated by an extra capacitance, if necessary.

8.5.2 The C-tank driver

In this driver, the pulse shape is also built up by combining two pulses. However, the second current pulse is not delivered by a second transistor, but deliv-

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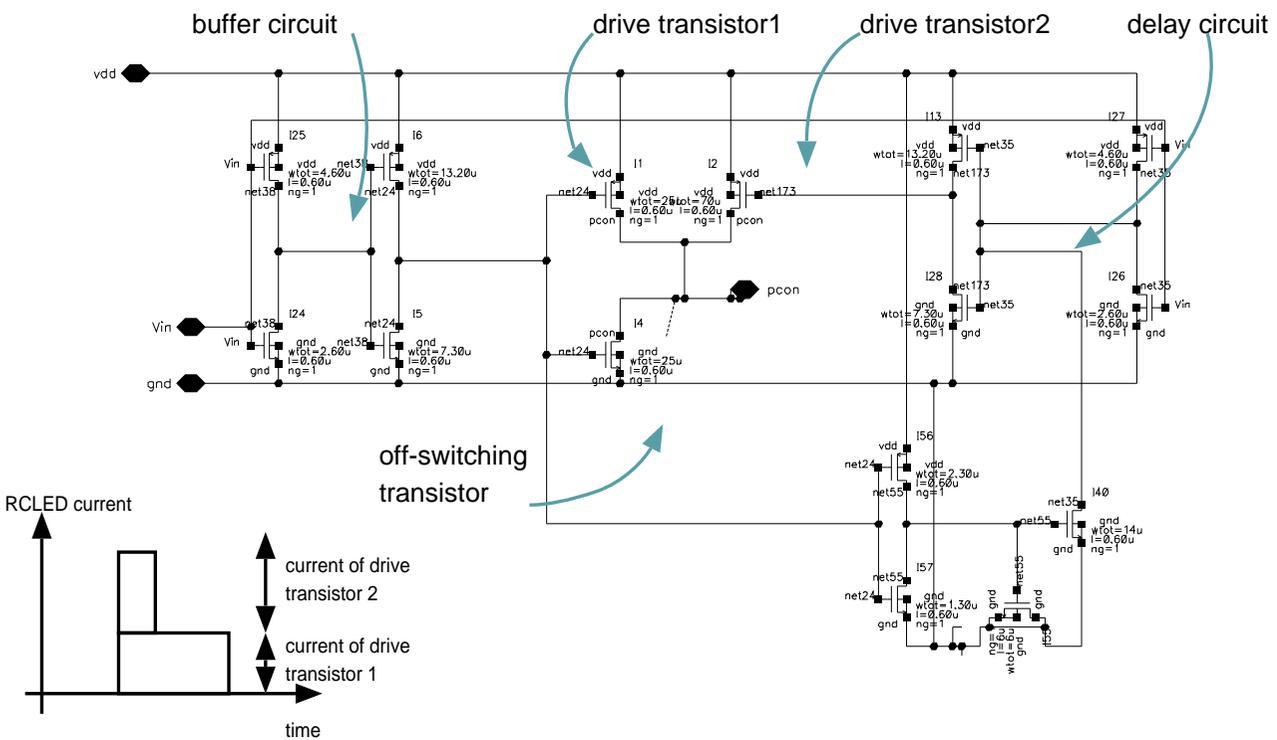[1]AMS stands for Austria Micro Systems.

Figure 8.10: Circuit diagram of the combined pulses driver.

ered by an extra capacitor (the tank capacitor). This capacitor is charged during the transmission of ZERO bits. This charge is then injected in the RCLED at the transmission of a ONE-bit. In this way, the current variations on the supply lines are minimised. However, the charging of the tank capacitor results in a small current dissipation during the transmission of ZERO bits, increasing the power dissipation. This type of driver is called a C-tank driver. There is no need for a delay-circuit, but a rather large tank capacitor needs to be implemented.

The tank capacitor can be dimensioned as follows. The charge that has to be injected in the RCLED is given by:

$$Q = nqVol = I_{inj}\sqrt{\frac{qVol}{BI_{inj}}}$$

This charge is injected from the tank capacitor. If the voltage over this tank capacitor is switched from V_{cc} to V_{LED}, then the charge extracted from the tank capacitor is given by $Q = C_{tank}(V_{cc} - V_{LED})$. The charge is injected in the tank capacitor during a single period. This condition sets the minimal bit period as a function of the RCLED drive current: $Q = T_{bit}I_{inj}$. As a consequence, there is a minimal bit period for this type of driver:

$$T_{bit} > \sqrt{\frac{qVol}{BI_{inj}}}$$

The rise time of this type of driver is thus a factor of 1.49 shorter than that of a constant-current driven RCLEDs. In practice, this type of driver performs better, as it allows to compensate for the parasitic capacitances of the driver by increasing the tank capacitor. The pulse width is determined by the tank capacitor and the series resistance of the interconnection between the tank capacitor and the RCLED (including the channel resistance of the driving transistor).

The calculated rise and fall times for 20-μm RCLEDs are 760 ps and 400 ps. This is slightly longer than that of the combined pulses driver, as expected from the presented analysis. The corresponding tank capacitor is 3 pF. This corresponds to a 60×60 μm large capacitor, if a linear metal-oxide-metal capacitor is used. However, a more elegant solution makes use of the gate capacitance of a transistor. This has a larger capacitance per unit of area, but it is a non-linear capacitor. Fortunately, the linearity of the capacitor is not important in this application. The size of the resulting capacitor is 28×35 μm.

8.5.3 The constant current driver

In the third driver design, a constant current is drawn from the current supply, which is driven entirely into the RCLED during the pulse (both off-switching transistors are off), and only partially to the RCLED during the static part of the transmitted bit (off-switching transistor 2 starts to conductor after a delay, set by the delay circuit).
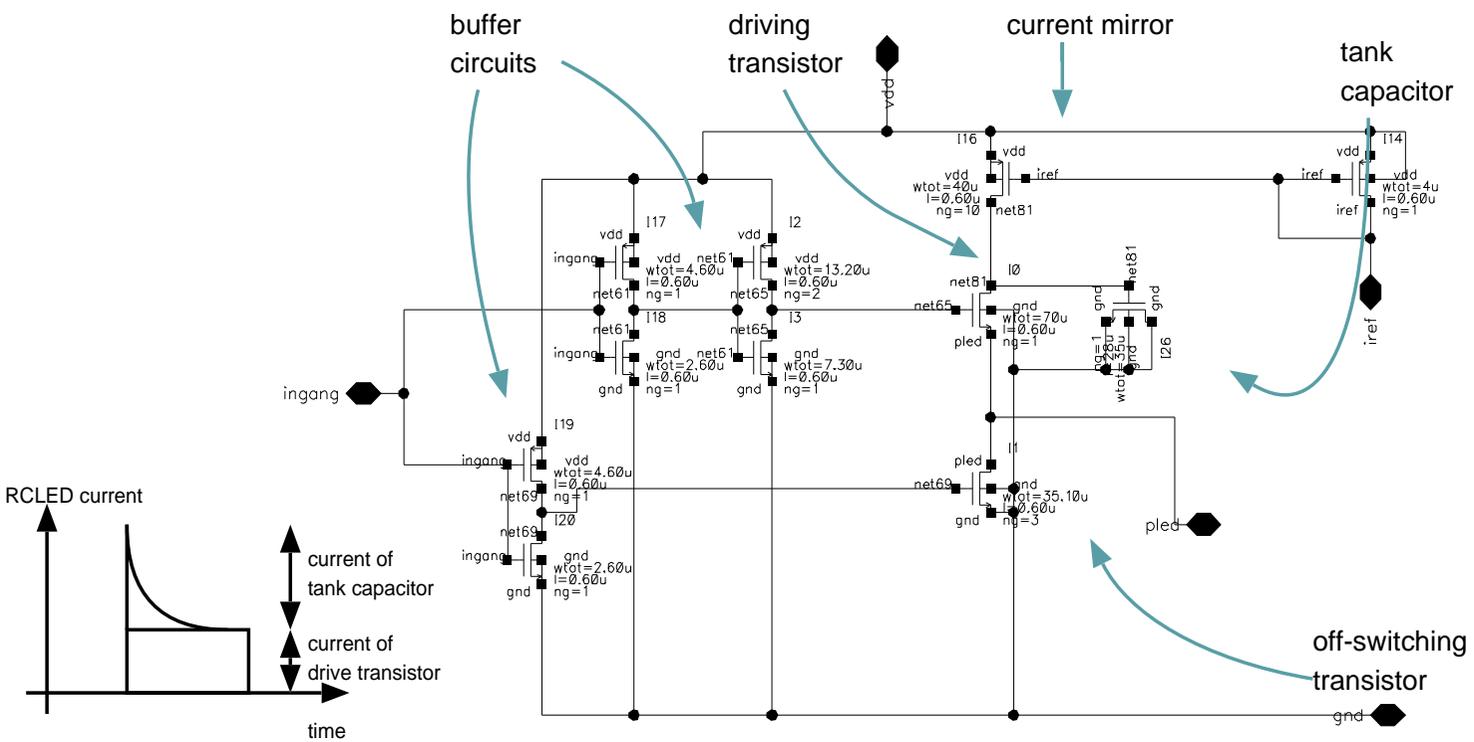
Figure 8.11: Circuit diagram of the C-tank driver.
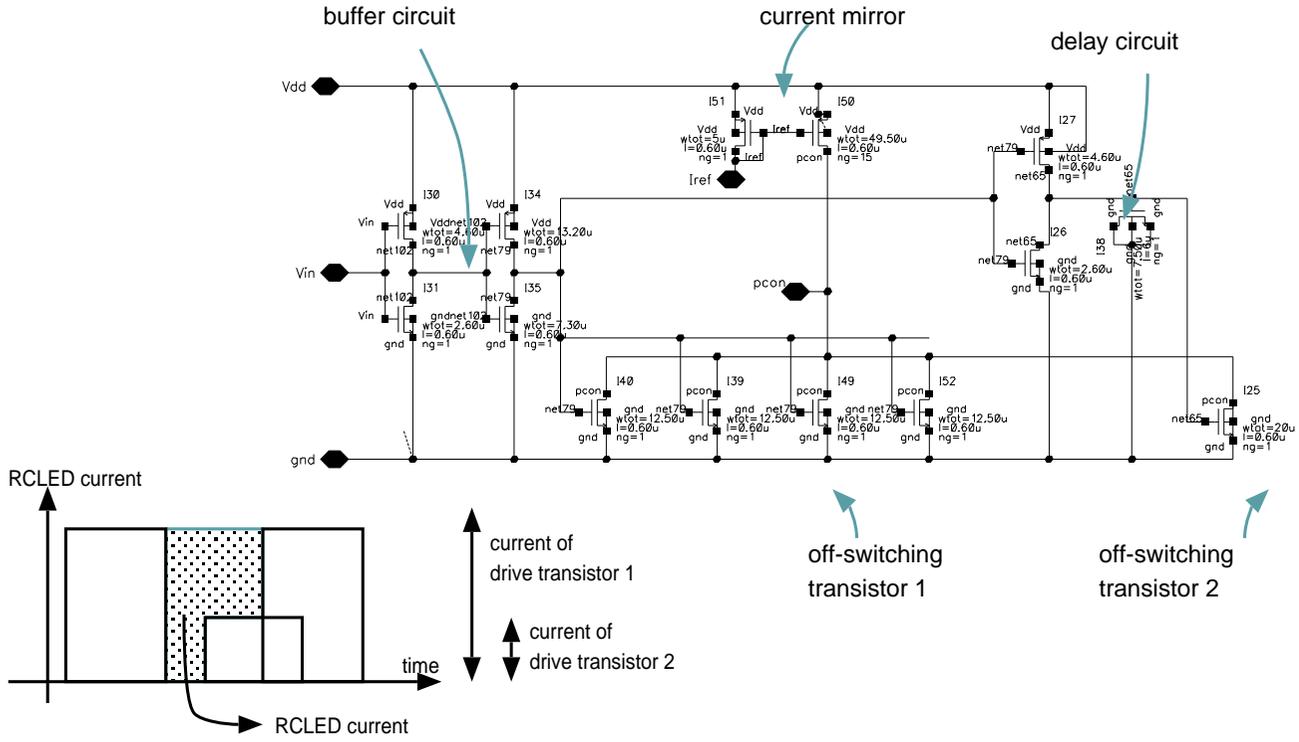
Figure 8.12: Circuit diagram of the constant current driver.
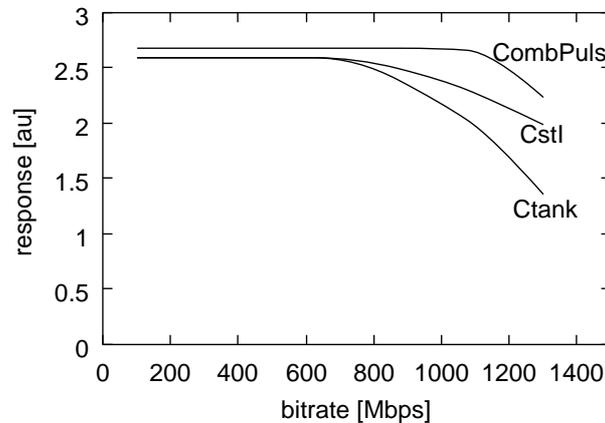
Figure 8.13: Comparison of simulated performance of the three driver designs.

This design results in a low-noise driver design, because a constant current is drawn from the supply source. However, there is a continuous power dissipation. In the design, a 8 mA current is drawn, setting the amplitude of the current pulse. This implies a continuous power dissipation of $8 \times 3.3 = 26mW$. The switching is obtained by using n-MOS transistors, which can be chosen smaller than a pMOS transistor driving the same current level. This should result in a faster design. However, the transistors in this design must drive a relatively large current (up to 8 mA for the current mirror transistors), resulting in large parasitic capacitance.

The simulated rise time for a 20-μm RCLED is 650 ps, the fall time is 390 ps. The overall performance of the driver is thus comparable to the other designs.

8.5.4 Comparison of the driver designs

Three driver designs, all generating a pulsed current shape, show sub-nanosecond rise and fall times, when driving a 20-μm RCLED. Figure 8.13 shows the calculated peak-to-peak response of the driver-RCLED combination, when a square wave input was applied. All drivers cease abruptly to operate with increasing bit rate, at around 1.4 Gbps. This is explained by the fact that the inverse current pulse has not completely disappeared at the end of the ZERO period, resulting in a bad signal. The combined pulses driver is the fastest, showing over 1 Gbps operation, according to the simulations.

The annotated lay-out of the three designs is shown in appendix B.

8.6 Experimental results

In this paragraph, an overview of measurements on RCLED-driver modules is presented. Two driver chips were available: the GLTXIMEC chip contain-
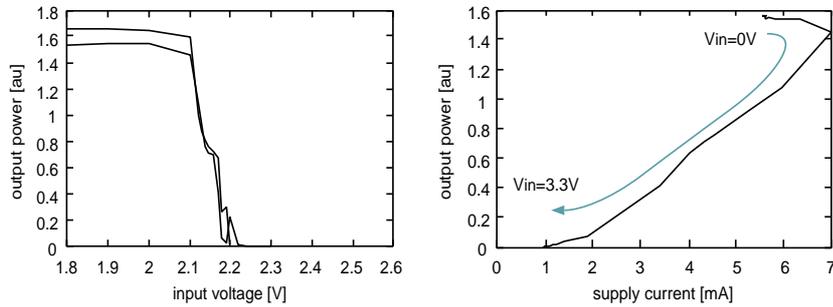
Figure 8.14: Measured DC characteristics of combined pulse driver: output as a function of the input voltage (left, for two different drivers), and output power as a function of the supply current (right).

ing the driver circuits discussed in the previous paragraph, and the GLTXLP chip containing another pulsed-current driver circuit. Unfortunately, too large RCLED diameters were mounted on the chips. This implied that the desired bit rate will not be obtained.

8.6.1 The GLTXIMEC chip

A 4×8 array of 32-μm RCLEDs was mounted on the chip. The chip was directly probed using needles. This complicates the impedance matching of the chip. A 50 Ω resistor was soldered between the probing needles, but this is not a perfect impedance matching. The inductance of the needles, and the wires towards the needles could not be compensated. This mismatching certainly influenced the high-speed measurements. Nevertheless, some characteristics of the driver-RCLED combination were measured. On the GLTXIMEC chip, only the combined pulses driver was characterised.

Figure 8.14 shows the measured DC characteristics of the combined pulses driver. The driver works as an inverter: if the digital input is HIGH, then the RCLED is switched off. The threshold voltage (about 2.15 V) is set by the properties of the input CMOS buffer, a standard cell from the AMS library. The same plot shows the measured optical output power as a function of the supply current, when only one driver is operational. The supply current is given by the RCLED current, and the supply current of the buffer and the driver circuit. A part of the total supply current is proportional to the optical output power. This represents the RCLED current. During switching, there is an extra current added to the RCLED current. This is the supply current of the driver and the buffer circuits. The power dissipation of the driver and buffers originates from the fact that during the switching, both nMOS and pMOS transistor are conducting a (small) current. This current is not negligible, the maximal amplitude is estimated at 1.8 mA from this measurement. If the digital input voltage is low, then the supply current is mainly determined by the RCLED
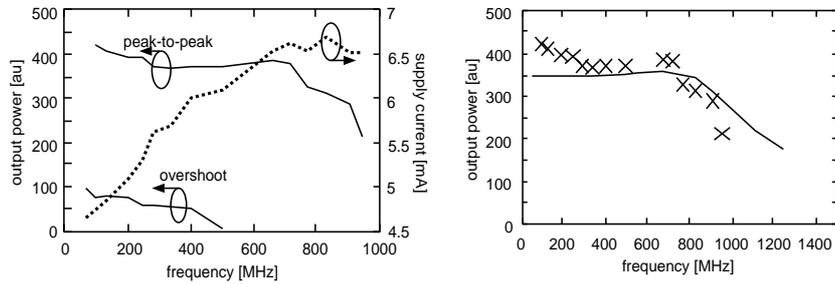
Figure 8.15: Measured speed response of combined pulses driver: peak-to-peak response and optical overshoot as a function of bit rate, and measured supply current as a function of bit rate (left), and comparison with simulations (right, full line is simulation, crosses are measurements).

current.

Figure 8.15 shows the measured speed characteristics of the driver. The optical overshoot was not taken into account when the peak-to-peak response is measured (the measurements represent thus the static part of the pulse). The plot also shows the measured supply current. This supply current increases as a function of the switching rate. The linear increasing part is attributed to the buffer and driver circuit, as was discussed previously. The measurements of the static response are compared to the simulations, with a reasonable agreement, except at the very high frequencies.

Measured eye-diagrams at 400 Mbps and 660 Mbps are shown in figure 8.16. There is clearly some optical overshoot, resulting in a faster rise time. This indicates that the pulse amplitude or the pulse width (both set on-chip) are larger than expected.

8.6.2   The GLTXLP chip

A second chip with high-speed RCLED drivers was available for measurements. The chip was designed at ETH Zurich, in the framework of the OIIC project [139]. This chip, with the RCLED array, was mounted on a glass carrier with impedance matched transmission lines, SMA connectors and a 50 Ω impedance matching resistor close to the CMOS chip. This allows to do better high-speed measurements.

The driver circuit allowed to drive pulsed current shapes [139]. The principle is summarised in figure 8.17. The peak current is set internally on the chip, and can only be influenced by the supply voltage. The drive current is set by a reference current, and the pulse width can be controlled through a reference voltage signal. A large reference voltage results in a small pulse width. The same figure shows the measured rise time as a function of the reference voltage. The pulse width equals the bit period if the reference voltage is zero volt. In that case, the output power and the rise time do not depend on the reference
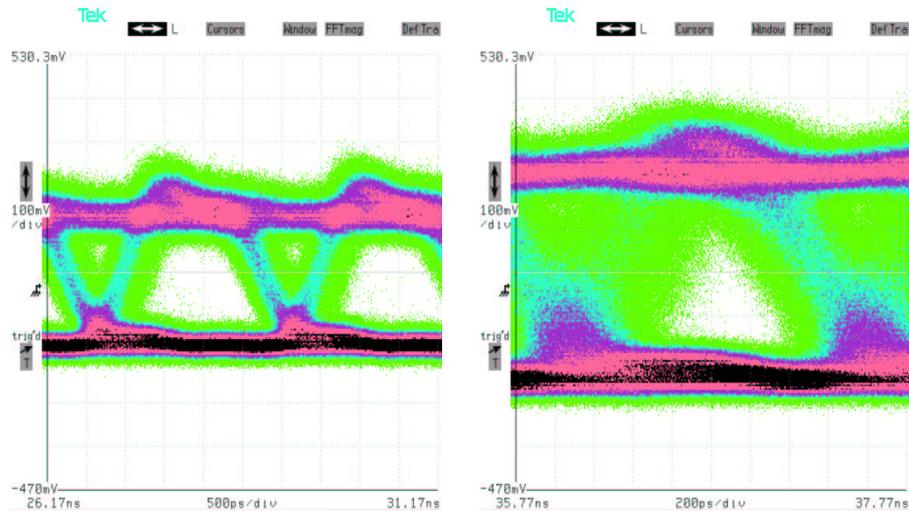
Figure 8.16: Measured eye-diagrams of the combined-pulse driver at 400 Mbps and 660 Mbps.

current. This corresponds to a constant current-driven RCLED, with a rather large drive current. On the other hand, if the pulse width is very small (corresponding to a large reference voltage), then there is no influence of the current peak. At intermediate reference voltages, the pulse width is sufficiently wide to fill the active layer, but not too wide to induce an optical overshoot. This corresponds to a strong reduction of the rise time.

Figure 8.18 shows the measured rise time as a function of the static current level, without current pulsing (by applying a very large reference voltage) and with current pulsing (the pulse width was actively optimised). The driving of RCLEDs using a pulsed current leads to an important decrease of the rise time, especially at very small drive currents, as was discussed in section 6.7.5.

The influence of the current pulsing is visualised in figure 8.19, where measured eye-diagrams at 400 Mbps are shown as a function the reference voltage. If the pulse width is too wide, then there is an important optical overshoot. There is an important jitter at the downward transition: up to three distinct lines are visible. It is believed that this jitter is caused by a slow switching of one or more transistors inside the driver circuit. Most probably, the input capacitance of the off-switching transistor is driven by a buffer with a too small output current. This implies that the voltages at the internal nodes in the driver are not at their static value at the end of the bit. Depending on the number of preceeding ONEs, some transistors in the circuit are still driving some current,
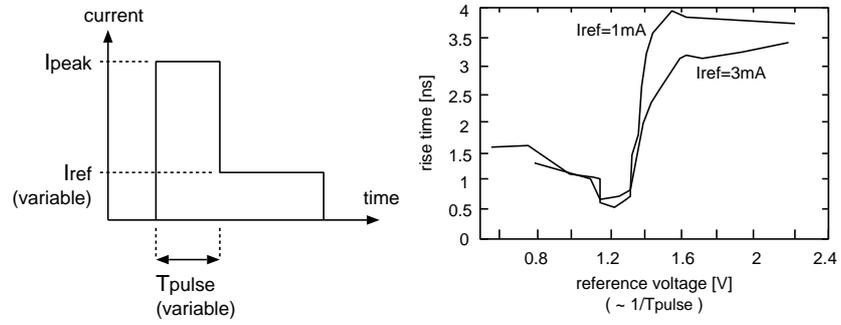
Figure 8.17: Driver principle of GLTXLP driver and measurement rise time.
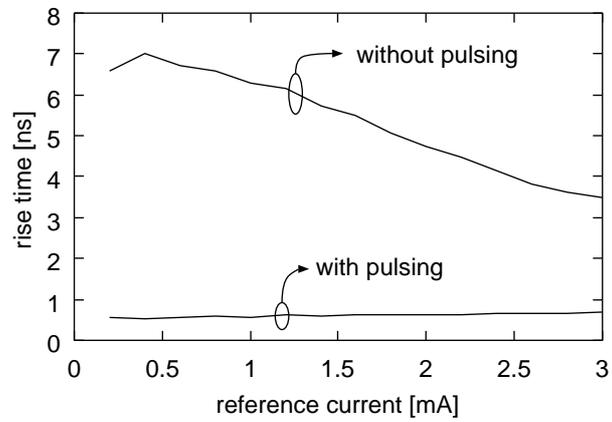
Figure 8.18: Comparison of rise time of driver with and without current pulsing principle.
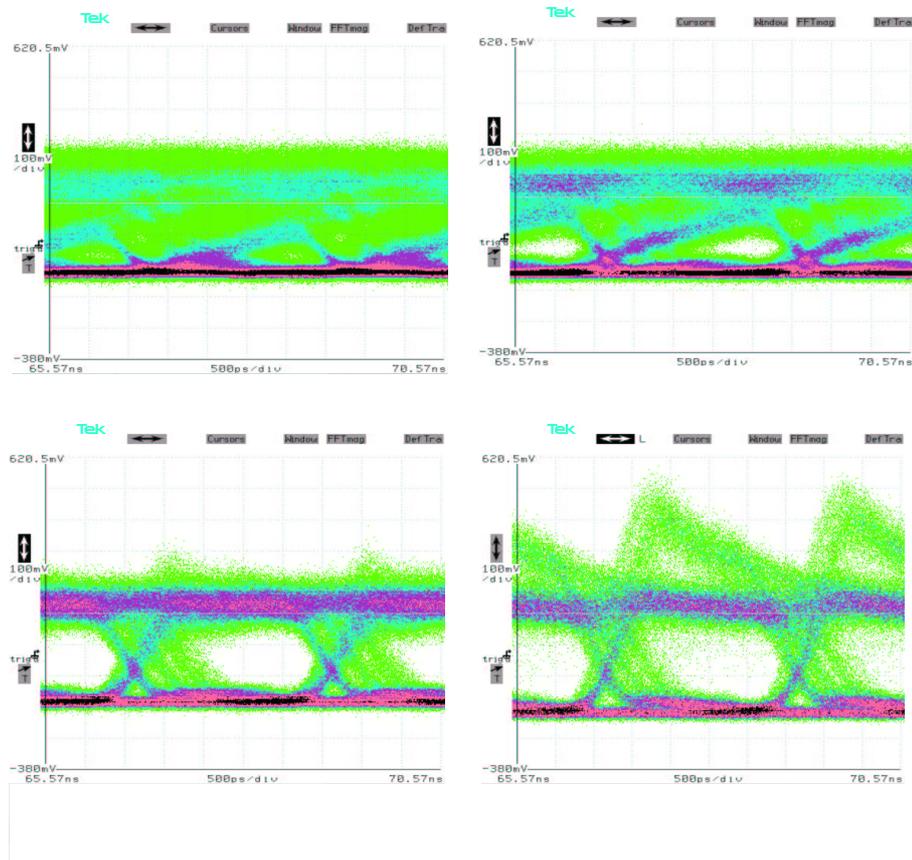
Figure 8.19: Measured eye-diagrams at 400 Mbps of 32-μm RCLEDs mounted on the GLTXLP driver chip.

resulting in a faster switch-off. This problem can be avoided by a better design of the driver.

8.7   Conclusion

In this chapter, the design of high-speed CMOS-integrated drivers is presented. In a previous chapter, it was found that a peaked current waveform results in a faster optical response of the RCLED. Therefore, driver circuits based on this technique were studied. Firstly, an overview of CMOS drivers found in literature was given. Different drivers circuits have been presented in literature, but only few circuits include advanced driving techniques as the peaked current pulse. The influence of the CMOS circuit on the speed response of the RCLED was studied, both theoretically and using simulations (with the high-
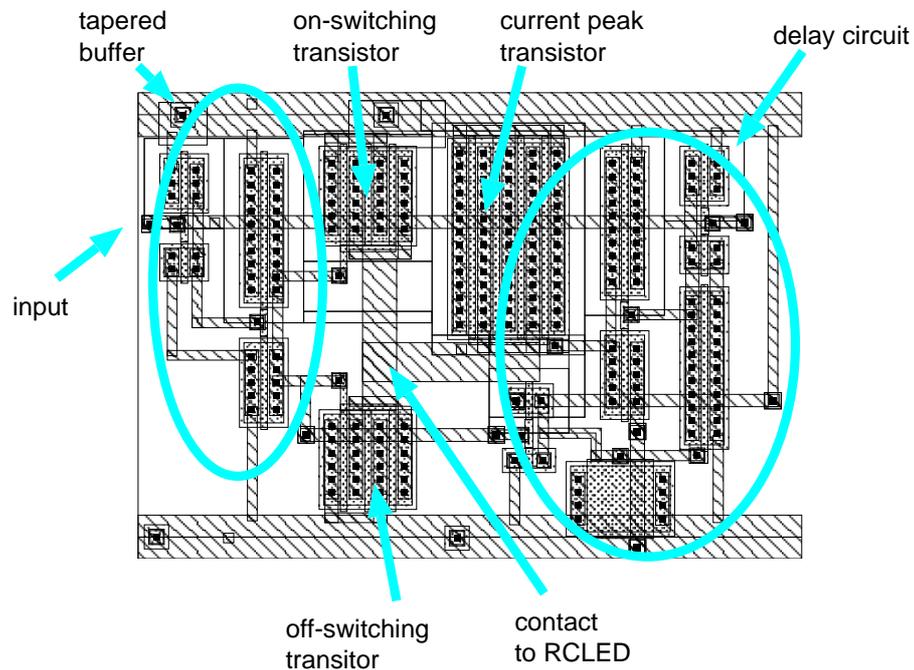
Figure 8.20: Lay-out of combined pulses driver.

speed RCLED model). The rise time of the RCLED depends linearly on the output capacitance of the driver.

Several driver circuits have been designed and realised in a 0.6-μm CMOS technology, using the high-speed RCLED model presented in the previous chapter. All drivers are able to drive the RCLED at 1 Gbps (if the RCLED diameter is sufficiently small, 20 μm is the optimal diameter). Some first-test driver circuits were realised and characterised. However, a 32-μm RCLED was mounted on the devices. The measured eye-diagrams shows operation up to 660 Mbps. Furthermore, it was found that the current peaking principle depends on the operating point of the RCLED, resulting in an optical overshoot if the amplitude of the current pulse is not optimised on the drive current of the RCLED. This is in agreement with earlier theoretical predictions.

Appendix A: lay-out of the driver circuits.

Next figures are the lay-out of the driver circuits, as they are designed and realised. The lay-out should be compared to the schematics of the circuits, as shown in figures 8.10, 8.11 and 8.12.

tapered buffers

current source

tank capacitor

input

RCLED contact

off-switching transistor

drive transistor
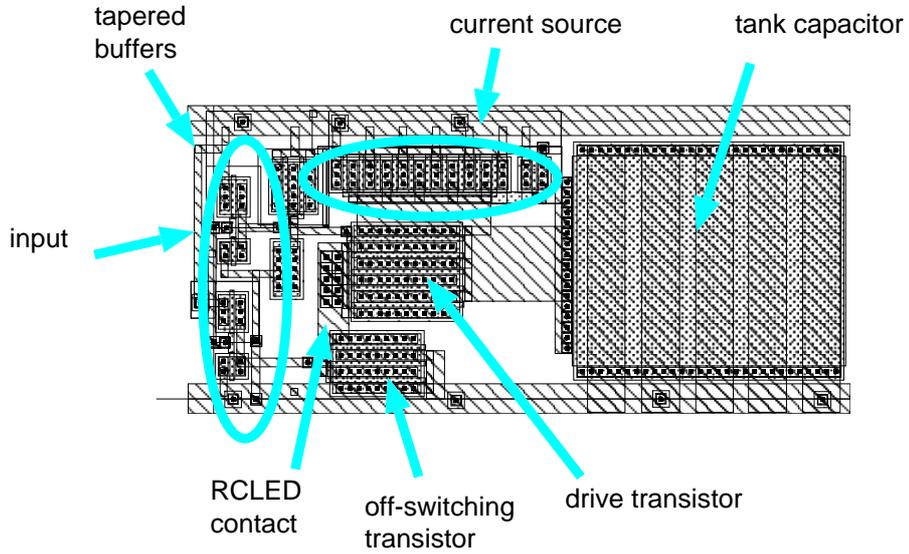
Figure 8.21: Lay-out of C-tank driver.

buffers

delay circuit

current mirror

input

RCLED contact

transistor2

transistor1
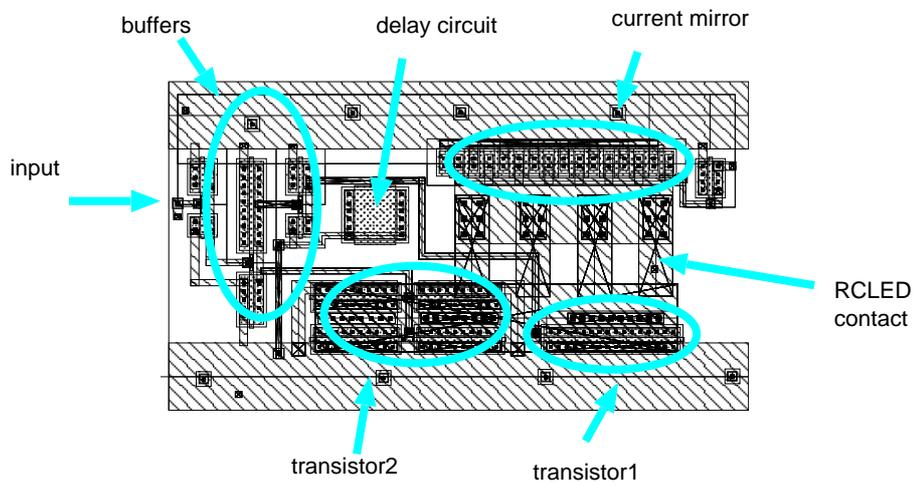
Figure 8.22: Lay-out of constant current source.

Chapter 9

Modelling of parallel interconnect links

In this chapter, the modelling and design of a RCLED based interconnect link is discussed. This allows to study the dependency of the overall link performance on the RCLED and driver characteristics. This model will be used to discuss the design of RCLED based parallel interconnect links.

9.1 Simulation tools for optical interconnects

Long-distance optical interconnections are extremely important nowadays. Several software tools are available to optimise the link design and the link exploitation for optimal performance and cost. Examples are LinkSIM from Rsoft Inc., fibre_CAD from Optiwave Corp. and PTDS (Photonic Transmission Design Suite) from VPI. The same tools could help to optimise the design of parallel optical interconnect links. Unfortunately, these tools are not straightforwardly usable for this task. The components used in parallel optical interconnect links differ from the components typically used in long-distance optical links. This could be solved by introducing new components to the link simulator. Most simulator tools allow this. However, it is rather complex in practice. Therefore, these software tools are not usable for estimating the performance of parallel optical interconnects links.

Currently, a few experimental programs exist to analyse free-space and guided-wave optical interconnect links. Their most important feature is the combination of electrical and optical signals in a single simulation. Chatoyant is such a computer-aided-design tool for free-space optical links, based on VCSELs or modulators, a lens system and receiver and driver circuits in CMOS technology [140]. Other tools make use of a hybrid simulation environment. In reference [141], a ray-tracing tool and an electronics circuit simulator (HSpice) are used together, to simulate links based on multi-mode VCSELs and polymer waveguides. The simulation is done in two steps: firstly, the properties of the

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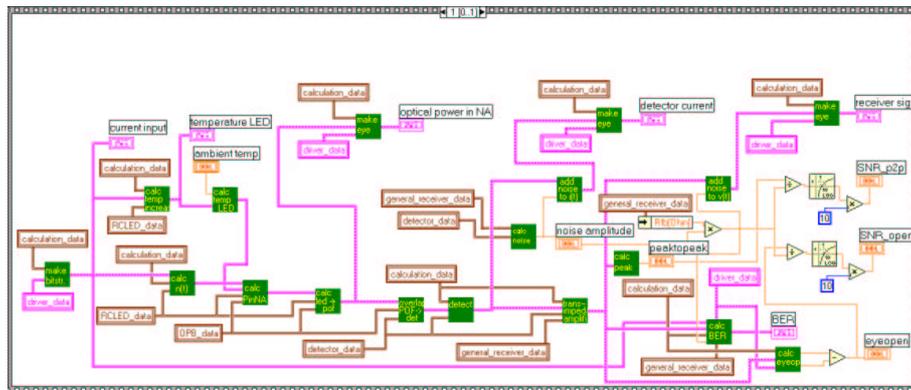
Figure 9.1: Screen shot of the LabView graphical program. The variables are presented by wires, the functions and in and output blocks are presented by the icons.

waveguide are calculated using the ray-tracing tool. And secondly, these results are used in the electrical simulator to calculate the overall link properties. As similar approach is used in reference [142]. In reference [143], a simulation tool for parallel optical interconnects was built up as an extension to an existing tool for long-distance optical interconnections, iFROST, which is written in ANSI C [144].

9.1.1   LabView as programming language

In this work, a simple link simulator for RCLED based optical interconnect links is presented. LabView was chosen as the programming language. This graphical programming language offers an user-friendly programming environment, with many predefined graphical interface elements and predefined function blocks. It allows an easy creation of a graphical user interface. The number-crunching performance is smaller compared to compiled C code, but this is compensated by a shorter development time. Moreover, LabView is used in commercially available link simulators for long-distance optical interconnect links, as OPALS and GOLD.

Figure 9.1 shows a screen shot of the program. The wires represent variables, the icons represent functions. When the calculation in a certain block is finished, then the variables are passed to the next block over the wires. The program can thus be read from left to right. The icon is just a graphical presentation of the function. Beyond the icon sits the LabView code.
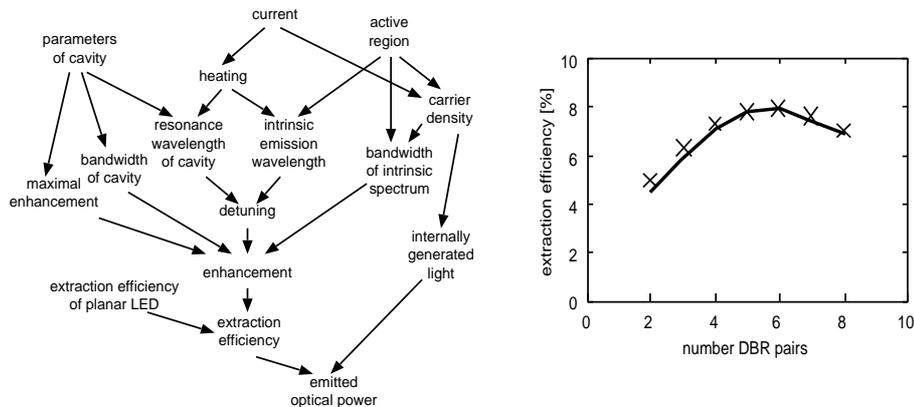
Figure 9.2: Schematics of RCLED model is built up (left), and comparison between this model and a rigorous calculation of the extraction efficiency (right).

9.2 Modelling the optical link

The complete link consists of a data generator, a data coding unit, the light source, an optical pathway, a detector, a receiver circuit and a data decoding circuit. The modelling of the RCLED and the other parts of the link will be discussed in this paragraph. The choice of the specific components is in most cases determined by the design choices made for the OIIC system demonstrator (see section 2.3.6).

9.2.1 Modelling of the RCLED

Within this work, the RCLED is considered the most important part of the link. The modelling of the RCLED is divided into three parts: the modelling of the switching dynamics, the modelling of the extraction efficiency and the modelling of the fibre-coupling efficiency. The basic variable is the carrier concentration inside the active region, which is calculated as a function of time, taking into account the driver parasitics. The basic equation is thus the rate equation (equation 6.2), together with the voltage-carrier density relation. The driver parasitics are presented by a single capacitor in parallel with the RCLED, as was discussed in section 8.4. All differential equations are solved using a one-step Euler algorithm.

Once the carrier concentration is known, the output power is calculated, as given by equation 3.4. The most important factor in this equation is the extraction efficiency into the desired numerical aperture. In this model, the extraction efficiency is calculated by multiplying the extraction efficiency of a planar LED with the microcavity enhancement. The analytical expression for the enhancement, as derived in paragraph 3.5.4, is used. The model takes into account the broadening of the intrinsic spectrum and the cavity detuning due
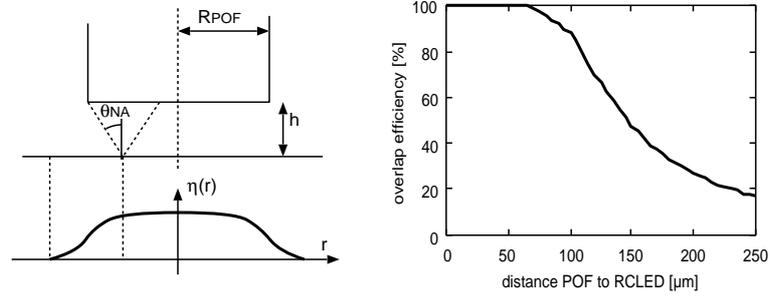
Figure 9.3: Calculation of overlap efficiency between a 50-μm diameter RCLED and a POF.

to heating. Figure 9.2 shows how the output power of the RCLED is calculated.

Finally, the coupling between the RCLED and the POF is calculated. The total optical power coupled into the POF depends on the far-field pattern of the emitted light (the extraction efficiency into NA=0.5), and the geometrical overlap between the light beam and the POF (the overlap efficiency).

The fibre coupling efficiency is written as the product of the extraction efficiency into the numerical aperture of the waveguide (NA=0.5 in case of POFs) and the overlap efficiency. The calculation of the extraction efficiency was discussed in the previous paragraph. The overlap efficiency depends, in general, on the diameter of the light emitter and the fibre, on the distance between the emitter and the fibre, on the lateral misalignment and on the tilt angle between emitter and fibre.

An expression for the overlap efficiency is derived in this work, which is valid for RCLEDs, located at a distance h from the POF, with no lateral misalignment. Consider a small emitting area, located at a distance r from the POF-axis, with extraction efficiency into NA given by $\eta(r)$. If the area is located close to the POF axis, then all light propagating within the NA will be captured in the POF: the coupling efficiency is η_{NA}, as was calculated in the previous paragraph. This is valid as long as $r < R_{POF} - h \tan \theta_{NA}$ (with R_{POF} the diameter of the POF). If the area is located far away from the axis, then no light will be captured into the POF. This is valid if $r > R_{POF} + h \tan \theta_{NA}$. For an emitting area located in between these boundaries, only a part of the light will hit the POF surface. An approximation for the coupling efficiency can be found, assuming that the efficiency depends linear on the distance to the POF axis, if the emitting area is located in the intermediate region. The overlap efficiency is given by:

$$\eta\left(r\right) = \begin{cases} \eta_{NA} & r < R_{POF} - h \tan \theta_{NA} \\ \frac{(R_{POF} + h \tan \theta_{NA}) - r}{2h \tan \theta_{NA}} \eta_{NA} & R_{POF} - h \tan \theta_{NA} < r < R_{POF} + h \tan \theta_{NA} \\ 0 & R_{POF} + h \tan \theta_{NA} < r \end{cases}$$

The overall overlap efficiency is found by averaging the overlap efficiency

over the RCLED surface. This is given by:

$$\eta_{overlap} = \frac{1}{\pi R_{LED}^2} \int_{RCLED} \eta(r) 2\pi r dr$$

Figure 9.3 shows the calculated overlap efficiency of a 50-μm RCLED and a 120-μm POF. The coupling is 100 % as long as the distance between the RCLED and the fibre is smaller than 63 μm. This equation is implemented in the link simulator. Finally, an extra loss factor was introduced, which compensates for the the Fresnel losses at the air-POF interfaces, and losses due to the irregularities at the POF interface.

9.2.2   Modelling of the other parts of the link

In this circuit simulator, the data generation unit is a random data generator, using a predefined LabView block. There is no coding circuitry included in the circuit simulator. The first stage in the simulator is a current pulse shaping block, which generates a current signal (as function of time). The RCLED block converts the current in an optical power signal, as previously mentioned.

The next part of the optical link is the optical pathway. In the simulator, only the absorption and the delay in the plastic optical fibre are implemented. Dispersion effects are not taken into account. These effects are neglected in the simulator, which is plausible because of the short length of the pathway. The absorption and the delay are calculated from the material parameters and the length of the pathway. An absorption of 12 dB was used.

The next stage is the detector, which converts the optical signal in a current. In this link simulator, a PiN detector is used. The responsivity of the detector is assumed to be constant (thus independent of wavelength). The detector results in two delay effects: the transit time, representing the time-of-travel of the generated carriers, and the depletion capacitance. The transit effect originates from the propagation delay of the carriers in the absorption region. This is neglected in the link simulator, because of the small thickness of the absorption region. The depletion capacitance is included in the transimpedance amplifier, where it is part of the input capacitance.

The receiver converts the small detector current in a voltage level. In general, the receiver consists of a transimpedance amplifier, one or more voltage amplifiers and a decision stage (see figure 9.4). In the circuit simulator, only the first stage of the receiver is implemented: the transimpedance amplifier. The steady-state output voltage signal of the transimpedance amplifier is proportional to the input current (or the detector current):

$$v_{out} = -\frac{A}{A+1} R_{fb} i_{det} \tag{9.1}$$

A is the amplification of the amplifier, R_{fb} is the feedback resistance, and i_{det} is the detector current. The bandwidth of the transimpedance amplifier is, neglecting the bandwidth of the voltage amplifier, given by:
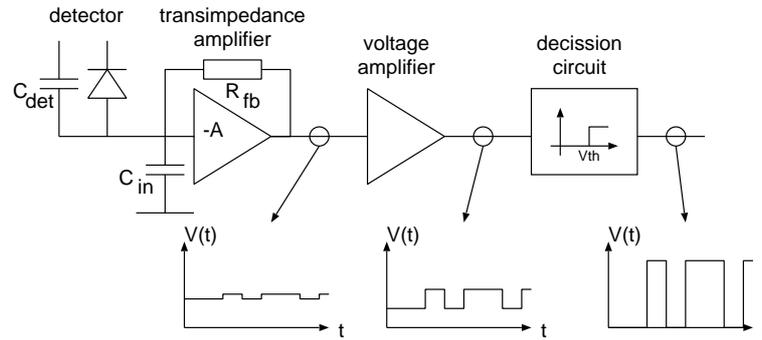
Figure 9.4: Principle of a fibre-optic receiver system.

$$BW_{rec} = \frac{A+1}{R_{fb}C_{tot}} \tag{9.2}$$

C_{tot} presents the total input capacitor: this is the input capacitance of the amplifier and the depletion capacitance of the detector ($C_{tot} = C_{in} + C_{det}$). This equation shows that the gain of the voltage amplifier should be maximised. However, the increased gain also results in an increased input capacitance, which might limit the bandwidth. Furthermore, the maximal gain is also limited by the stability of the transimpedance amplifier. In this link simulator, the transimpedance amplifier is based on a single-stage gm-gm voltage amplifier with a resistive feedback. Several receiver circuits based on this type of amplifier have been presented in literature [145][146]. The properties of this amplifier are summarised in appendix A.

The receiver determines the noise performance of the link. Traditionally, all noise generated in the link is written as an equivalent input current at the receiver. The noise sources can be divided in the 'internal' sources and the 'external' sources. The internal noise sources are generated by the receiver circuit itselves, whilst the external noise sources are generated by the other parts of the system[1]. In this paragraph, the internal noise sources will be discussed. The external noise sources will be discussed afterwards. The internal noise sources include the noise generated in the channel of the first stage of the transimpedance amplifier, and the noise generated in the feedback resistor. Other noise sources, as the shot noise generated by leakage currents and the 1/f noise, are neglected. The equivalent input noise of the complete transimpedance amplifier is given by [147]:

---

[1]In traditional telecom systems, the receiver is isolated from the rest of the system, and the external noise is always neglected. This is not valid for the parallel interconnect systems studied in this work, in which the receivers are located close to the transmitters and the digital circuitry (the 'digital noise').

$$< i^2_{eq,in} > = 4\frac{kT}{R_{fb}}I_2 BW + 4kT\Gamma\frac{(2\pi C_{in})^2}{g_m}I_3 BW^3 \qquad (9.3)$$

With BW the bandwidth of the noise (which equals the bandwidth of the receiver), R_{fb} the feedback resistor, C_{in} the total input capacitance of the receiver, g_m the transconductance of the input transistor (given by $\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)$, see appendix), Γ the channel thermal noise factor (typically 2/3 for CMOS transistors), and I_2 and I_3 two factors, determined by the signal bandwidth. For on-off keying modulations schemes, I_2 is 0.6 and I_3 is 0.09. The first term presents the noise generated in the feedback resistor, the second term represents the noise generated in the first stage of the amplifier. The noise is determined by the detector and the amplifier characteristics (both C_{in} and g_m depend on the input transistor parameters). This expression is implemented in the simulator tool. It allows to calculate the signal to noise ratio and the bit error rate (BER).

9.3 Design of the optical link

The design cycle of the optical link consists of two steps. Firstly, the structure of the link and the type of components needs to be determined. This includes, amongst others, the choice of the integration technology and the choice of the optical pathway. In this work, a RCLED-POF based link is chosen. The second step in the design of an optical link is the determination of the component parameters. This last step is done using the LabView based simulation tool. The most important parameters are the RCLED dimensions, the detector dimensions and the drive current. For this optimisation, a fixed POF length is used (30 cm). Table 9.1 summarises the parameters of the link, and their default value.

The goal is the design of a low-power, moderate speed optical link. The performance of the link is determined by its weakest component, implying that each subpart of the link has to be designed for maximal performance.

9.3.1 Design of the receiver

The design of a receiver is a complex task, which falls outside the scope of this work. However, it is an essential part of the optical link, and some realistic numbers for the receiver parameters need to be found. In this section, some well-considered design rules for a gm-gm-amplifier based transimpedance amplifier will be derived. The basic requirement for the transimpedance amplifier is a sufficiently large voltage swing at the output of the transimpedance amplifier, at a given modulation speed. This allows to estimate the minimal detector current for the given conditions. In this analysis, only first-order systems are taken into account. This enables to do some fast estimations.

parameter	value
bit rate	200 Mbps
RCLED current	3 mA
RCLED diameter	32 μm
distance RCLED-POF	50 μm
POF diameter	62.5 μm
NA POF	0.5
length POF	0.3 m
connector/bend loss	2 dB
POF-detector distance	50 μm
detector diameter	60 μm
responsivity of detector	0.7 A/W
sensitivity of receiver	10 μA
L (amplifier)	0.6 μm
ambient temperature	300 K

Table 9.1: Operating conditions for the optical link. In all simulations shown is this chapter, these values are used, except if mentioned.

9.3.1.1   Speed-limited design

The value of the feedback resistor is determined by the output voltage swing and the input detector current (see equation 9.1). The bandwidth depends on this feedback resistor, the input capacitance and the amplification of the receiver (see equation 9.2). Combining these equations allows to write the receiver bandwidth as a function of the amplifier design parameters:

$$BW = \frac{i_{det}}{v_{out}} \frac{A\left(W_i, L_i\right)}{C_{det} + C_{in}\left(W_i, L_i\right)}$$

with i_{det} the input detector current, v_{out} the required voltage output swing, A the amplification of the amplifier, C_{det} the detector capacitance and C_{in} the input capacitance of the amplifier. This equation allows to determine the parameters W_i, L_i of the gm-gm type amplifier. Assume that the output transistor has a minimal-dimension ($W_{out} = L_{min} = L$). The corresponding amplification is $A = W_{in}/L$ (see appendix A). In that case, a condition for W_{in} can be found:

$$W_{in} > L \frac{C_{det}}{\frac{i_{det}}{BW v_{out}} - \frac{2}{3} C_{ox} L^2} \tag{9.4}$$

This condition expresses that the input transistor width must be sufficiently large to achieve a certain speed at the receiver. This sounds as a contradiction, because a large input transistor corresponds to an increased input capacitance, and a slow response. However, the amplification increases also, which results in an increased speed response. There is a minimal detector current for which a positive width of the input transistor is achieved:

$$i_{det} > BW \frac{2}{3} C_{ox} L^2 v_{out} \tag{9.5}$$

This simple expression shows that the required detector current for this type of amplifier increases linearly with the bandwidth of the signal, and decreases as a function of the smaller CMOS technologies.

9.3.1.2 Noise limited design

In this analysis, the parameters of the transimpedance amplifier are determined to minimise the noise in the receiver. For this analysis, the bandwidth of the noise is assumed to be constant. This is a variant on the theory of Personick[147]. He found that the input capacitance of the optimal CMOS receiver (for minimal noise) equals the detector capacitance ($C_{in} = C_{det}$). However, he assumed that the biasing settings of the input transistor were independent on the width of this transistor. In this work, the optimisation was redone, this time for a gm-gm amplifier, in which the width of the input transistor do influence the biasing settings (see appendix A). The noise generated in the transimpedance amplifier is given by expression 9.3. The high frequency limit is given by:

$$< i_{eq,in}^2 >= (2\pi)^2 \frac{8kT}{3} I_3 \frac{C_{in}^2 BW_{noise}^3}{g_m}$$

with BW_{noise} the bandwidth of the noise (which is assumed to be constant), C_{in} the input capacitance of the amplifier and g_m the transconductance of the input transistor. This expression can be minimised as a function of the width of the input transistor W_i. The optimal width of the input transistor is given by:

$$\frac{W_{opt}}{L} = \frac{1}{6} \left(\frac{C_{det}}{C_{min}} - 2 + \sqrt{\left(\frac{C_{det}}{C_{min}} \right)^2 + 20 \frac{C_{det}}{C_{min}} + 4} \right) \tag{9.6}$$

with C_{det} the capacitance of the detector, and C_{min} defined as $\frac{2}{3} C_{ox} L^2$. In general, the detector capacitance is much larger compared to C_{min}. The optimal input width is then given by: $W_{opt} = \frac{L}{3} \frac{C_{det}}{C_{min}}$. The corresponding input capacitance of the receiver is given by $C_{in} = \frac{1}{3} C_{det}$. This implies that the width of the input transistor can be chosen smaller, compared to the result of Personick's theory. Combining this result with the result of previous paragraph, it is found that the width of the input transistor of the gm-gm based transimpedance amplifier is given by equation 9.6 (design for minimal noise), if the input current is sufficiently large and the signal bandwidth is sufficiently small. If this is not the case, then the width of the input transistor is given by expression 9.4.

It is possible to estimate the minimal detector current at which the input width corresponding to a noise-limited receiver (given by equation 9.6) fulfils
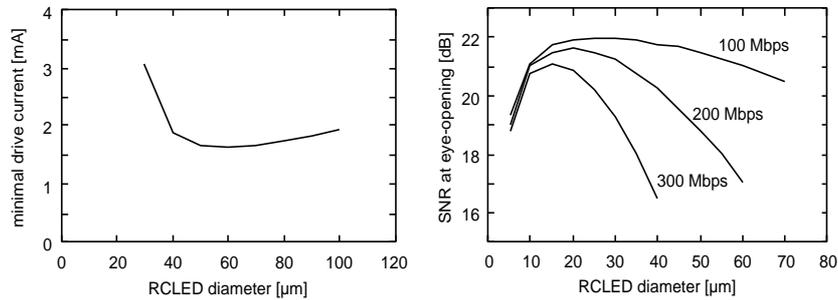
Figure 9.5: Calculation of link performance as a function of the RCLED diameter.

the speed requirement (equation 9.4). The minimal detector current for a noise-limited receiver design is given by:

$$i_{det} > \frac{8}{3} BW\, v_{out} C_{min}$$

This is a factor 4 larger compared to the minimal current for receiver operation at the desired bandwidth. In the link simulator, the input parameter of the gm-gm amplifier was determined from the required data rate and output voltage swing. In general, the expression for a minimised input noise was chosen, except if the speed response was a problem.

This analysis is valid for the gm-gm based transimpedance amplifier. In practice, more advanced receiver circuits are used, including multi-stage amplifiers. These complex circuits do not allow to make some simple estimations for the receiver performance. Therefore, this simple amplifier is implemented in the circuit simulator, because it allows to do some estimations of the receiver parameters, instead of choosing the receiver parameters at random.

9.3.2 Design of the RCLED

The design of the RCLED includes the design of the layer structure, and the design of the RCLED diameter. The influence of the layer structure on the efficiency has been discussed extensively in chapters 3 and 4, and the design presented in paragraph 4.2.1 was chosen. The optimal device diameter was found using the link simulator.

Figure 9.5 shows the calculated minimal drive current as a function of the RCLED diameter, and the calculated signal to noise ratio of the detector current at the receiver, as a function of the RCLED diameter. There is an optimum RCLED diameter, at which the drive current is minimised. Small RCLEDs have a decreased efficiency, due to saturation effects, whilst large RCLEDs have both a decreased coupling to the fibre and a decreased eye-opening due to the slower response. The optimum RCLED diameter decreases at higher data rates, due to the important decrease of the eye-opening as a function of the
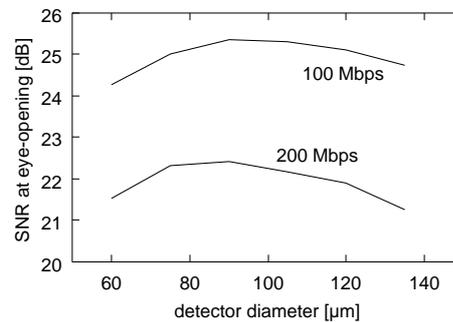
Figure 9.6: Calculation of the link performance as a function of the detector diameter.

data rate. Therefore, it was found that the optimal RCLED diameter is slightly smaller than the fibre diameter, depending on the desired bit rate.

9.3.3 Design of the detector

A similar analysis was done to determine the optimal detector diameter. In this case, there is a trade-off between a high responsivity (implying a larger detector, to optimise the overlap between the light spot and the detector), and a small input capacitance as load of the receiver (to minimise the noise and maximise the speed response).

The optimal detector diameter is slightly smaller than the fibre diameter. The signal to noise ratio decreases as a function of the bit rate, because the noise is now directly proportional to the signal bandwidth. In case of the RCLED, the bandwidth influences only the maximal eye-opening.

9.4 Conclusion

In this chapter, the design of RCLED based interconnect links was discussed. A simulator tool was developed, which simplified the design. The tool was realised in the LabView programming language, and it includes an advanced model of the RCLED and a simple model for the optical pathway and the optical receiver. Special attention was given to the noise performance of the receiver. The design of the receiver was discussed, because its performance was found to be critical to describe the performance of the complete link. Finally, it was found that the optimal RCLED diameter should be slightly smaller compared to the fibre diameter, depending on the bit rate of the system. The same conclusion holds for the detector diameter.
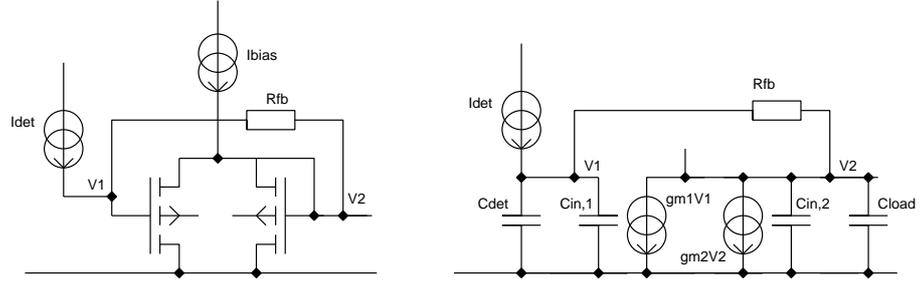
Figure 9.7: Circuit and equivalent small-signal circuit of gm-gm amplifier.

Appendix A: properties of receivers

In this section, the properties of the CMOS based gm-gm amplifier will be discussed. The circuit of the gm-gm amplifier is shown in figure 9.7.

biasing point analysis

The biasing point is calculated as follows. Consider that no input current is applied to the amplifier, and that the load is purely capacitive (in a later section, the input current will be considered as a small-signal perturbation to the biasing settings). Therefore, there is no current through the feedback resistor, and the input and output voltage are equal. Applying Kirchhoff Law:

$$I_{bias} = \frac{\mu C_{ox}}{2} \frac{W_1}{L_1} \left(V_{bias} - V_T\right)^2 + \frac{\mu C_{ox}}{2} \frac{W_2}{L_2} \left(V_{bias} - V_T\right)^2$$

This determines the biasing voltage at the input and output node, as a function of the biasing current. Furthermore, the small-signal parameters can be found:

$$g_{m,1} = \frac{dI_{DS}}{dV_{GS}} = 2\frac{W_1}{L_1} \sqrt{\frac{\frac{\mu C_{ox}}{2} I_{bias}}{\frac{W_1}{L_1} + \frac{W_2}{L_2}}}$$

DC small-signal analysis

Now, a small current is applied at the input node. For small input current (as the detector current is), a first order approximation can be made. The small-signal equivalent circuit is given in figure 9.7.

The current continuity relation is written out:

$$I_{det} = g_{m,1}V_1 + g_{m,2}V_2 = g_{m,1}\left(V_{out} + R_{fb}I_{det}\right) + g_{m,2}V_{out}$$

From this expression, the voltage amplification can be calculated:

$$\frac{V_2}{V_1} = \frac{1 - R_{fb}g_{m,1}}{1 + R_{fb}g_{m,2}}$$

The transconductance gm must be sufficiently large, to get an inverting action. This implies that the biasing current must be sufficiently large.

The transfer function of the transimpedance amplifier is written as (with $A = g_{m,1}/g_{m,2}$ the voltage amplification of the amplifier):

$$\frac{V_{out}}{I_{det}} = \frac{1 - g_{m,1}R_{fb}}{g_{m,1} + g_{m,2}} \approx -R_{fb}\frac{A}{A + 1}$$

The transconductance are calculated from the biasing settings.

Time domain small-signal analysis

The amplifier has an input and output capacitance given by:

$$C_{in} = C_{det} + C_{in,1} = C_{det} + \frac{2}{3}W_1 L_1 C_{ox}$$

$$C_{out} = C_{in,2} + C_{load} = \frac{2}{3}W_2 L_2 C_{ox} + C_{load}$$

From the equivalent circuit, the time domain small-signal response can be written down as a set of coupled linear differential equations:

$$\begin{cases} \frac{dV_1}{dt} = \frac{I_{det}}{C_{in}} + \frac{V_2 - V_1}{R_{fb}C_{in}} \\ \frac{dV_2}{dt} = \frac{V_1 - V_2}{R_{fb}C_{out}} - \frac{g_{m,1}V_1}{C_{out}} - \frac{g_{m,2}V_2}{C_{out}} \end{cases}$$

These equations can be easily solved in the simulator using the Euler method.

Frequency domain small-signal analysis

In this section, the transfer function of this amplifier is determined. This is written as:

$$\frac{v_{out}}{i_{det}} = \frac{1 - R_{fb}g_{m,1}}{g_{m,1} + g_{m,2}} \frac{1}{1 + j\omega\frac{C_{in}(1+R_{fb}g_{m,2})+C_{out}}{g_{m,1}+g_{m,2}} - \omega^2\frac{R_{fb}C_{in}C_{out}}{g_{m,1}+g_{m,2}}}$$

Assuming $R_{fb}g_{m,1} \gg 1$ and that $C_{out} \ll C_{in}$, and $A = g_{m,1}/g_{m,2}$, this can be written as:

$$\frac{v_{out}}{i_{det}} = -R_{fb}\frac{A}{A + 1}\frac{1}{1 + j\omega\frac{R_{fb}C_{in}}{A+1}}$$

which is in agreement with the general expression of the transimpedance amplifier.

Chapter 10

Characterisation of optical interconnections

In this chapter, measurements on parallel RCLED based interconnect links will be presented, discussed and compared with the simulations, using the simulation tool described in the previous chapter. Special attention will be given to the cross-talk. This chapter will end with a comparison between RCLEDs and VCSELs, as light sources for optical interconnect applications.

10.1 Introduction

In the previous chapters, the different aspects of RCLEDs for optical interconnect links were discussed. In this chapter, measurements on RCLED based parallel optical interconnect links are presented. These measurements are important, as they are an experimental proof of the feasibility of RCLED based interconnect links. These measurements allow to discuss features of the component which are not possible to identify when studying a single device. Cross-talk is such an issue.

10.2 Measurements

In this section, measurements on the RCLED based optical interconnect link are presented. All measurements were done on the OIIC system demonstrator. The structure of this interconnect demonstrator was discussed in paragraph 2.3.6.

10.2.1 Measurement setup

The chip with the optical interconnections was plugged in a digital tester, to test the digital functionality of the link. This allowed to drive and monitor
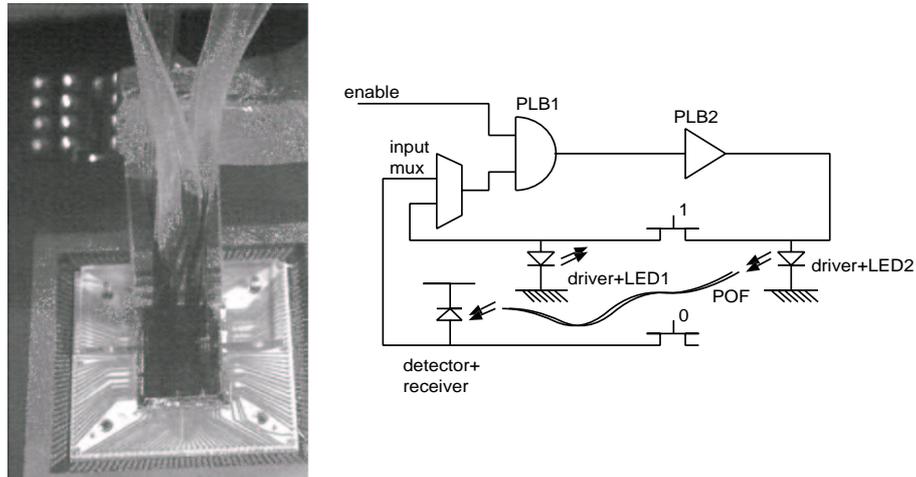
Figure 10.1: Picture of OIIC system demonstrator measurement setup with loop optical pathway (left), and setup of electrically and optically connected ring-oscillator (right).

all the digital signals to and from the chip. The on-chip FPGA functionality proved to be a very flexible environment to test the optical links: the chip can be programmed for a specific measurement, as the determination of the maximal speed, the latency or the influence of parallelism. More information on the functionality of the system, and the testing methodologies, can be found in reference [148]. However, this digital tester was also the limiting factor during the measurements. For example, the tester limits the bandwidth of the signals transported to and from the chip.

Two different measurements were done. Firstly, an intra-chip link was characterised. A special optical pathway with a loop was used (see figure 10.1). The first measurements were done by manually aligning the pathway block (with the fibres) above the chip. A translation stage with μm precision and 5 degrees of freedom was used. Next, precision spacer parts were mounted on the chip, allowing the use of a passively aligned, connectorised pathway. However, this approach does not allow to optimise the position of the fibres relative to the RCLEDs. The position of the pathway relative to the RCLEDs is determined by the dimensions and the tolerances on the spacer and the connector.

10.2.2 It works !

First measurements were done using the fibre loop and the manual alignment method (see figure 10.1). Stable operation of all optical links was found. Figure 10.2 shows the output trace of a parallel interconnect link, in which 4 channels are operational. The minimal drive current of the RCLEDs was 2 mA. There is some oscillation visible when all 4 channels emit light simultaneously. This is
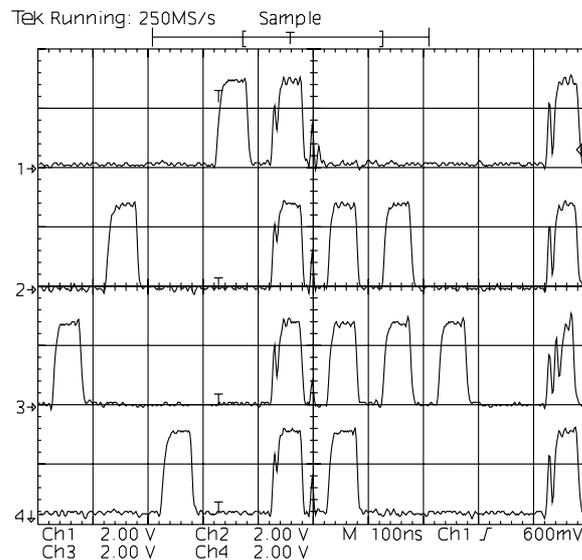
Figure 10.2: First measurements on the OIIC system demonstrator, indicating operation of (at least !) four RCLED-POF channels in parallel.

related to the receiver performance, in combination with the bad decoupling of the power supply around the chip. This was solved by adding more decoupling capacitors around the chip.

These measurements prove the functionality of the RCLED based optical link, and are therefore extremely important within this thesis. The RCLEDs emit a sufficiently large amount of light.

10.2.3 Latency of RCLED based interconnect links

For the FPGA application, the latency of the link is very important: it determines the maximal clock frequency of the system, and the latency should therefore be minimised. Optical interconnects should lead to a shorter latency compared to metallic interconnects. A feeling for typical numbers of the latency was determined by programming a ring oscillator in the FPGA chip. Two versions are available: one using a metallic interconnection in the feedback loop, and one using an optical interconnection in the feedback loop (see figure 10.1). This allows to compare the time-of-flight of the signal in both cases. Figure 10.3 compares the output traces: the optically interconnected chip exhibits faster rise and fall times, indicating the advantage of the optical interconnections.

Figure 10.4 shows the measured period of the ring oscillator, in case of an optical feedback, as a function of the drive current of the RCLEDs. As expected, the latency decreases slightly as a function of the drive current. This is because the influence of the rise and fall times of the RCLEDs on the total latency is
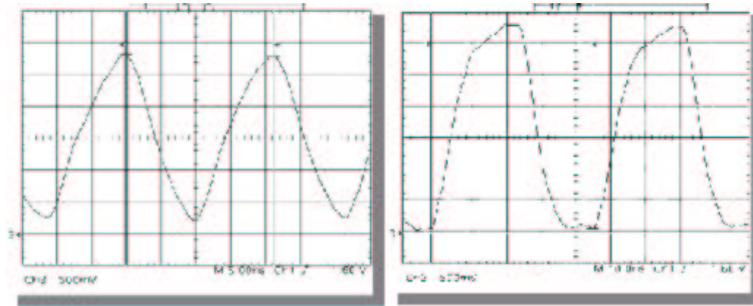
Figure 10.3: Measurements on OIIC system demonstrator: output of electrically interconnected ring oscillator (left) and optically interconnected ring oscillator (right).
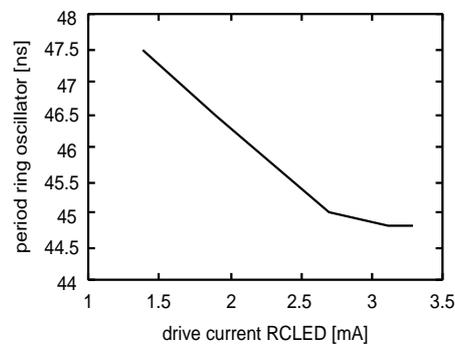
Figure 10.4: Measurement of round trip time of the optical interconnected ring oscillator. (round trip time of the electrically interconnected oscillator is 22.2 ns).

rather small.

Figure 10.5 shows how the latency is distributed over the complete link. This is a calculated result, using the circuit simulator (taking into account the real driver and receiver circuits) and the high-speed model of the RCLED. It shows that the largest latency is generated in the RCLED and the receiver. There is a strong asymmetry in latency generated at the receiver, between the rising and the falling edge. This is due to the fact that a non-balanced code was used. The circuits are designed for Manchester-coded signals. In the receiver, the average value of the incoming detector current is used as the threshold reference. This average value is obtained using a low-pass filter. However, this low-pass filter has a slow response, and during the simulation, the threshold value was not yet at its static value. The threshold value is too small. At the rising edge, the signal reaches the threshold value rather fast, and a small latency is noticed. However, at the falling edge, there is a longer latency due to
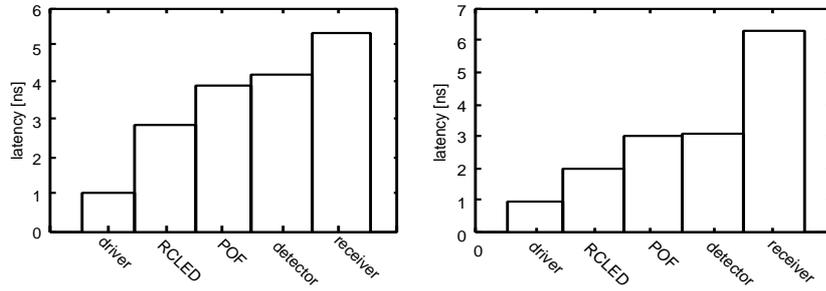
Figure 10.5: Calculated *cumulative* latency of the RCLED links in the OIIC system demonstrator, at rising edge (left) and falling edge (right).

the too small threshold value.

The latency consists of 1 ns time of flight through the POF, 1 ns delay in the CMOS driver circuit, a negligible delay in the detector, an average latency of 1.5 ns in the RCLED (1 ns at the rising edge, 2 ns at the falling edge) and an average latency of 2.5 ns in the receiver circuit. The expression for the latency of current-driven RCLEDs (defined as the 0->50 % delay) is given by (see equations 6.7 and 6.8):

$$t_{lat,up} = 0.88\sqrt{\frac{qVol}{BI_{inj}}}, \quad t_{lat,down} = 0.41\sqrt{\frac{qVol}{BI_{inj}}}$$

The fall time is much longer compared to the rise time, due to the long tail in the transient signal. However, this tail does not affect the latency, hence the shorter latency at the down transition.

The total delay of the complete link is about 6 ns, only 25 % of it comes from the RCLED. This implies that the use of faster light emitters in this link would result in a marginal increase of the overall latency. The importance of the RCLED latency compared to the overall latency gets even smaller if the data is transmitted over longer distances.

10.2.4 Further measurements

Finally, a connectorised POF-based optical pathway was placed above the chips, interconnecting 2 different chips (this setup is shown in figure 2.5). In this way, an optically interconnected system consisting of 2 FPGA chips is realised. Compared to the previous measurement, the aligment is now done by using guiding pins in the connectors: no manual fine aliment is done. Figure 10.6 shows the measured eye-diagram of the complete link. The data rate per channel of this inter-chip link is 50 Mbps, the drive current is about 4 mA. The response of the channels is not uniform: the third channel exhibits an increased jitter. This is related to a reduced coupling from the RCLED to the plastic optical fibre, due to the non-uniformity of the position of the fibres in the optical
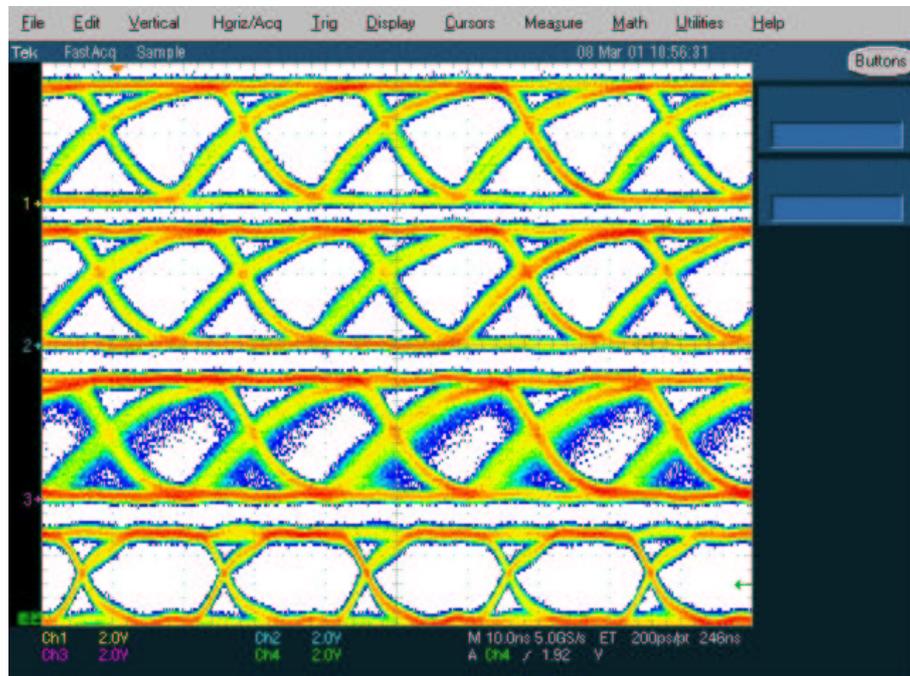
Figure 10.6: Eye-diagram at 50 Mbps of 3 (simultaneously transmitting) channels (with a connectorised POF-pathway), measured at the output of the receivers.

pathway. The smaller optical power results in a slower response of the receiver, and an increased jitter. The best channels shows a good operation, even if the RCLEDs are driven by current levels as small as 2 mA.

In conclusion, it was found that RCLED based interconnections are feasible, but the power budget is tight. This, in combination with the stringent requirements on the alignment tolerances, is a disadvantage. It implies that the optical pathway has to be well-designed: both the propagation losses and the coupling losses must be minimised.

10.3 Cross-talk analysis

Cross-talk is the degradation of the performance of a single optical channel, due to the operation of other parts of the (parallel) link, mostly a neighbouring link. In this section, the different sources of cross-talk in the CMOS optical interconnect link are discussed. These include thermal, optical and electrical cross-talk.

The study of cross-talk is very complex because most of the effects depend heavily on system-specific issues (such as the layout of the chip), are influenced by statistical numbers (such as the data transmission probability) and because the effects are heavily time-dependent. In this study, a worst-case analysis is performed. The influence of the crosstalk is presented as an equivalent detector current. This allows to compare the relative importance of different cross-talk mechanisms. This approach is similar to the noise analysis, which was presented before.

10.3.1 Thermal cross-talk

The thermal cross-talk represents the decrease of the optical power due to the heating in another channel in the link. The thermal cross-talk in a RCLED array was discussed in section 5.1.3. In the current section, the influence of the driver is also taken into account. There are several heat sources in the system. Firstly, there is heat generated in the RCLED and the underlying driver circuit. Secondly, there is heat generated in the other RCLEDs and other drivers, and finally there is heat generated in the rest of the CMOS circuit. This last heat source exists even if no light is transmitted, and results in an increased static temperature of the RCLED:

$$T_{LED,idle} = T_{amb} + \Delta P_{CMOS} R_{amb}$$

This equation assumes that all RCLEDs are on the same temperature as the CMOS chip. This is valid if the thermal resistance between the RCLED and the CMOS is negligible. This thermal resistance is determined by the mounting technique and the material choices. In the OIIC system demonstrator, the RCLEDs are flip-chip mounted onto the CMOS. If the flip-chip bumps are good thermal contacts, then the light emitting chip is on the same temperature as the CMOS chip. The dissipated power of the CMOS chip can be estimated from the supply current. This depends strongly on the functionality and the design of the chip. A typical value for the supply current is a few ampere at 3.3 V, so dissipated power is some ten Watts.

The thermal cross-talk is investigated using the thermal circuit, shown in figure 10.7. If only one RCLED is considered, then the temperature increase is given by:

$$\Delta T_{LED2} = \frac{R_{vert,1} R_{vert,2}}{R_{vert,1} + R_{vert,2} + R_{lat,eq}} \Delta P_{LED1}$$

with $R_{vert,1}$ the vertical thermal resistance from the RCLED to the environment, and $R_{lat,eq}$ the lateral thermal resistance. The thermal resistance towards the environment is assumed to be independent on the RCLED-site ($R_{vert,1} = R_{vert,2}$). This is valid for RCLEDs localised in the centre of the RCLED array. The temperature increase is then written as:

$$\Delta T_{LED2} \approx \frac{R_{vert,eq}^2}{2R_{vert,eq} + R_{lat,eq}} \Delta P_{LED1} = R_{th,eq}^{Xtalk} \Delta P_{LED1}$$
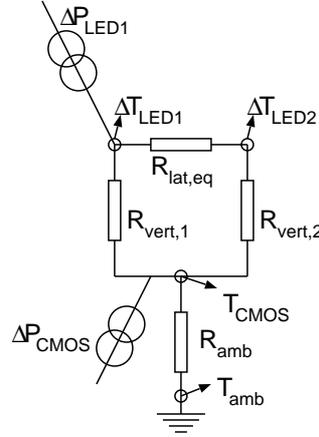
Figure 10.7: Equivalent thermal diagram of RCLEDs mounted on CMOS.

This is a rough estimation for the temperature increase due to the thermal crosstalk. For example, assume a flip-chip mounted RCLED array. The thermal conduction in vertical direction is mainly given by the heat flow through the bumps. The under fill has a much smaller thermal conductivity, and is therefore neglected. The thermal conductivity of solder is about 50 W/mK, the bump height is 5 μm, the bump diameter is 50 μm. The vertical thermal resistance is therefore given by $R_{vert} = \frac{1}{\sigma}\frac{d}{S} \approx 10\frac{K}{W}$. The lateral thermal resistance is determined by the thermal conductivity of GaAs, the thickness of the GaAs substrate (d), and the pitch P between the components $R_{lat} = \frac{1}{\sigma}\frac{d}{S} = \frac{1}{44}\frac{P}{dP} \approx 250\frac{K}{W}$. The temperature increase is thus given by $\Delta T_{LED2} = 1.6\Delta P_{LED1}$. The corresponding temperature increase is very small. The generated heat in the RCLEDs will mainly flow in the CMOS chip, to the thermal environment.

This small temperature increase results in a reduction of the optical output power. Assume that the temperature dependent output power is written as $P = P_0 \exp -T/T_0$ (with T_0 the characteristic temperature, typically 120K), then the resulting variation on the output power is given:

$$\frac{\Delta P_{out}}{P_{out}} = -\frac{\Delta T}{T_0} = -\frac{R_{th,eq}^{Xtalk} 4 V_{driver} I_{LED}}{T_0} \tag{10.1}$$

the factor 4 corresponds to 4 neighbouring RCLEDs (the influence of the other RCLEDs in the array is neglected, because of the larger lateral thermal resistance). V_{driver} is the voltage drop over the driver, I_{LED} is the RCLED current.

10.3.2 Optical cross-talk

This type of cross-talk depends heavily on the type of optical pathway. In case of a guided-wave optical path, the cross-talk (if any) occurs at the incoupling

and outcoupling of the light, or through coupling at closely placed waveguides. Furthermore, optical cross-talk can occur at irregularities in the optical pathway, such as bends, at fibre imperfections or at connectors. This is negligible if the optical system is well-designed. In the case of the OIIC system demonstrator, the distance between the cores of the individual plastic fibres in the pathway is sufficiently large, so that optical coupling can be neglected. This would not be the case if the cores a closely spaced (as in fused single-mode couplers). Furthermore, the location of the optoelectronic components compared to the fibre facet is such to avoid the coupling from light rays of a source to an undesired fibre. If the distance between the opto arrasy and the pathway is sufficiently small, then the light from a neighbouring source will have a to skew propagating angle. Such light is never coupled into the fibre because of the limited capture angle (numerical aperture) of the fibre. This situation would be considerably different in case of a free-space link. In that case, optical cross-talk needs more attention, due to the spreading (divergence) of the optical beam.

Optical cross-talk can also occur in a single channel: back reflections can cause an instable detector current (comparable to reflections in an unmatched transmission line). In most cases, these back reflections are negligible, except if metal-semiconductor-metal detectors are used [149]. These detectors have a rather large reflection coefficient. Moreover, in case of VCSEL based links, these back-reflections can cause a severe degradation of the SNR of the optical signal.

10.3.3 Electrical cross-talk

This cross-talk is very important in the CMOS based inter-chip or intra-chip interconnect links, because driver and receiver circuits are placed closely together on the same system board, multi-chip module or even on the same chip. They share the same electrical power supply and substrate, through which interference occurs.

The analysis of electrical cross-talk depends strongly on the specific implementation of the circuits. Therefore, a more general approach will be presented here. For each subcircuit (in this case, the subcircuits are the driver stage and the receiver), the generated voltage variation on the supply lines is calculated, and the induced variation of the supply voltage at another place on the chip is derived. In a second stage, the sensitivity of the output signal of each subcircuit to variations on the (local) supply voltage is calculated.

10.3.3.1 Noise generation by the driver

The noise generated by the driver circuit depends on the design of the circuit and on the characteristics of the power supply. An ideal voltage supply has no internal impedance: the output voltage of the supply does not depend on the delivered current. In practice, there is some internal impedance and, more important, the series resistance of the supply wires on the system. These factors
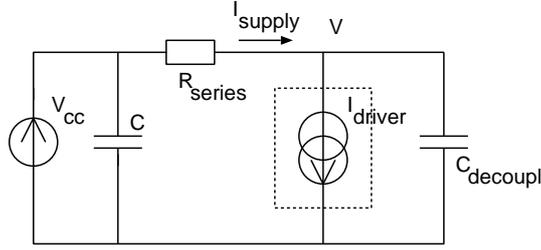
Figure 10.8: Equivalent circuit of supply lines.

imply that the supply voltage over the chip varies if some drivers are operational. Figure 10.8 shows an equivalent circuit of the power supply lines. There is a series resistance between the circuit and the voltage supply. An extra decoupling can be added close to the driver circuit, to reduce the transient effects.

The voltage at the driver is determined by the following differential equation:

$$C_{decoupl}\frac{dV}{dt} + \frac{V}{R_{series}} = \frac{V_{cc}}{R_{series}} - i_{driver}(t)$$

Assume that the supply voltage at the input of the driver is initial V_{cc}, and that the driver is switched on at t=0. The drive current is ΔI_{driver}. The supply voltage at the driver is given by:

$$V(t) = V_{cc} + R_{series}\Delta I_{driver}\left(\exp\left(-\frac{t}{\tau}\right) - 1\right)$$

with τ the time constant, defined as $\tau = R_{series}C_{decoupl}$. The supply current waveform is given by:

$$I_{supply}(t) = \Delta I_{driver}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right)$$

A decoupling capacitor can be used to slow down the influence of the crosstalk due to the resistive drop, but it won't alter the maximal variation. This slowing down of the transient is absolutely necessary to reduce the capacitive and inductive coupling. However, this is not taken into account in this work.

The static variation on the supply voltage is given by:

$$\Delta V_{supply} = -R_{series}\Delta I_{driver}$$

The series resistance depends on the actual dimensioning of the supply grid over the chip, and on the technology. Assume a copper layer, with a thickness of about one μm. The square resistance of this metal is given by:

$$R_{series} = \frac{\rho}{d} = \frac{1.7 \cdot 10^{-8}\Omega m}{1 \cdot 10^{-6}m} = 17m\Omega$$

The driver current is estimated at a few mA. The local variation on the supply voltage is a few tens μV.

10.3.3.2 Noise generated by the rest of the circuit

The rest of the circuit, especially the digital part of it, also generates switching noise on the supply lines. The importance of this digital switching noise depends strongly on the type of digital circuit. In case of synchronous systems, there is a clock signal at which the signal in the receiver is sampled. This clock signal can be choosen to sample the receiver signal at moments when the digital part is not active, i.e. when the supply voltage is 'quiet'. In this way, the influence of the digital switching noise can be minimised. However, in asynchronuous systems, the sampling of the receiver signal is done at random moments, and the influence of the digital switching noise is more important. In this work, the digital switching noise is not taken into account, implying that the analysis is only valid for synchronous systems.

10.3.3.3 Electrical cross-talk mechanism

In general, the cross-talk can be generated in through three different mechanisms: resistive, capacitive and inductive cross-talk. In this section, only the resistive noise will be discussed.

Assume that all circuits share the same supply line. Consider a disturbing circuit A, and a disturbed circuit B. The worst-case cross-talk over the resistive power supply lines occurs if both circuits are closely together, and if they are far away from the reference voltage supply. In that case, the variation on the local supply voltage of the disturbed circuit is almost the same as the variation on the local supply voltage of the disturbing circuit, because the series resistance of the supply line between the 2 drivers is negligible compared to the series resistance from the circuits to the reference supply voltage. This variation is given by (assume that the internal resistance to the reference supply voltage is R_{series}):

$$\Delta V_{supply}^{disturbed} = R_{series} \Delta I_{supply}^{disturbing}$$

In a parallel optical interconnect, many drivers are operational at the same time. The variation on the supply current is then larger. This is written as:

$$\Delta V_{supply} = R_{series}^{avg} N^2 \Delta I_{supply}$$

With N^2 the number of channels in the array, and R_{series}^{avg} is the averaged series resistance from the disturbing circuits to the reference power supply. A typical value for the variation on the power supply lines is (assuming an 8×8 array and $10 \ m\Omega$ average series resistance) is 2mV.

10.3.3.4 Sensitivity of the CMOS driver stage

The RCLED drive current is influenced by small variations on the supply voltage. The sensitivity is calculated in this section. Assume that the RCLED is

driven by a single transistor. Most of the driver circuits presented in chapter 5 fall in this category. The RCLED current is determined by:

$$V_{supply} = V_{early} \left(\frac{I_{LED}}{\frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{supply} - V_t \right)^2} - 1 \right) + \frac{mkT}{q} \ln \left(\frac{I_{LED}}{I_{sat}} + 1 \right)$$

with V_{early} the Early voltage, describing the output resistance of the transistor (see section 8.2.2). The sensitivity can be written as (assuming that $I_{LED} > I_{sat}$):

$$S = \frac{\frac{dI_{LED}}{I_{LED}}}{\frac{dV_{supply}}{V_{supply}}} = 2 \frac{V_{supply}}{V_{supply} - V_t} \frac{V_{early} + V_{DS} + \frac{1}{2} \left(V_{supply} - V_t \right)}{V_{early} + V_{DS} + \frac{mkT}{q}}$$

For large supply voltages and large Early voltages, the sensitivity S equals 2. This value increases for smaller CMOS technologies, because the threshold voltage of the transistor is not negligible compared to the supply voltage, and because the Early voltage is relatively small. In this work, S is assumed to be 2. The variation on the RCLED current can be written as:

$$\frac{\Delta I_{LED}}{I_{LED}} = 2 \frac{\Delta V_{supply}}{V_{supply}} = 2 \frac{N^2 R_{series}^{avg} \Delta I_{driver}}{V_{supply}}$$

This variation on the RCLED current is written as an equivalent input current at the receiver. This will allow to compare the influence of the different crosstalk mechanisms on the performance of the link. The RCLED current and the variation on it needs both to be multiplied by the efficiency of the optical pathway. Therefore, the noise to signal ratio of the detector current is given by:

$$\frac{i_{det}^{Xtalk}}{i_{det}} = \frac{\Delta I_{LED}}{I_{LED}} = \frac{2}{V_{supply}} \Delta V_{supply} \qquad (10.2)$$

This implies that, assuming a detector current of 10 μA, there is a variation of 13nA, due to the influence of the resistive cross-talk on the drive current.

10.3.3.5   Sensitivity of the receiver

The influence of the supply voltage onto the receiver performance depends on the receiver configuration. In this work, only the transimpedance amplifier, based on the gm-gm amplifier, is taken into account. The sensitivity of the gm-gm based transimpedance amplifier is evaluated using a small-signal scheme (see figure 10.9).

The static response of the output voltage to the input noise voltage is given by:

$$\frac{v_{out}}{v_{noise}} = \frac{1}{1 + R_{out} g_{m,1} + R_{out} g_{m,2}}$$
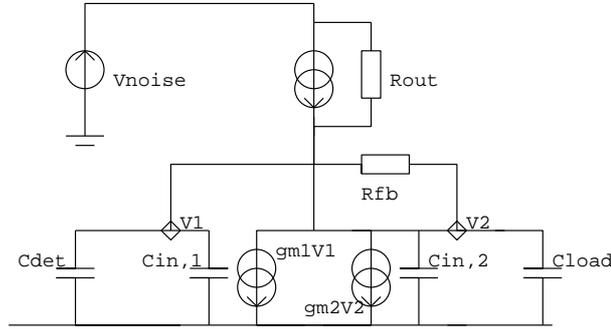
Figure 10.9: Small-signal circuit of the transimpedance amplifier, to calculate the influence of the variations on the power supply.

R_{out} is determined by the Early voltage (see section 8.2.2), g_m is determined by the biasing settings of the amplifier. This can be written as:

$$\frac{v_{out}}{v_{noise}} = \frac{1}{1 + 2V_{early}\sqrt{\frac{\mu C_{ox}}{2I_{bias}}\left(\frac{W_1}{L_1} + \frac{W_2}{L_2}\right)}} = \frac{1}{1 + \frac{2V_{early}}{V_{bias} - V_T}}$$

V_{bias} is the static voltage at the input node if no input current is applied to the receiver (this is the biasing setting). A typical value is v_{out}/v_{noise}=0.03.

The variation on the output voltage is also calculated back to an equivalent variation on the input current of the receiver. This depends on the frequency response of the transimpedance amplifier. In the low frequency regime, this is determined by the feedback resistor:

$$i_{det}^{Xtalk} = \frac{v_{out}}{R_{fb}} = \frac{0.03}{R_{fb}}\Delta V_{supply} \Rightarrow \frac{i_{det}^{Xtalk}}{i_{det}} = \frac{0.03}{R_{fb}i_{det}}\Delta V_{supply} \qquad (10.3)$$

The sensitivity of the receiver circuit decreases if the output voltage swing of the receiver (defined as $R_{fb}i_{det}$) is sufficiently large.

It should be noted that this is a static analysis. In the receiver, the detector is represented by a capacitor which is, at sufficient large frequencies, a short-circuit. This implies that, in a dynamic analysis, the noise on the supply lines is coupled directly on the input node of the transimpedance amplifier, and amplified. This influence is far more important compared to the coupling of supply line noise on the receiver output discussed in this paragraph. However, this capacitive coupling is not taken into account in this work.

10.3.4 Comparison between the cross-talk mechanisms

The influence of the different cross-talk mechanisms is compared in this section. The thermal cross-talk increases as a function of the drive current, due to
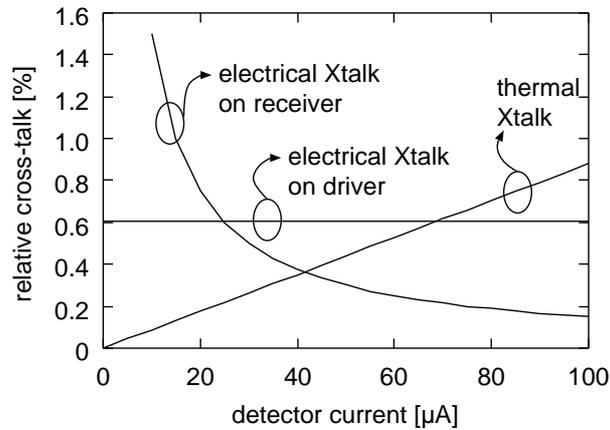
Figure 10.10: Comparison of different cross-talk mechanisms.

the increases heating (see equation 10.1). The influence of the electrical cross-talk on the driver current does not depend on the drive current (see equation 10.2), and the influence on the receiver decreases as a function of the detector current (thus it decreases as a function of the drive current) (see equation 10.2). It is found that the dominant crosstalk mechanism depends on the detector current.

This is summarised in figure 10.10. This is just a rough estimation. For this calculation, the equivalent lateral thermal impedance $R_{lat,eq}$ was estimated at 4 K/W, the characteristic temperature T_0 was 120 K, and the efficiency of the optical pathway was 1 % (10 μA detector current for 1 mA drive current). This efficiency allows to write the thermal crosstalk as a function of the detector current. The feedback resistance of the receiver was 2000 Ω, the supply voltage was 3.3 V and the variation on the supply voltage was 10 mV. The figure shows that the thermal crosstalk is negligible compared to the electrical crosstalk. The dominant factor is the influence of the cross-talk on the receiver circuit. It should be mentioned that this analysis is based on the simple gm-gm based amplifier, and that the results might be different if other receiver circuits are used.

10.3.4.1 Influence on the signal to noise ratio

The type of cross-talk discussed in this paragraph is a deterministic signal: the influence on the detector current can be calculated once the complete circuit and the signals are known. In this section, the static influence of the resistive cross-talk was investigated. This is a worst-case estimation for the cross-talk: it assumes that all channels are operational.

This cross-talk can be interpreted as a noise source. The input current of the detector can be seen as an averaged value, with an unknown variation on

it (or at least a variation which is hard to estimate). This approach is similar to the way noise is treated in communication systems. However, noise is well-characterised: the statistical distribution is known. This distribution allows to estimate the bit error rate. Unfortunately, the statistical distribution of the cross-talk induced variations on the signals in not known. It is certainly not a normal distribution, because there is a clear upper and bottom limit for the variation on the detector current.

However, it is possible to estimate the influence of the cross-talk on the signal-to-noise ratio (SNR). Assume the worst case situation: the amplitude of the detector current decreases strongly due to the cross-talk. The signal to noise ratio of the detector current is given by:

$$SNR_{det} = \frac{i_{det} - \Delta i_{det}^{Xtalk}}{\sqrt{\langle i_{noise}^2 \rangle}} = SNR_{det}^{noXtalk} \left(1 - \frac{\Delta i_{det}^{Xtalk}}{i_{det}} \right)$$

The SNR is expressed in dB (assuming that $\Delta i_{det}^{Xtalk} < i_{det}$):

$$SNR_{det}[dB] \approx SNR_{det}^{noXtalk}[dB] - 10\frac{\Delta i_{det}^{Xtalk}}{i_{det}}$$

This expression allows to estimate the maximal variation of the supply voltage. Assume that the maximal decrease of the SNR equals 1 dB, and that the sensitivity of the the drive current is the limiting cross-talk mechanism. The maximal variation on the supply voltage is given by:

$$1 > 10\frac{\Delta i_{det}^{Xtalk}}{i_{det\,det}} = 10\frac{2\Delta V_{supply}}{V_{supply}} \Rightarrow \Delta V_{supply} < \frac{1}{20}V_{supply}$$

The maximal allowed variation (assuming a 3.3V supply) is about 150mV.

10.4 Performance of RCLEDs versus VCSELs

In this paragraph, a comparison between RCLEDs and VCSELs will be presented. This includes, amongst others, a discussion of the efficiency, the speed, the series resistance (and thus power dissipation) and the uniformity. The discussion will be restricted to RCLEDs and VCSELs. Both devices have a similar structure, and are therefore interchangeable components in the link.

10.4.1 Optical efficiency

In this section, the current needed for a given optical power is studied. The efficiency of the RCLED was discussed in detail in chapter 3. The power characteristics of VCSELs are described in the appendix at the end of this chapter. In this analysis, saturation effects are not included. The desired VCSEL current for a given optical power P_{out} is given by:

$$I_{VCSEL} = I_{th} + \frac{P_{out}}{\frac{h\nu}{q}\eta_{VCSEL}} \tag{10.4}$$

with I_{th} the threshold current (which is proportional to the area of the device). In comparison, the RCLED current is given by:

$$I_{LED} = \frac{P_{out}}{\frac{h\nu}{q}\eta_{LED}}$$

In case of RCLEDs, the current is proportional to the desired optical output power, whilst in case of a VCSEL, the current is always at least the threshold current. This implies that the required RCLED current will be smaller, if a smaller amount of light is required. There is a trade-off optical power, defining which light source is the most efficient. Above this number, the VCSEL needs the smallest drive current. The RCLED is preferable if the desired optical power is smaller than this number. This optical power is given by:

$$P_{trade-off} = \frac{h\nu}{q}\frac{\eta_{VCSEL}\eta_{LED}}{\eta_{VCSEL} - \eta_{LED}}I_{th}$$

Assuming η_{VCSEL} equals 80 %, η_{LED} is 5 % and I_{th} is 0.8 mA, then the trade-off power is about 50 μW. Figure 10.11 shows the calculated drive current as a function of the required optical output power. In this calculation, saturation effects are neglected. In case of the VCSEL, a threshold carrier density of $5 \cdot 10^{18}$ cm^{-3} and an extraction efficiency of 80 % is assumed, in case of the RCLED, an extraction efficiency of 5 % is assumed. The required drive current depends on the VCSEL diameter, because the threshold current depends on the volume of the active region. This is not the case for RCLEDs.

This comparison changes completely when the optical pathway is taken into account. For example, a low-efficient light source at a wavelength corresponding to a low loss in the waveguide might be preferable over a highly-efficient light source at another (high-loss) wavelength (see section 2.2.4).

10.4.2 Beam shape

The beam profile of RCLEDs is wider than that of VCSELs. The microcavity effect can reduce the divergency of the beam, but it was found that RCLEDs optimised for a maximal coupling into a limited numerical aperture have still a rather broad far-field pattern. The beam divergency of VCSELs is determined by the mode profile inside the cavity. Single-mode VCSELs can have a rather small beam divergency.

The beam shape has an important influence on the coupling efficiency to fibres. This is taken into account by defining the extraction efficiency as the efficiency into the numerical aperture of the fibre. For example, the efficiency of RCLEDs is taken as 5 %, which implicitly assumes a 15 % overall efficiency and a 33 % coupling efficiency. In case of a VCSEL, the efficiency into the
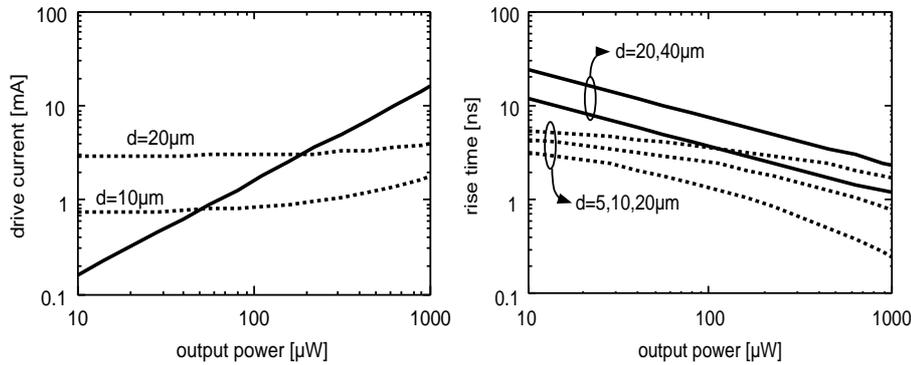
Figure 10.11: Required drive current and corresponding rise time of RCLEDs (full line) and VCSELs (dashed line), for different device diameters.

numerical aperture is close to the overall efficiency (the coupling efficiency is typically about 90 %).

The broad beam shape of RCLEDs in an advantage in other applications, as in visual indicators.

10.4.3 Speed

A VCSEL is known as a fast light emitter, compared to an LED. This is due to the fast stimulated emission. In this section, a detailed analysis of the switching behaviour of both light emitters is presented. Assume that both light sources emit an optical power P_{out}. This determines the drive current and the carrier concentration in the active layer. In case of a RCLED, the carrier density depends on the output power and the device dimensions. In case of a VCSEL, the carrier density is mainly determined by the threshold carrier density. This threshold carrier density is in first approximation independent on the output current or the device diameter.

If the devices are driven by a constant current source, then the rise time can be estimated from the time necessary to fill the active region to the desired carrier density. This delay can be derived from the rate equations. Figure 10.11 shows the calculated rise time, in case of a current-driven RCLED and a current-driven VCSEL, as a function of the optical output power. In case of the VCSEL, a threshold carrier density of $5 \cdot 10^{18}$ cm^{-3} and an extraction efficiency of 80 % is assumed, in case of the RCLED, an extraction efficiency of 5 % is assumed.

In conclusion, the VCSEL is not necessarily much faster compared to a RCLED, especially if both devices would have the same diameter. This is because in both devices an active layer needs to be filled up by a constant current source, which limits the rise time of the signal. However, in practice, VCSELs have a smaller diameter, and the rise time is an order of magnitude smaller

compared to a RCLED. In chapter 6, the influence of advanced techniques on the switching behaviour of RCLEDs was discussed. The use of a pulsed current shape results in a smaller rise time for RCLEDs. However, the same technique can be applied to VCSELs, also resulting in a faster response.

The comparison changes completely if a biasing is taken into account. The carrier concentration in VCSELs remains at the threshold concentration, and the optical output reacts very fast on the drive current. Modulation frequencies up to tens of GHz were measured. However, the low-power applications (as the inter-chip interconnects) demand zero-biasing operation. In practice, the maximal speed of zero-biased VCSELs is limited by the laser turn-on time. This is the delay between the injection of the current and the emission of the optical mode, which is mainly determined by the time to fill the active region, as discussed above.

Extra turn-on effect occur in multi-mode VCSELs, related to the mode competition [22]. Typically, a few modes exist (with different lateral field profile, and thus a different gain profile over the area of the VCSEL, resulting in a different carrier density profile). During the transient, the lateral carrier diffusion in the active region determines the relative importance of the modes, and several higher-order modes might be initiated, reducing the available gain for the main mode of the VCSEL. This effect increases the turn-on time[150]. In some cases, this carrier dynamics effect also induces a small power bounce at the off-switching transient. The lateral diffusion redistributes the carrier profile at the off-switching transient, and the resulting carrier profile might induce a lasing of a higher-order mode in the VCSEL, resulting in an extra light pulse during the off-switching transient. The mode competition has more consequences. It also limits the VCSEL modulation speed in fibre-coupled experiments. The coupling to the fibre depends on the emission profile of the VCSELs. Higher-order modes can be emitted at higher temperatures, making the coupling to the fibre dependent on the thermal transient, which has typically a rather large time constant (a few microseconds)[150]. These effects do only occur in multi-mode VCSELs, and dissappear when single-mode VCSELs are used.

10.4.4 Power dissipation

The overall power dissipation determines the power conversion efficiency. The power dissipation is given by:

$$P_{diss} = I_{LED} V_{LED} = I_{LED} \left(V_j + R_{series} I_{LED} \right)$$

The junction voltage is determined by the carrier density inside the active region. VCSELs need a minimal voltage drop equal to the bandgap of the active layers, to start the stimulated emission. In RCLEDs, the light emission starts at smaller voltages. However, the difference in voltage drop across the active region is typically only a few hundred millivolts, which is small compared to the typical operation voltage (1.4 V in case of 850-nm devices). A second factor is the series resistance. This depends heavily on the device structure, and

the device diameter. VCSELs have typically smaller diameters compared to RCLEDs, thus a larger series resistance can be expected. Again, the difference between the voltage drop across the devices is small, due to the small drive current (typically a few mA). This implies that there is only a small advantage for RCLEDs compared to VCSELs.

10.4.5 Thermal issues

A temperature increase introduces in both RCLEDs and VCSELs a decreased internal quantum efficiency and a detuning: the cavity resonance wavelength and the intrinsic emission wavelength both shift towards longer wavelengths, but at a different rate. In case of a RCLED, the detuning results in a decreased extraction efficiency, as discussed in paragraph 5.1.1. In case of a VCSEL, a cavity detuning alters the threshold current, as the gain of the active material at the cavity resonance wavelength changes. The change of the optical output power as a function of the temperature is given by:

$$P_{out}(T) = \frac{h\nu}{q}\eta(T)(I - I_{th}(T)) \Rightarrow \frac{dP_{out}}{dT} = P_{out}\left(\frac{1}{\eta}\frac{d\eta}{dT} - \frac{1}{I - I_{th}}\frac{dI_{th}}{dT}\right)$$

This expression shows that the temperature dependency of a VCSEL depends on the current level. The temperature coefficient can be very large if the VCSEL is biased just above threshold. If the operating current is chosen well above the threshold current, then the temperature coefficient of a VCSEL can be better compared to a RCLED. The spontaneous emission spectrum of the RCLED should be chosen as small as possible, to allow for a larger cavity enhancement and a larger extraction efficiency. The gain spectrum of the VCSEL can be chosen broader without having an important impact on the threshold current density. This implies that, for a given heating, the detuning has a larger influence in case of the RCLED.

10.4.6 Manufacturability

The fabrication method depends strongly on the device geometry, both for RCLEDs and VCSELs. For example, bottom-emitting components emitting at a substrate-transparent wavelength are much easier to fabricate compared to top-emitting components with two intra-cavity contacts. Components with an intra-cavity contact need a precise control of the etch-depth, to guarantee that the metal contacts are deposited on the proper layer within the stack. This is harder to achieve in the VCSEL case, as the layer structure is much thicker. The smaller RCLED structure allows a much tighter control on the absolute location of the contacts.

In conclusion, the manufacturability depends both on the type of device and the structure of the device. However, the easiest devices to realise remain through-substrate emitting RCLEDs.

10.4.7   Uniformity

The uniformity of RCLEDs and RCLED arrays have been described in paragraph 5.3.1. The conclusion remains valid for VCSELs: the uniformity is strongly determined by the growth and processing facilities. As mentioned in the previous paragraph, the characteristics of VCSEL depend more on deviations during the processing. For example, the uniformity of the diameter of the oxide aperture is of utmost importance in case of VCSELs, as this aperture determines the threshold current. In the early days, a uniformity of 10 % was achieved. Now, improvements on the selective oxidations (as the use of in-situ monitoring techniques) result in tighter deviations (4 % has been obtained).

10.5   Performance of parallel interconnect links

In the previous paragraph, the performance of individual components was discussed. In parallel optical interconnects, the performance of all channels in the link determines the success of the product. This is determined by many factors, of which the light source is only a part.

10.5.1   Performance of an individual link

The measurements presented in paragraph 9.3 showed that the RCLEDs have only a small influence on the latency of the complete optical link. This implies that, if the same receiver circuit is assumed, a faster light emitter (as a VCSEL) leads to a marginal decrease of the latency. However, a VCSEL has a larger efficiency, and is capable to emit more light into the pathway. This results in a larger power budget for the optical link. The designer of the optical link has the choice to use this power budget to increase the transmission distance, or to increase the bit rate. Equation 9.5 shows that a larger detector current increases the output voltage swing of the receiver (for a constant bit rate), or increases the bit rate (for a constant output voltage swing). The advantage of a larger bit rate is clear, and a larger output voltage swing can be used to reduce the number of amplification stages after the receiver circuits, resulting in a reduced latency.

10.5.2   Uniformity of parallel interconnects

In this paragraph, the uniformity of the interconnect characteristics over an array is discussed. The performance of all links inside the array can be different, due to several reasons:

- the properties of the light emitters are not constant over an array. Due to several growth and processing specific issues, parameters as efficiency or threshold current can vary over the array. However, this variation can be minimised by improving the growth and processing tolerances, or by selecting the best (most uniform) arrays. Both solutions will increase the cost of the arrays.

- the driver and receiver circuits are implemented in a CMOS technology, and therefore their performance depends on the non-uniformities of the CMOS process. This uniformity (which originates from several technology-related issues, as the uniformity of doping profiles) becomes more important in the modern, deep sub-micron technologies. This non-uniformity problem can be solved by using advanced circuits designs. However, these solutions always have a drawback, typically an increased area or power consumption.

- The optical pathway also introduces non-uniformities. For example, there might be some deviation on the position of the fibres in the connectors [89]. This results in a random lateral misalignment between the light source and the fibre, or between the fibre and the detector. In case of a connectorised optical pathway block (OPB), this deviation will also result in a non-uniform coupling between the two connectors. Another non-uniformity results from the differences in length of the individual fibres. This might be the case if the fibre ribbon is bent: fibres closer to the centre of the bend will be shorter. This results in smaller absorption losses.

All these factors result in a variation on the detector current, just as the cross-talk and the noise sources in the link also results in an uncertainty on the detector current. However, the uncertainty due to the non-uniformities could be measured and compensated for (by tailoring the drive current, for example). In practice, this is quite impractical, as it would need extra circuitry, measurements and device handling[1]. Therefore, it is proposed to handle these uncertainties as an equivalent to the noise sources. The overall noise is then written as[2]:

$$\langle i_{noise,tot} \rangle^2 = \langle i_{noise,electr} \rangle^2 + \langle i_{noise,unif} \rangle^2$$

with $i_{noise,electr}$ the classical electrical noise term (representing the thermal noise, shot noise and other electrical noise source in the circuit), and $i_{noise,unif}$ an equivalent noise source representing the (uncontrollable) non-uniformities of the link parameters. This is allowed because the statistical distribution of the quantities is well-characterised. This is not the case for the variation on the signals due to the cross-talk.

In this section, the influence of the non-uniformities on the output power of the driver circuits is investigated. It should be noticed that the corresponding variation on the detector current is not a good measure for the influence of the non-uniformities on the performance of the complete link. Depending on the specific design, some receiver circuits are more robust against static (or

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[1]This technique is usable in designing individual links. It is used in designing long-distance fibre-optic networks, where the laser components are selected on individual basis, and feedback circuits are used to control the optical output power.

[2]This step assumes that the influence of the non-uniformities can be written as a random variable. However, the time-domain characteristics of the non-uniformity noise differ strongly from the electrical noise. Therefore, this technique is only usefull to estimate the relative importance of both noise terms.

slow-varying) variations on the input detector current. This implies that the resulting variation on the detector current is difficult to compare with other variation (such as the electrical noise). Nevertheless, such an anlysis is performed, because it allows to estimate the relative importance of the different non-uniformitites at the sender side.

Consider a nMOS transistor, acting as a current source. The output current is given in table 8.1. The variation on the drive current is given by:

$$\frac{\Delta I_{drive}}{I_{drive}} = \sqrt{\left(\frac{\Delta \beta}{\beta}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \frac{2\Delta V_g^2 + 2\Delta V_t^2}{\left(V_g - V_t\right)^2}}$$

The first term in this expression depends on the CMOS technology. The other terms depend on the transistor dimensions or the biasing point. An estimation of the variation on the drive current is given. Assume that the RCLED is driven with a 25×8 μm transistor (the combined pulses driver uses such a drive transistor). The deviation on the transistor dimensions are neglected. An expression for the variation on β and V_T was given in table 8.3. These variations can be calculated for the given transistor dimensions (assuming A_β=2 %μm, and A_T=10 mVμm):

$$\left(\frac{\Delta \beta}{\beta}\right)^2 = \frac{A_\beta^2}{WL} = 2 \cdot 10^{-5}, \; \Delta V_T = \sqrt{\frac{A_T^2}{WL}} = 2.2mV$$

From this analysis, it is found that the variation on β is the most important. The variation on the threshold voltage is smaller, because the gate voltage is large. The corresponding variation on the drive current is about $\Delta I_{drive} = I_{drive}4.5 \cdot 10^{-3}$. A drive current of 3 mA corresponds to an uncertainty of about 12 μA. This uncertainty decreases if wider transistors are used. However, this also results in a slower response of the driver.

This drive current is converted into an optical signal in the optoelectronic component. The deviation on the emitted optical power is given by:

$$\frac{\Delta P_{out}}{P_{out}} = \sqrt{\left(\frac{\Delta \eta}{\eta}\right)^2 + \left(\frac{\Delta I_{th}}{I - I_{th}}\right)^2 + \left(\frac{\Delta I}{I - I_{th}}\right)^2}$$

$\Delta \eta$ and ΔI_{th} depend on the light emitter (and the second term disappears in case of a RCLED), whilst the last term was calculated in the previous section. From this equation, it is found that the threshold current has an important influence on the non-uniformities, especially if the VCSEL is driven just above the threshold. The threshold current should therefore be as small as possible. This is a clear advantage for RCLEDs.

Figure 10.12 shows the calculated signal-to-noise ratio of the drive current and the optical power, as a function of the emitted optical power, for a RCLED and a VCSEL. The extraction efficiency of the RCLED was 5 %, the extraction efficiency of the VCSEL was 80 %, and the threshold current was 0.8 mA. The VCSEL is more efficient, resulting in more light emission. The variation on the
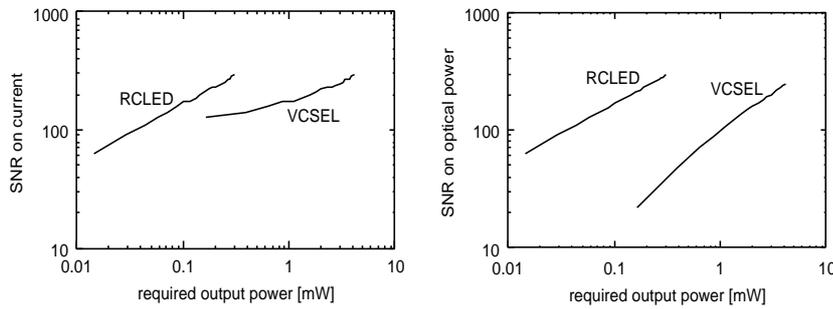
Figure 10.12: Calculation of variation on drive current and variation on optical power, for a VCSEL and a RCLED.

drive current is comparable for both light emitters, and decreases as a function of the drive current, because the variation on β decreases due to the larger drive transistor. The SNR of the driven current of the RCLED is larger, because of the larger drive current. The SNR on the optical power of the VCSEL is smaller, due to the threshold current.

10.6 Conclusion

In this paragraph, experimental results of a functional, parallel RCLED based interconnect link have been presented. These results are extremely important, as they prove the concept and feasibility of these links. These measurements also show that the RCLEDs determine only a part of the overall link performance. Other parts, as the receiver, have also an important influence on the system characteristics.

Next, the cross-talk within parallel optical interconnect links was discussed. This includes the thermal cross-talk, the optical cross-talk and the electrical cross-talk. The electrical cross-talk over the resistive power supplies was studied in depth, and it was found that both the driver and the receiver circuit are susceptible to this type of cross-talk.

Finally, a comparison between the RCLED and the VCSEL was given. It was shown that the performance of VCSELs is in most cases better compared to RCLEDs. However, the uniformity of the VCSEL properties is poor compared to RCLEDs, especially if the VCSELs are driven just above its threshold current. In practice, VCSELs are driven at this operating point to minimise the power consumption.

Appendix A: VCSEL characteristics

In this appendix, some elementary relations on lasers, and VCSELs in particular, will be recalled. The output power of a VCSEL is given by [151]:

$$P_{VCSEL} = \frac{h\nu}{q} \eta_{VCSEL} \left(I - I_{th} \right)$$

Consider a laser cavity, consisting of two mirrors (reflections R_1 and R_2), at a distance L. The medium inside the cavity has an optical gain g, and an optical absorption α. If there is no gain applied, then a part of the photons inside the cavity will be extracted through the mirrors, during each round-trip. This results in a photon lifetime:

$$\tau_{cav} = \frac{2nL}{c} \frac{1}{\ln \frac{1}{R_1 R_2} + 2\alpha L}$$

This number indicates how fast the photons are extracted from the cavity. The refractive index of the medium is n. In case of a laser operation, the medium must have a minimal optical gain to overcome the optical losses (due to absorption and transmission at the mirrors). This is the threshold gain, which is given by:

$$g_{thres} = \alpha + \frac{1}{2L} \ln \frac{1}{R_1 R_2}$$

The gain in the laser depends on the carrier concentration, and is given by:

$$g = g_0 \ln \frac{n}{n_{tr}}$$

with n_{tr} the transparency carrier density, this is the carrier density at which the optical gain of the medium is zero (or the gain compensates for the intrinsic absorption of the active region). These equations allow to estimate the threshold current density:

$$n_{thres} = n_{tr} \left(\frac{1}{R_1 R_2} \right)^{\frac{1}{2g_0 L}} \exp \frac{\alpha}{g_0} = n_{tr} \exp \frac{n}{\tau_{cav} c g_0}$$

This threshold carrier density determines the threshold current of the device.

Only a part of the generated photons escape the cavity in the good direction. The other photons are absorbed somewhere in the cavity, or extracted through the wrong mirror. This determines the extraction efficiency of the laser:

$$\eta_{VCSEL} = \frac{\ln \frac{1}{R_1}}{\ln \frac{1}{R_1 R_2} + 2\alpha L} = \frac{2nL}{\tau_{cav} c} \ln \frac{1}{R_1}$$

Chapter 11

Conclusions and outlook

RCLEDs and RCLED based parallel optical interconnect links have been studied. At the beginning of this work, overall efficiencies up to 22 % were achieved for large RCLEDs. In this work, smaller RCLEDs were optimised for coupling to a Plastic Optical fibre (POF), the speed characteristics were studied in detail, and their application in parallel optical interconnect links was studied.

11.1   Efficiency of RCLEDs

Firstly, the general properties of the optical power characteristics of the RCLED were discussed. It was found that the extraction efficiency is the most adequate parameter to compare the performance of different light emitters. A novel extraction method for the extraction efficiency was proposed, which allows to distinguish between the internal efficiency and the extraction efficiency.

An overview of the properties of spontaneous emission in semiconductors was given. Special attention was paid to the properties of the spontaneous emission, such as the radiative lifetime and the spectral broadening. These are important parameters for the microcavity effect. The influence of a microcavity on the spontaneous emission was pointed out, using the k-space picture.

A new analytical model for the extraction efficiency in microcavities was derived. The rather simple expression allows to explain the most important effects in microcavities, as the influence of the detuning on the efficiency and the far-field pattern. Using this equation, several design rules for microcavities were derived. The optimisation of the overall extraction efficiency requires an overtuned cavity: the cavity resonance wavelength should be slightly larger than the intrinsic spontaneous emission wavelength. This results were already found and reported in literature. However, if the cavity is optimised for coupling to a limited numerical aperture, then the cavity resonance should (almost) match the intrinsic emission wavelength.

Several bottom-emitting RCLEDs, emitting at 980 nm (using InGaAs based active regions) and 850 nm (using GaAs based active regions), have been de-

signed, realised and characterised. The devices have been realised in 8×8 arrays, suitable for flip-chip mounting. This implies that the light had to be extracted from the backside of the chip (bottom-emitting RCLEDs). A mask set, including test structures, was developed for this purpose. A novel technique for determining the deviation on the layer thickness was introduced. This allows to select the parts of the wafer with the desired thickness and cavity resonance wavelength, in a non-destructive way.

At 980 nm, devices with an AlAs/GaAs DBR outcoupling mirror have been designed. The maximal extraction efficiency in NA=0.5 is about 7 %, the corresponding far-field pattern is rather broad: the emission angle is about 90°. The cavity can be optimised for much smaller divergence angles. Far-field patterns with full width at half maximum of 40° are possible. However, the corresponding extraction efficiency into NA=0.5 is much smaller compared to the optimal case.

The RCLEDs have been realised and characterised. They have an overall quantum efficiency of 13.4 % (devices with a diameter of 50 μm), and 16 % was achieved using larger device sizes (85 μm diameter). Next, devices using a selectively oxidised current confining window have been realised. The goal was the realisation of very small RCLEDs (diameter smaller than 20 μm). However, it was found that the performance of these components was limited by the lateral carrier diffusion in the active region. This results in light emission under the oxide window. This limits the possibilities of this technique, in spite of its usefulness for the realisation ultra-small VCSELs. This was explained by the longer recombination lifetime in RCLEDs compared to VCSEL, resulting in an increased diffusion length. Finally, RCLEDs with an oxidised DBR have been realised. Simulations have shown that the use of the high-contrast results in an increased extraction efficiency into a limited numerical aperture. Devices with good electrical characteristics have been realised.

The realisation of RCLEDs, suitable for flip-chip mounting, at 850 nm required the removal of the GaAs substrate. A literature study was done to find the best technique for the substrate removal. A wet etching technique was proposed, using $NH_4OH:H_2O_2$ as etching mixture, and an AlAs etch stop layer. Several experiments were undertaken to optimise the etch stop layer. It was found that 500 nm $Al_{70}Ga_{30}As$ had the best properties, without introducing much strain in the RCLED layer structure. To increase the yield of the substrate removal of 8×8 arrays, a rather thick mechanical stabilisation layer was included (2 μm $Al_{15}Ga_{85}As$). Several tests were done to optimise the efficiency of the active region. It was concluded that the carrier confinement plays an important role in the efficiency of substrate-removed 850-nm RCLEDs. The best results were obtained using a sufficiently thick $Al_{60}Ga_{40}As$ spacer material, with $Al_{20}Ga_{80}As$ barrier layers between the active GaAs and the spacers. The realised components have an overall efficiency of 7 %. This is rather small number, compared to 16 % for 980-nm RCLEDs. This implies that the proposed 850-nm bottom-emitting RCLED structure is not deployable as a light source in inter-chip interconnections.

11.2 Speed properties of RCLEDs

The speed properties of RCLEDs were investigated, both theoretically and experimentally. Expressions for the rise and fall times were derived, starting from the standard rate equation for LEDs. The results were compared with measurements, and a good agreement was found. It was found that large, current-driven RCLEDs are rather slow, with rise and fall times in the order of a few nanoseconds. Smaller RCLEDs have a better speed response. Voltage driven RCLEDs exhibited better speed response, and an open eye-diagram at 1 Gbps of a voltage-driven RCLED was measured. Different advanced driving techniques for RCLEDs were investigated, and the best results are obtained using a pulsed current shape. The optical and electrical small-signal behaviour was experimentally characterised, and compared to theory. Evidence for an important lateral carrier diffusion was found, confirming the measurements on the 980-nm RCLED with selectively oxidised current window.

Next, an adequate high-speed model for RCLEDs was derived and implemented in the VerilogA behavioural modelling language. The model was based on the rate equation, and extended to allow a better modelling of the transient during the off-switching using a voltage source. A parameter extraction procedure was proposed. The model allows to simulate the speed response of RCLEDs under various conditions. For example, it predicts the small-signal response of RCLEDs, including the anomalies at very small biasing currents.

Finally, CMOS-integrated drivers for driving RCLEDs have been designed, realised and characterised. The design of the circuits made use of the high-speed model for RCLED. The influence of the driver on the speed response of the RCLEDs was investigated theoretically and confirmed using simulations with the RCLED model. It was found that the parasitic capacitance of the driver circuit has an important influence on the switching characteristics of the RCLED. Three different driver circuits have been realised in an 0.6-μm CMOS technology from AMS. All circuits generate a pulsed current shape, to speed up the RCLED response. Simulations showed that the drivers, with an 20 μm diameter RCLED, are able to drive the RCLEDs at 1 Gbps. First experiments on the drivers, with a 32-μm RCLED, showed operation of at least 660 Mbps. This is already a much faster response compared to a RCLED driven by a constant current source.

11.3 The RCLED based link

Finally, the parallel RCLED based interconnect link is the studied. Firstly, a simple link simulator was designed, using the LabView programming environment. An accurate RCLED model was implemented, using the analytical expression for the extraction efficiency of the RCLED. An expression for the coupling efficiency to the POF was derived, taking into account the alignment of the fibre to the RCLED. The absorption in the POF was taken into account. The

transimpedance amplifier, based on the gm-gm amplifier, was implemented. Using the model, it was found that the optimal RCLED diameter should be slightly smaller than the fibre diameter. This is explained by the trade-off between a large overlap efficiency with the fibre, and a fast response. The same conclusion was found for the optimal detector diameter.

Measurements have been done on a RCLED based interconnect link, using plastic optical fibre as the optical pathway. The link works, even for RCLED currents as small as 2 mA. The latency of the RCLED link was characterised. The experimental results were in agreement with the expectations from theory. The cross-talk in the parallel optical link was investigated theoretically.

Finally, the performance of the RCLEDs was compared to another light source, suitable for inter-chip interconnections: the VCSEL. The VCSEL outclasses the RCLED on different levels: the efficiency is larger, the speed response is better (mainly because the VCSEL has typically a much smaller active region), even the temperature dependency is (slightly) better. However, the RCLED has a better uniformity, especially in arrays driven by CMOS circuits. The uniformity of VCSELs is poor if the drive current is close to the threshold current. This implies that VCSEL based parallel interconnect links must have receivers with a large dynamic range, whilst RCLED based parallel interconnects links need highly sensitive receivers.
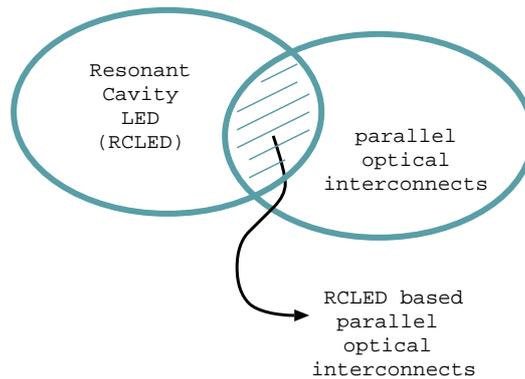
11.4   The future

At the end of this work, some interesting questions arise:

- What is the future for RCLEDs ?

- What is the future for optical interconnects ?

- What is the future for RCLEDs based parallel optical interconnects ?

RCLEDs have a bright future. The efficiency of RCLEDs is up to 10 times larger compared to planar LEDs. This is achieved using an advanced layer structure.

The processing of the device is similar to standard LEDs, implying that the devices can be realised at low cost. The low-cost and the high-performance makes the RCLED an attractive light emitter. They can replace every LED (at least, if the drive current can be down scaled). Typical applications for these components are highly efficient indicators, multi-colour displays, and POF based interconnects.

This work showed the feasibility of small, highly efficient and high-speed RCLEDs. This implies that RCLED can be used as light source in short-distance optical networks, especially if there are no VCSELs available emitting at the desired wavelength. This is the case at 650 nm and 1.3 μm. The industry has seen the opportunity at 650 nm, and the first RCLEDs emitting at these wavelengths are commercially available. Unfortunately, the industry has not seen the opportunity at 1.3 μm. The main effort was put in the development of 1.3-μm VCSELs. Only very recently, first 1.3-μm VCSELs with acceptable performance have been presented at the research level, whilst good performing RCLEDs exist for years.

The future for on-chip optical interconnects is also shining. As mentioned in first chapter, the ITRS road map predicts an interconnect bottleneck in and between chips, and no solutions are known. Alternatives for metal based interconnects need to be developed urgently. Currently, optical interconnects is a rather mature technology, compared to its competitors (such as 3D interconnects). Nevertheless, a lot of work needs to be done, and a strong competition of advanced metal based interconnects can be expected.

As mentioned in the last chapter, the optimisation of the efficiency of the complete link and the minimisation of the non-uniformities are basically the biggest challenges for the future optical interconnection. Currently, the non-uniformity of the CMOS-VCSEL combination is too large, which is attributed to the small difference between the driving current and the threshold current. The RCLED perform better on this issue, but their efficiency is smaller. Currently, there is far more research on VCSELs compared to RCLEDs, especially in the USA. The total amount of money spent on VCSEL research worldwide during the last ten years is roughly $500 million [152], far more compared to the money spent on the development of RCLEDs. Future research should look for components with the best properties of both RCLED and VCSELs: a low-threshold, high-speed device, with a large uniformity and yield.

This work demonstrated the feasibility of RCLED based interconnects, with a good yield and a better performance compared to current PC busses. This is a small step for the single RCLED, but...

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